群馬大学アナログ集積回路研究会

高周波RFCMOS回路を実現する半導体素子のコンパクトモデリング技術

2021年7月29日

KIOXIA　株式会社
メモリ設計統括部　第三メモリ設計部　主幹
吉富貞幸

Head of Information Owner Section　　3rd Circuit designing Dept.

KIOXIA

自己紹介

出身

長崎県佐世保市生まれ(小１夏まで）→鹿児島市（中三）→熊本市（高三から）

Dominus Flevit Churchの窓を通してみた
エルサレム旧市街　（2014年12月小生撮影）

家族

妻１人（イスラエル国籍）、娘２人

大学での専攻

博士　電気工学（論文　液相堆積法を用いた二酸化シリコン膜のSI　MOS集積回路への応用　横浜国立大学）

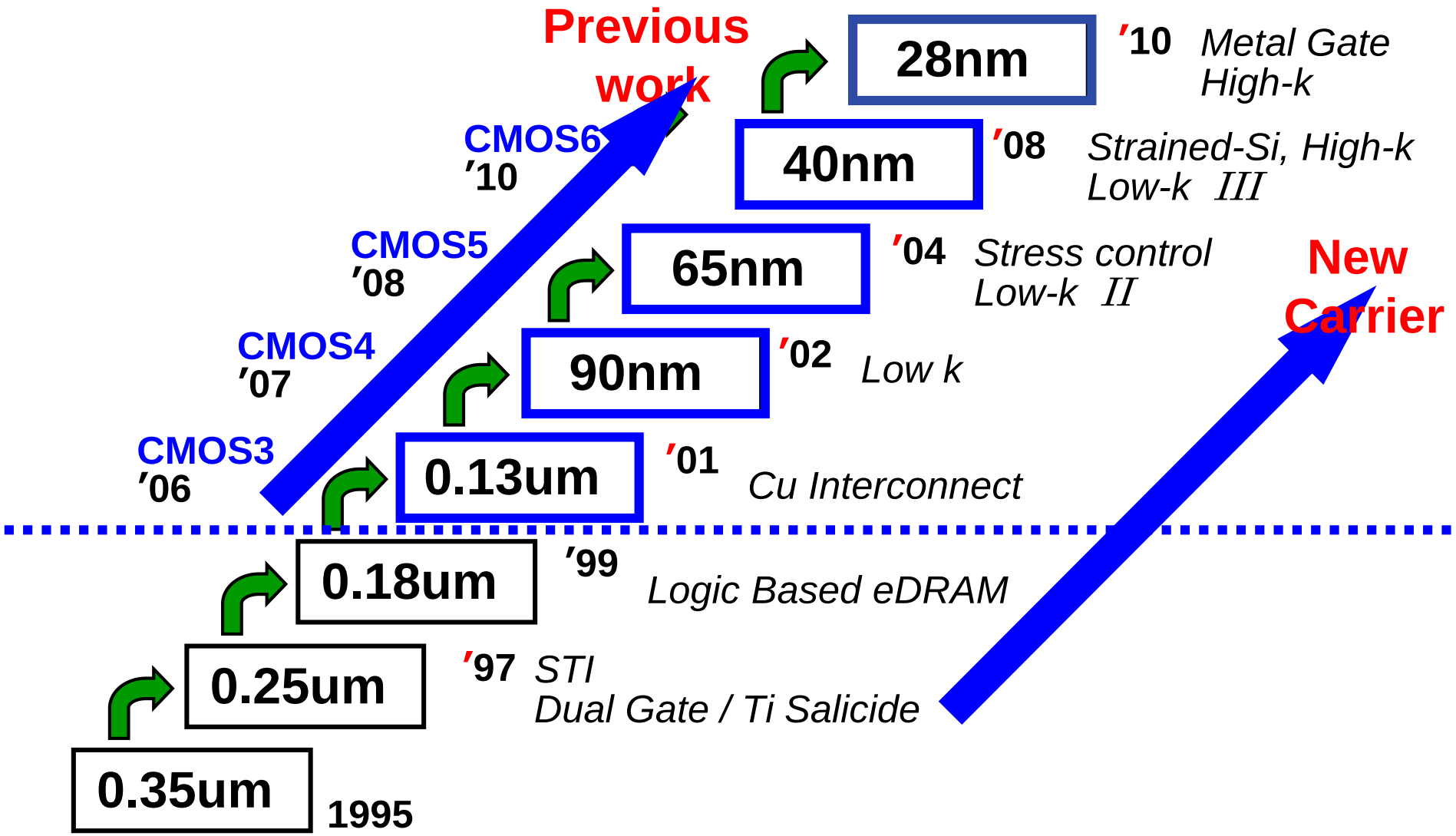
趣味

アマチュア無線、写真撮影、窯元/骨董屋巡り

仕事

1993年　株式会社東芝研究開発センター入所、高周波C/Bi-CMOSデバイス開発,システムLSI設計に従事。
2008年から　同システムLSI事業部で高周波CMOS製品開発向け設計環境開発（高周波SPICEモデル開発）
2016年から　現KIOXIA株式会社でBiCS FLASH™周辺CMOS回路設計環境(Process Design Kit)開発

Footprints of CMOS Technology Innovation [1]



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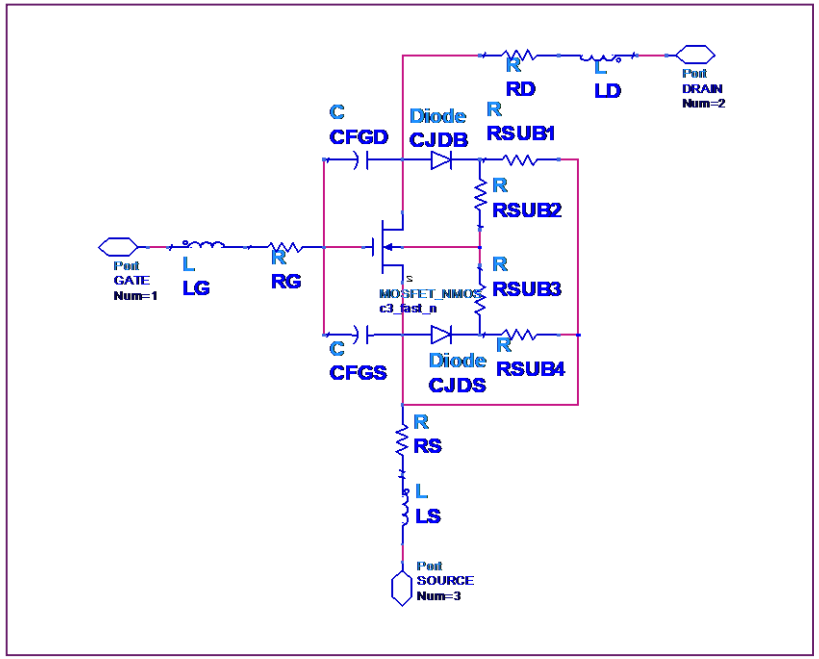
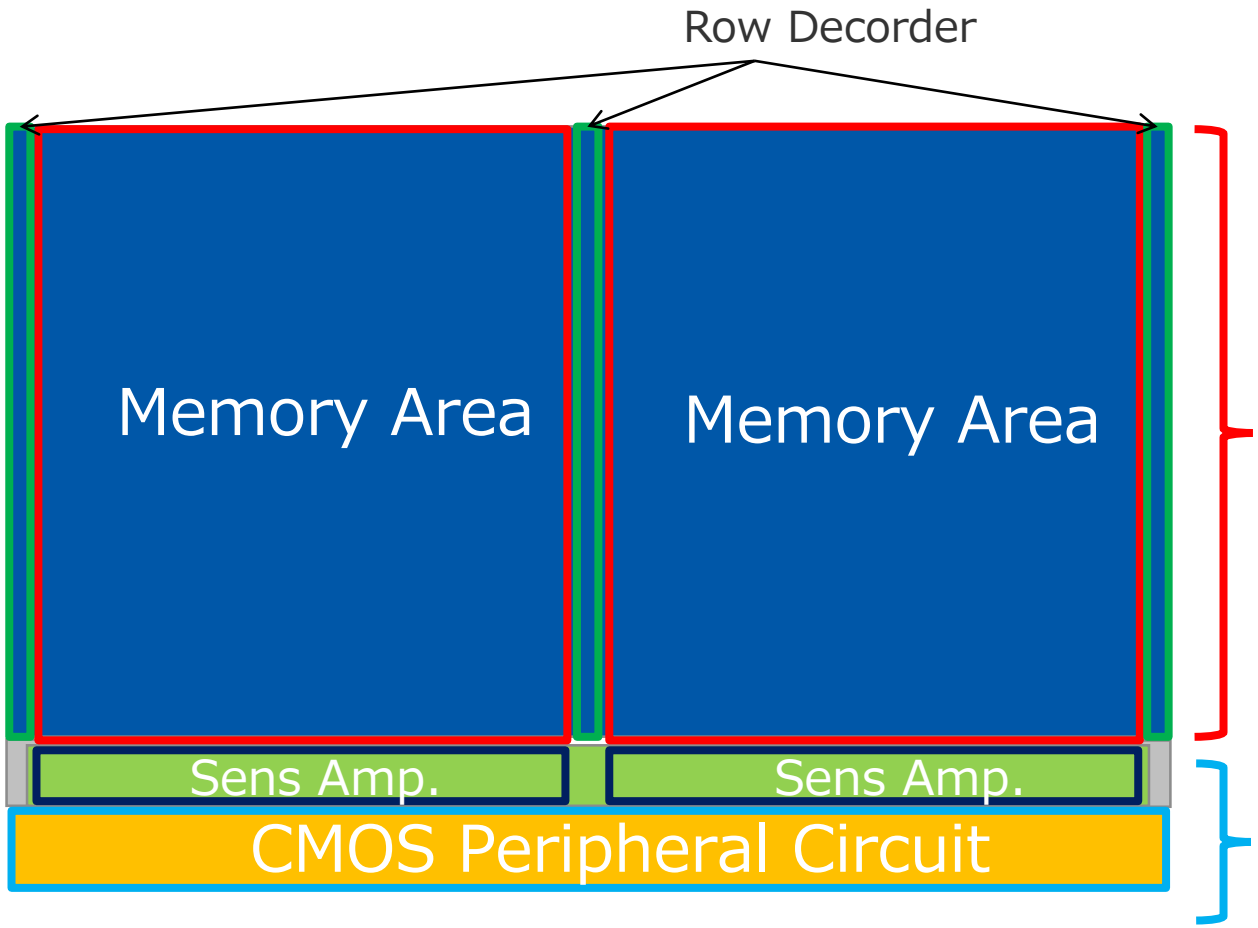
Prologue

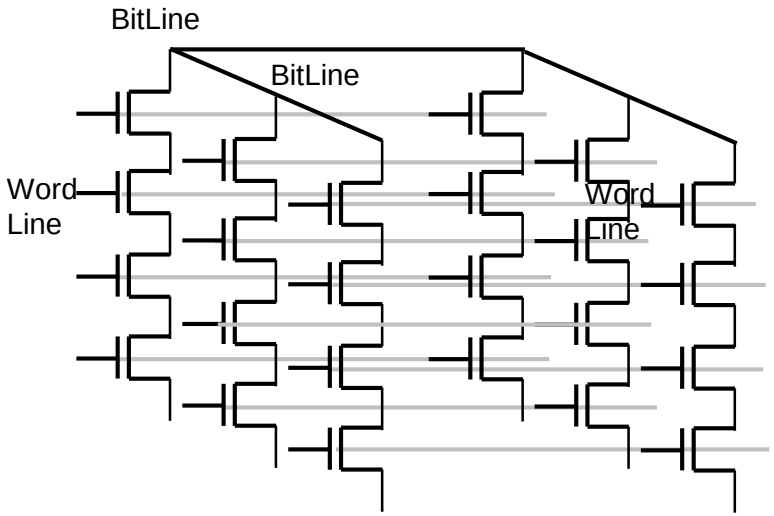


Compact modeling technology in 3D-NAND flash memory development



– Bi state switching device

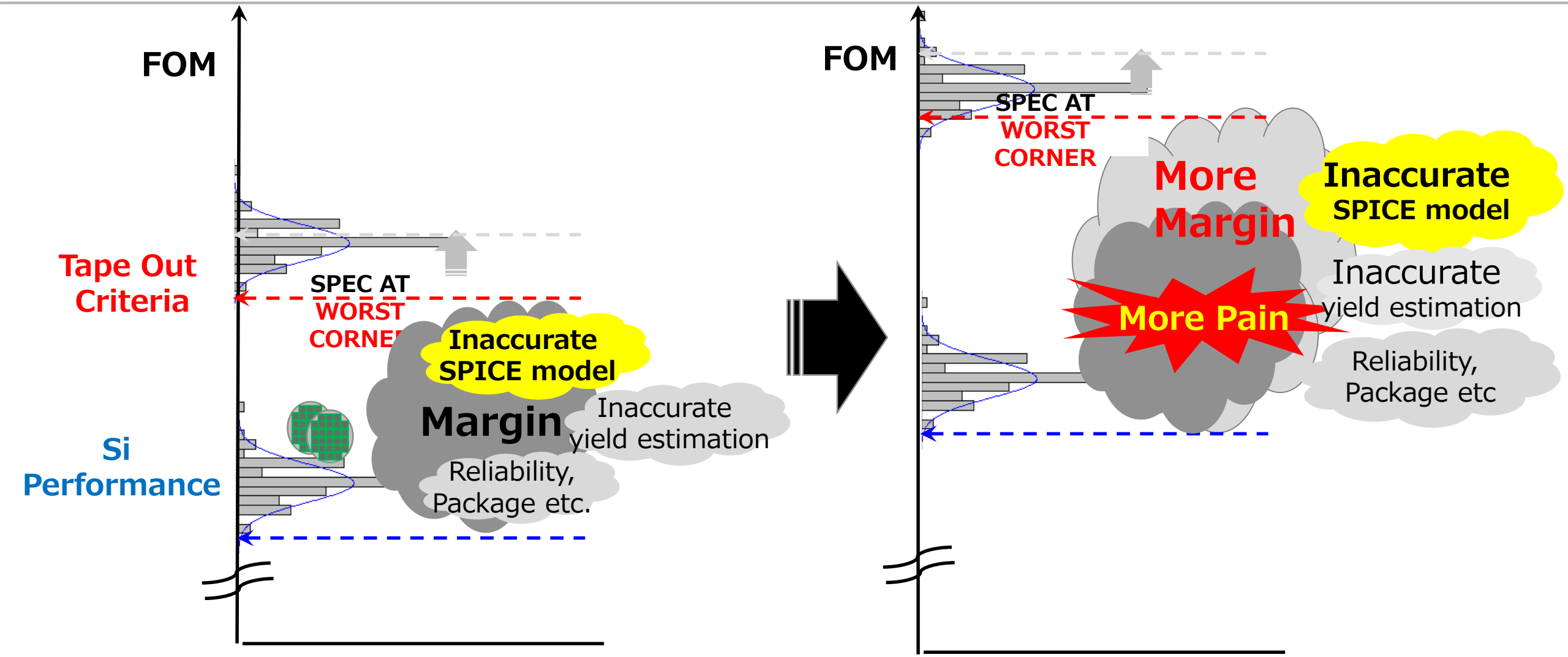
Fully customized model



Deep submicron CMOS

- Smaller Die Size
- Faster burst cycle-time → RFCMOS
- Low power consumption

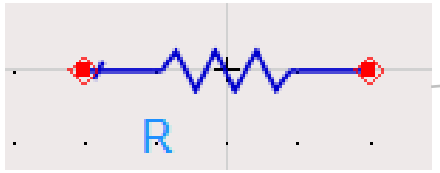
回路設計者の抱える痛み



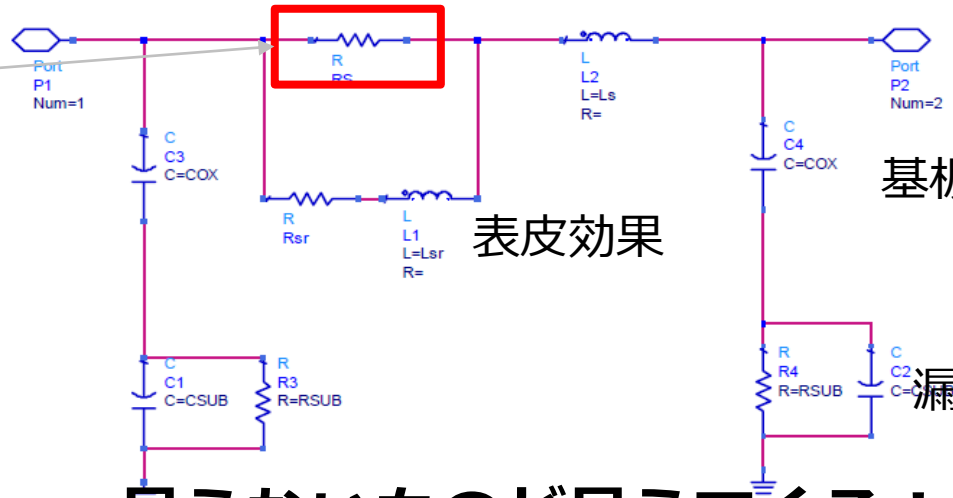
微細化と高速動作化が進むにつれて広がるマージン→広くなるほど設計難易度は上がる
高速動作→**高周波動作を高精度に表現できるSPICEモデル**が治療薬の1つ。

高周波動作を高精度に表現するモデル？？

低周波数の世界
DC~ hundreds MHz



高周波の世界
RF/mm-wave/THz



基板との容量

表皮効果

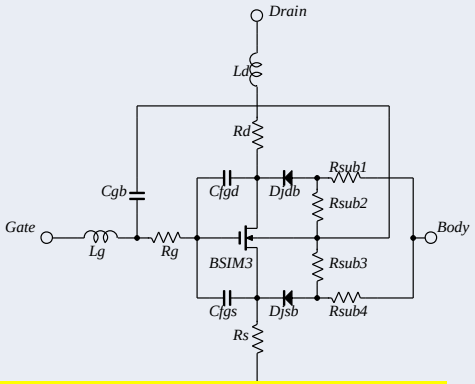
漏れ信号による損失

見えないものが見えてくる！

半導体基板上に作成された素子の特性を電気モデルで表現し
SPICE系回路シミュレータで動作させたい。

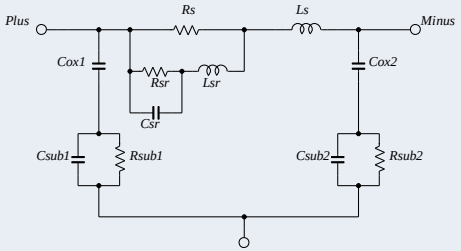
高周波CMOS回路設計で使う素子のSPICEモデル一覧

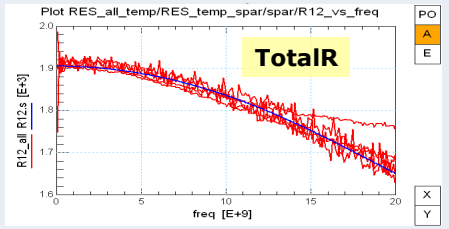
MOSFET



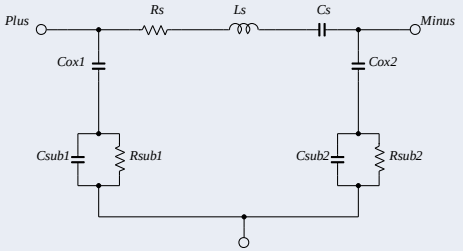
特技→Smithチャートからチャネル濃度の高低を推測できる。

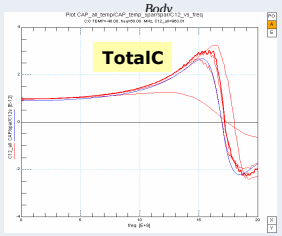
Resistor



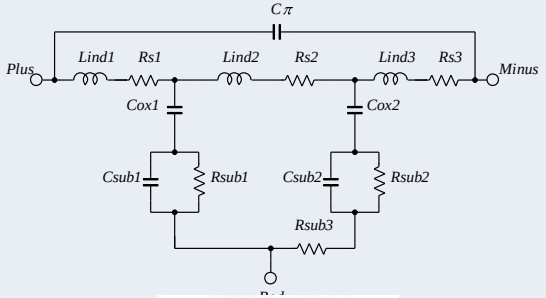


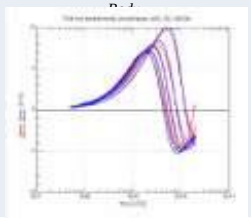
Capacitor



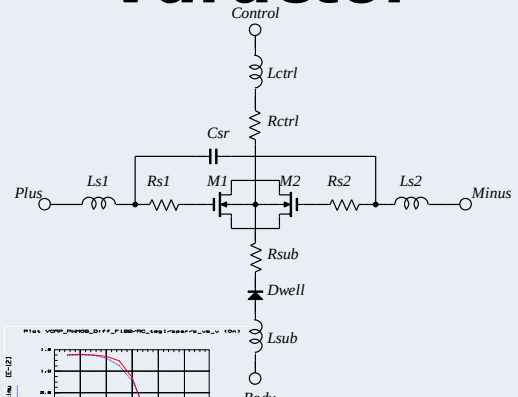


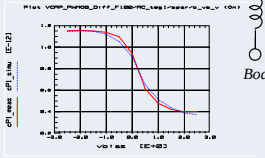
Inductor



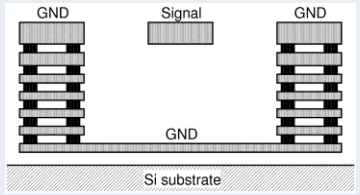


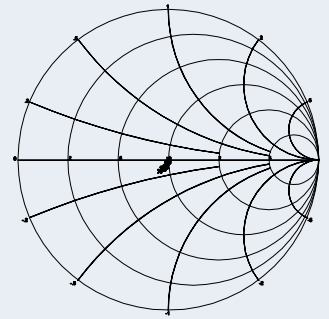
Varactor





Transmission Line





01

序章

見えないものを見よう。
　道具
　Y行列

測定
推定
モデル化そして確定

測定→道具立て

① Network Analyzer

For S-parameter Measurement

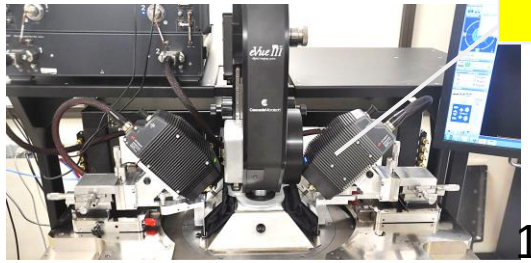
Keysight Technologies
Rhode & Schwartz
ANRITSU
等がある。

②Probe Station

Semi-Auto Prober

Form Factor
MPI Corporation等

latest model to access Wafer

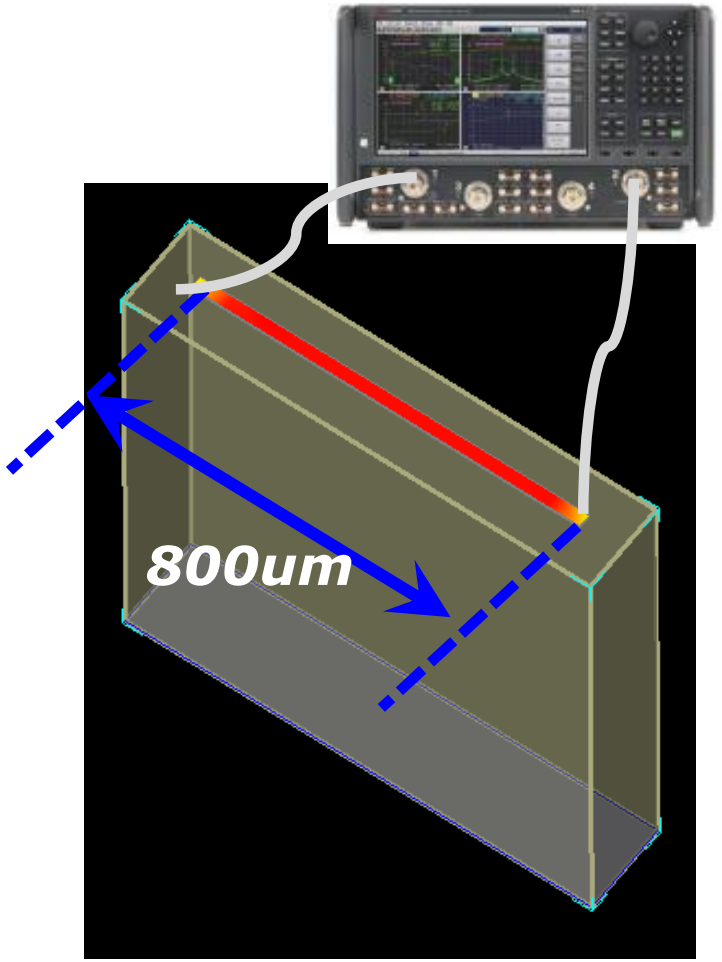


Positioner

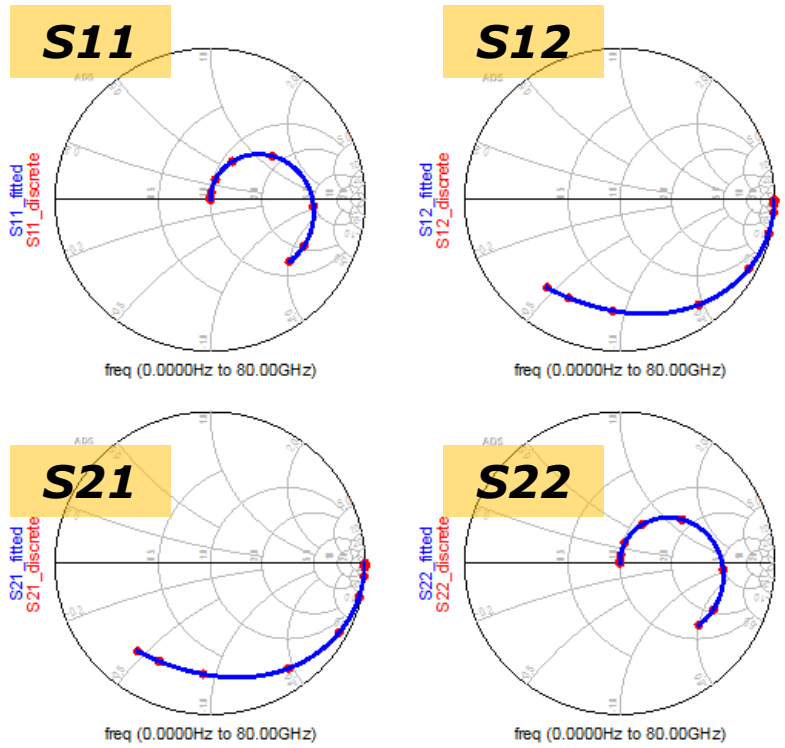
110GHz以上の測定では
特殊な治具を必要とする。

近年ソフトと画像認識技術が発展し、全自動でSパラメータ測定ができるようになった

推定　→　単純な配線なのに何か違う？？



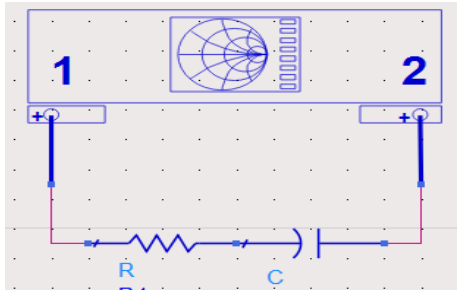
Metal line (800um) on Si

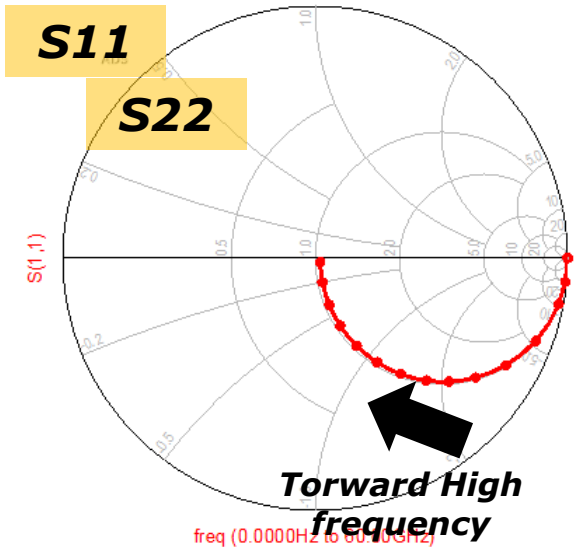


Measured S-Parameters

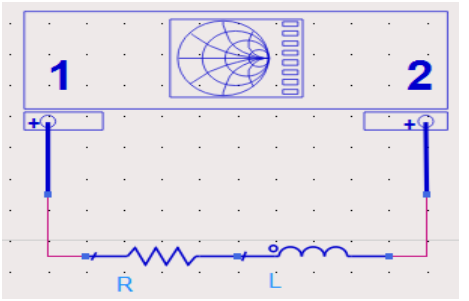
推定　→　何が違う？？

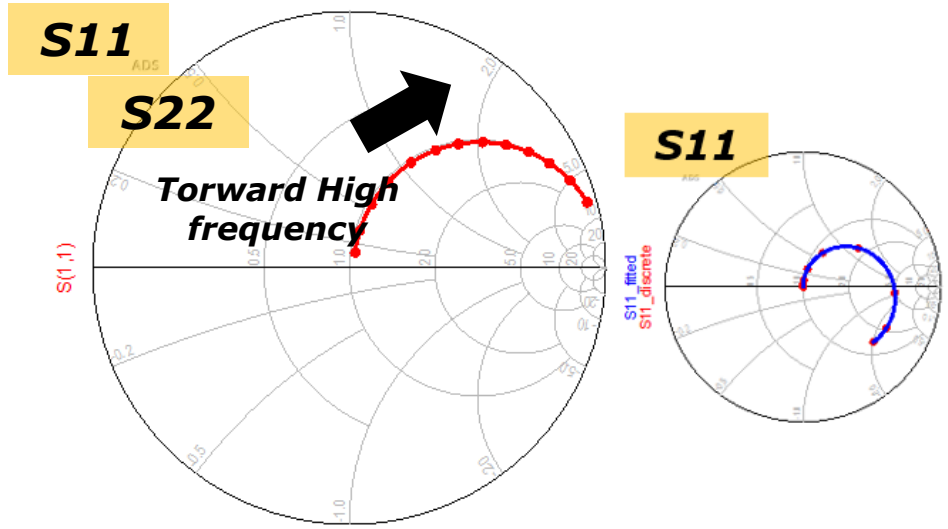
R+1/(jwC)





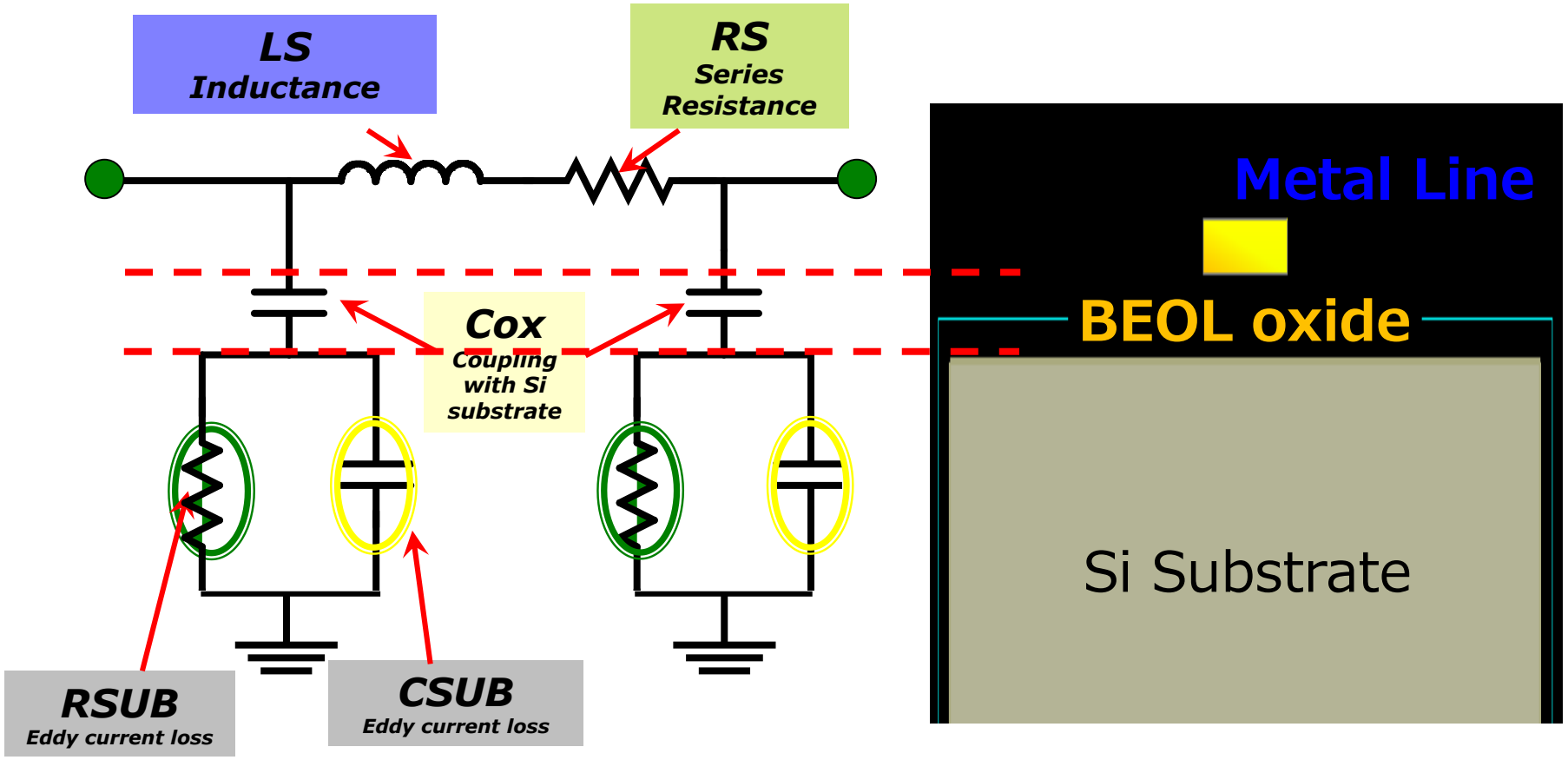
R+jwL





今回のデータは右図のR+jwLに従った特性を示しているようだ。

推定　→　寄生容量・抵抗どうつながっている？？

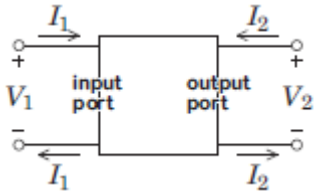


Cox, Csub and Rsub represent equivalent circuit of Si substrate in most cases.

モデル化そして確定　全てはPI型・Tee型変換で。

Y matrix

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = Y \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}.$$

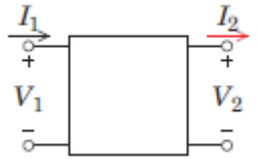


$$y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0}, \quad y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0},$$

$$y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0}, \quad y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0}.$$

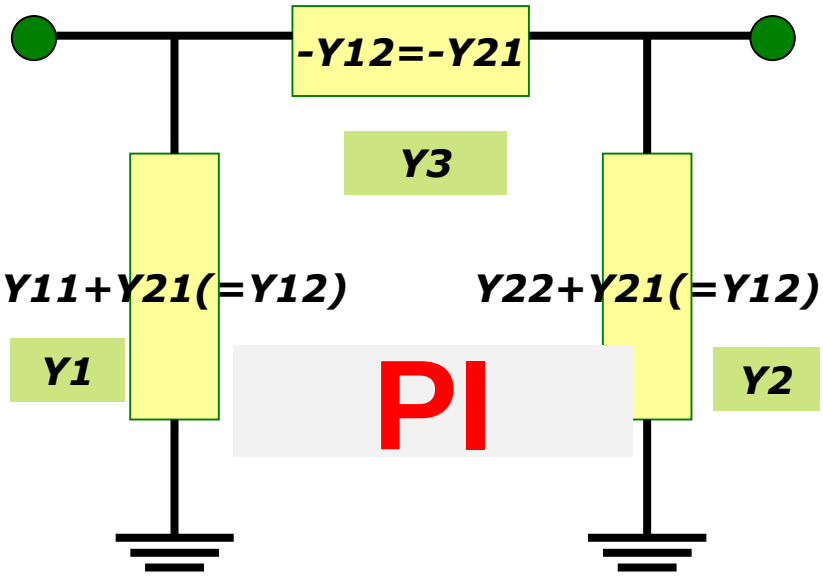
Z matrix

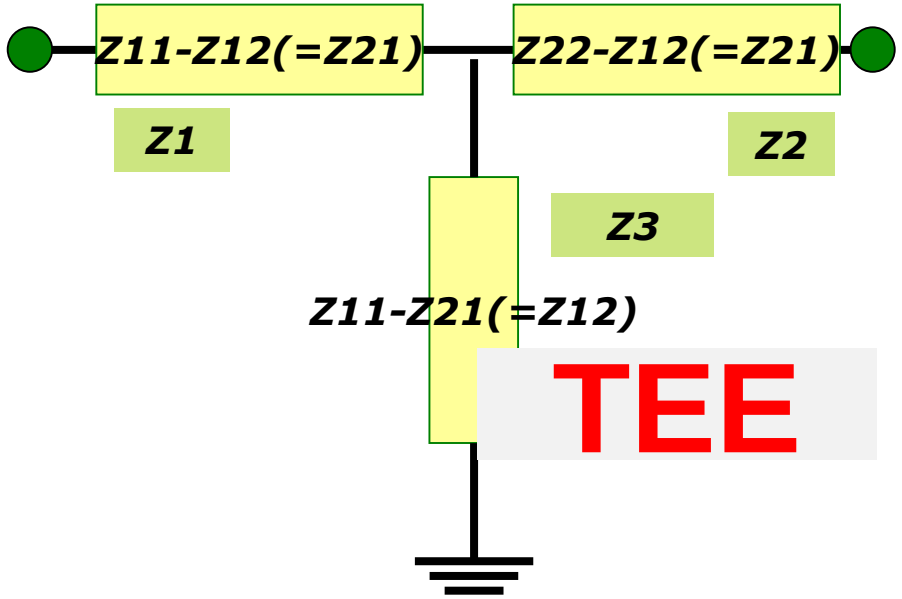
$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = Z \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}.$$



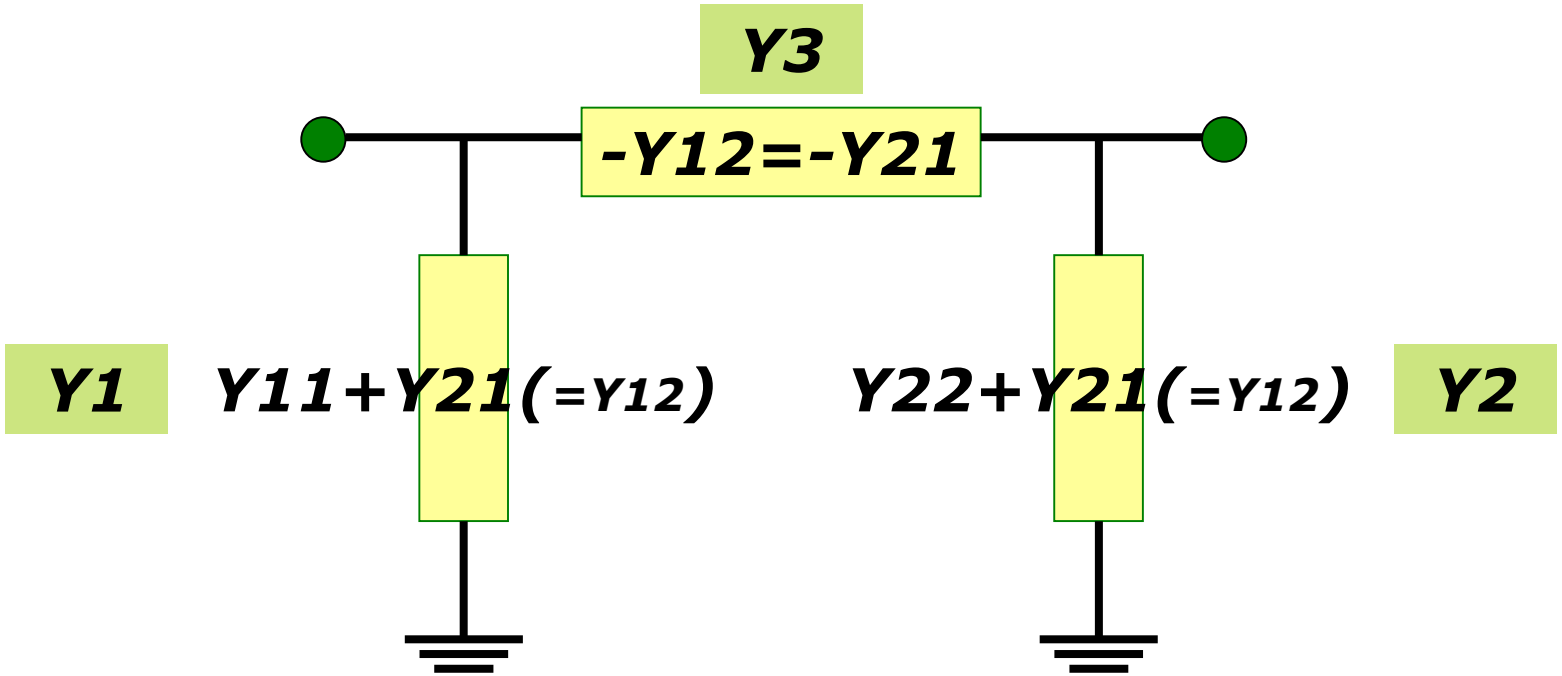
$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0}, \quad z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0},$$

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0}, \quad z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0}.$$





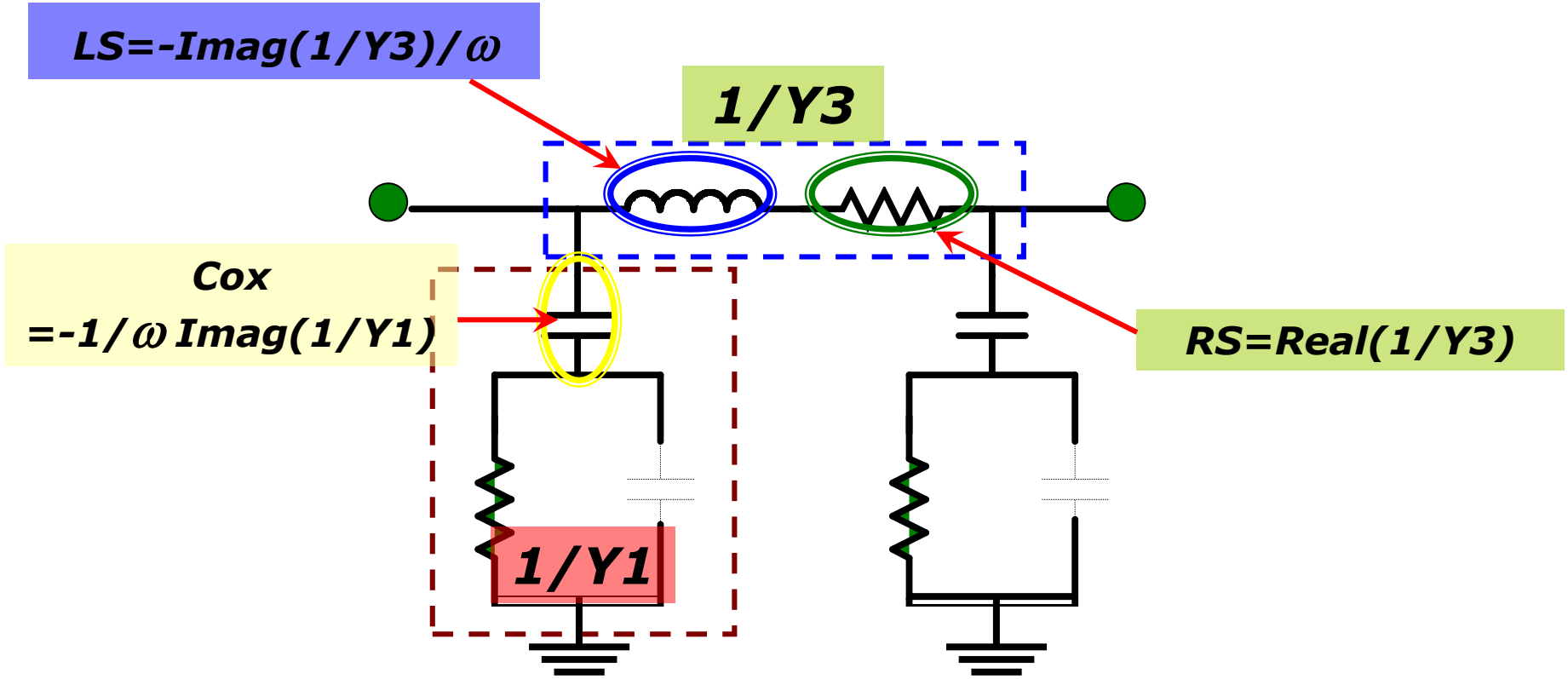
PI型　等価回路を使ってみる



- Conversiion from S-parameter to Y-parameters.
- Generation of “pi-equivalent” circuit using Y-parameters.

Step 1

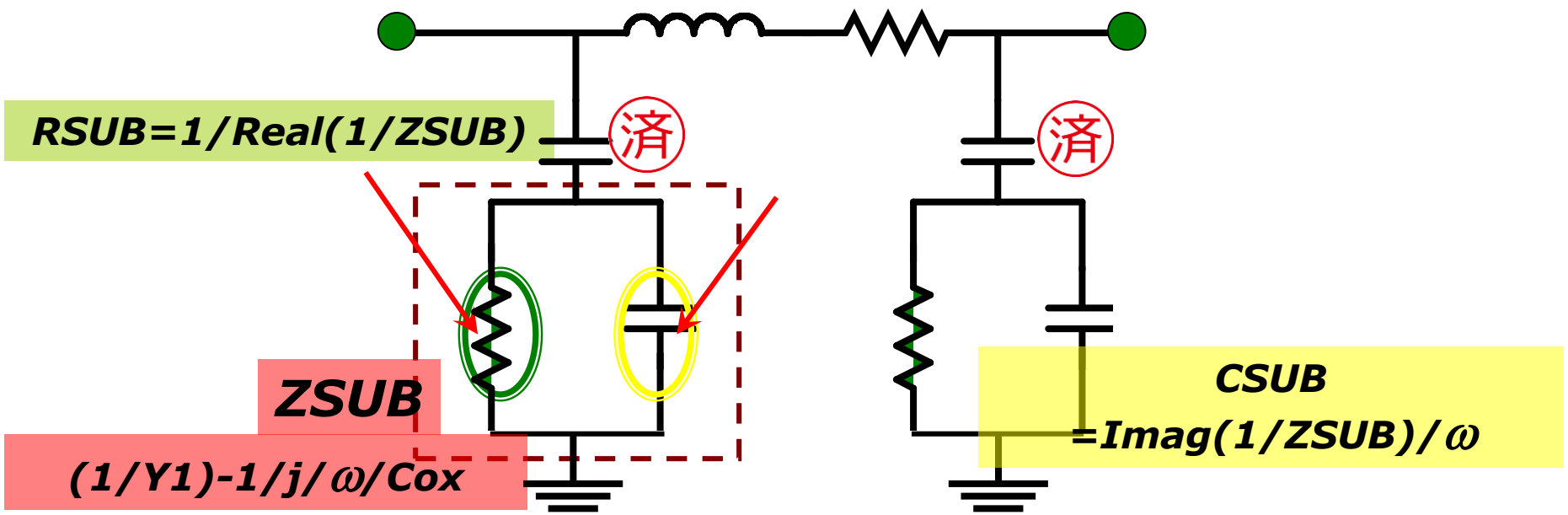
Low frequency



- Assumption “CSUB” << “COX” is valid in most cases.
- CSUB node can be treated as “OPEN” at low frequency.

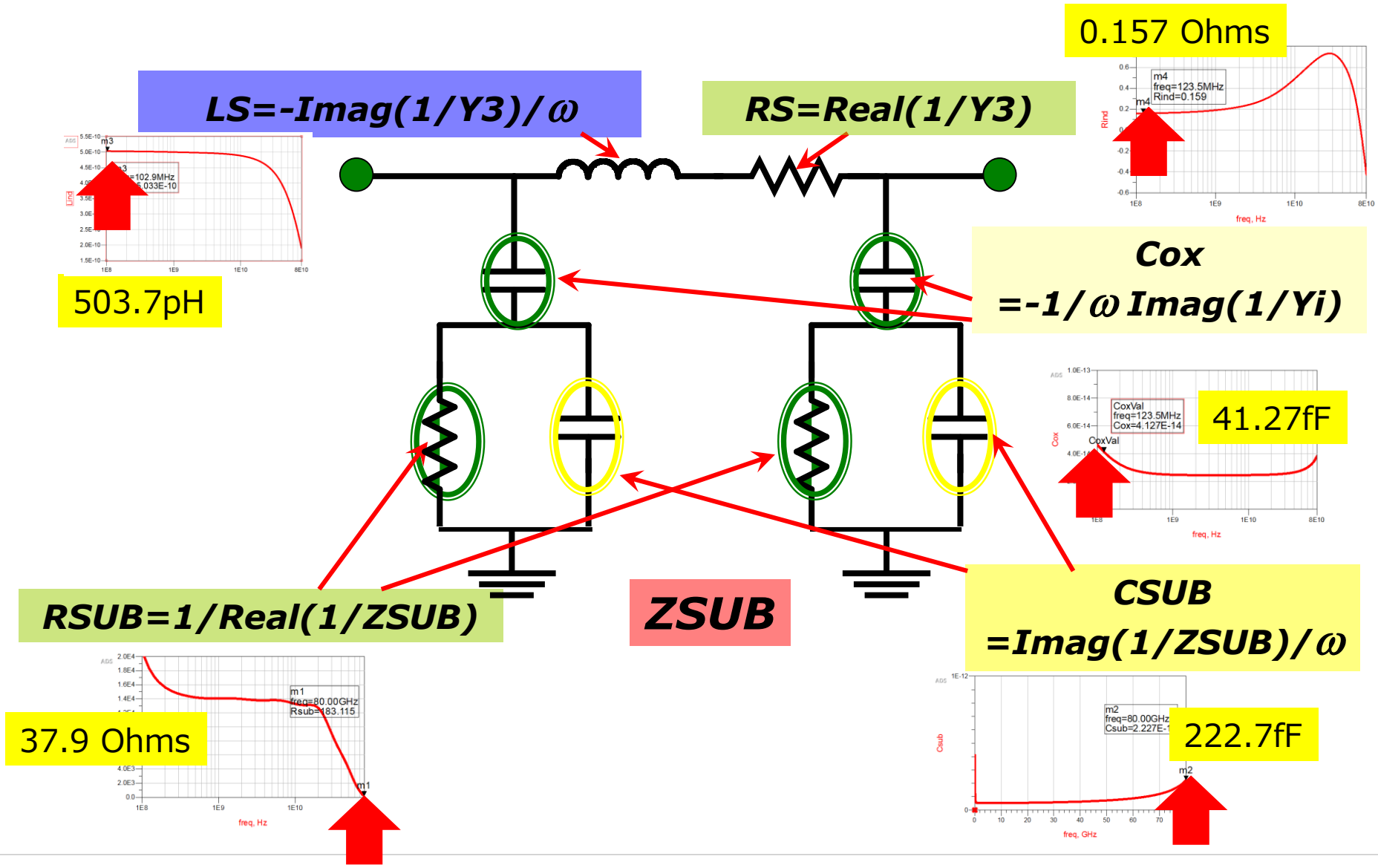
Step 2

High frequency

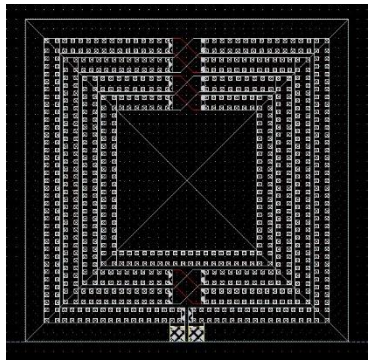


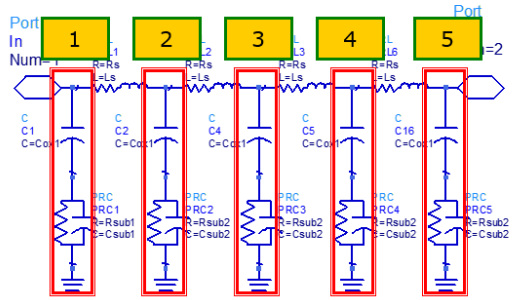
- Define “ZSUB” by subtracting Cox impedance from 1/Y1 .
- “RSUB” and “CSUB” defined by real and imaginary part of “ZSUB” respectively.

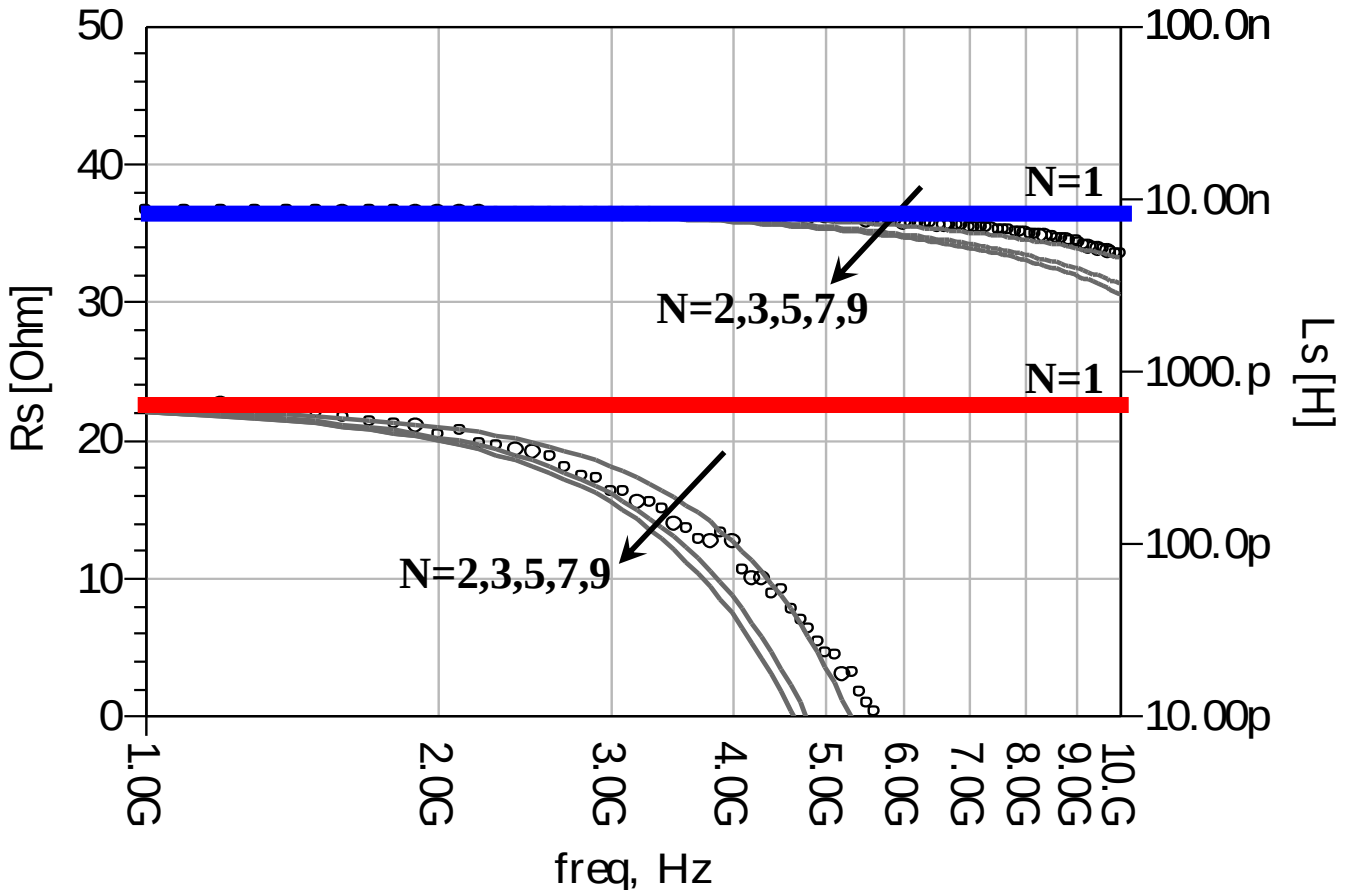
Complete formula



大きなサイズ→分割アプローチを利用し精度向上



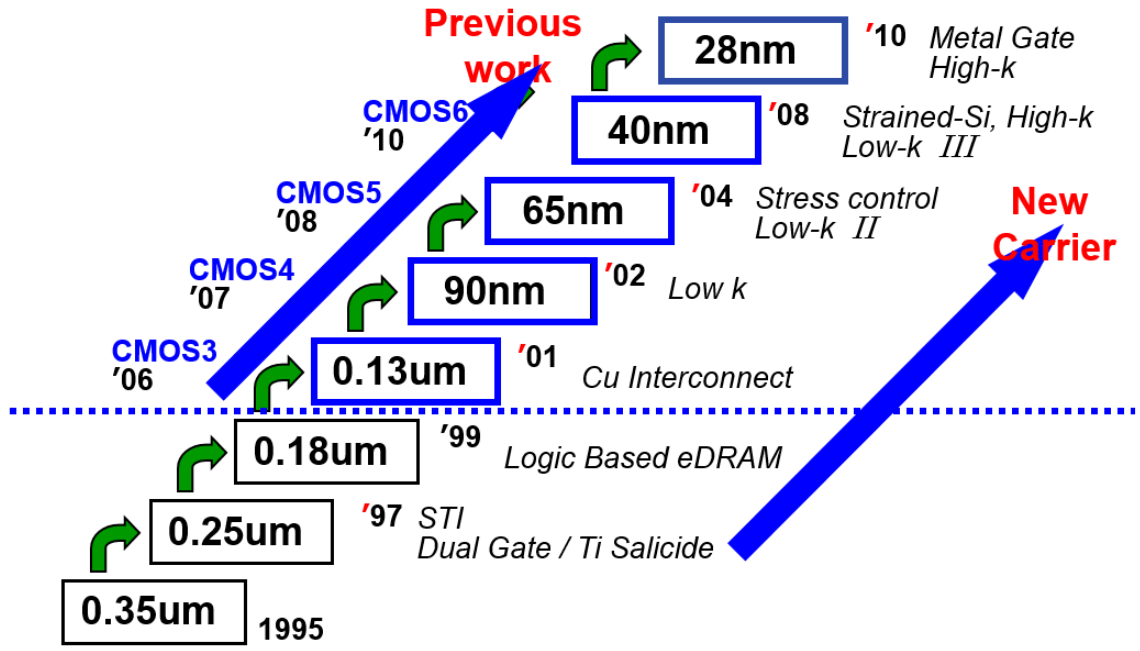




長い、広い構造の特性を表現する場合→ざっくり求めて詳細に分割するとよい。

02

5Gを支える微細CMOSトランジスタの課題

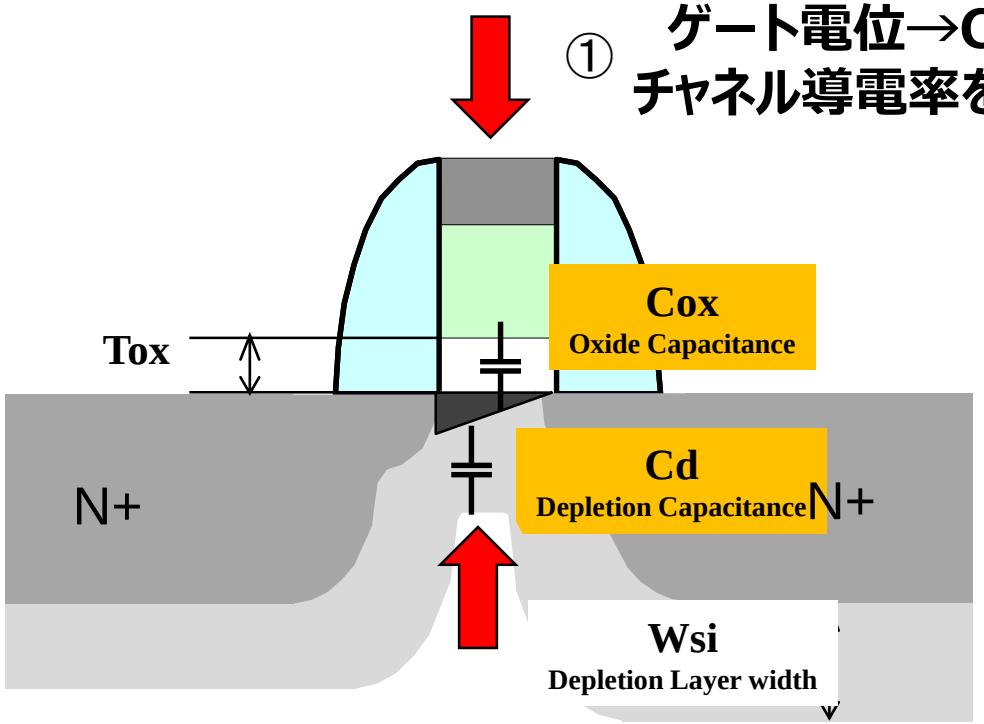


設計を悩ませる微細効果

1　ゲートリーク（漏れ）電流
2　ストレス効果
4　Well 近接効果　(Well　Proximity　Effect)

最近のコンパクトモデルでは取り込まれている。

MOSFETとは何か？



$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \quad [F/cm^{-2}]$$

$$C_d = \frac{\varepsilon_{si}}{W_{si}} \sim \frac{1}{3} \cdot C_{ox} \quad [F/cm^{-2}]$$

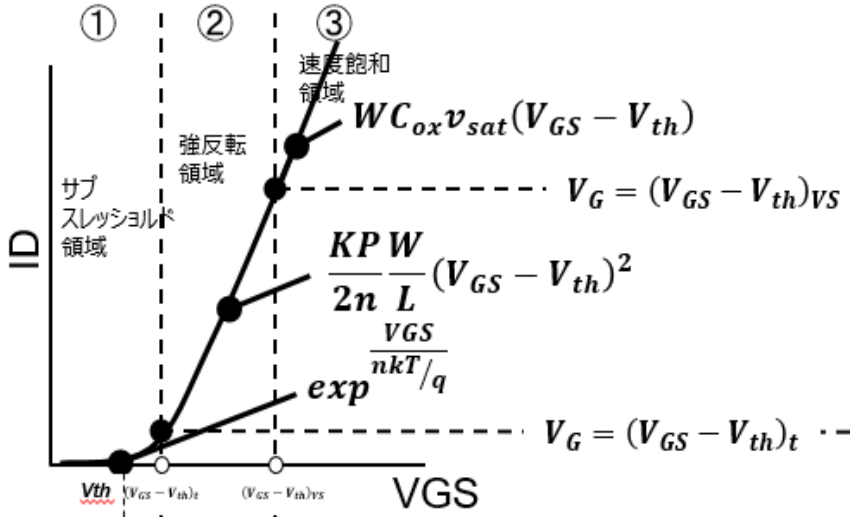
$$\frac{C_d}{C_{ox}} = n - 1 = \frac{3T_{ox}}{W_{si}} \equiv \alpha$$

n：1.2 ~ 1.5
n(pmos)> n(nmos)

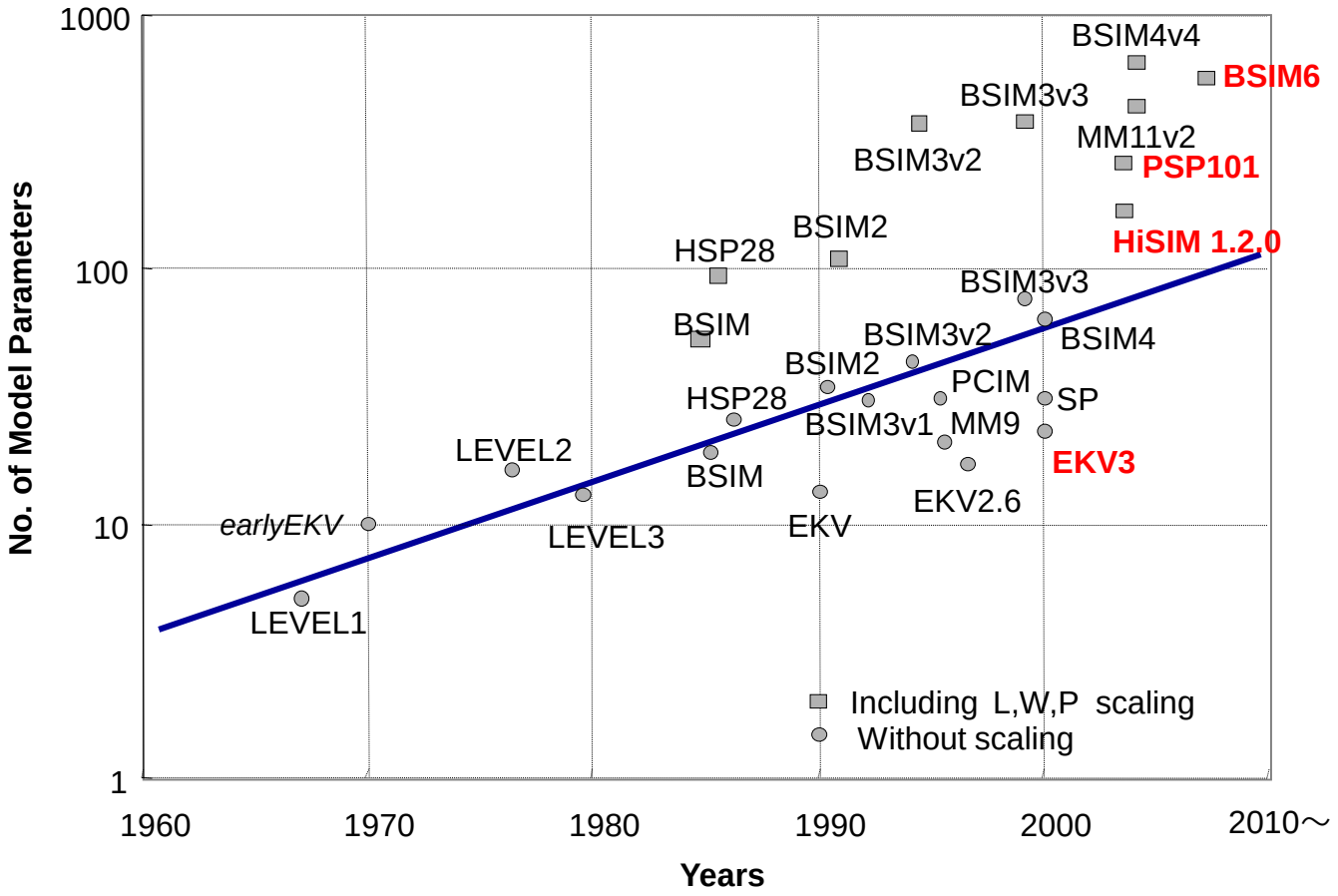
キーワード：MOSFETは容量結合で導電性制御

オーバードライブ電圧でMOSFETを語ることが出来る

弱反転領域	強反転領域	速度飽和領域
$I_D = I_{D0}\frac{W}{L}exp^{\frac{VGS}{nkT/q}}$	$I_D = \frac{\frac{KP}{2n}\frac{W}{L}(V_{GS}-V_{th})^2}{1+\theta(V_{GS}-V_{th})}$	$WC_{ox}v_{sat}(V_{GS}-V_{th})$ $= \frac{\frac{KP}{2n}\frac{W}{L}(V_{GS}-V_{th})}{\theta}$
$g_m = \frac{I_{DS}}{nkT/q}$	$g_m = \frac{2I_{DS}}{VGS-Vth}$	$g_m = WC_{ox}\,v_{sat}$ $= \frac{\frac{KP}{2n}\frac{W}{L}}{\theta} = WC_{ox}\frac{\mu}{2nL\theta}$
$\frac{g_m}{I_D} = \frac{1}{nkT/q}$	$\frac{g_m}{I_D} = \frac{2}{VGS-Vth}$	$\frac{g_m}{I_D} = \frac{1}{VGS-Vth}$
$(V_{GS}-V_{th})_t$ $= 2n\frac{kT}{q}\sim 70mV$	$(V_{GS}-V_{th})_{VS}$ $= \frac{1}{\theta}\sim 2nL\frac{v_{sat}}{\mu}\sim 5L$	Lに比例
$I_{DSt} = \left(2n\frac{kT}{q}\right)^2$	$= \frac{KP}{2n}\left(2nL\frac{v_{sat}}{\mu}\right)^2$	



CMOSトランジスタモデルの変遷



W.Grabinski "MOS-AK", IWCM2007

HiSIM→広島大学

BSIM→University of
California Berkeley

MM9 (MosModel9)
→Philips

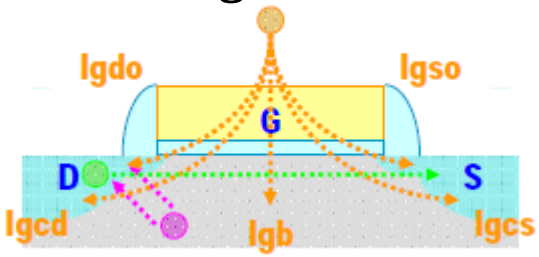
EKV (Enz Krummenacher Vittoz)
→EPFL (スイス)
TUC（ギリシャ）

Gateリーク電流

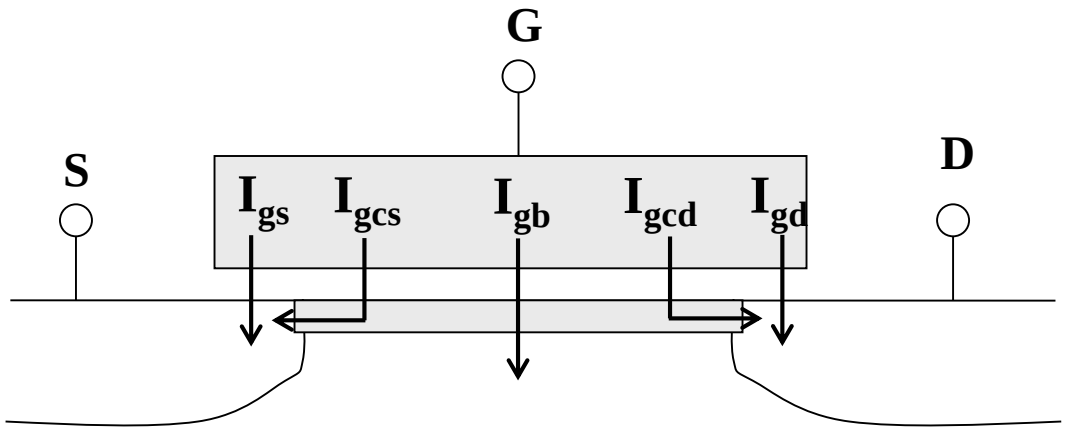
スマホのリーク電流が
Ioff/Tr is ~100nAあると

⇒ SmartPhone（@1億Transistors）
⇒Off Leak current≒**10A**

Gate leak current is not ignorable due to the higher tunneling probability of thinner gate oxide



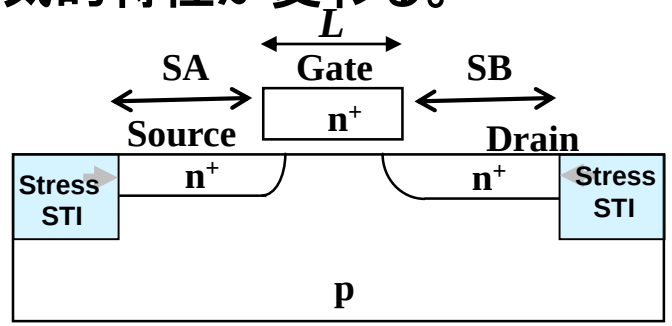
⇒Subthreshold leak current
⇒Gate Induced Drain leakage current
⇒Gate leak current



In latest CMOS compact model, several current sources as I_{gb}, I_{gs}, I_{gd}, I_{gc}(I_{gcs}, I_{gcd}) having Vg dependency, which gives bias dependence, and mathematical smoothing transforming function from accumulation to inversion mode, via depletion.

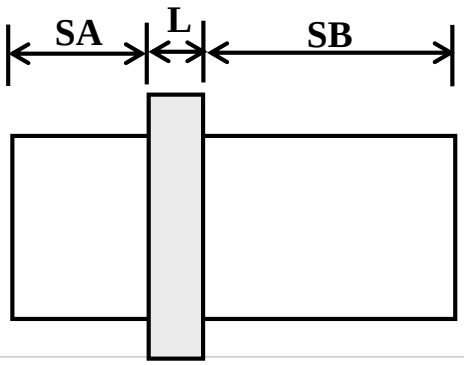
ストレス効果

トランジスタが横・縦方向にあるべつの材料から押されたり引っ張られたりする（ストレス）と電気的特性が変わる。



This was focused as a big-problem to degrade Transistor performance from 130nm generation.

Recent Compact Model formulates Vth shift as a linear form of SA and SB difference from reference Transistor.



$$\mu_{eff} = \frac{1+\rho_{\mu_{eff}}(SA,SB)}{1+\rho_{\mu_{eff}}(SA_{ref},SB_{ref})}\mu_{eff\,org}$$

$$\rho_{\mu_{eff}} = KU0(Inv\_sa + Inv\_sb)$$

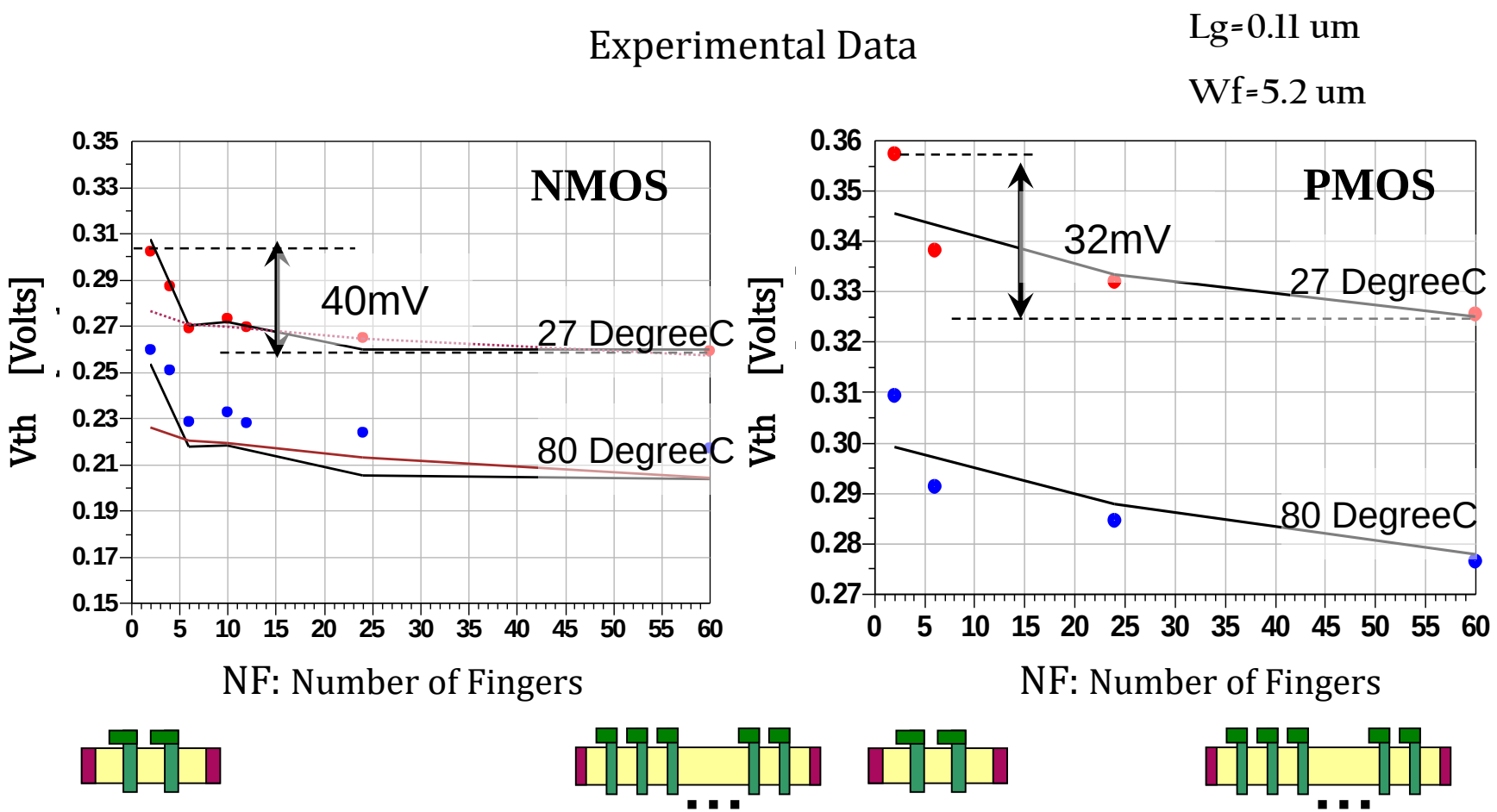
$$VTH0 = VTH0_{org} + KVTH0(Inv\_sa + Inv\_sb - Inv\_sa_{ref} - Inv\_sb_{ref})$$

$$Inv\_sa = \frac{1}{SA+0.5L}, \qquad Inv\_sb = \frac{1}{SB+0.5L}$$

$$Inv\_sa_{ref} = \frac{1}{SAref+0.5L}, \qquad Inv\_sb_{ref} = \frac{1}{SBref+0.5L}$$

SAref, Sbref -> SA,SB value of a reference MOSFET.

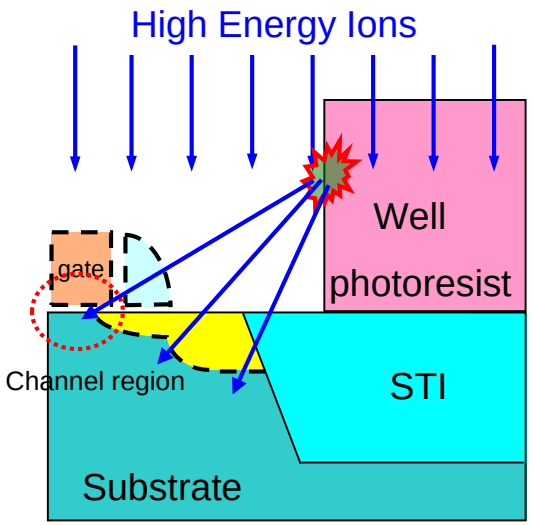
STI stress effectの事例 –VTH shit of 130nm CMOS-



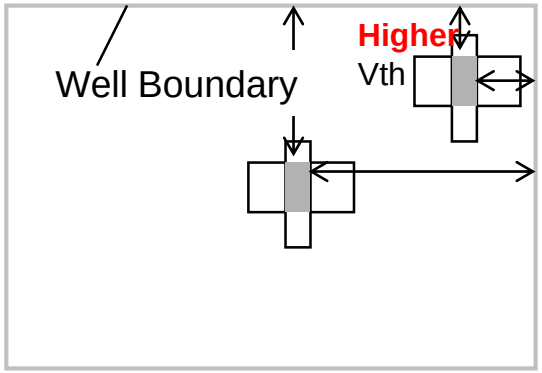
同じゲート長なのに閾値電圧が変化し、電流値が変動

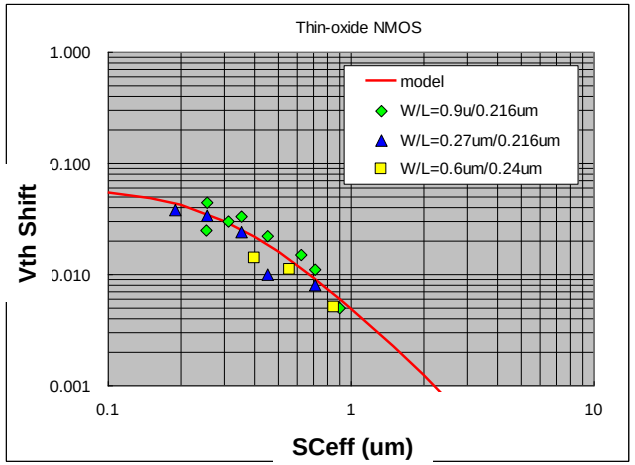
ウェル近接効果

MOSFET with adjacent well boundary tends have higher Vth. This is due to the highly doped area generated by back-scattering of impurity atoms against photo resists. Which occur in the Well Ion Implantation process.



WPE = Well Proximity Effect



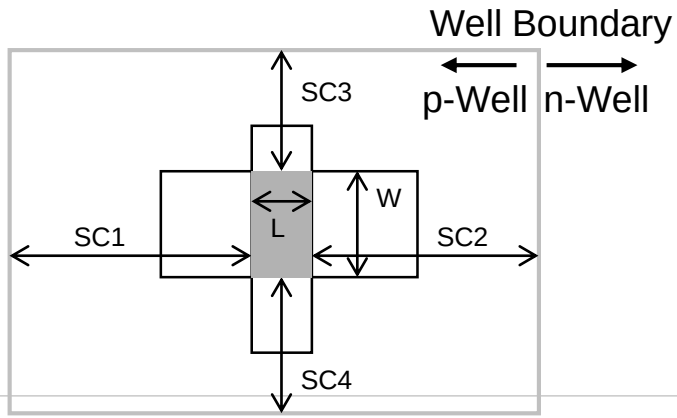


Recent Compact Model formulates
Vth and Mobility shift as a linear form of SCi (i=1~4) .

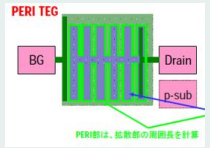
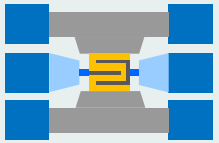
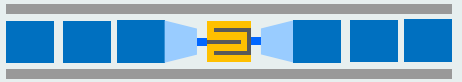
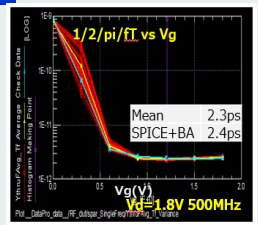
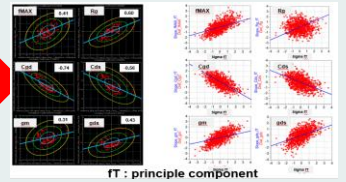
$$Vth0 = Vth0_{org} + KVTH0WE \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC)$$

$$\mu eff = \mu eff_{org} \cdot (1 + KU0WE \cdot (SCA + WEB \cdot SCB + WEC \cdot SCC))$$

（SCi (i=A,B,C..), is effective distance determined by the use of SC1~SC4 (between outer edge of MOSFET and Well boundary)）



最近のCMOSトランジスタモデル開発の技術紹介

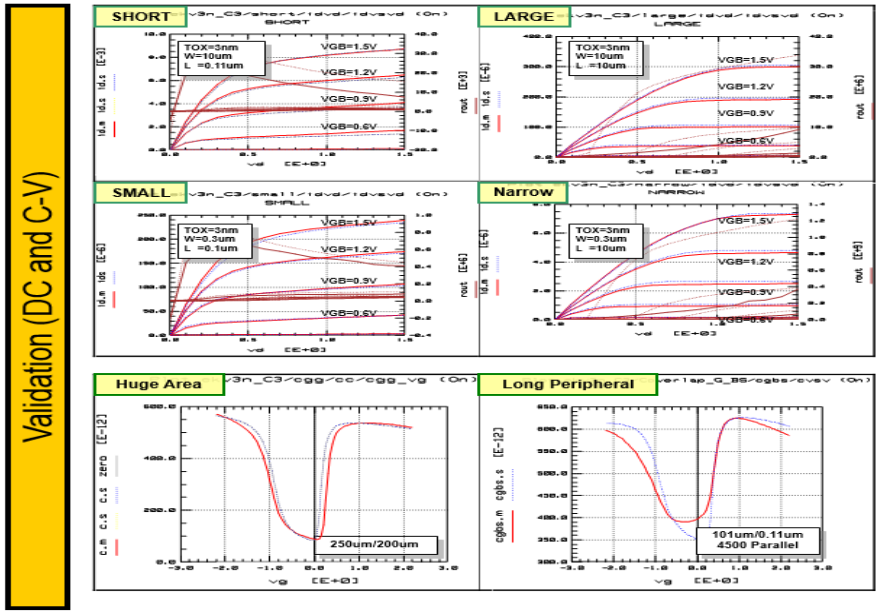
Past	Now	Future
Test structure design.	Phylosophical change	Optimize for MP use
 Bulky patterns for CV modeling	 GSG-TEG	 GSG-type SL-monitor
High-volume meas.	Wafer level	Full-Auto meas. Usage of Big Data
Manual measurement. Not enough numbers of datasets.	 120 GHz Semi-Auto	 
SPICE and FAB link	Accurate AC stat model	Physical stat model / Fab-Link model
Fixed use of Typical model. Over spec was set in Corner and MC model.		

Trモデルの開発手順

パラメータ初期化

DC/CV-TEG

容量パラメータ抽出/最適化
DCパラメータ抽出/最適化
温度特性抽出/最適化

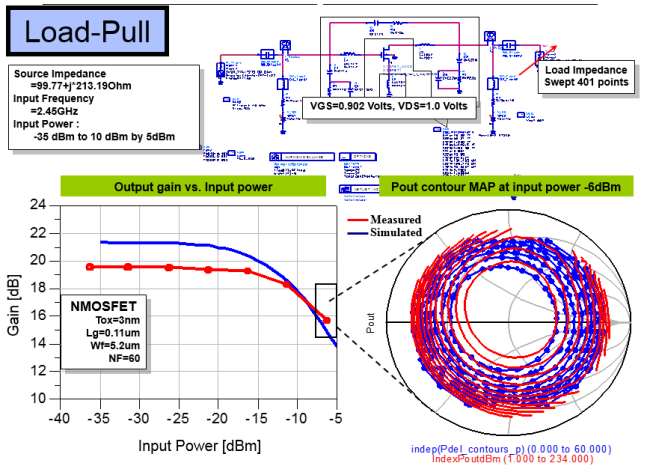


RF-TEG

RF測定値からPAD成分を
De-embedding

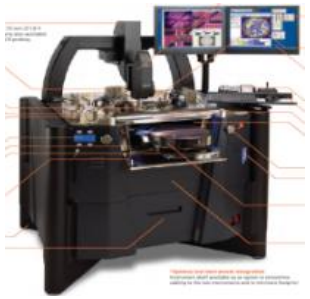
DCパラメータ最適化

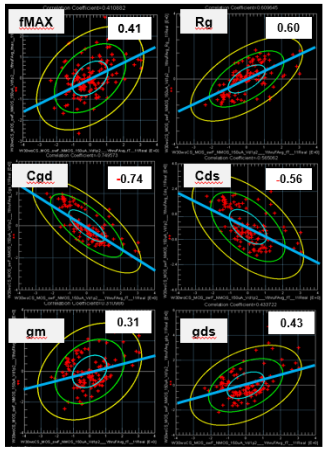
ACパラメータ最適化

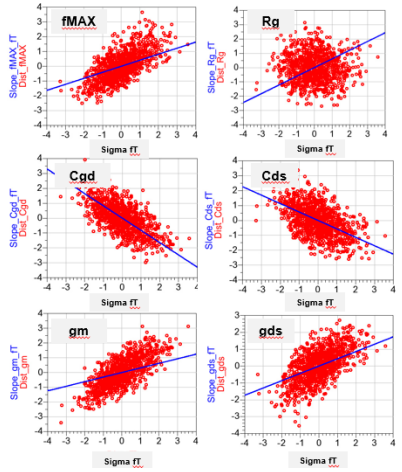


03

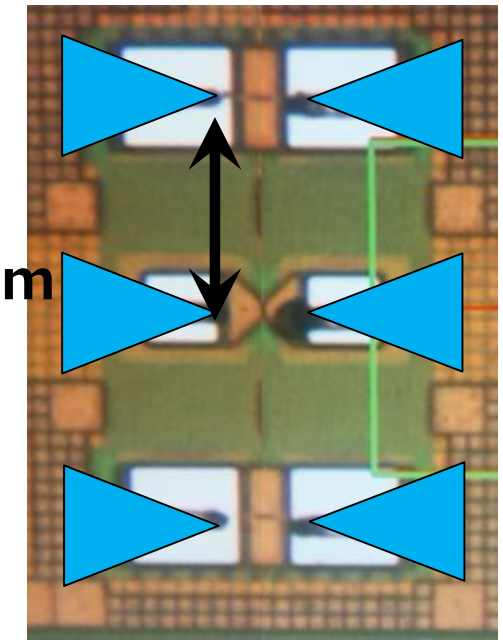
High Volume measurement



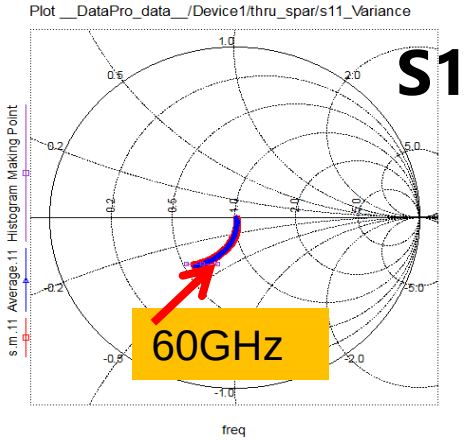


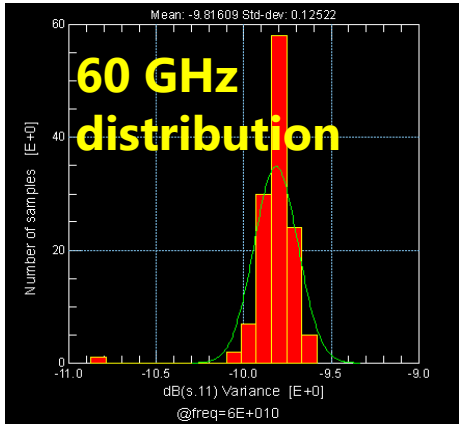


Issues of high volume millimeter-wave measurement. [1]

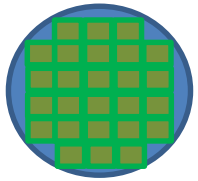


- Precise Probe skating
- Precise Wafer alignment
- Hardware Drift
  - Mandatory frequent de-embedding





RF-CMOS
12 inch test
wafer
> 100 Dies



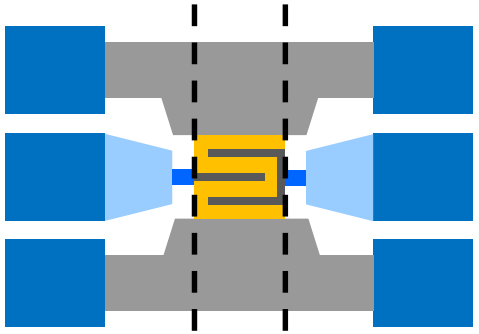
Mean=-9.80dB
Sigma=0.13dB

手動測定の時代は終わり、SパラのBigData取得が可能に。

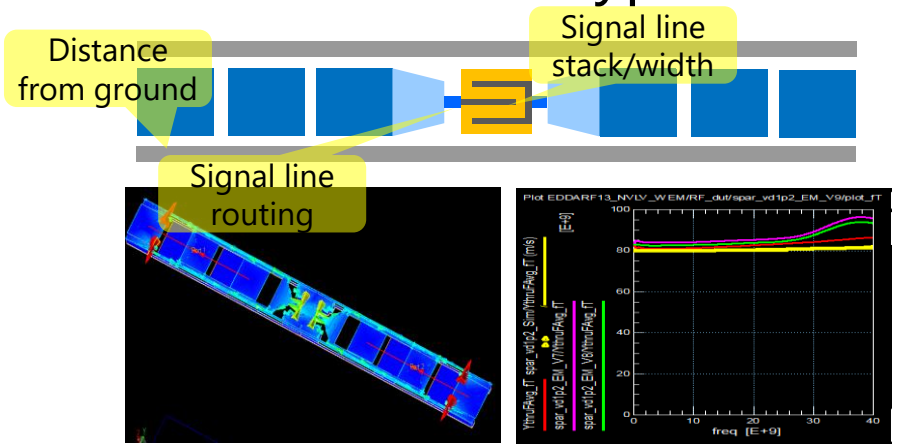
Design of scribe-type GSG test structure.

Compatibility kept upto 35GHz. Needs improvement.

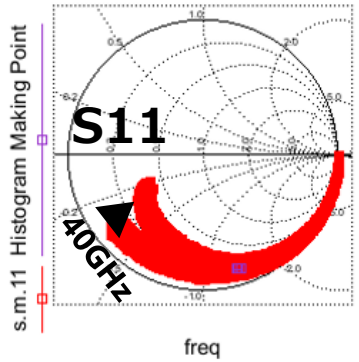
Conventional GSG

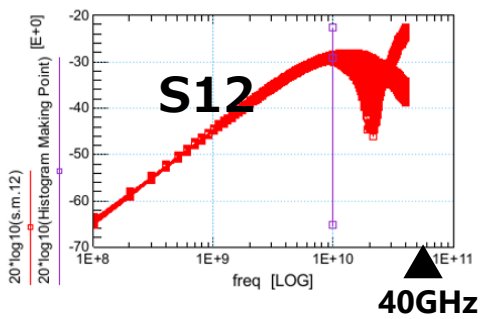


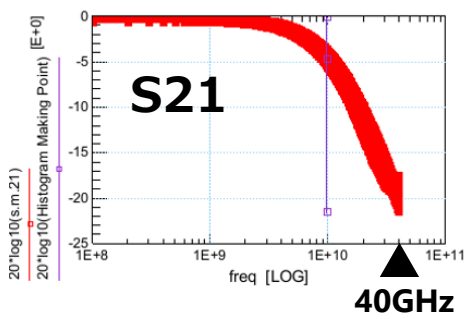
Scribe-line Type GSG

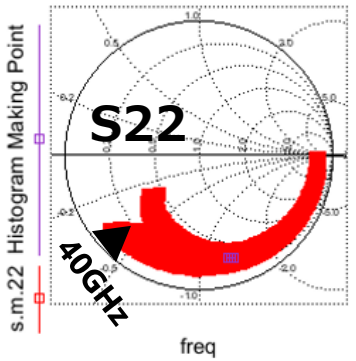


Optimized layout has been determined by SOLT de-embedding with simulated data of SHORT,OPEN and DUT patterns.



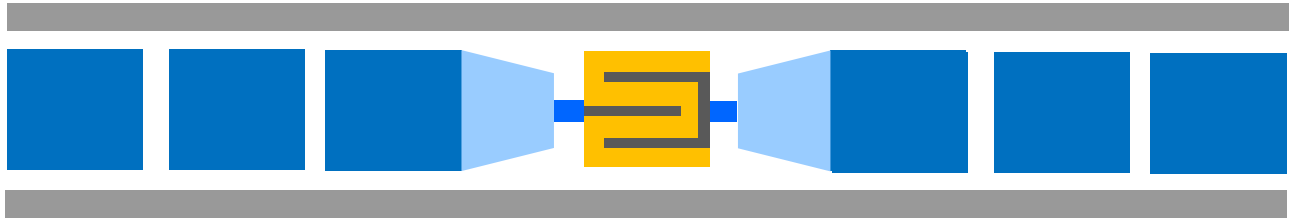






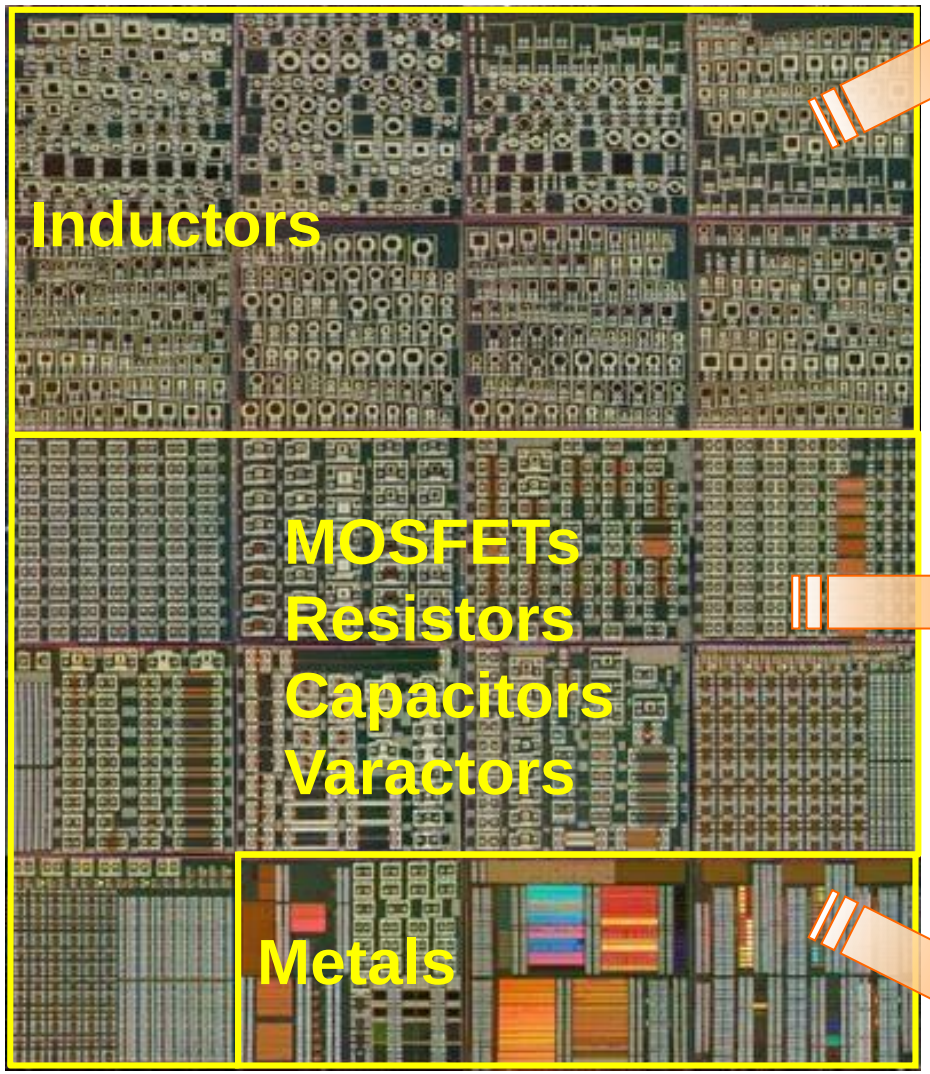
04

Test structure design for high volume measurement.



[4]

Test structure for ONE GENERATION



s-parameter evaluation for Inductor
→Equivalent circuits model
→Electro-magnetic analysis model

DC/s-parameter evaluation for MOSFETs
→Equivalent circuits model
→Spice parameter extraction
→Noise model (Flicker and RF noise)

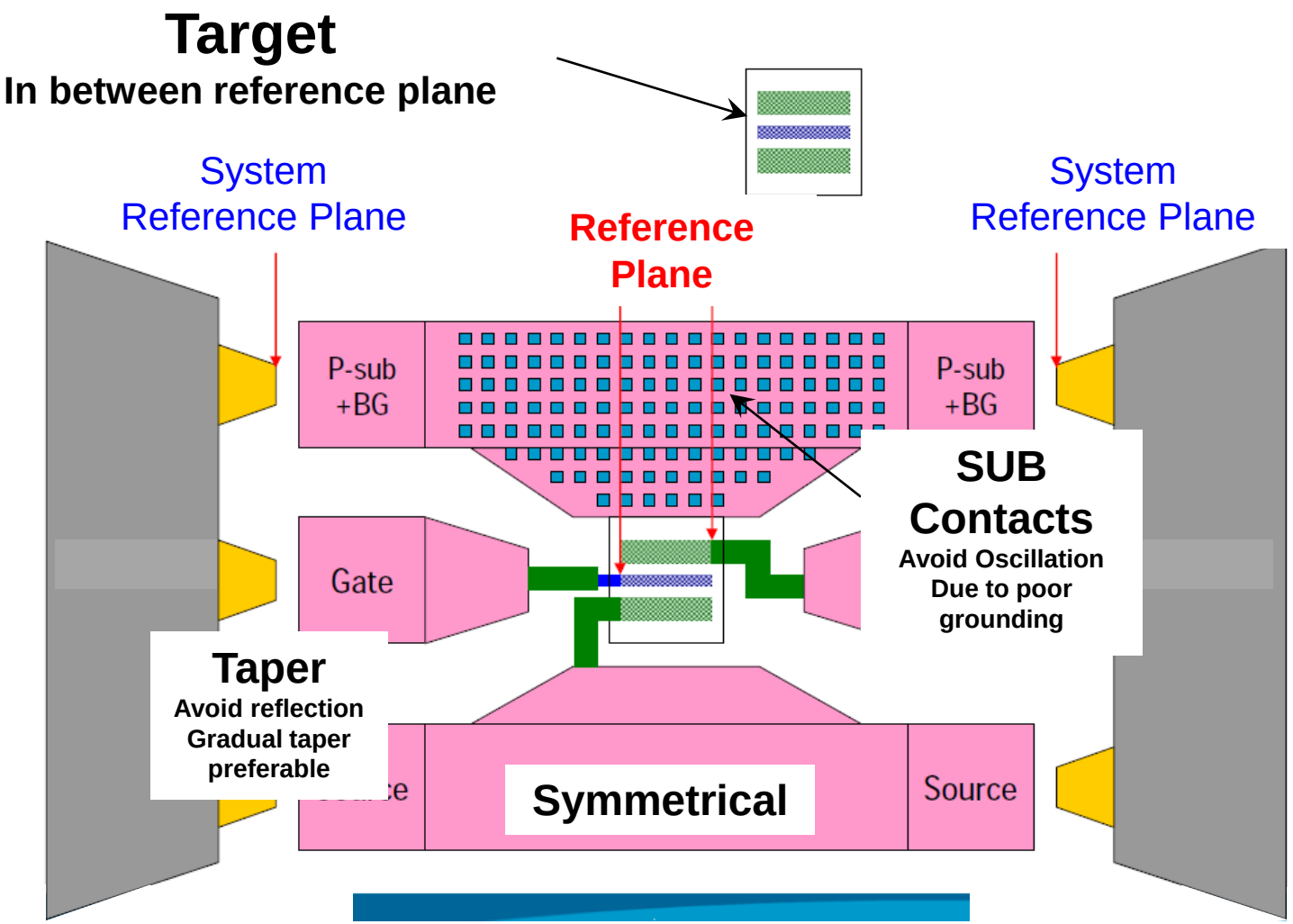
s-parameter evaluation for resistors
→Equivalent circuits model

s-parameter evaluation for capacitors
→Equivalent circuits model

CV/s-parameter evaluation for varactors
→Equivalent circuits model
→Spice parameter extraction

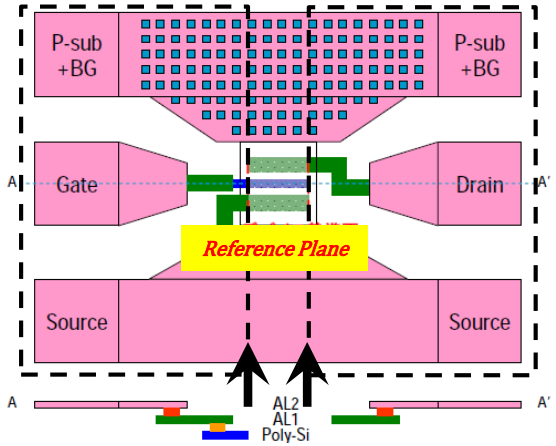
Metal-Line Evaluation
→Equivalent circuits model
→Transmission line model

GSG-Test Structure for Device Modeling

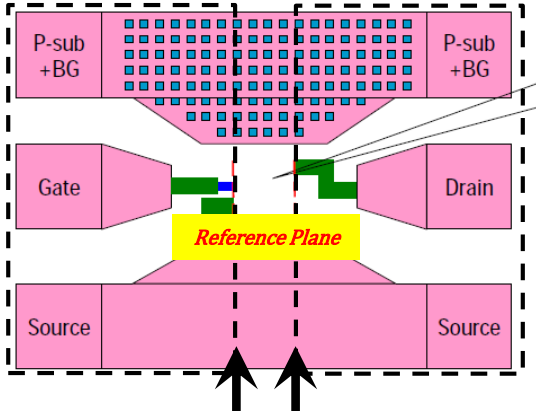


Complete Set for Precise Device Modeling

1. DUT

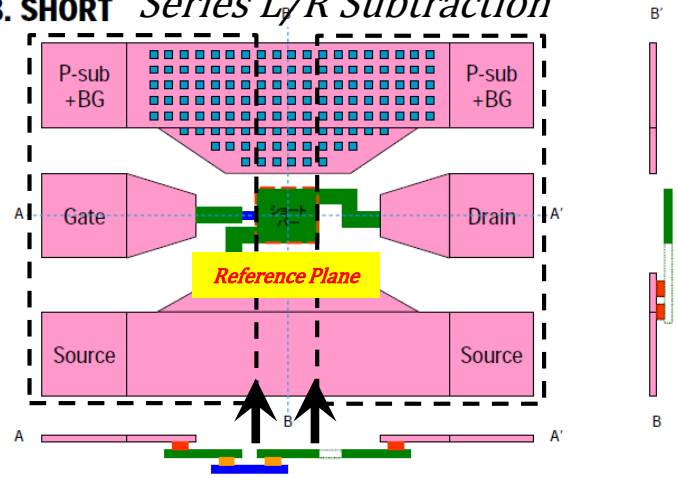


2. OPEN *Parallel C Subtraction*

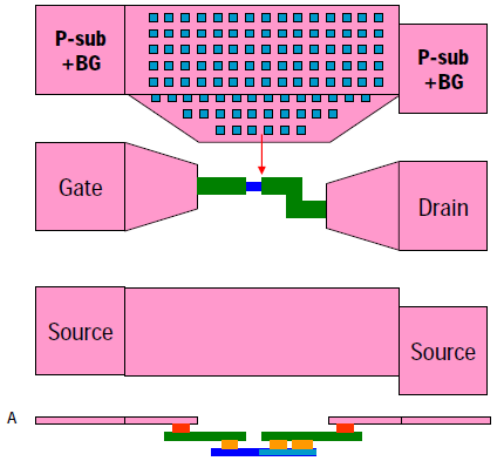


Simply remove device cell from DUT, **Chop signal line** at the point of reference plane

3. SHORT *Series L/R Subtraction*

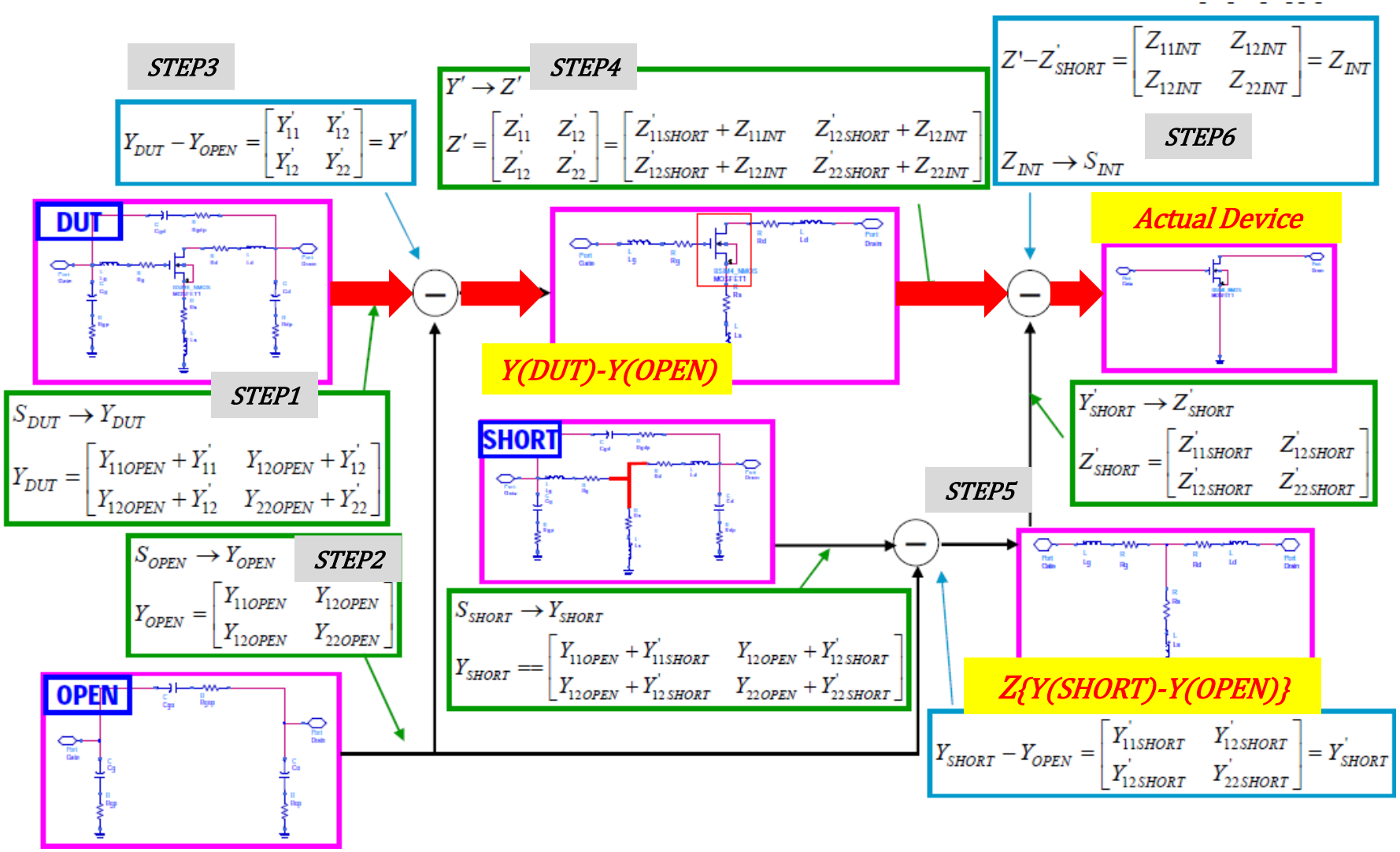


4. THRU *Verification*

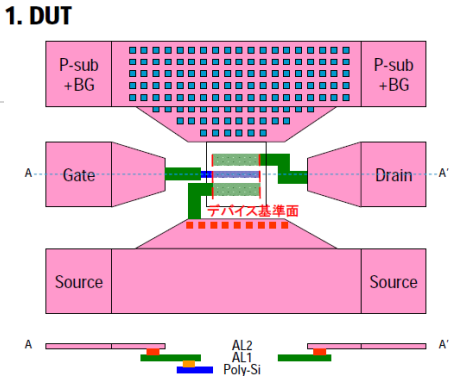


Adjust Left and Right pattern to configure THRU line.

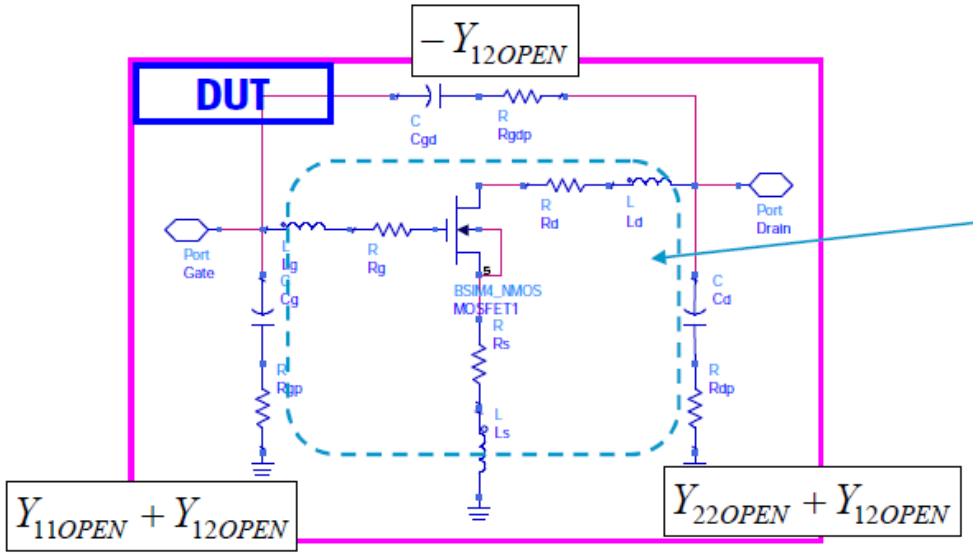
OPEN and SHORT De-embedding の手順

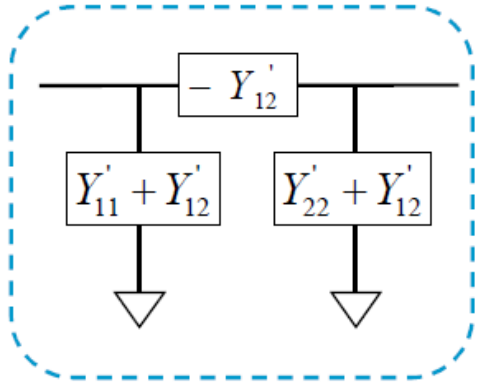


De-embedding (STEP1)



Realization of PAD capacitance in DUT data.



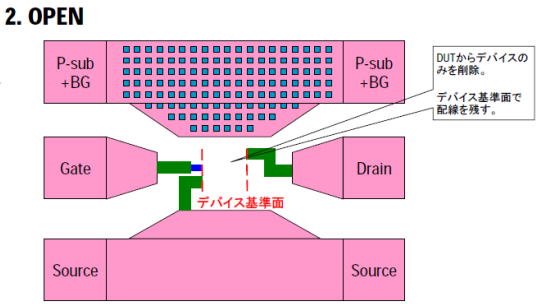


Y-matrix operation is useful to operate Π configured circuit

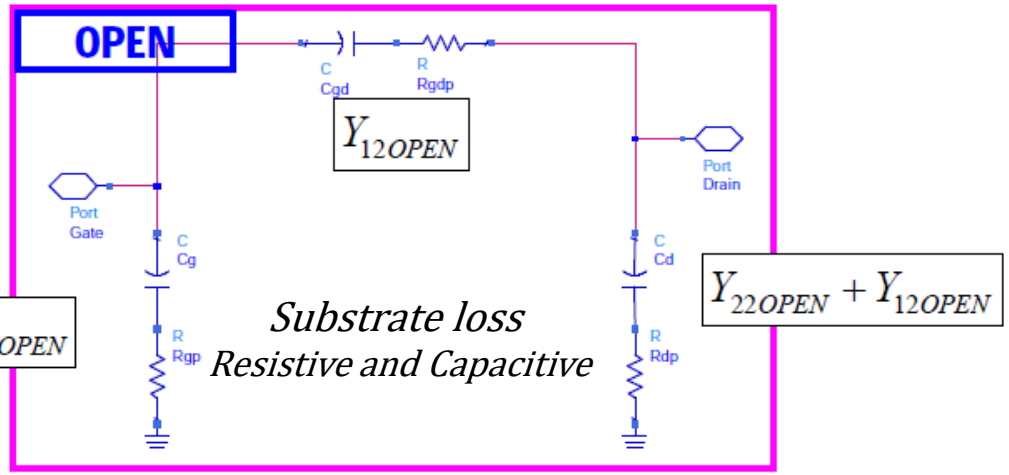
$$S_{DUT} \rightarrow Y_{DUT}$$

$$Y_{DUT} = \begin{bmatrix} Y_{11DUT} & Y_{12DUT} \\ Y_{12DUT} & Y_{22DUT} \end{bmatrix} = \begin{bmatrix} Y_{11OPEN} + Y_{11}' & Y_{12OPEN} + Y_{12}' \\ Y_{12OPEN} + Y_{12}' & Y_{22OPEN} + Y_{22}' \end{bmatrix}$$

De-embedding (STEP2)



OPEN pattern simply contain PAD related parasitic.



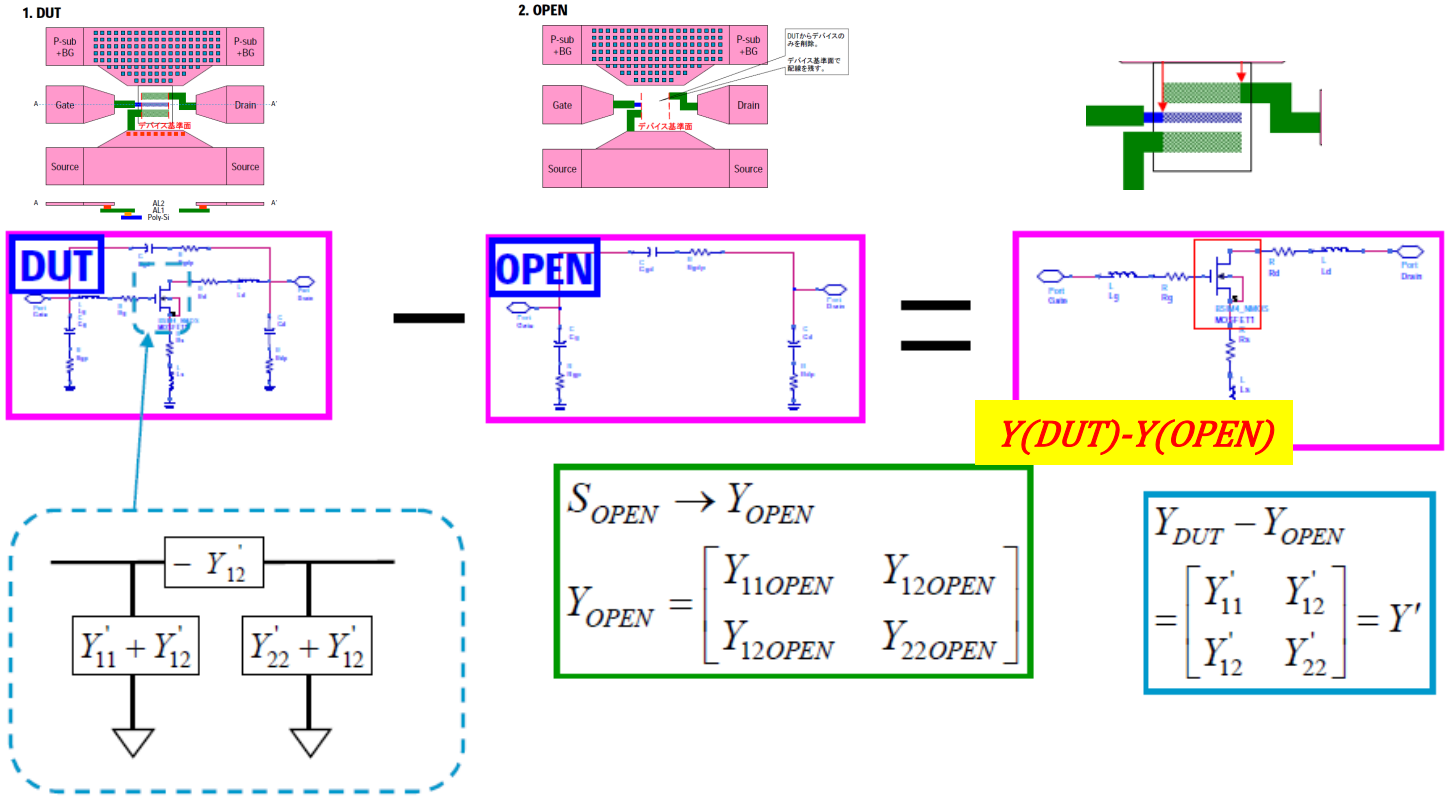
Y-matrix operation is useful to operate Π configured circuit

$$S_{OPEN} \rightarrow Y_{OPEN}$$

$$Y_{OPEN} = \begin{bmatrix} Y_{11OPEN} & Y_{12OPEN} \\ Y_{12OPEN} & Y_{22OPEN} \end{bmatrix}$$

De-embedding（STEP3)

Y(DUT)-Y(OPEN) でPADの容量を減ずる



$$-Y_{12}' \qquad Y_{11}'+Y_{12}' \qquad Y_{22}'+Y_{12}'$$

$$S_{OPEN} \rightarrow Y_{OPEN}$$

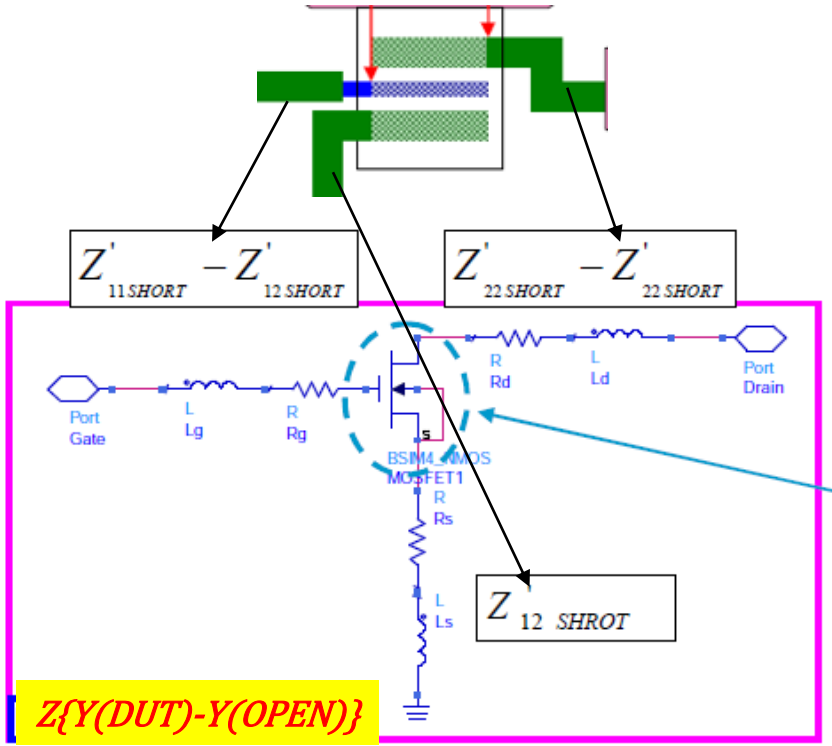
$$Y_{OPEN}=\begin{bmatrix} Y_{11OPEN} & Y_{12OPEN} \\ Y_{12OPEN} & Y_{22OPEN} \end{bmatrix}$$

$$Y_{DUT}-Y_{OPEN} = \begin{bmatrix} Y_{11}' & Y_{12}' \\ Y_{12}' & Y_{22}' \end{bmatrix} = Y'$$

$$S_{DUT} \rightarrow Y_{DUT}$$

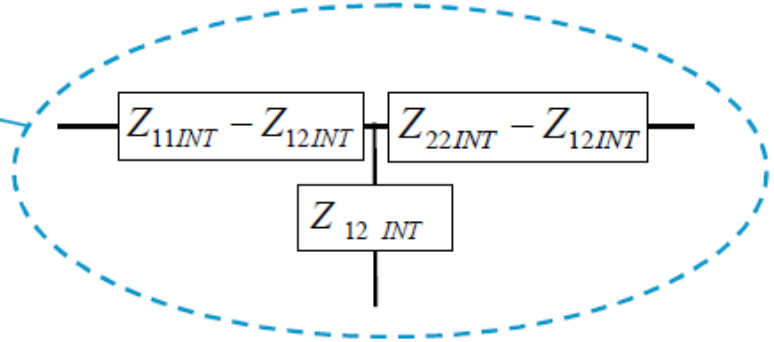
$$Y_{DUT}=\begin{bmatrix} Y_{11DUT} & Y_{12DUT} \\ Y_{12DUT} & Y_{22DUT} \end{bmatrix} = \begin{bmatrix} Y_{11OPEN}+Y_{11}' & Y_{12OPEN}+Y_{12}' \\ Y_{12OPEN}+Y_{12}' & Y_{22OPEN}+Y_{22}' \end{bmatrix}$$

De-embedding（STEP4)



STEP3後の残留成分

After STEP3 operation, transistor and series L and R of unwanted wiring are left.

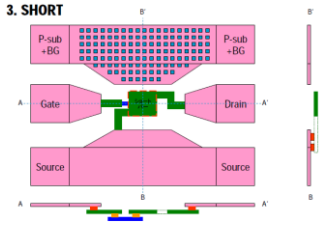


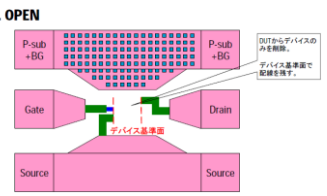
$$Y' \rightarrow Z'$$

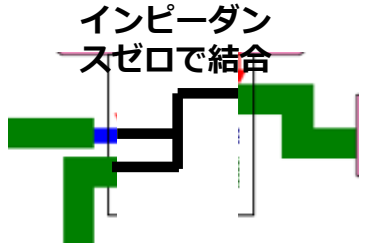
$$Z' = \begin{bmatrix} Z'_{11} & Z'_{12} \\ Z'_{12} & Z'_{22} \end{bmatrix} = \begin{bmatrix} Z'_{11SHORT} + Z_{11INT} & Z'_{12SHORT} + Z_{12INT} \\ Z'_{12SHORT} + Z_{12INT} & Z'_{22SHORT} + Z_{22INT} \end{bmatrix}$$

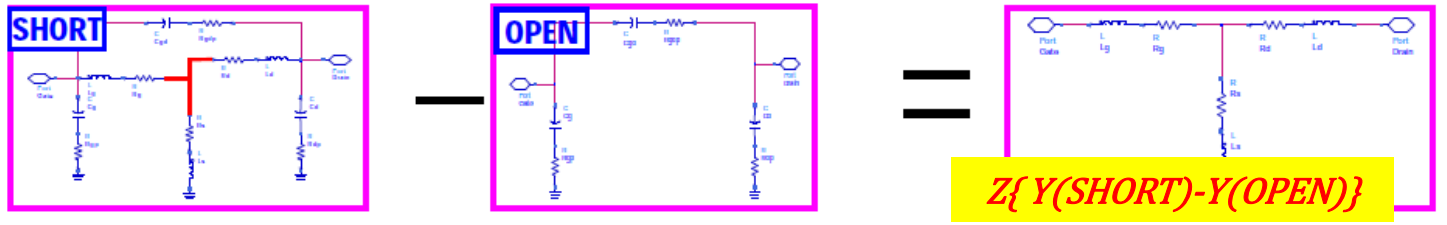
De-embedding （STEP5）

配線成分を見える化









$$S_{SHORT} \rightarrow Y_{SHORT}$$

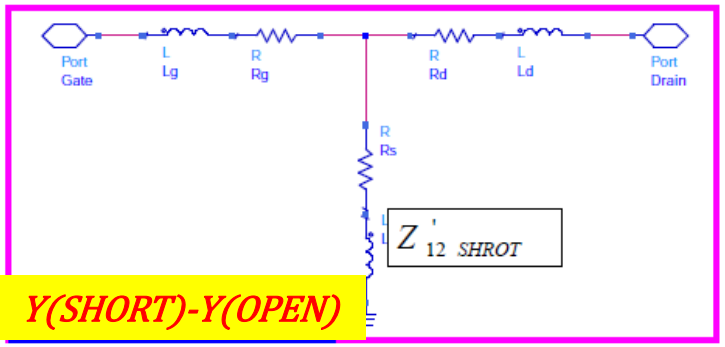
$$Y_{SHORT} = \begin{bmatrix} Y_{11OPEN} + Y'_{11SHORT} & Y_{12OPEN} + Y'_{12SHORT} \\ Y_{12OPEN} + Y'_{12SHORT} & Y_{22OPEN} + Y'_{22SHORT} \end{bmatrix}$$

$$Y_{SHORT} - Y_{OPEN} = \begin{bmatrix} Y'_{11SHORT} & Y'_{12SHORT} \\ Y'_{12SHORT} & Y'_{22SHORT} \end{bmatrix} = Y'_{SHORT}$$

Unwanted series L and R can be obtained by Z{ Y(SHORT)-Y(OPEN) }

$$Z'_{11SHORT} - Z'_{12SHORT}$$

$$Z'_{22SHORT} - Z'_{22SHORT}$$



Z-matrix operation is useful to operate T configured circuit

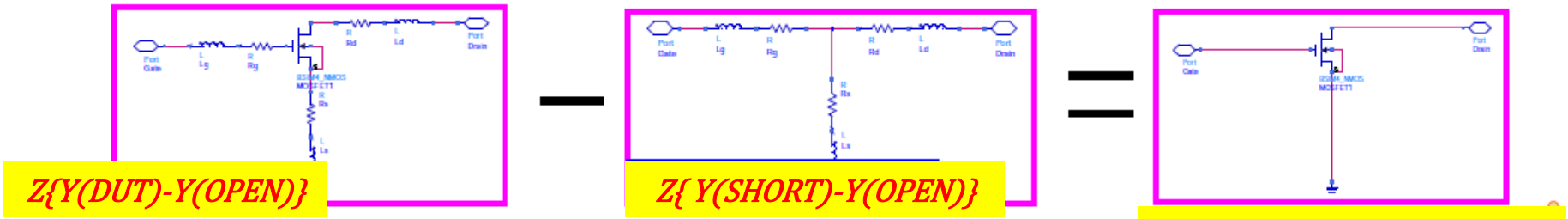
$$Y'_{SHORT} \rightarrow Z'_{SHORT}$$

$$Z'_{SHORT} = \begin{bmatrix} Z'_{11SHORT} & Z'_{12SHORT} \\ Z'_{12SHORT} & Z'_{22SHORT} \end{bmatrix}$$

De-embedding (STEP6)

(STEP4)の状態から(STEP5)の結果を減ずる→トランジスタの性能。

STEP4 *STEP5*



Z{Y(DUT)-Y(OPEN)} *Z{ Y(SHORT)-Y(OPEN)}* *Z matrix of TRANSISTOR*

$$Y' \rightarrow Z'$$

$$Z' = \begin{bmatrix} Z'_{11SHORT} + Z_{11INT} & Z'_{12SHORT} + Z_{12INT} \\ Z'_{12SHORT} + Z_{12INT} & Z'_{22SHORT} + Z_{22INT} \end{bmatrix}$$

$$Y'_{SHORT} \rightarrow Z'_{SHORT}$$

$$Z'_{SHORT} = \begin{bmatrix} Z'_{11SHORT} & Z'_{12SHORT} \\ Z'_{12SHORT} & Z'_{22SHORT} \end{bmatrix}$$

$$Z' - Z'_{SHORT} = \begin{bmatrix} Z_{11INT} & Z_{12INT} \\ Z_{12INT} & Z_{22INT} \end{bmatrix} = Z_{INT}$$

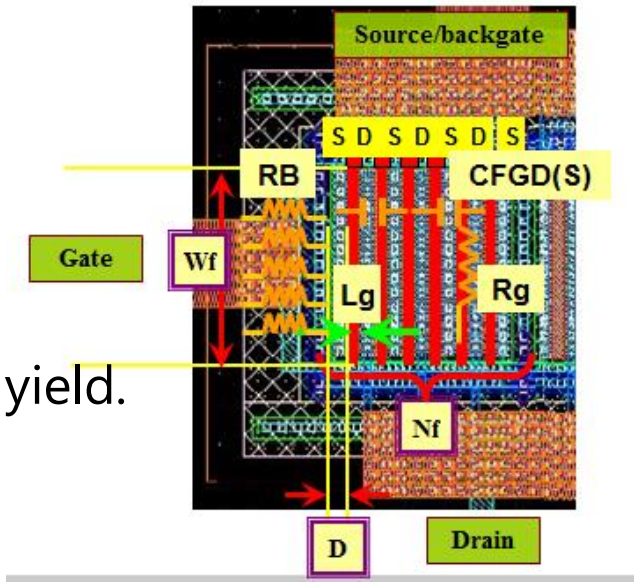
$$Z_{INT} \rightarrow S_{INT}$$

Ready for unveil device behavior !

03

Fab-linked scalable compact model.

- How is the typical model specs ?
- Linking MC model and In-line data.
- How to corporate with factory for high yield.



What is needed for RF-CMOS compact model ?

Scalable and compact

For portability, parasitic elements should be scalable function of

- Lg (Gate Length) and Wf (Finger Length)
- NF (Finger Numbers)
- Length Of Diffusion (SA,SB,SD)

Accurate for all design purpose

LNA (NQS effect, Thermal noise)

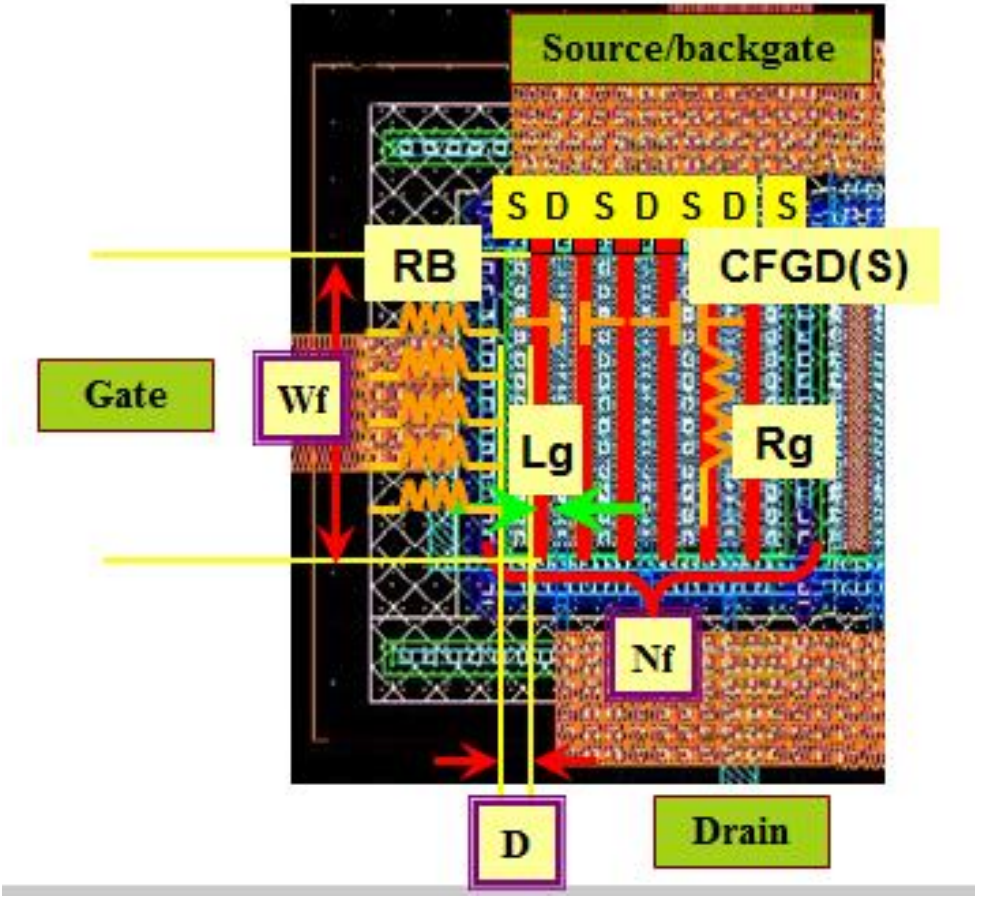
- Linear: S-parameters > 100GHz
  - De-embedding: SOLT ? TRL ?

VCO and Mixer (Harmonic distortion, Flicker noise)

- Flicker noise close to the carrier.
- ACPR, EVM

Power amplifier

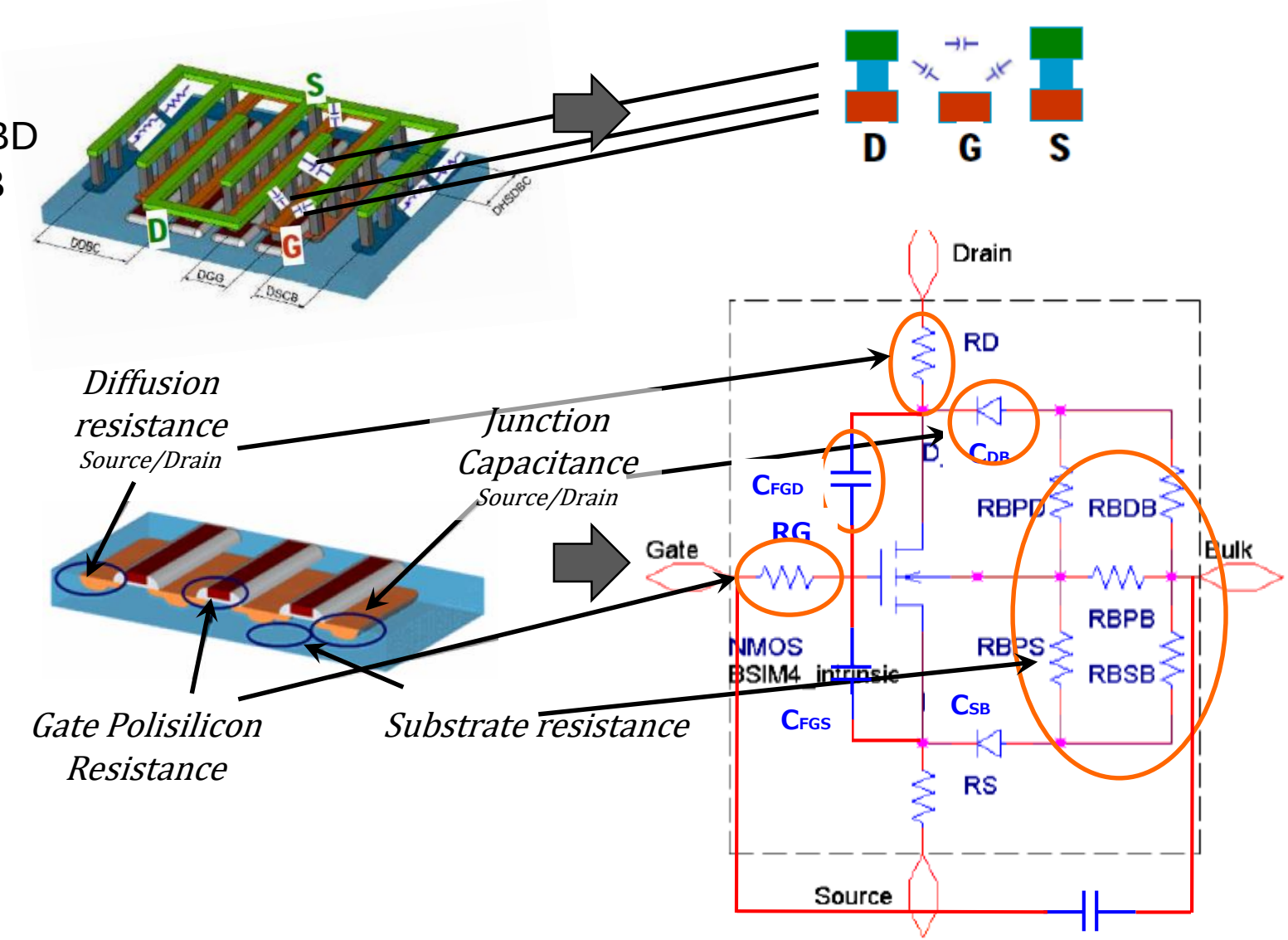
- Self Heating
- Load-pull



Physical configuration of RF MOSFET

Variables need to scale

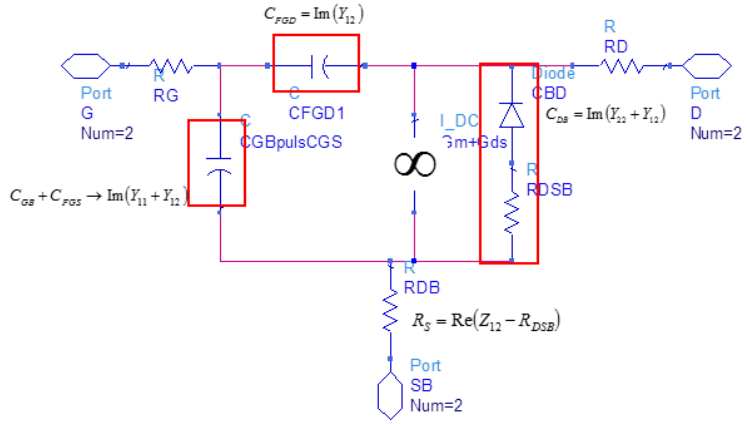
Gate resistance : RG, RD, RS
Overlap capacitance : CFGD, CFGS, CBD
Substrate resistance : RBPD/S, RBD/SB
RBPB



Cold measurement helps to extract layout parasitic. [1]

Source and Back-gate grounded

VG=VD=VS=VB=0



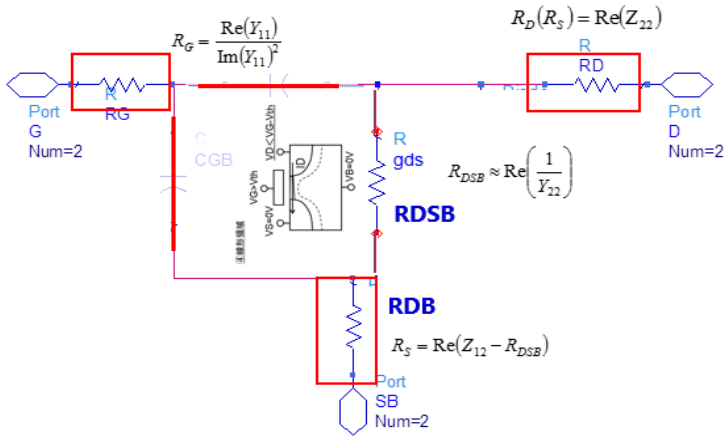
$$C_{BD} = \frac{imag(y_{22}+y_{12})}{2\pi \cdot freq} \qquad C_{GB} = \frac{imag(y_{11}+y_{12})}{2\pi \cdot freq}$$

$$C_{FGD} = \frac{-imag(y_{12})}{2\pi \cdot freq} \qquad C_{ox} = \frac{imag(y_{11}-y_{12})}{2\pi \cdot freq}$$

$$R_{dsb} = Re\left(\frac{1}{y_{22}}\right)$$

Source and Back-gate grounded

VG=VDD, VD=low, VS=VB=0



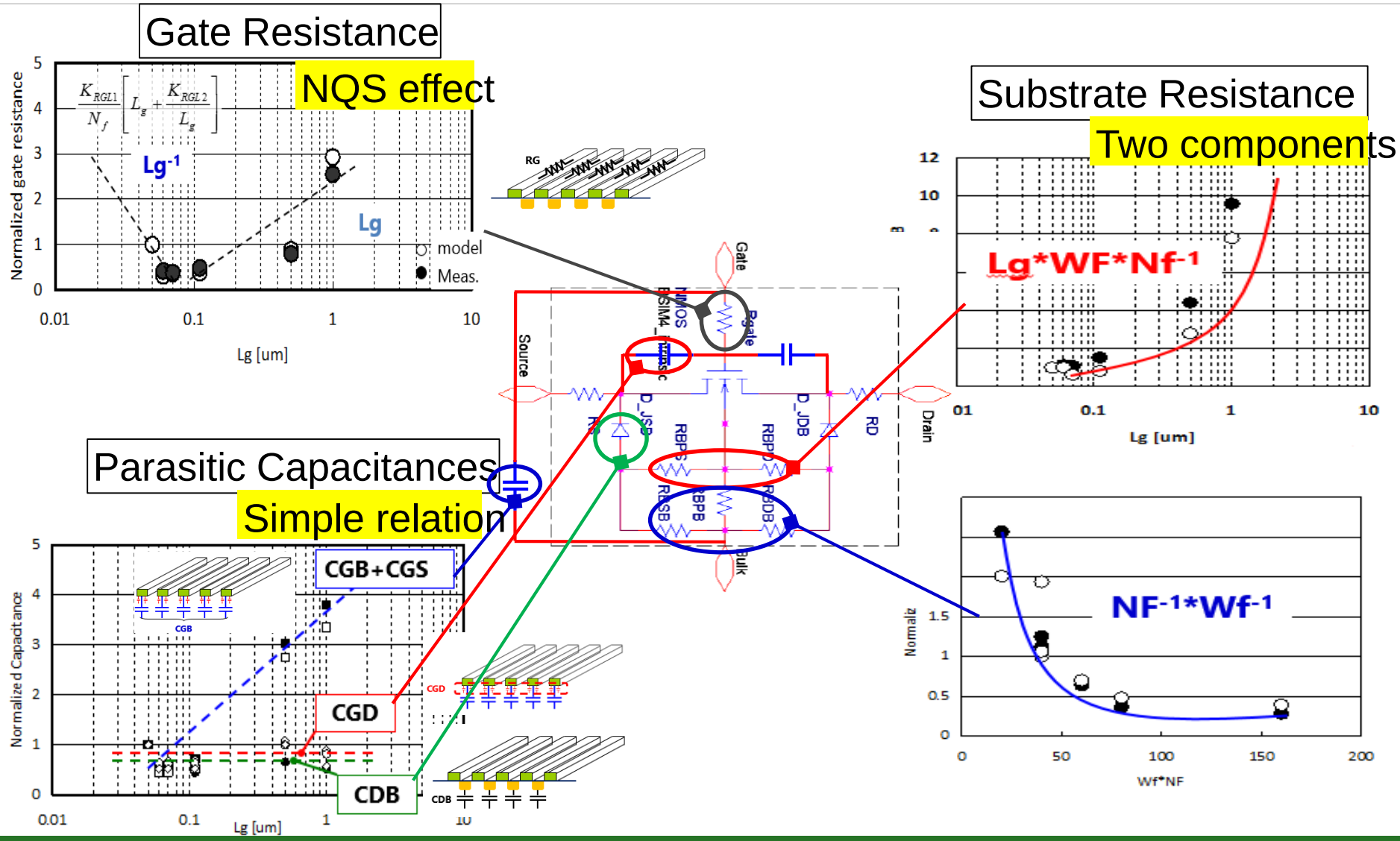
$$R_G = \frac{Re(y_{11})}{Im(y_{11})^2}$$

$$R_D = Re(z_{11})$$

$$R_S = Re(z_{12}) - R_{dsb}$$

Good indicator of transistor monitoring.

Scalable parasitic model vs. measurement data [1]



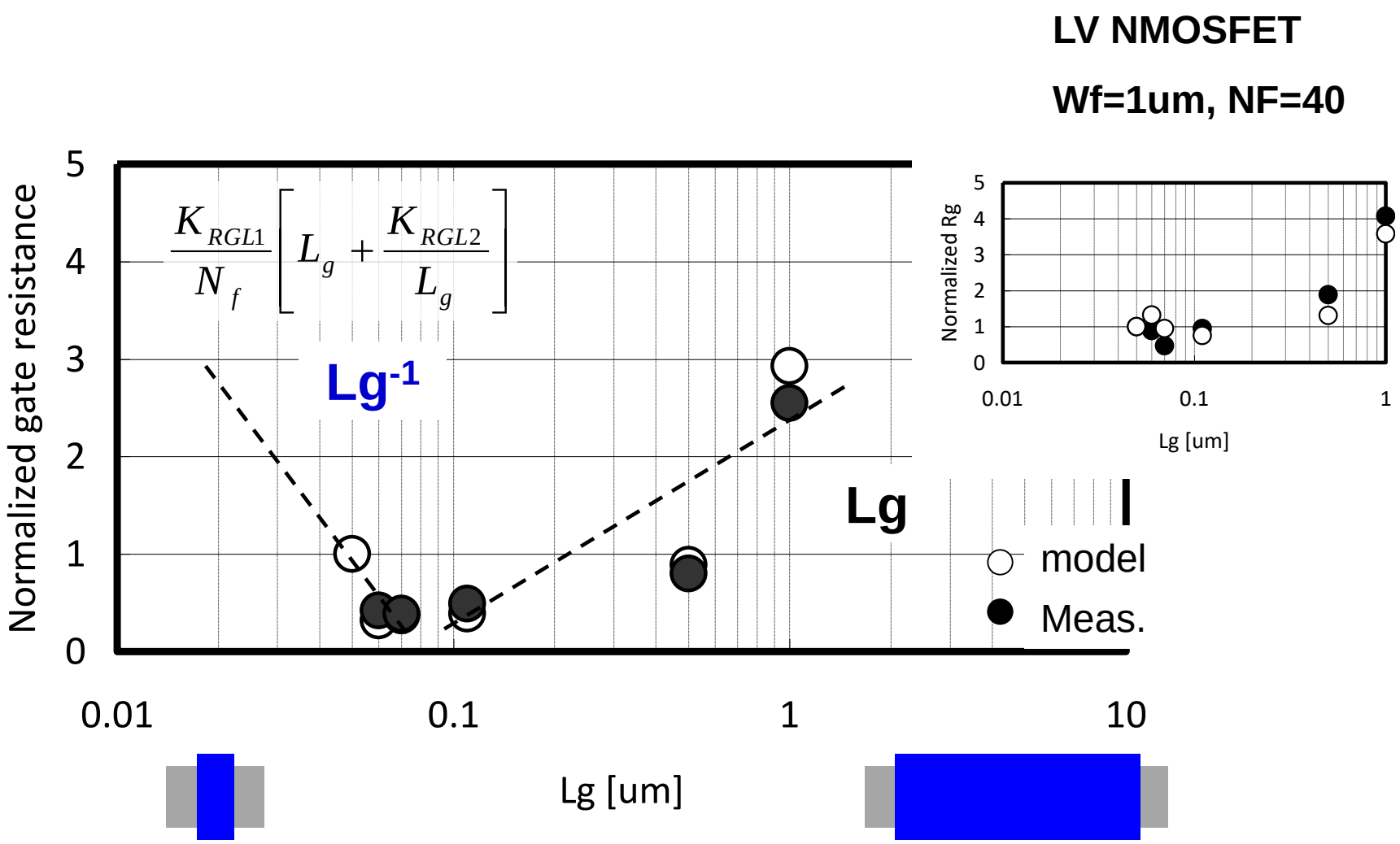
Layout dependency works well with many CMOS generations (130nm to 40nm.)

Q1 Does RG scaling follows classical ohmic-law ?

$$R_G = \rho_{rg} k \cdot \frac{Wf}{Lg \cdot Nf}$$

K : constant depending on the configuration of gate contact

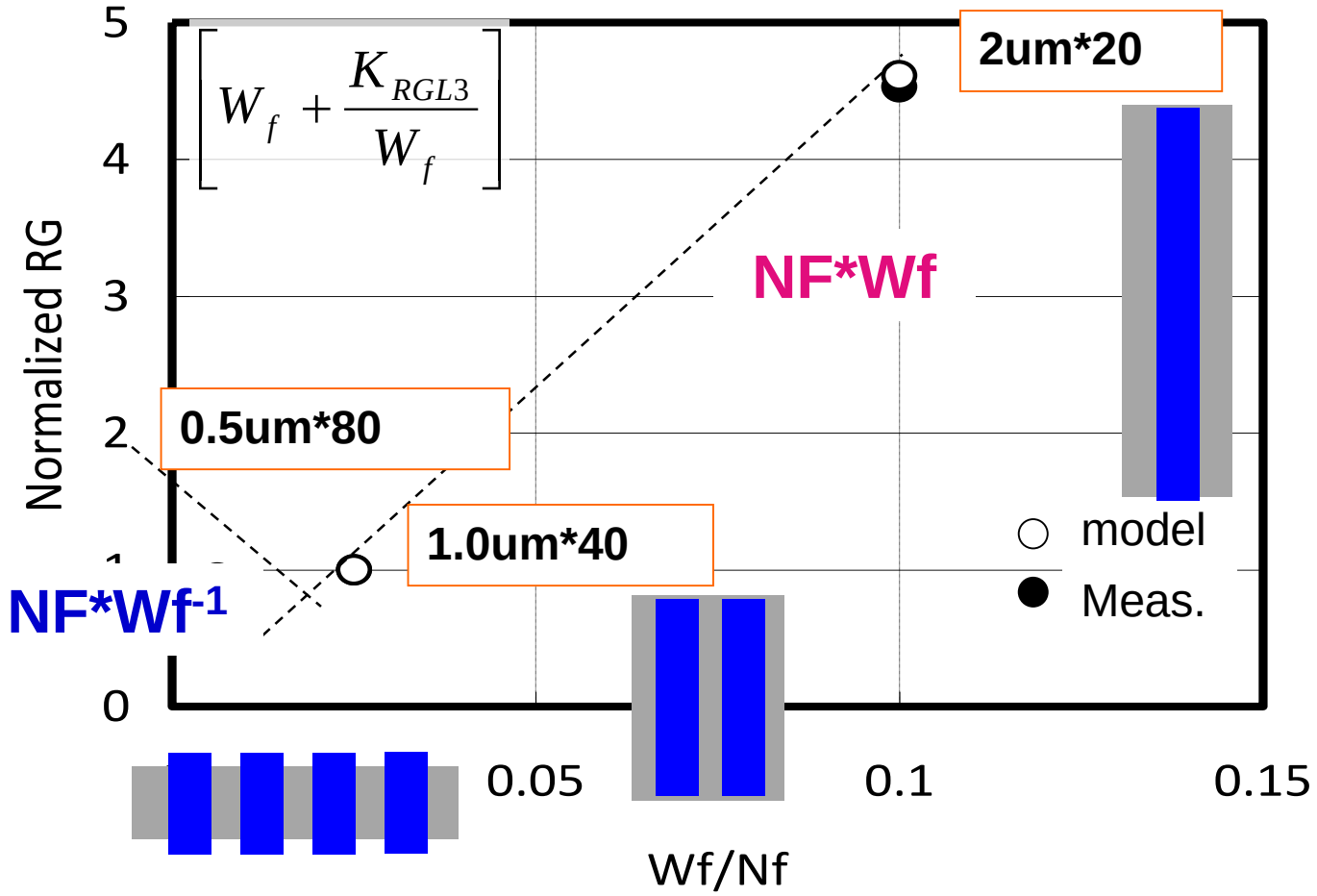
NO : Gate resistance behaves complex behavior



Scaling dependence of **Rg** on gate-length (**Lg**)

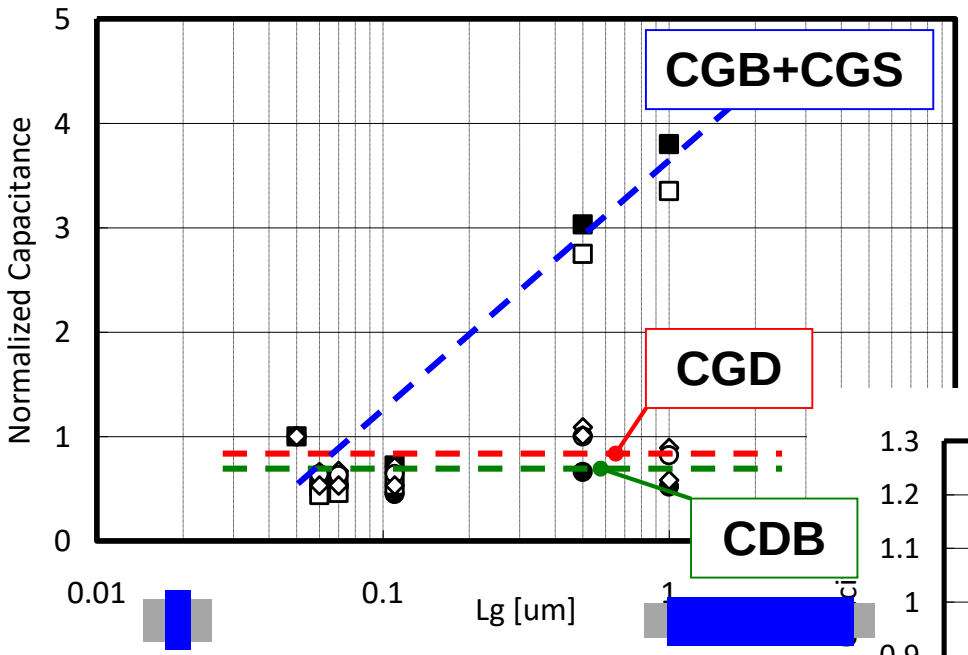
Scaling dependence of Rg on Wf/Nf

NMOSFET
Lg=50nm
Wf*NF=40um

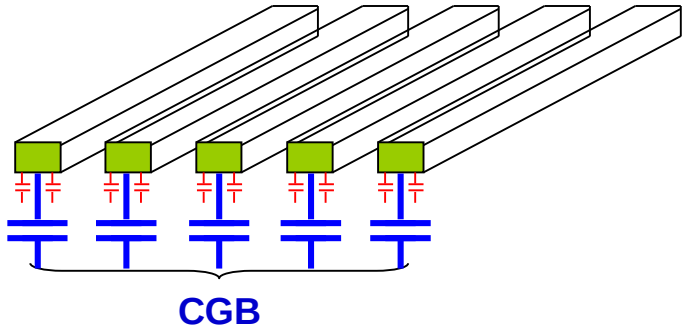


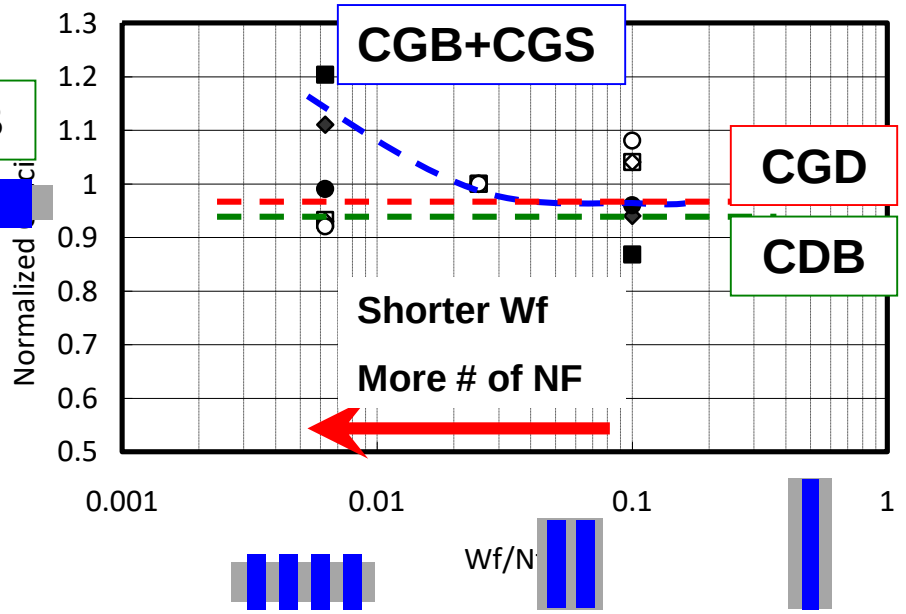
Q2 Does capacitance scaling has unique behavior ?

NO : It is NOT unique behavior.



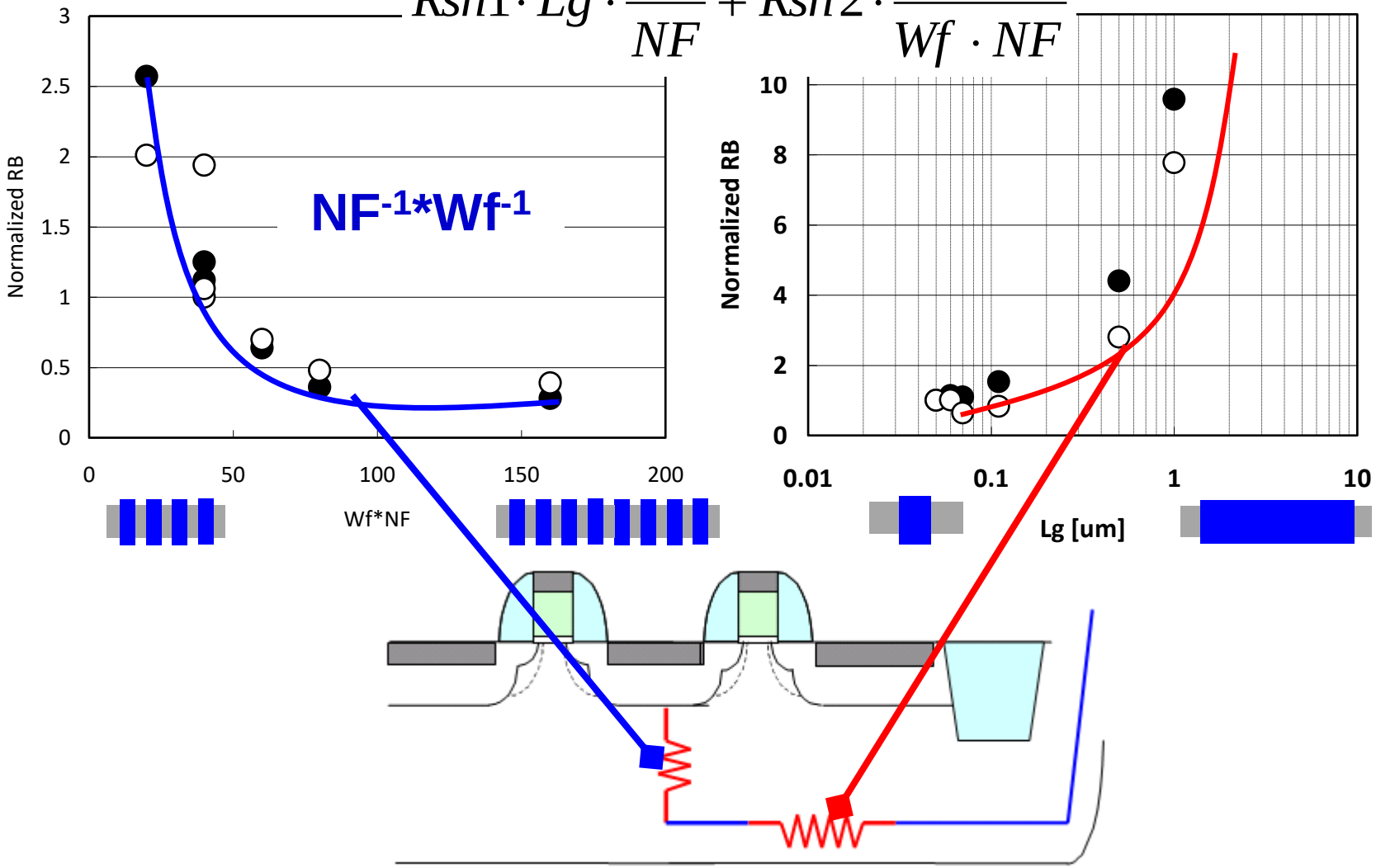
$$C_{GD} \rightarrow \mathrm{Im}(Y_{12})$$
$$C_{DB} \rightarrow \mathrm{Im}(Y_{22} + Y_{12})$$
$$C_{GB} + C_{GS} \rightarrow \mathrm{Im}(Y_{11} + Y_{12})$$





Observation of the RB scaling

$$Rsh1 \cdot Lg \cdot \frac{Wf}{NF} + Rsh2 \cdot \frac{1}{Wf \cdot NF}$$

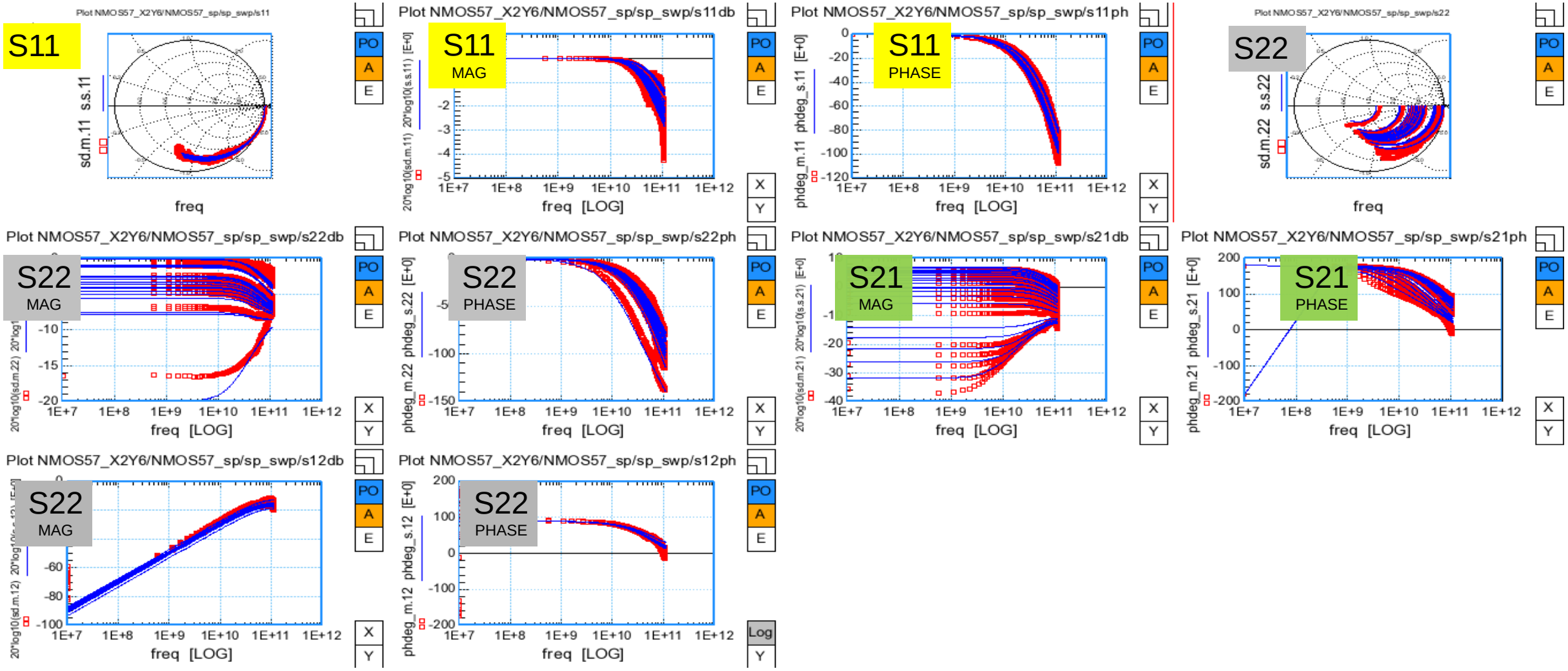


RF-CMOS modeling summary

Component name	Item name	Geometric dependency
NQS Gate resistance	RG	$\frac{K_{RGL1}}{N_f}\left[L_g+\frac{K_{RGL2}}{L_g}\right]\left[W_f+\frac{K_{RGL3}}{W_f}\right]$
G-B capacitance	CGB	$CGB = K_{CGB}\cdot Lg\cdot Nf$
G-D,G-S overlap capacitance	CFGD CFGS	$K_{RCL}W_f N_f$
Substrate resistance	RSUB1 RSUB2 RSUB3 RSUB4	$Rsh1\cdot Lg\cdot\frac{Wf}{NF}+Rsh2\cdot\frac{1}{Wf\cdot NF}$

K_{CGB},K_{RGL1}, K_{RGL2}, K_{RGL3},K_{RCL},K_{Rsh1}, K_{Rsh2} : Constants

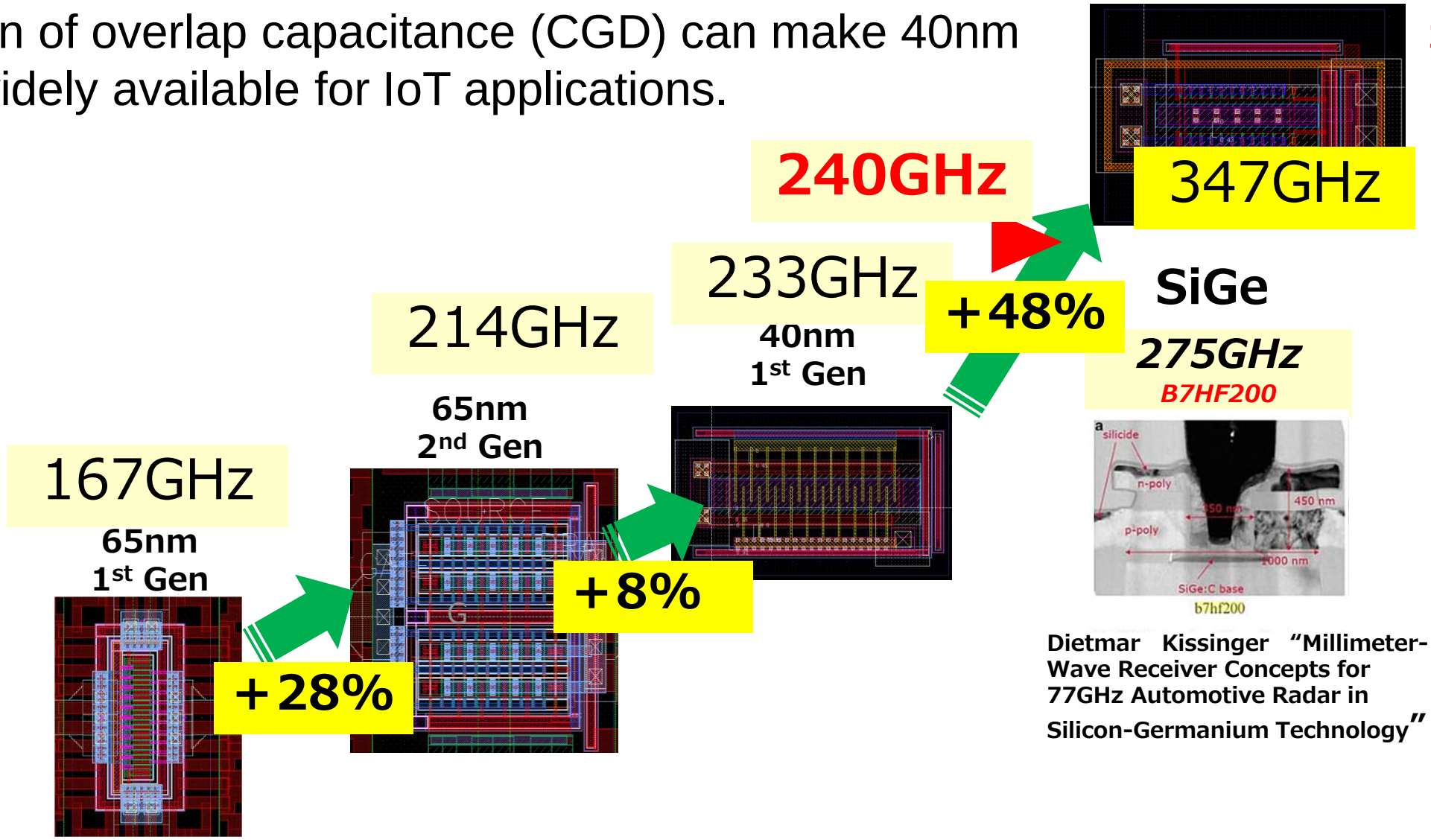
110GHz S-parameter model vs measurement.



Existing modeling technology is applicable up to 110GHz

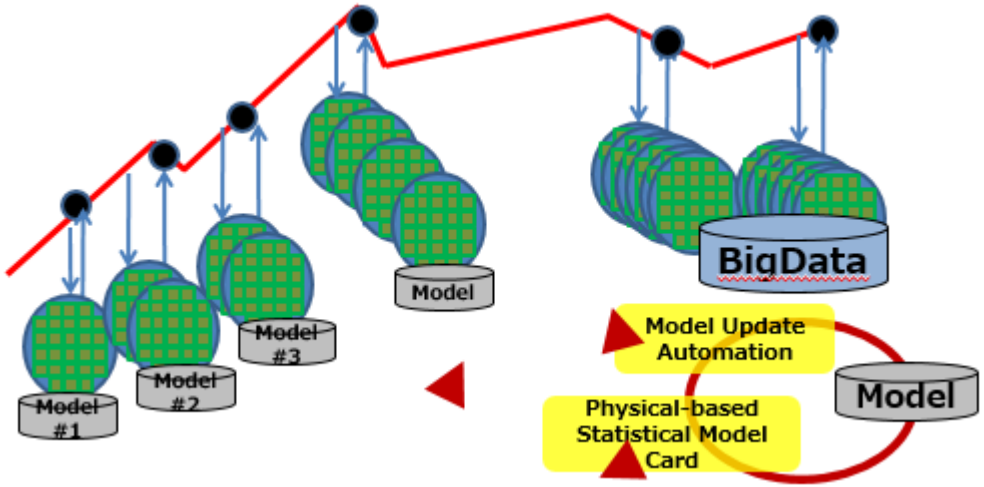
fMAX optimization of RF-NMOSFETs

Reduction of overlap capacitance (CGD) can make 40nm CMOS widely available for IoT applications.



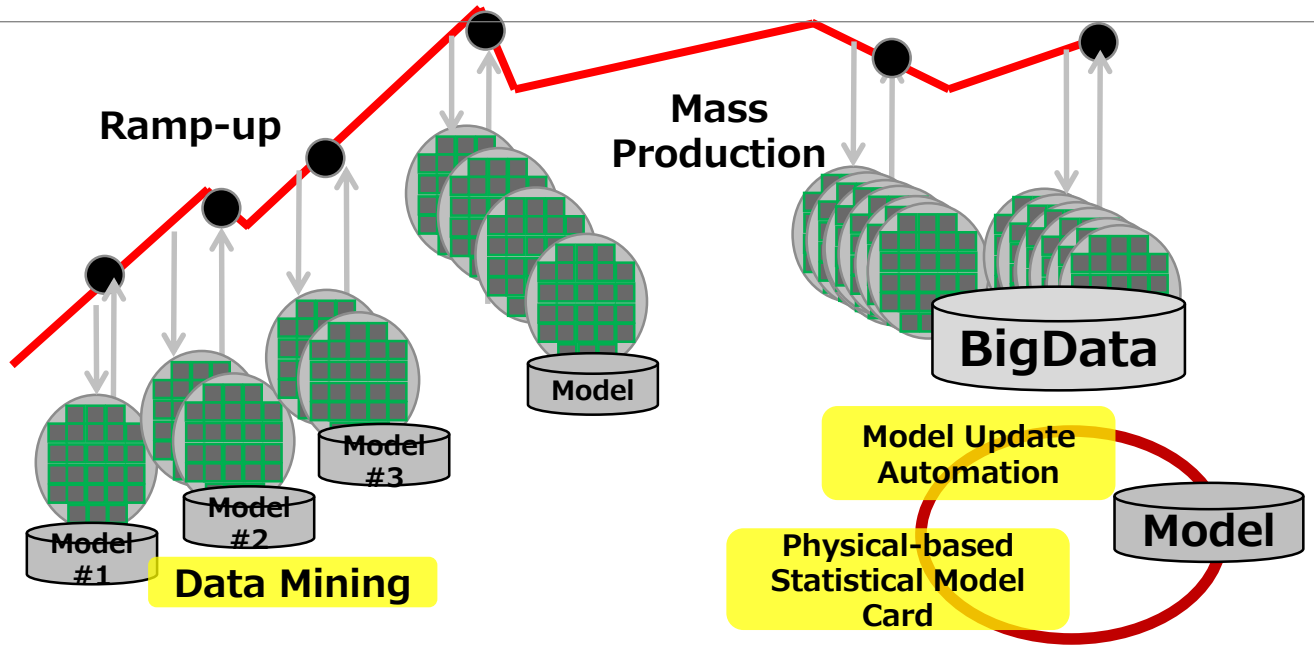
04

Synchronization of compact model with latest FAB output.



Solutions to Support RF circuit production chain.

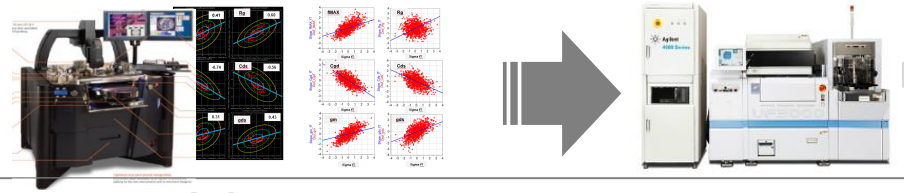
Fab Linked Compact Model



Data mining

Accurate Fab-Link model

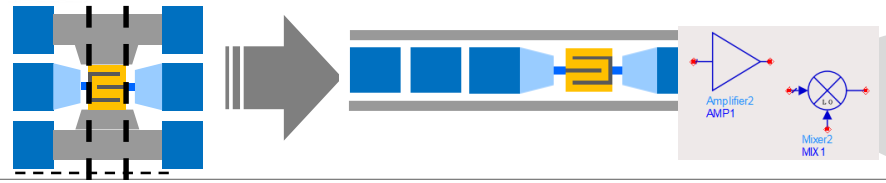
High Volume measurement



Shorter Measurement TAT **ET data** selection.

Reduction of Measurement TAT

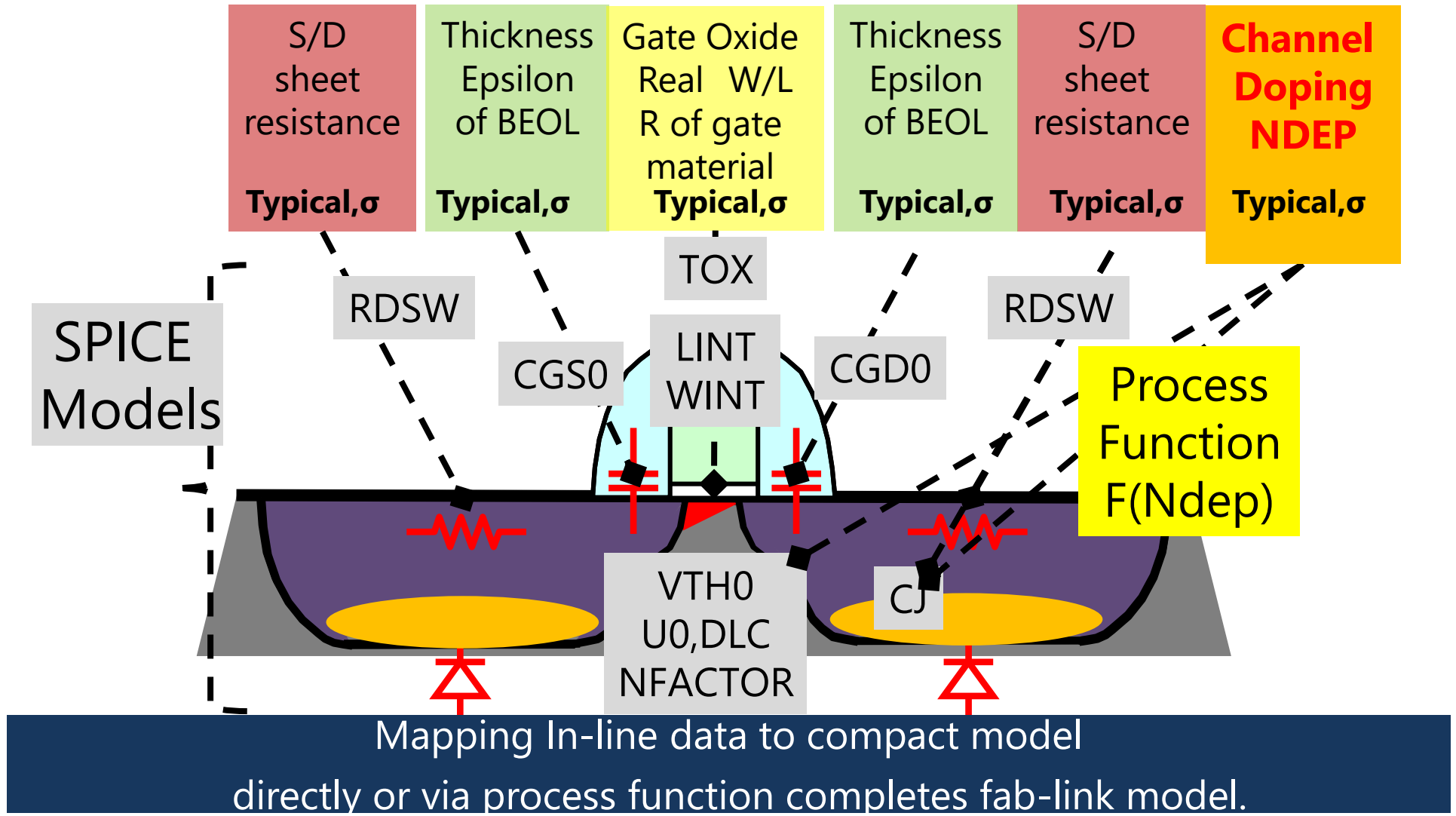
Layout of Test structure



Link Device-Small circuit -Products

Line up ?

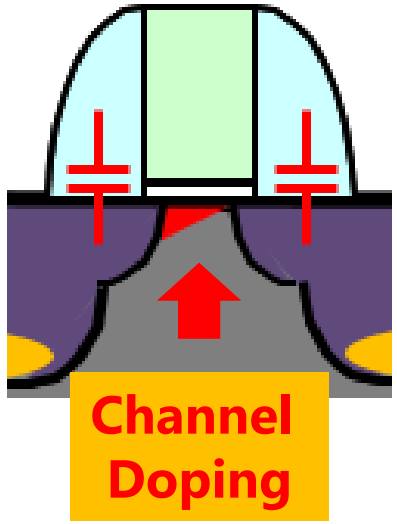
Fab-link model parameters vs In-line data.



How Process function looks like ?

In-line data ➡ Process functions ➡ Map to Compact Model

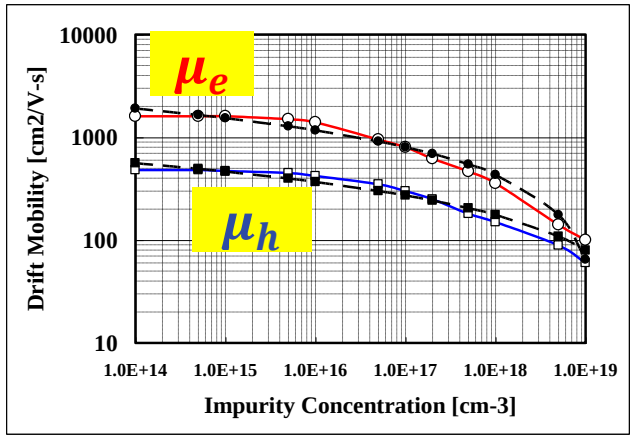
NDEP



$F\mu_{e/h}(N_{DEP}) \Rightarrow \mu_0$

$F\mu_{e/h}(N_{DEP})$

$= \mu_{oe/oh} - K_{e1/h1} \cdot log \frac{N_{DEP}}{K_{e2/h2}}$



$$U_0 = U_0 \cdot \frac{\mu_0(N_{DEP})}{\mu_0(N_{DEP0})}$$

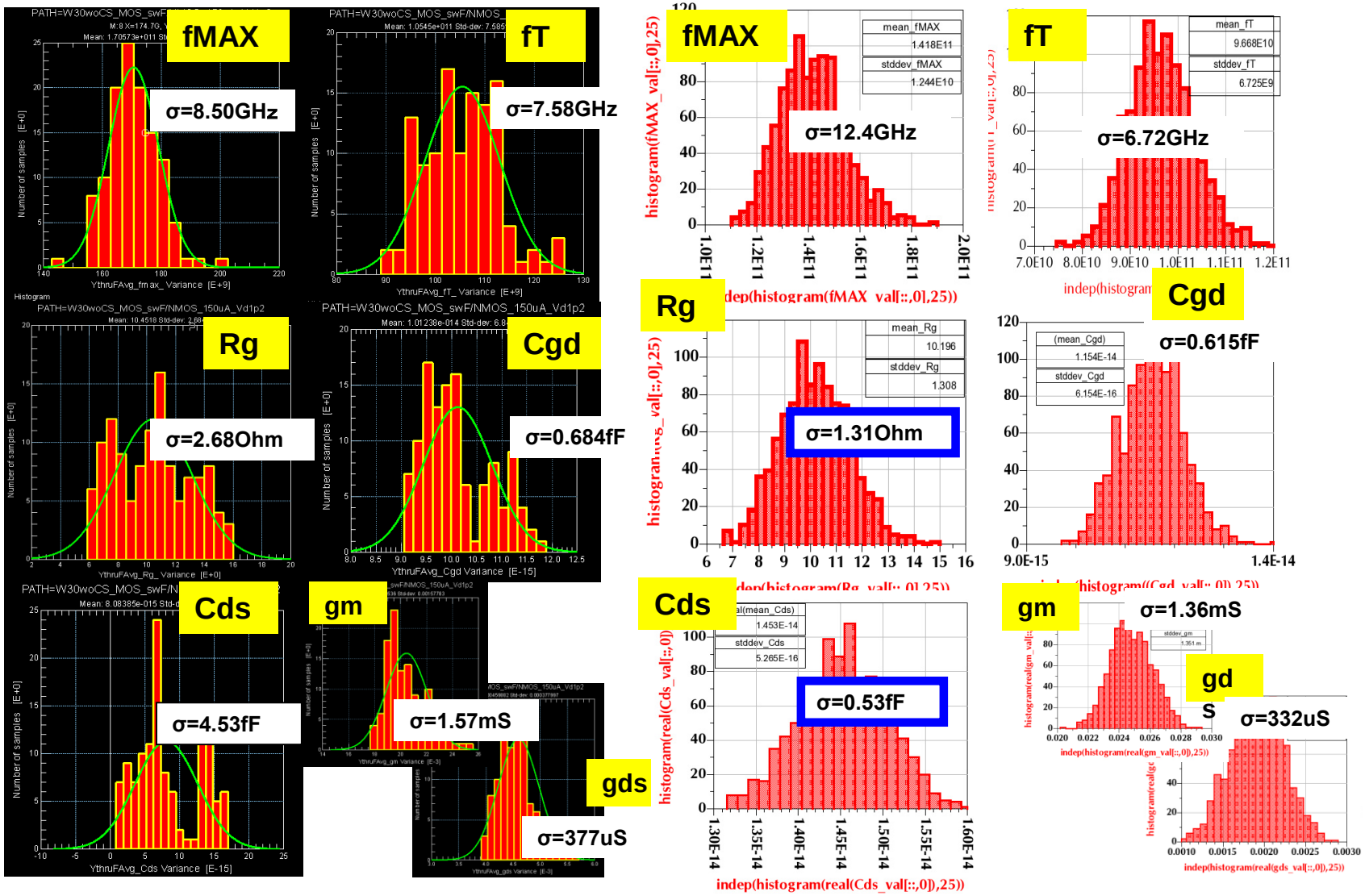
$$C_J = C_J \cdot \sqrt{\frac{N_{DEP}}{N_{DEP0}} \frac{lnN_D + lnN_{DEP0}}{lnN_D + liN_{DEP} - 2 \cdot n_i}}$$

.....

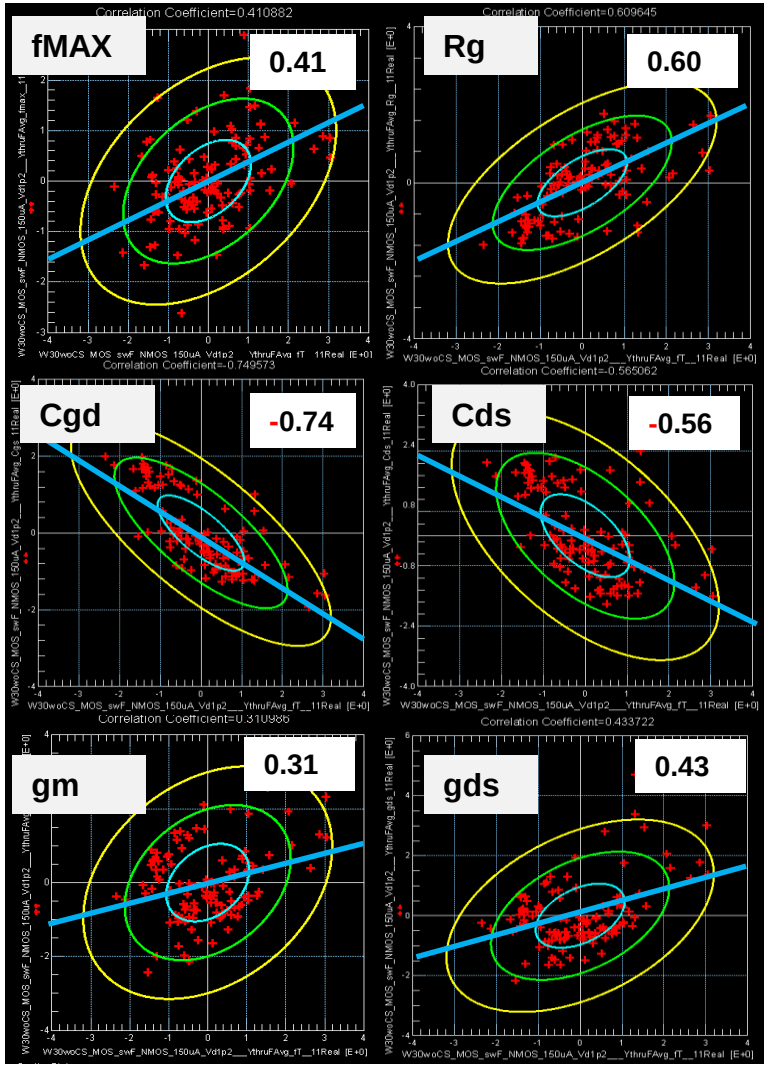
statistics {
  process {
    vary **Ndep** dist=gauss std=XX
      percent=yes
        } }

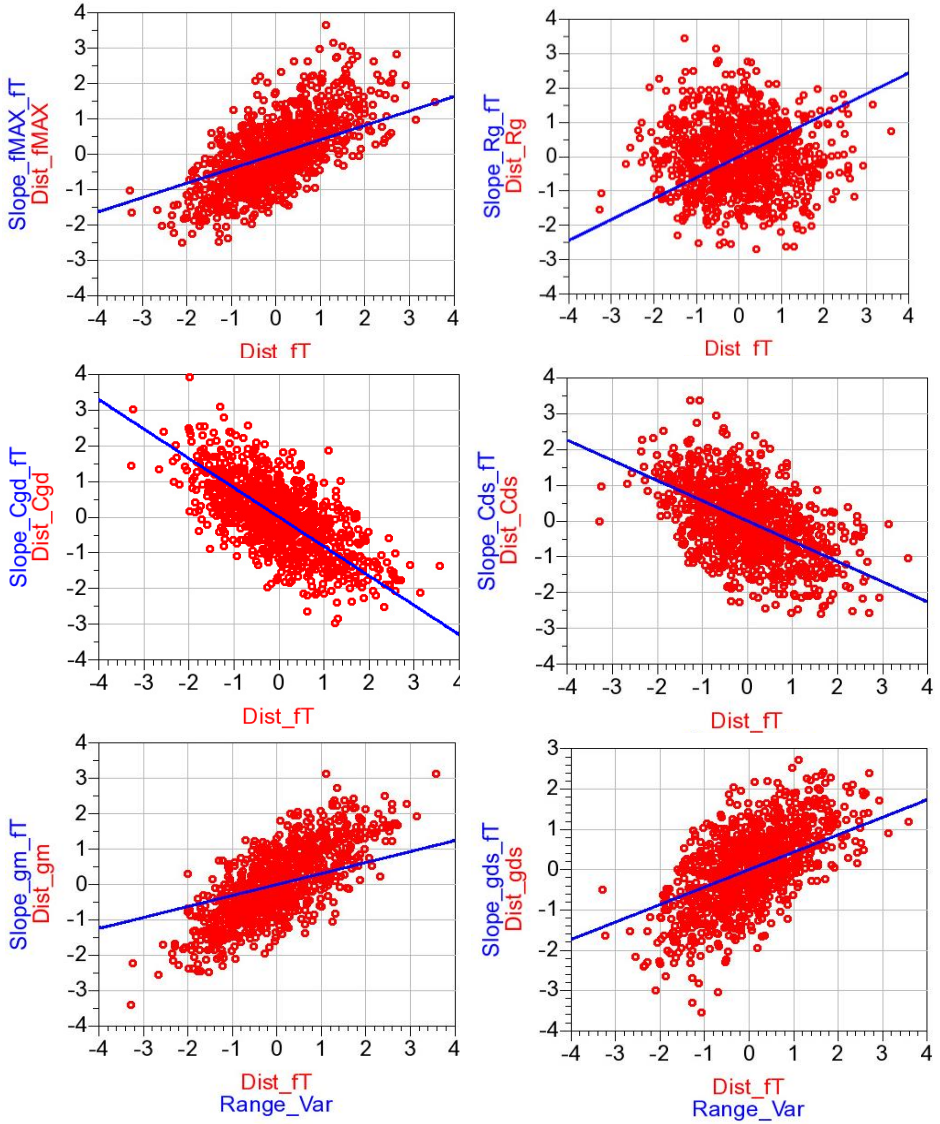
Establish direct link of li-line data with compact model.

Fab-link model vs. measurement at 60GHz. [1]



Fab-link model vs. measurement at 60GHz correlation. [1]

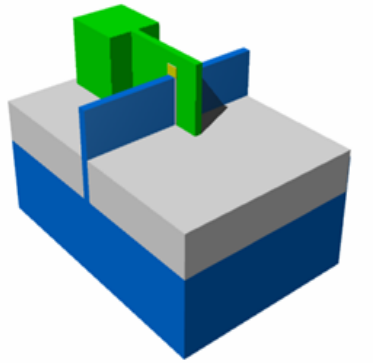




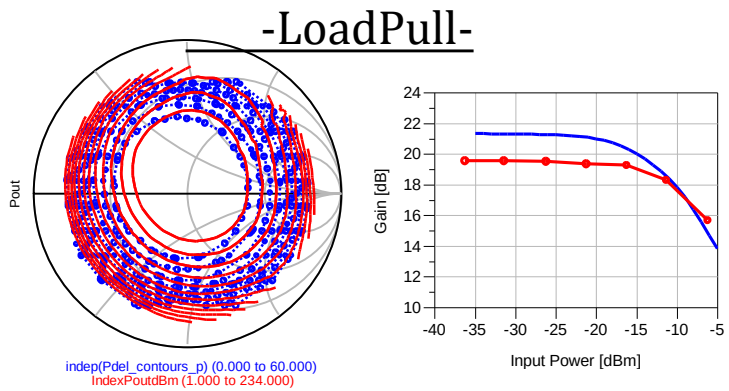
fT : principle component

Future MOSFET Modeling Challenges

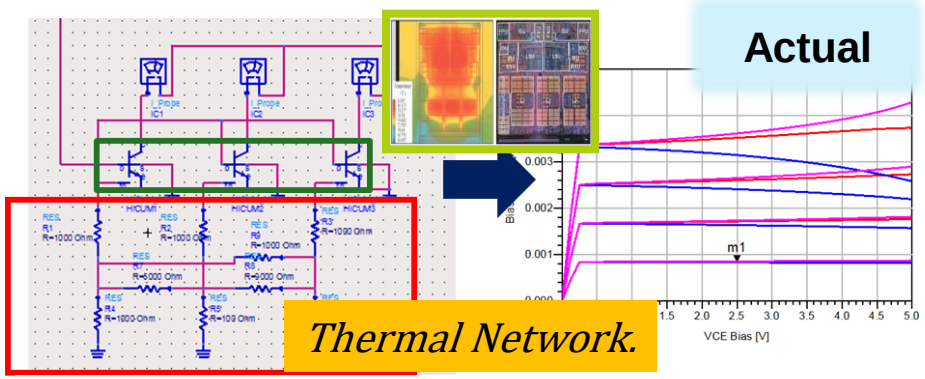
1 : *Ultra small dimensional effects, 3D structure.*



2 : *High Power Characterization*

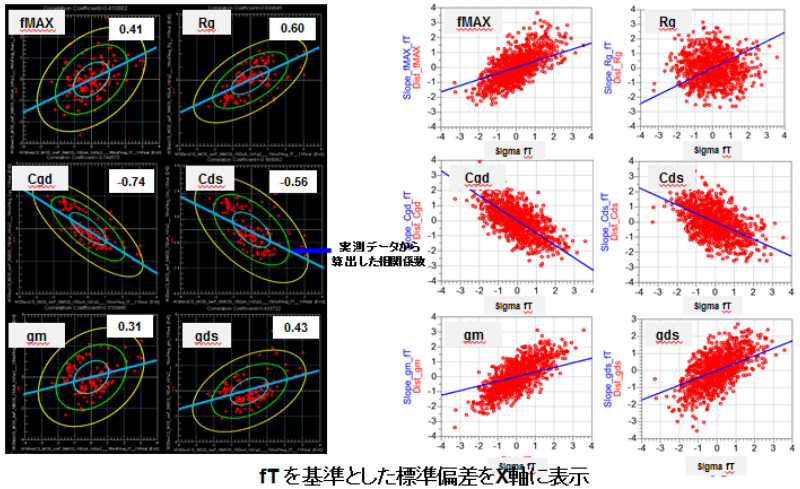


3 : *Self Heating*



Self-Heating degrades matching behavior among adjacent MOSFETs by thermal coupling.

4 : *RF Yield Estimation*



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MOS Compact Model web site

(Latest） MOS-AK http://www.mos-ak.org/

（BSIM Model） BSIM Group: http://www-device.eecs.berkeley.edu/bsim/

KIOXIA