# 20 Years History of University-Industry Research Collaboration in Analog IC Design & Test Area at Gunma University

Haruo Kobayashi, Professor Emeritus
Gunma University

koba@gunma-u.ac.jp

# Objective of This Talk

- Introduction of Gunma University research projects collaborating with semiconductor Industries to show one aspect of semiconductor industry history in Japan

# Self-Introduction

Haruo KOBAYASHI

Professor Emeritus, Gunma University, Japan

Analog/Mixed-Signal IC Design and Test

Signal Processing Algorithm

B.S. from U. Tokyo, Information Physics

M.S. from U. Tokyo, Information Physics

M.S. from UCLA, Electrical Engineering

Ph.D. from Waseda U. Electrical Engineering

# Contents (1/2)

- Introduction
- Case Studies of Research Collaboration with Industry
  - Charge Pump Circuit
  - Complex Bandpass ΔΣ ADC
  - High Performance Analog Filter
  - Envelope Tracking Power Supply
  - CMOS SAR ADC
  - On-Chip Jitter Measurement Circuit
  - Signal Generation for Analog IC Testing

# Contents (2/2)

# Where is Gunma University ?

Maebashi 1: Education, Social and Information Studies
Maebashi 2: Medicine
Kiryu: Science & Engineering
Ota: Science & Engineering

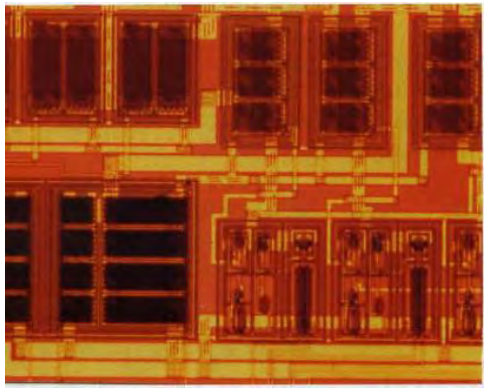
群馬大学
GUNMA UNIVERSITY

CAMPUS LOCATION

Gunma's Yuru-chara
Gunma chan

# Charge Pump Circuit

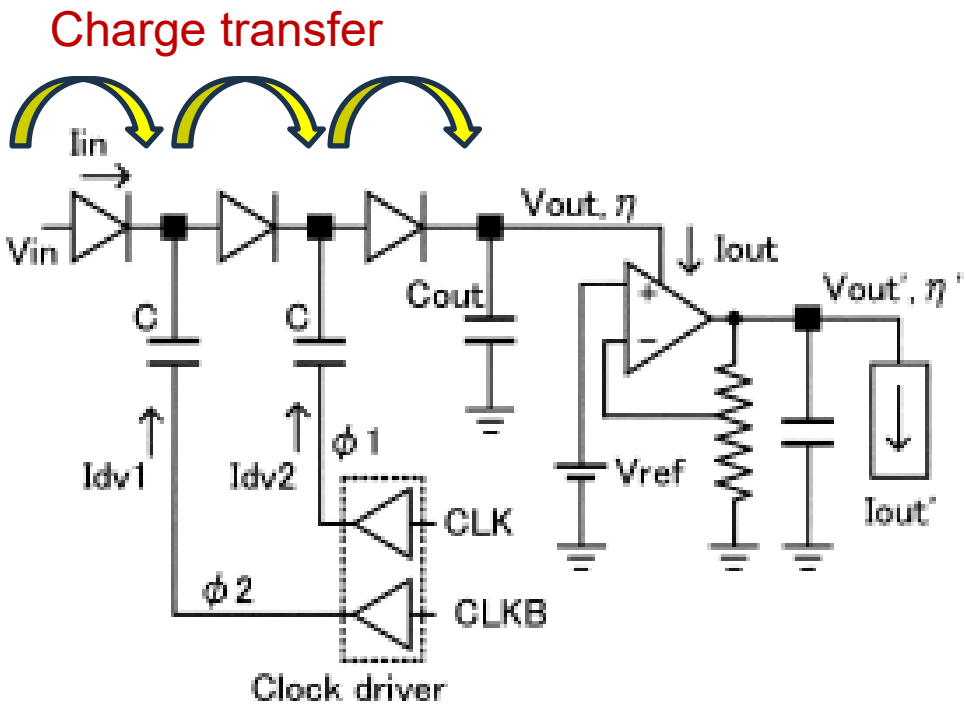
"High-Efficiency Charge-Pump Circuits which use a 0.5Vdd-Step Pumping Method", IEICE Trans. Fundamentals (Feb. 2003).



Charge pump IC developed by Sanyo

- Demand from audio-visual instrument company
  - Voltage boost DC-DC converter
  - W/O bulky inductor
  - High efficiency (<90%)
  - Large output current (10mA)

- Dickson-type charge pump circuit with improvements of
  - Circuit
  - Layout



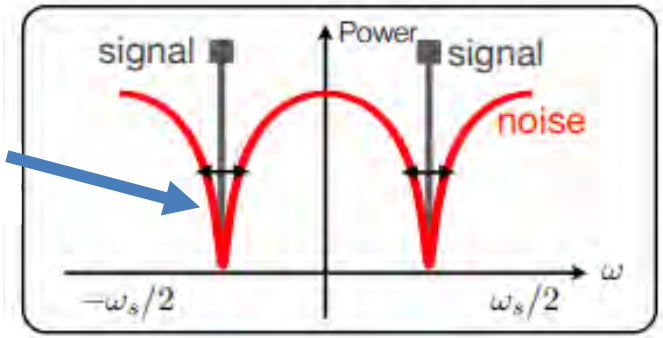
# Complex Bandpass ΔΣ ADC

"A Multibit Complex Bandpass Delta Sigma AD Modulator with I, Q Dynamic Matching and DWA Algorithm", IEEE Asian Solid-State Circuits Conference, Hangzhou, China (Nov. 2006).

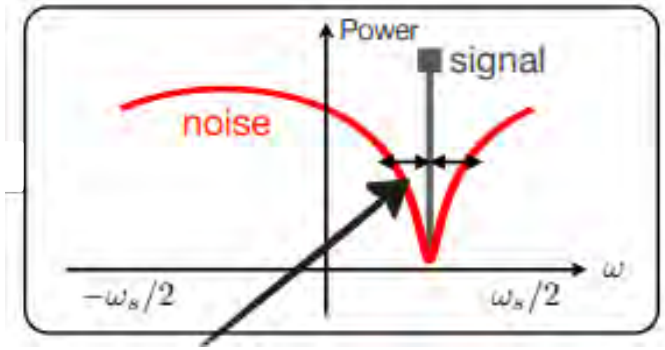
- Power efficient ΔΣ ADC
  - Low-IF architecture receiver
  - Complex Bandpass
  - Complex bandpass DWA algorithm for multi-bit DACs
  - I, Q dynamic matching to avoid I, Q path mismatch

Not use
(Power inefficiency)

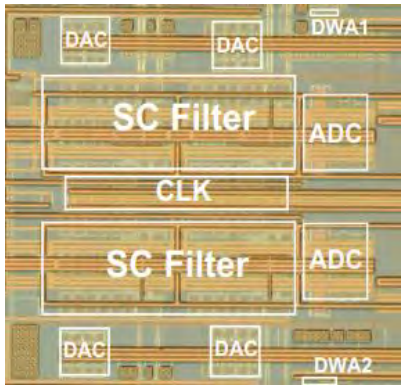
Conventional



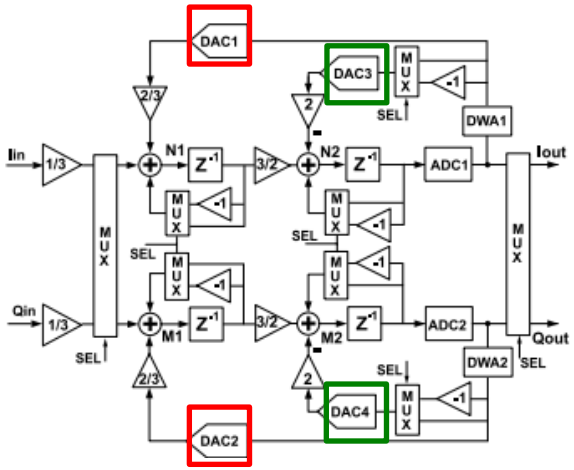

Complex bandpass




Low-IF signal band




0.18μm CMOS chip photo



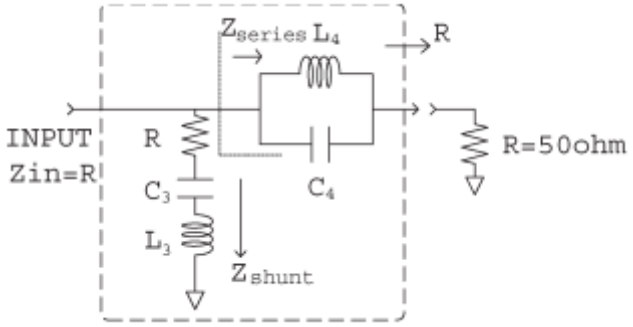
# High Performance Analog Filter

"Total Harmonic Distortion Measurement System for Electronic Devices up to100MHz with Remarkable Sensitivity"
IEEE Trans. Instrumentation and Measurement (Dec. 2007).

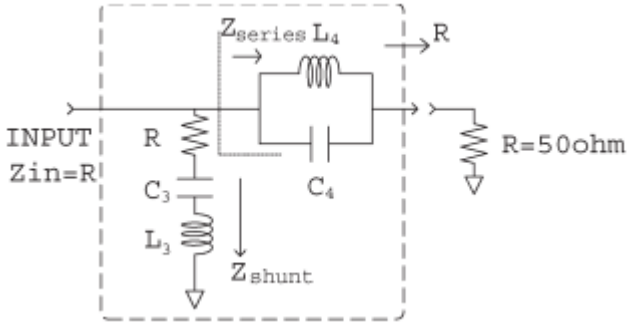
20-stage BPF:
Integration of discrete components

- Cascade of LCR passive filters
  - ⇨ Very linear, High Q

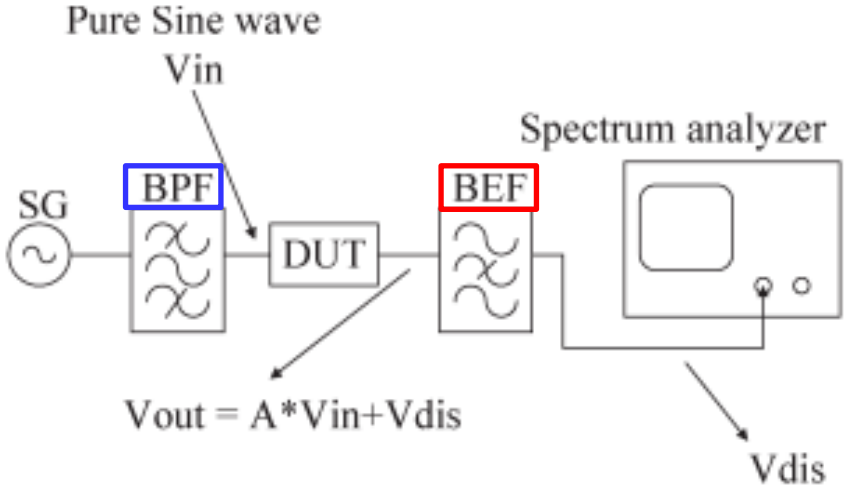
Constant input impedance




Single-stage of
Band Pass Filter (BPF)




Single-stage of
Band Elimination Filter (BEF)

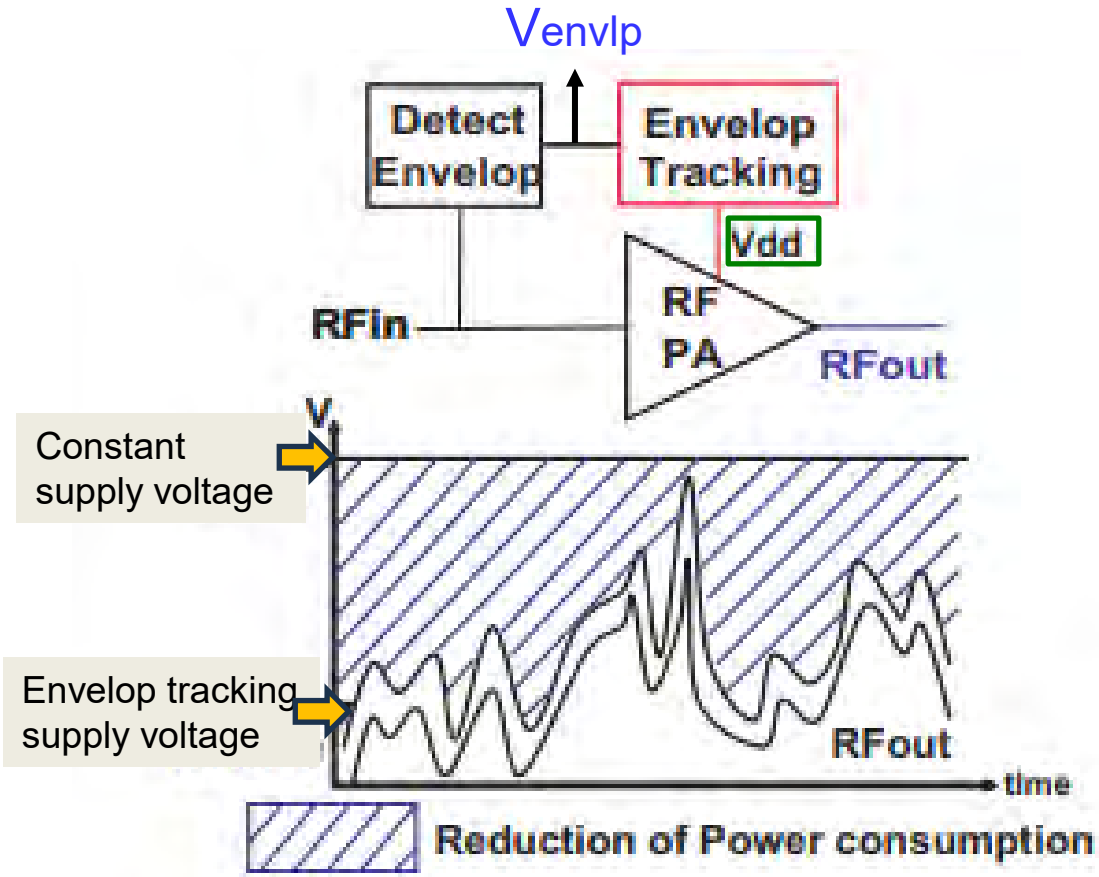


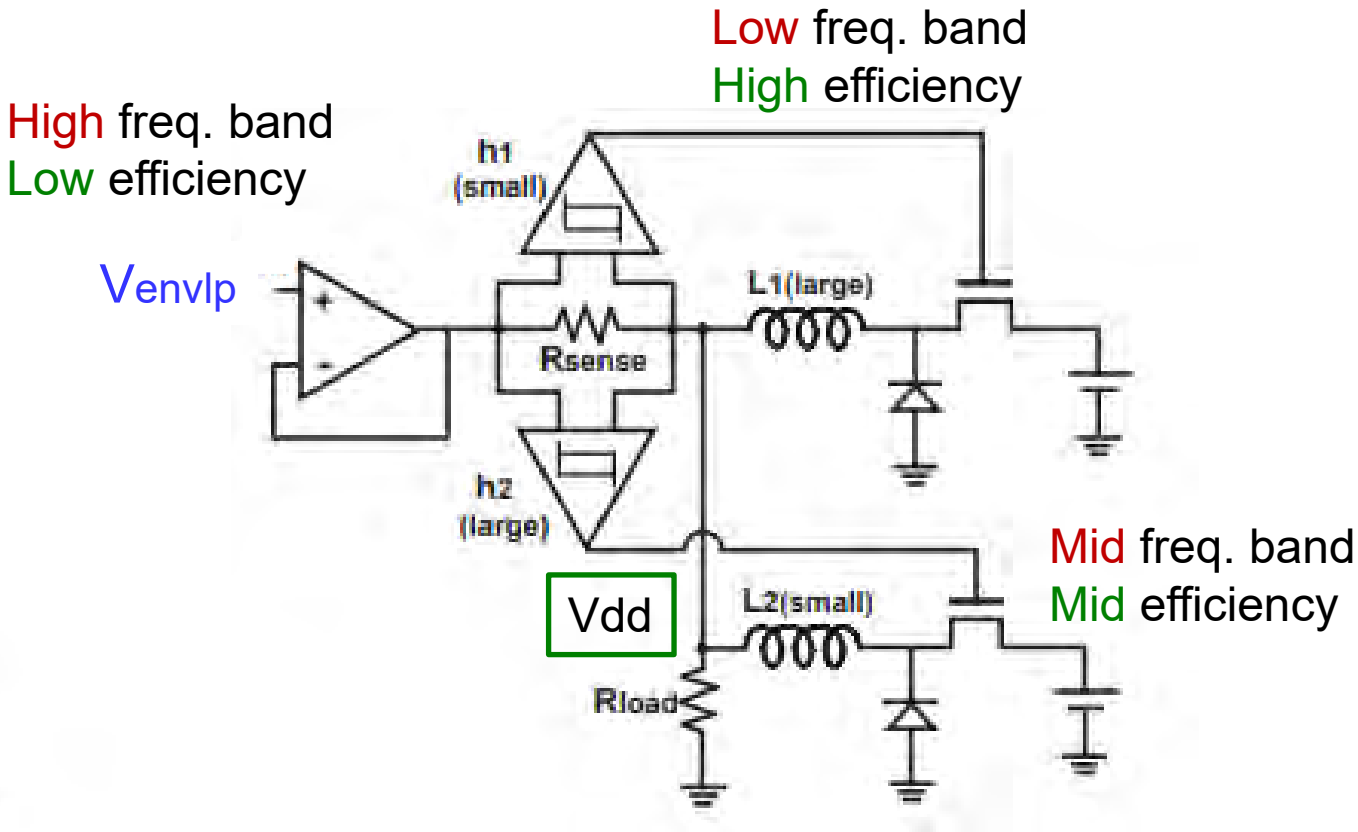

Total Harmonic Distortion (THD)
Measurement System

# Envelope Tracking Power Amp

"New Architecture of Envelope Tracking Power Amplifier for Base Station"

IEEE Asia Pacific Conference on Circuits and Systems, Macao, China Dec. 2008

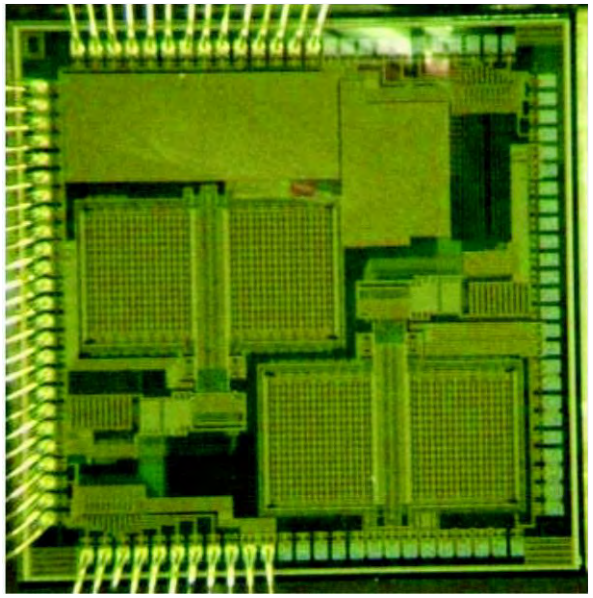


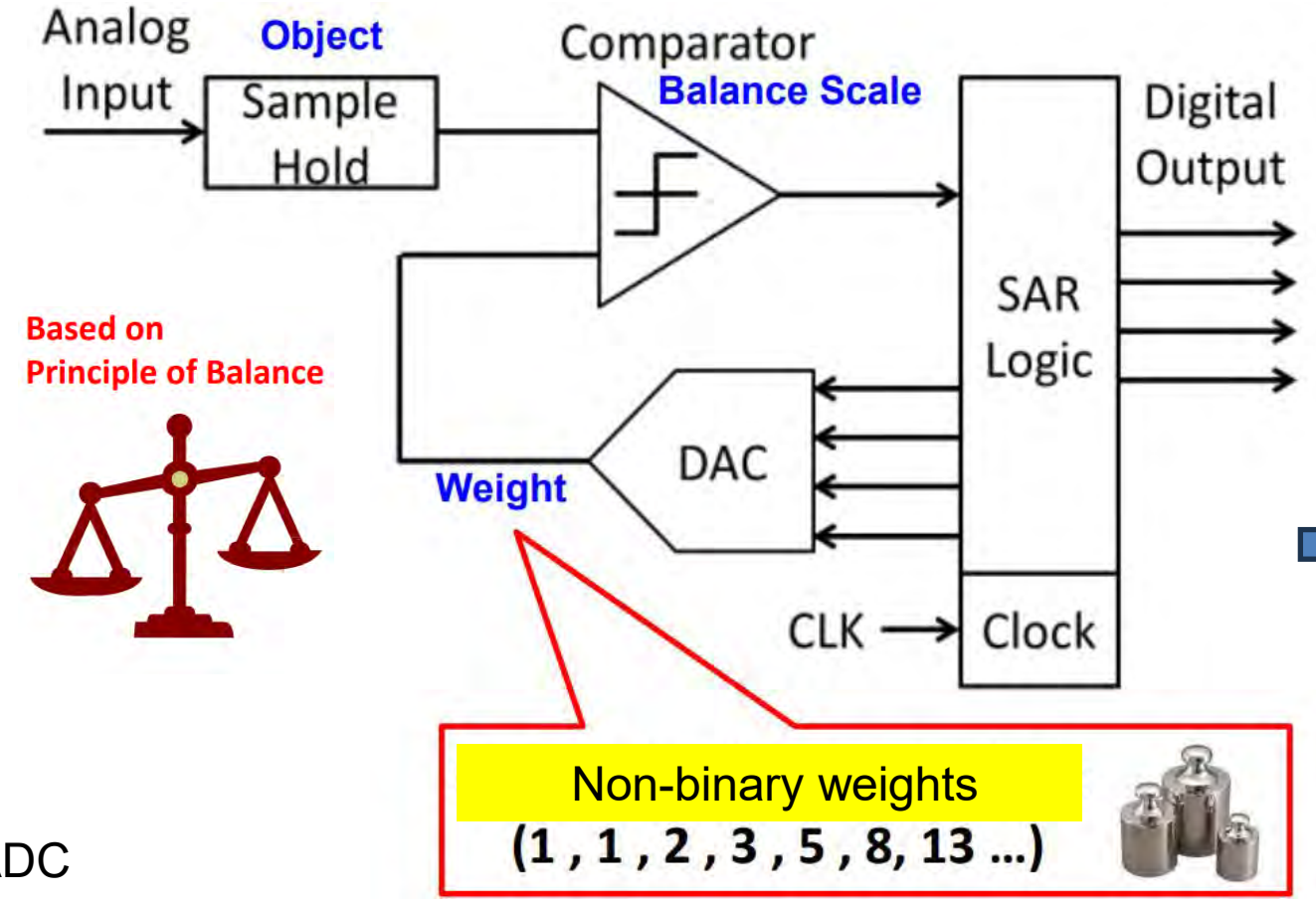

Proposed 3-stage envelope tracking power supply

# CMOS SAR ADC

"Design for Testability That Reduces Linearity Testing Time of SAR ADCs," IEICE Trans. Electronics (June 2011).



10-bit Successive-Approximation ADC

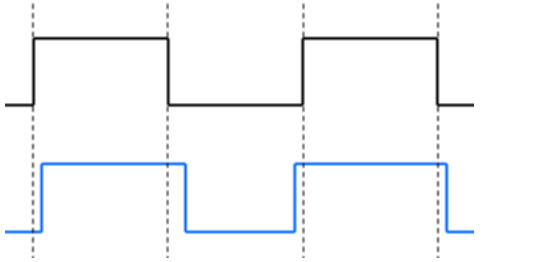


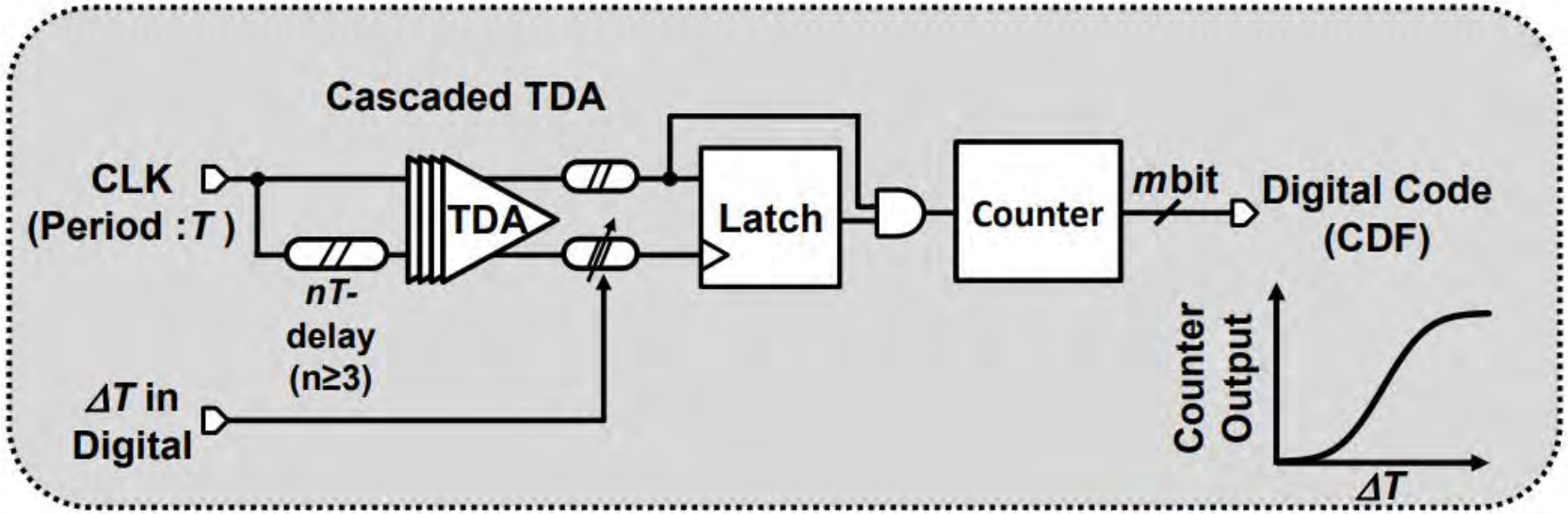

Error tolerant

# On-chip Clock Jitter Measurement Circuit

"CMOS Circuits to Measure Timing Jitter Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier with Duty-Cycle Compensation," IEEE Journal of Solid-State Circuits vo. 47, no.11, pp.2701-2710 (Nov. 2012)

Ideal CLK




Critical for
ADC performance

Experiments show that
1.67 ps RMS timing jitter
can be measured

Process : 65 nm CMOS
Supply Voltage : 1.2 V

# Signal Generation for Analog IC Test

"Low-Distortion Signal Generation for ADC Testing,"
IEEE International Test Conference, Seattle, WA (Oct. 2014).

AWG: Arbitrary Waveform Generator

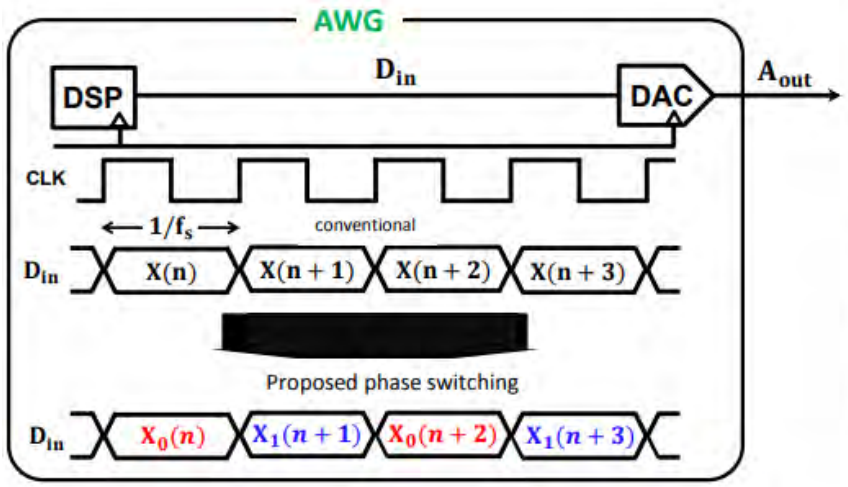
IMD3: 3rd-order Intermodulation Distortion

AWG nonlinearity

⇩

Its compensation
by digital algorithm

Low IMD3 two-tone signal generation for communication application ICs

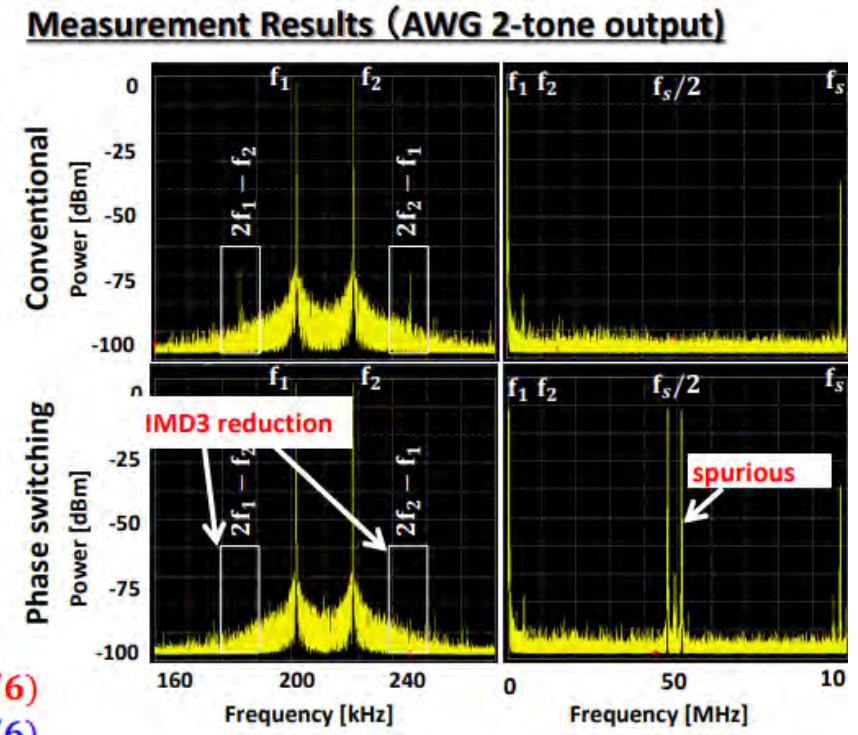



**Conventional**

$$X(n) = A\cos(2\pi f_1 nT_s) + A\cos(2\pi f_2 nT_s)$$

**Proposed phase switching**

$$X_0(n) = B\cos(2\pi f_1 nT_s + \pi/6) + B\cos(2\pi f_2 nT_s - \pi/6)$$
$$X_1(n) = B\cos(2\pi f_1 nT_s - \pi/6) + B\cos(2\pi f_2 nT_s + \pi/6)$$

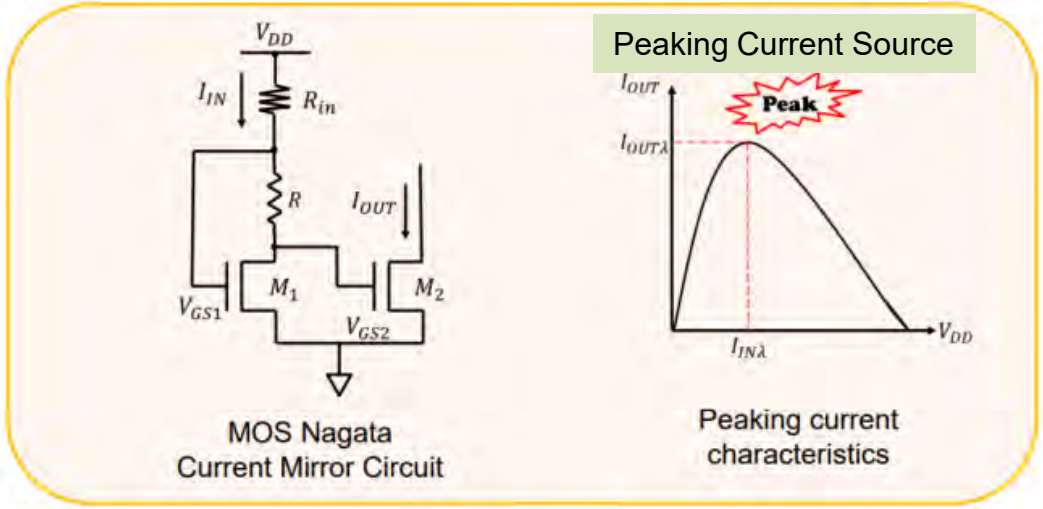


# CMOS Reference Current Source

"Silicon Verification of Improved Nagata Current Mirrors",
IEEE ICSICT, Qingdao, China (Nov. 2018)

Addition of multiple peaking current sources

Supply voltage insensitive current source



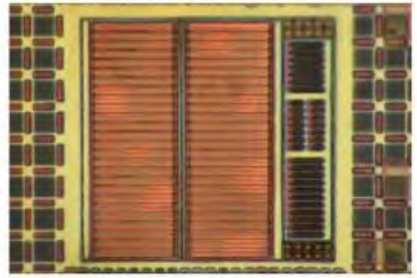
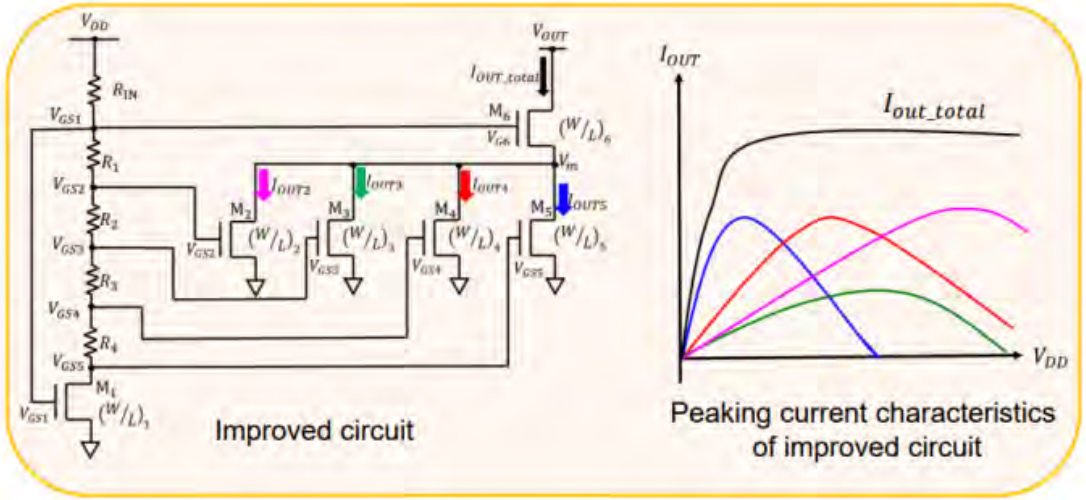



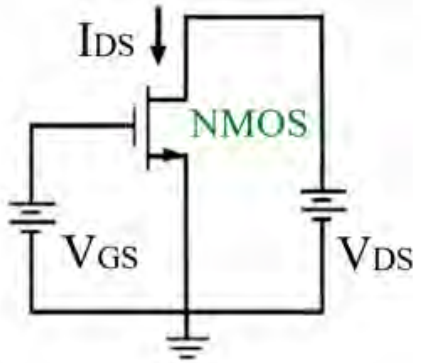
Photo of prototype chip

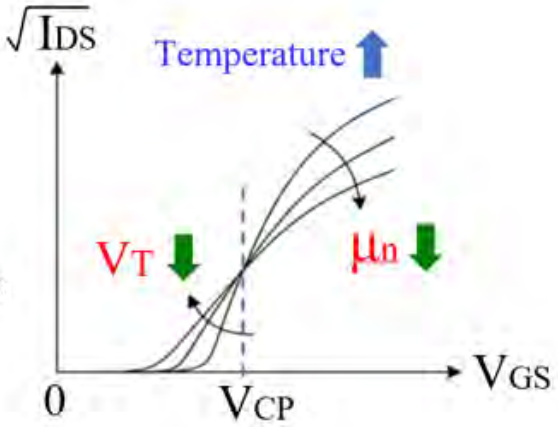



# CMOS Reference Voltage Source

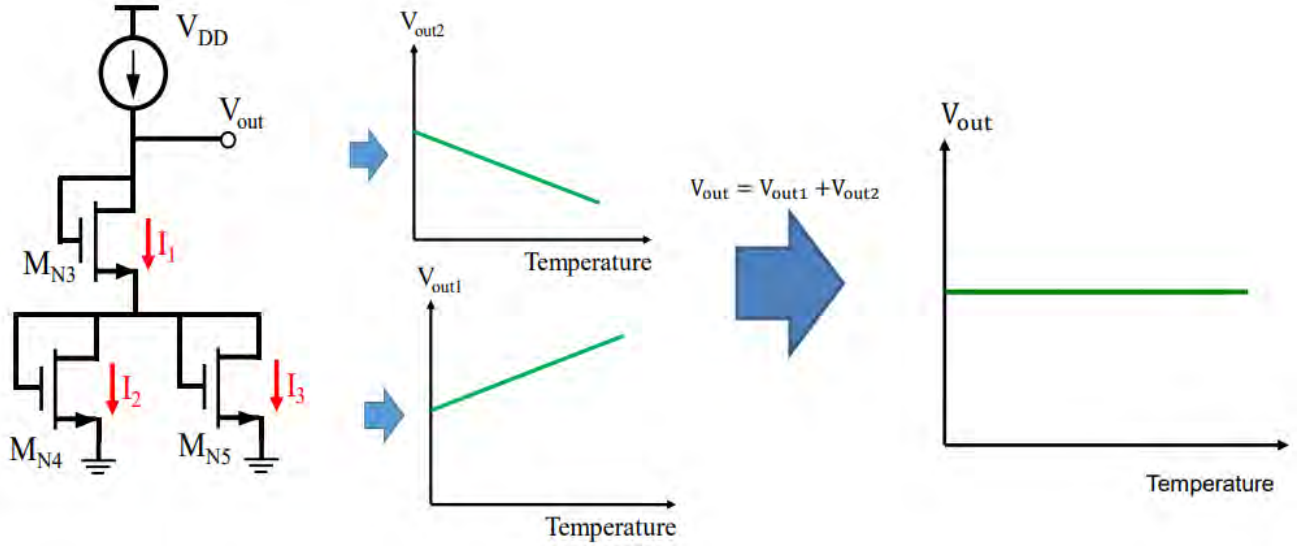
"CMOS Reference Voltage Source Using Drain Current Temperature Characteristics"
IEEE ICCE-Asia, Yeosu, South Korea (Oct. 2022)

MOS drain current temperature characteristics



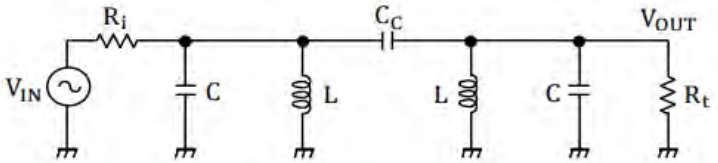

Temperature insensitive voltage source



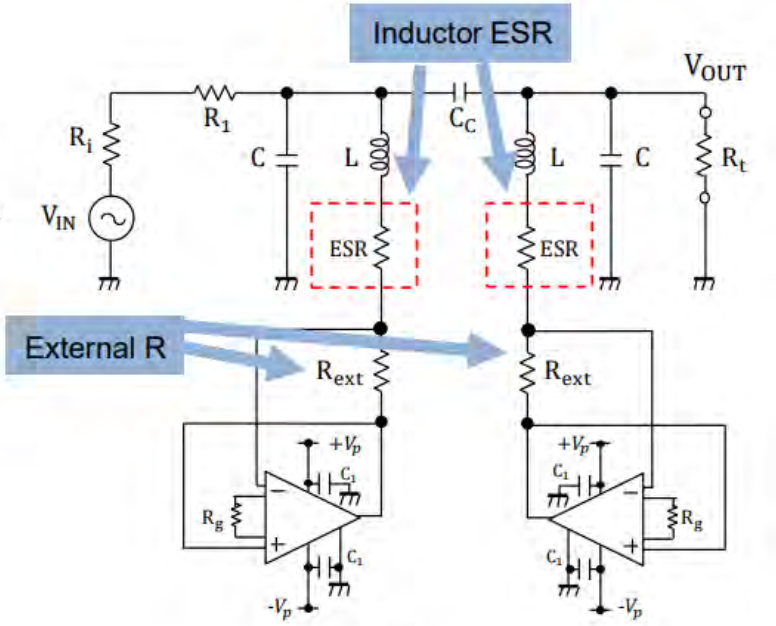
# Low Cost Analog Filter

"Design Consideration for LC Analog Filters:
Inductor ESR Compensation, Mutual Inductance Effect and Variable Center Frequency"
ICICT, London, UK (Feb. 2023)

Active compensation for series resistance of inductor *L*




Ideal LC BPF




LC BPF with
Active compensation

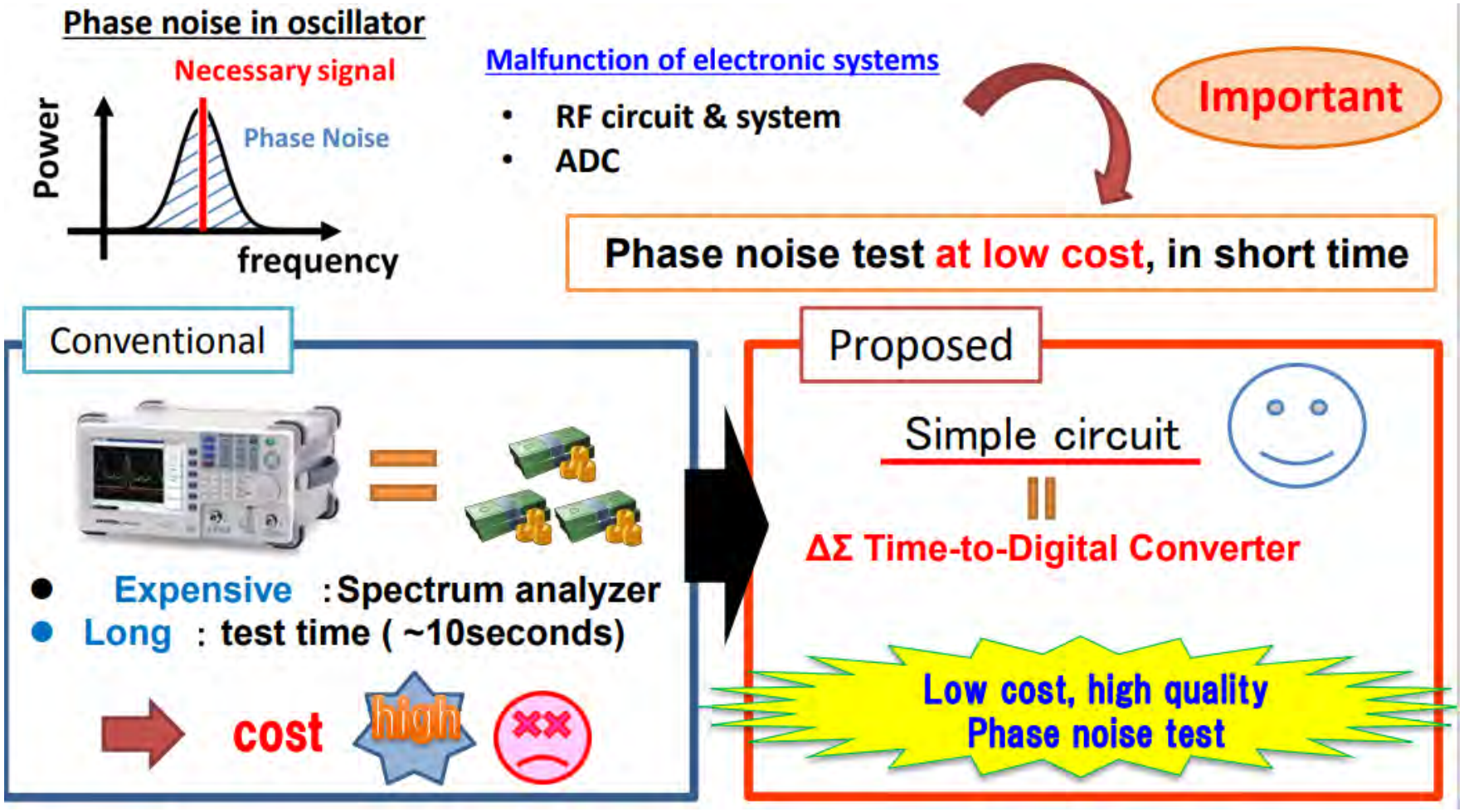
High Q filter

Only 4th-order filter

Low cost

# Phase Noise Measurement Circuit

"Phase Noise Measurement Techniques Using Delta-Sigma TDC",
IEEE International Mixed-Signals, Sensors and Systems Test Workshop, Porto Alegre, Brazil (Sept. 2014).



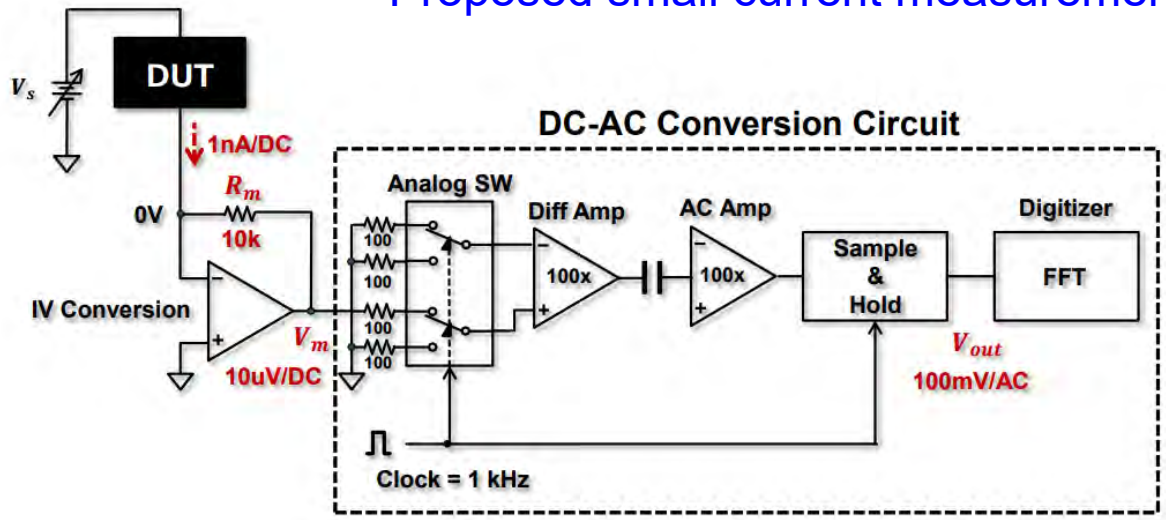
# Very Small DC Current Measurement

"Evaluation of High-Precision Nano-Ampere Current Measurement Method for Mass Production"
28th IEEE International Conference on Electronics Circuits and Systems
Sofitel Dubai The Obelisk, Dubai, UAE, (Nov. 2021).

Low power wearable devices
↓
Small DC bias current
↓
Fast, accurate testing
at mass production stage

FFT-based DC-AC Conversion
↓
Remove effects of
DC, low-freq. noises

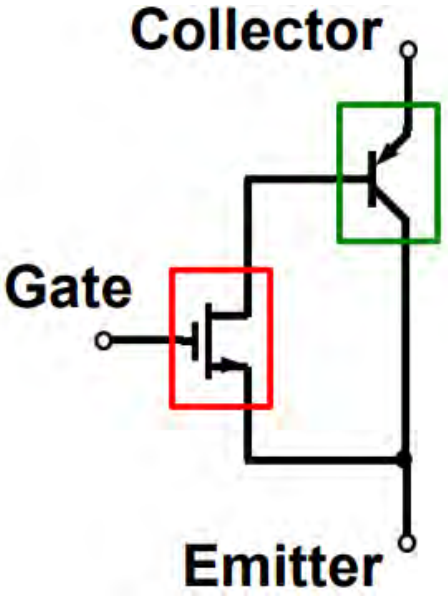
Proposed small current measurement



# IGBT Gate Driver

"Current-Driven IGBT Gate Driver Circuit Considering Four Operation Regions"
ICICT, London, UK, Feb. 2022

IGBT: Insulated Gate Bipolar Transistor




**Advantages**

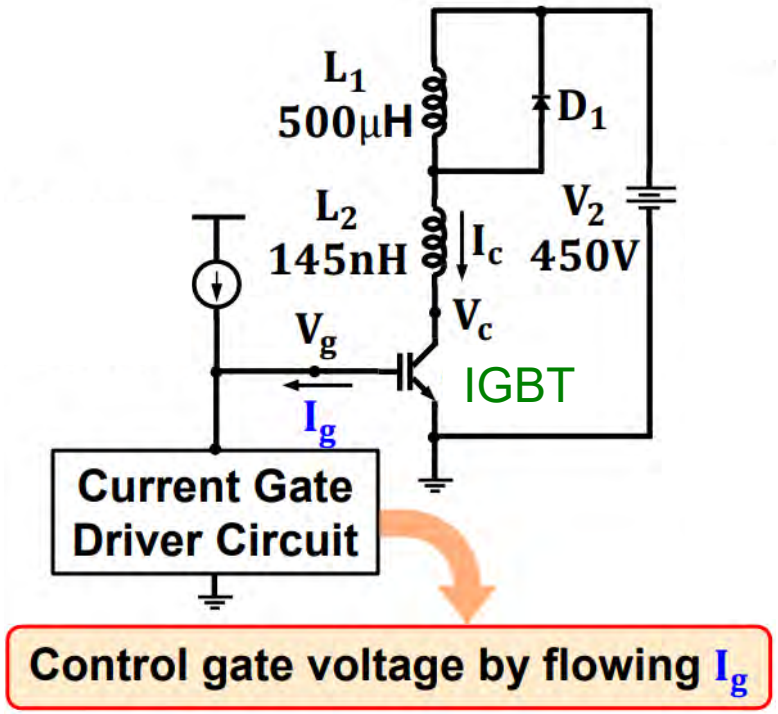
- Fast operating speed
- Large current amplification factor (~1.2kA)
- High withstand voltage (~3.3kV)

**Disadvantage**
Large gate capacitance

**Driver design is difficult**

Current Drive → **Reduction of Switching loss and Excessive overshoot**

**Simplification of control design**



# Conclusion

- University-Industry collaboration is important in analog IC design & test area.

## Benefits to University

- Advanced technologies info from industry
- Industry-oriented education to students

## Benefits to Industry

- Challenging research based on theory and fundamental principles

# Appendix: Time-to-Digital Converter for Timing Test

"Experimental Verification of Timing Measurement Circuit With Self-Calibration,"
IEEE International Mixed-Signals, Sensors and Systems Test Workshop, Porto Alegre, Brazil (Sept. 2014).


Single-bit ΔΣ TDC with analog FPGA

Multi-bit ΔΣ TDC with analog FPGA

Flash-type TDC with analog FPGA


Flash-type TDC with digital FPGA

TDC: Time-to-Digital Converter