2023 年 6 月 22 日

SSCS セミナー　参加記

群馬大学　小林春夫

(1) Abidi 先生のご講演を聴いて

「Timing Jitter in a CMOS Delay Stage」の最も基本的な導出式の、直感的な説明を思いつく。が、それを記すにはこの余白は小さすぎる。

(2) 懇親会にて

1980 年代末から 1990 年代にかけて、米国での物価は日本での物価に比べて格段に安かった。今は全く逆。

コロナ前に比べて米国往復の航空運賃・米国のホテル代は非常に高額になっている。

(3) 会場の東大（本郷）近くの池之端公園

「餌づけをしない」

人間社会でも同じであろう

IEEE Solid State Circuits Society (SSCS) Japan Chapter および
東京大学 d.lab D2T 寄附研究部門 主催

◆UCLA Asad Abidi 教授、Toronto 大 Ali Sheikholeslami 教授講演会

【日　時】2023 年 6 月 21 日（水）15:00 より 17:30

【会　場】東京大学 VDEC 武田先端知ビル 5F 武田ホール

【住　所】〒113-0032 東京都文京区弥生 2-11-16 武田先端知ビル 5F

【プログラム】

15:00~15:05 Brief introduction of SSCS JC

15:05~15:50 Prof. Abidi's talk "Optimal Design of DLL-Based Timing Circuits" (1st part)

15:50~16:05 Coffee Break (15min)

16:05~16:50 Prof. Abidi's talk "Optimal Design of DLL-Based Timing Circuits" (2nd part)

16:50~17:00 Break (10min)

17:00~17:30 Prof. Sheikholeslami's talk "Limits of Data Rates for Wireline Communication"

【Abidi 教授講演概要】

Associated with CMOS Delay Lines are many features that make them more desirable than oscillators for timing applications. Their stage delay can be tuned over decades with the bias current or supply voltage. They offer built-in phase shifts at multiple taps. They take very small chip area and offer straightforward tradeoffs between frequency, jitter, and power consumption that can be exercised dynamically during use.

We have developed an equation-based methodology for modelling DLLs and frequency synthesizers. The main parts of this methodology will be presented, for the first time, in this workshop. The topics are:

1. The Dispersion Index of Timing Jitter in a CMOS Delay Stage
2. A new Signal Flow Graph for CMOS Delay Lines
3. Compact, simple expressions for Phase Noise in a Ring Oscillator
4. Phase Noise Spectrum of Recirculating (Multiplexed) DLL in Open and Closed Loop, and Jitter Expression
5. Expressions for Spectral Spurs (Tones)
6. Validation from numerous experimental results
7. Insights into the optimal design of DLL-Based Frequency Synthesizers, and their Rapid Design

【Abidi 教授ご略歴】

Professor Asad Abidi received the BSc degree in Electrical Engineering from Imperial College, London in 1976, and the PhD from the University of California, Berkeley in 1982. He worked at Bell Laboratories, Murray Hill until 1985, and then joined the faculty of the University of California, Los Angeles where he is Distinguished Chancellor's Professor of Electrical Engineering. With his students he has developed many of the radio circuits and architectures that enable today's mobile devices.

Among other awards, Professor Abidi has received the 2008 IEEE Donald O. Pederson Award in Solid-State Circuits and the 2012 Best Paper Award from the IEEE Journal of Solid-State Circuits. The University of California, Berkeley's Department of EECS recognized him as a Distinguished Alumnus in 2015. He was elected Fellow of IEEE (1996), Member of the US National Academy of Engineering, and Fellow of TWAS, the world academy of sciences.

【Sheikholeslami 教授講演概要】

We review the fundamental limits of wireline signaling as determined by Shannon's Capacity, discuss the gap to capacity in reported per-lane data rates, and explore means of bridging this gap through multi-carrier schemes. In particular, we review the basic concepts of discrete multi-tone (DMT) and its suitability and requirements for wireline signaling.

【Sheikholeslami 教授ご略歴】

Ali Sheikholeslami is a professor of Electrical and Computer Engineering at the University of Toronto and has published over 50 papers in the area of wireline signaling. He is a co-author of "Understanding Jitter and Phase Noise". He currently serves as the ISSCC Education Chair the SSCS Vice President, Education.