1st IEEE International Workshop on Automotive Reliability & Test
ART Workshop

# Redundant SAR ADC Algorithms for Reliability Based on Number Theory

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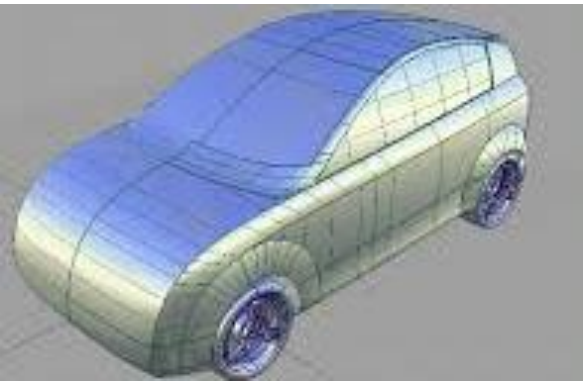
# Purpose of This Presentation

We show here
redundancy design example for reliability.

We hope that this stimulates
automotive reliability & test engineers



# Outline

- Objective
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Error Correction Range
  - Settling Time
- Realization of Fibonacci DAC
- Conclusion

# Outline

- **Objective**
- SAR ADC Redundancy Design
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# Research Objective

## Objective

- **Development of**
  **Reliable & High-speed SAR ADC**

## Our Approach

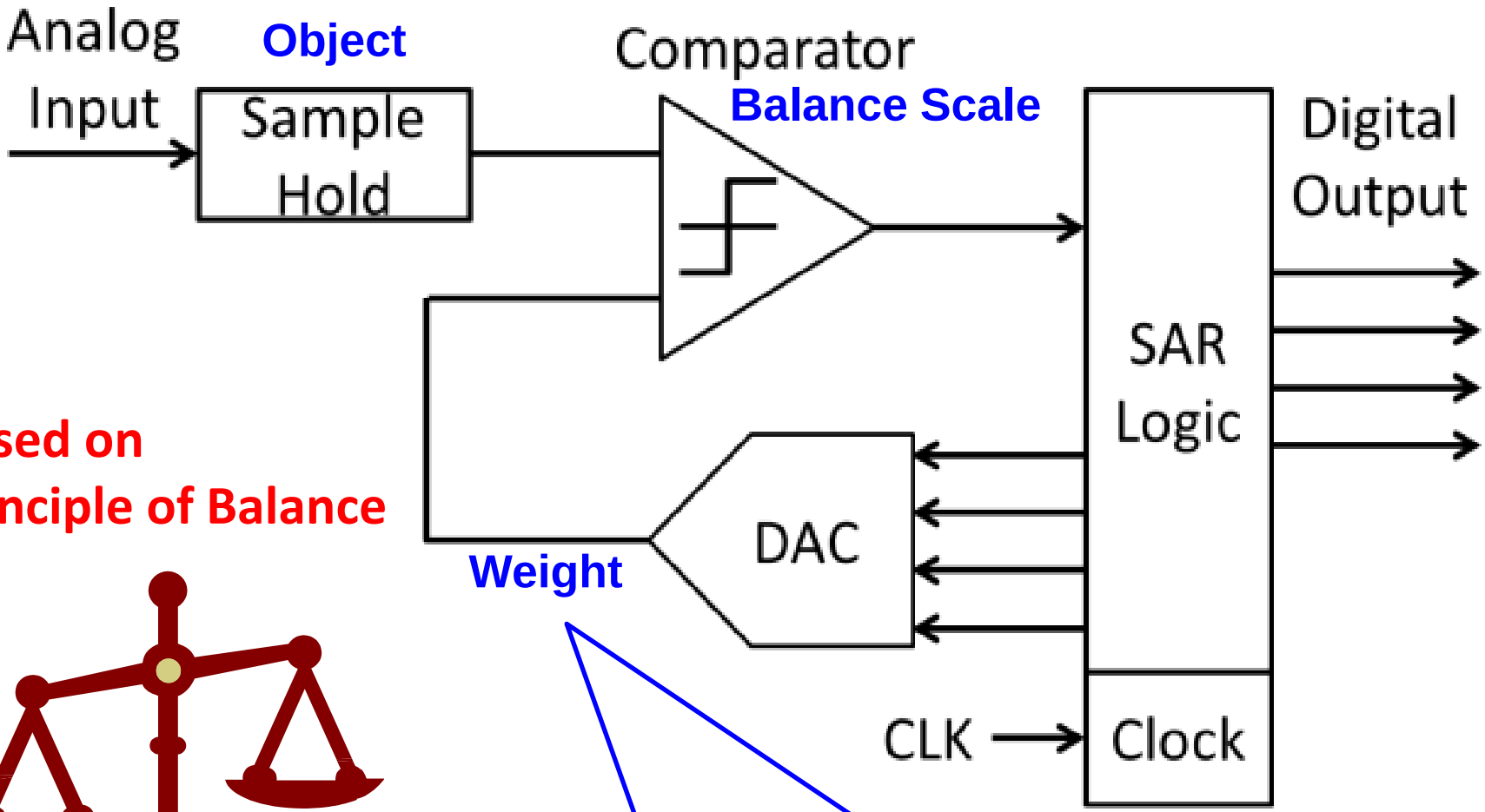
- **Redundancy search algorithm design with Number Theory**

Golden ratio ← Today's talk

Silver ratio

SAR ADC : Successive Approximation Register ADC

# SAR ADC Configuration




**Based on Principle of Balance**



**Generally use binary weight**

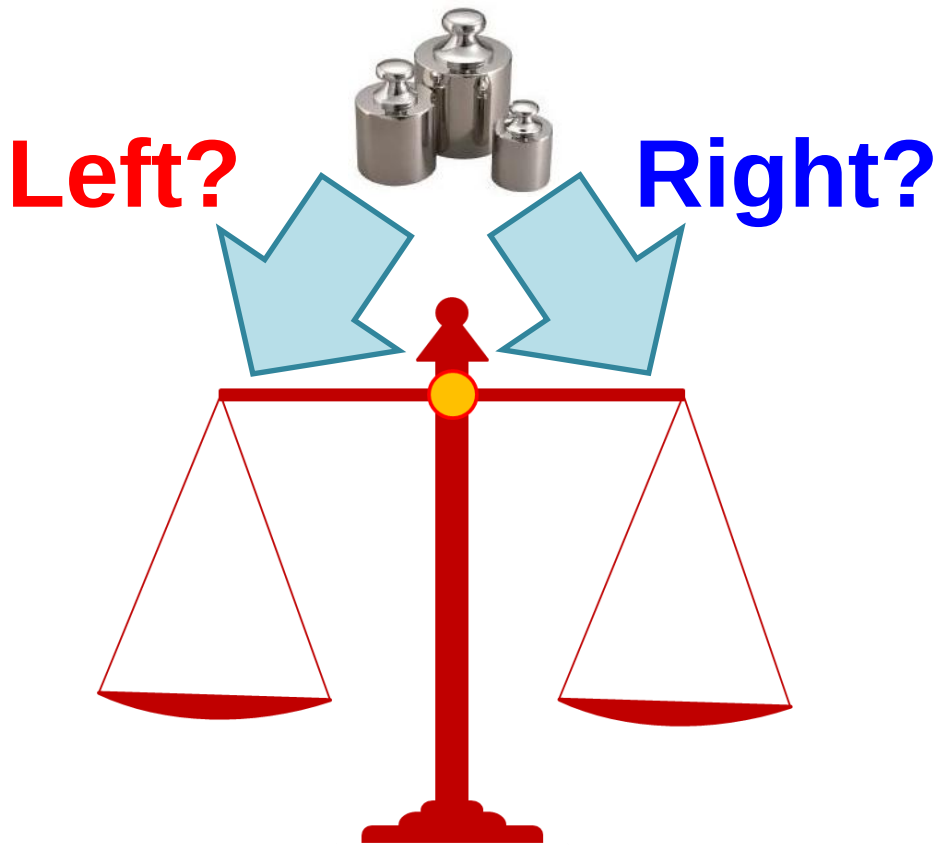
**(1 , 2 , 4 , 8 , 16 , 32, 64 …)**

# Binary Search SAR ADC Operation

## 5bit-5step SAR ADC

- Analog Input : 7.3 [V]
- Binary weight :

16, 8, 4, 2, 1




| Step | | 1st | 2nd | 3rd | 4th | 5th | output |
|---|---|---|---|---|---|---|---|
| Weight p(k) | | 16 | 8 | 4 | 2 | 1 | |
| Level | 31 | | | | | | 31 |
| | 30 | | | | | | 30 |
| | 29 | | | | | | 29 |
| | 28 | | | | | | 28 |
| | 27 | | | | | | 27 |
| | 26 | | | | | | 26 |
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| | 14 | | | | | | 14 |
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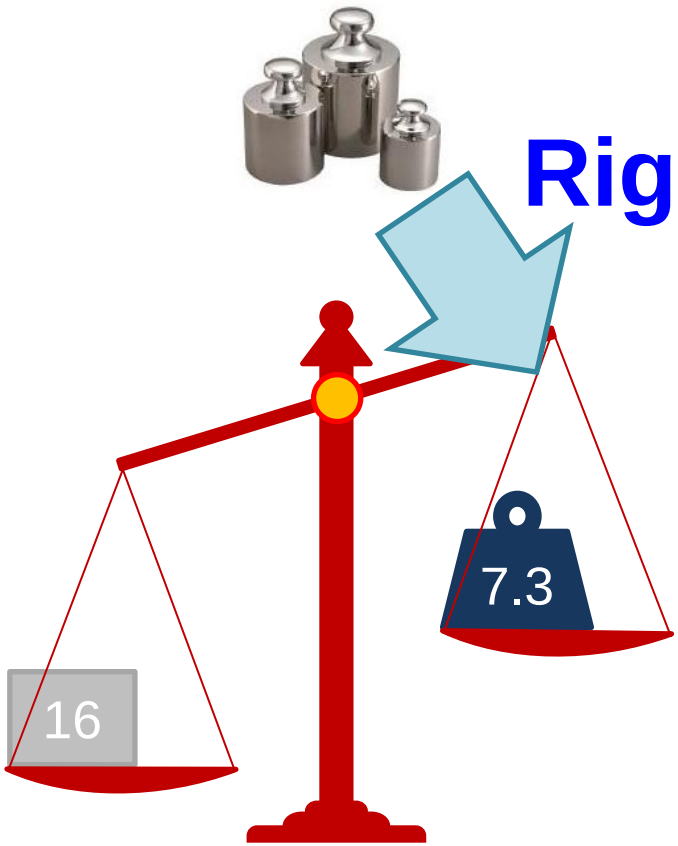
| | 11 | | | | | | 11 |
| | 10 | | | | | | 10 |
| | 9 | | | | | | 9 |
| | 8 | | | | | | 8 |
| | 7 | | | | | | 7 |
| | 6 | | | | | | 6 |
| | 5 | | | | | | 5 |
| | 4 | | | | | | 4 |
| | 3 | | | | | | 3 |
| | 2 | | | | | | 2 |
| | 1 | | | | | | 1 |
| | 0 | | | | | | 0 |

# Binary Search SAR ADC Operation

## 5bit-5step SAR ADC

- Analog Input : [V]
- Binary weight :

8, 4, 2, 1




| Step | | 1st | 2nd | 3rd | 4th | 5th | output |
|---|---|---|---|---|---|---|---|
| Weight p(k) | | 16 | 8 | 4 | 2 | 1 | |
| Level | 31 | | | | | | 31 |
| | 30 | | | | | | 30 |
| | 29 | | | | | | 29 |
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| | 14 | | | | | | 14 |
| | 13 | | | | | | 13 |
| | 12 | | | | | | 12 |
| | 11 | | | | | | 11 |
| | 10 | | | | | | 10 |
| | 9 | | | | | | 9 |
| | 8 | | | | | | 8 |
| | 7 | | | | | | 7 |
| | 6 | | | | | | 6 |
| | 5 | | | | | | 5 |
| | 4 | | | | | | 4 |
| | 3 | | | | | | 3 |
| | 2 | | | | | | 2 |
| | 1 | | | | | | 1 |
| | 0 | | | | | | 0 |

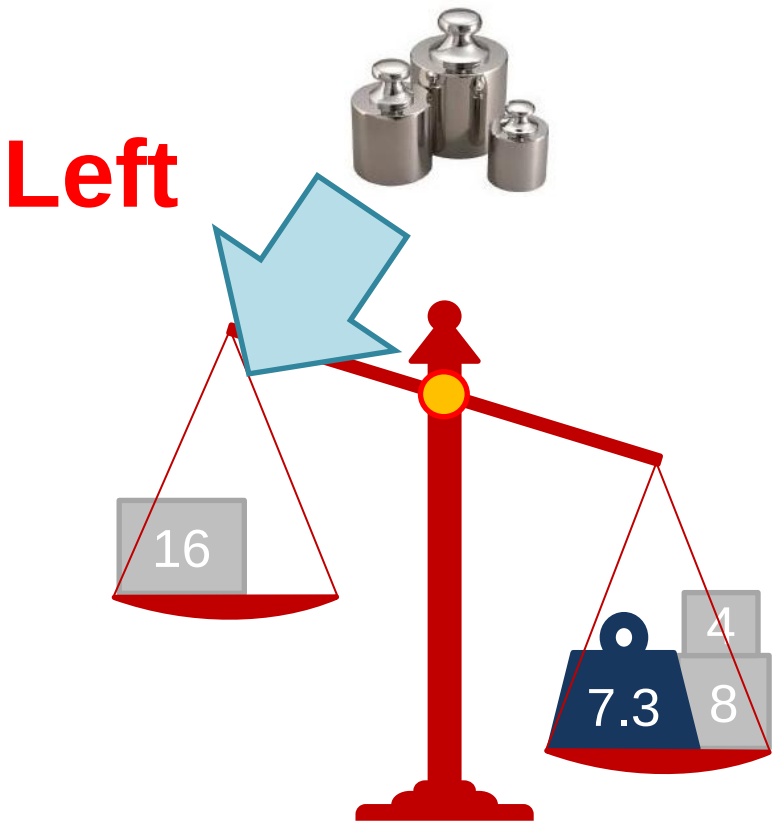
Down!

0

# Binary Search SAR ADC Operation

## 5bit-5step SAR ADC

- Analog Input : [V]
- Binary weight : 2, 1




| Step | 1st | 2nd | 3rd | 4th | 5th | output |
|---|---|---|---|---|---|---|
| Weight p(k) | 16 | 8 | 4 | 2 | 1 | |
| Level 31 | | | | | | 31 |
| 30 | | | | | | 30 |
| 29 | | | | | | 29 |
| 28 | | | | | | 28 |
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| 14 | | | | | | 14 |
| 13 | | | | | | 13 |
| 12 | | | | | | 12 |
| 11 | | | | | | 11 |
| 10 | | | UP! | | | 10 |
| 9 | | | | | | 9 |
| 8 | | | | | | 8 |
| 7 | | | | | | 7 |
| 6 | | | | | | 6 |
| 5 | | | | | | 5 |
| 4 | | | | | | 4 |
| 3 | 0 | 0 | 1 | | | 3 |
| 2 | | | | | | 2 |
| 1 | | | | | | 1 |
| 0 | | | | | | 0 |

# Binary Search SAR ADC Operation

## 5bit-5step SAR ADC

- Analog Input : [V]
- Binary weight :

**7.3⇒00111⇒7**

$16 - 8 - 4 + 2 + 1 + 0.5 - 0.5 = 7$


| Step | 1st | 2nd | 3rd | 4th | 5th | output |
|---|---|---|---|---|---|---|
| Weight p(k) | 16 | 8 | 4 | 2 | 1 | |
| Level 31 | | | | | | 31 |
| 30 | | | | | | 30 |
| 29 | | | | | | 29 |
| 28 | | | | | | 28 |
| 27 | | | | | | 27 |
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| 11 | | | | | | 11 |
| 10 | | | | | | 10 |
| 9 | | | | | | 9 |
| 8 | | | | | | 8 |
| 7 | | | | | | 7 |
| 6 | | | | | | 6 |
| 5 | | | | | | 5 |
| 4 | | | | | | 4 |
| 3 | 0 | 0 | 1 | 1 | 1 | 3 |
| 2 | | | | | | 2 |
| 1 | | | | | | 1 |
| 0 | | | | | | 0 |

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- **SAR ADC Redundancy Design**
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  - Settling Time
- Realization of Fibonacci DAC
- Conclusion

# SAR ADC Redundancy Design

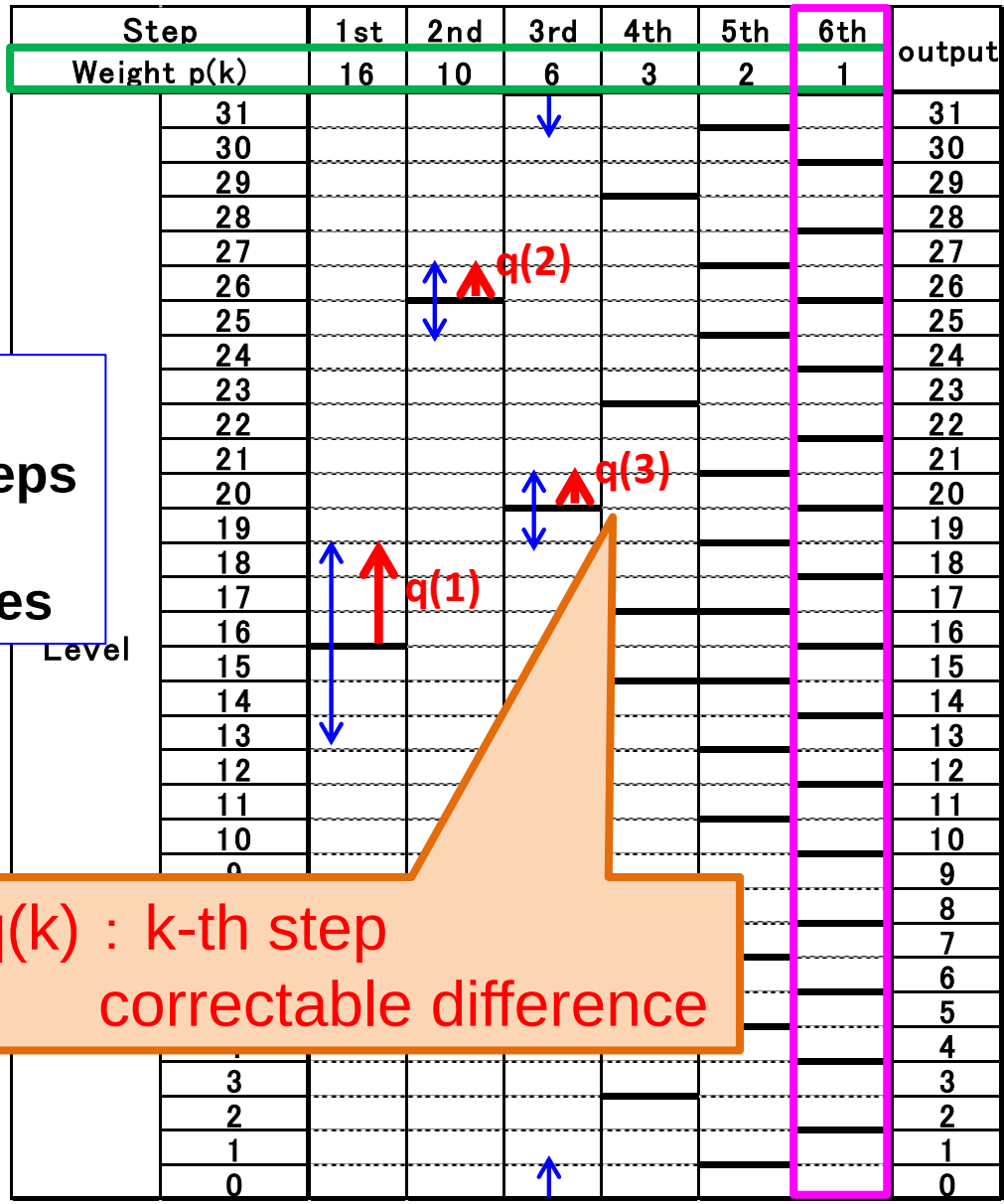
## Redundancy

- Surplus, Extra

**Using time redundancy**

- Increase Extra comparison steps
- Change reference to Non-binary voltages

**Enable digital error correction!**



# Redundancy Design Operation(No Error)

## 4bit-5step SAR ADC

- Analog input : 6.3
- Redundant weight :

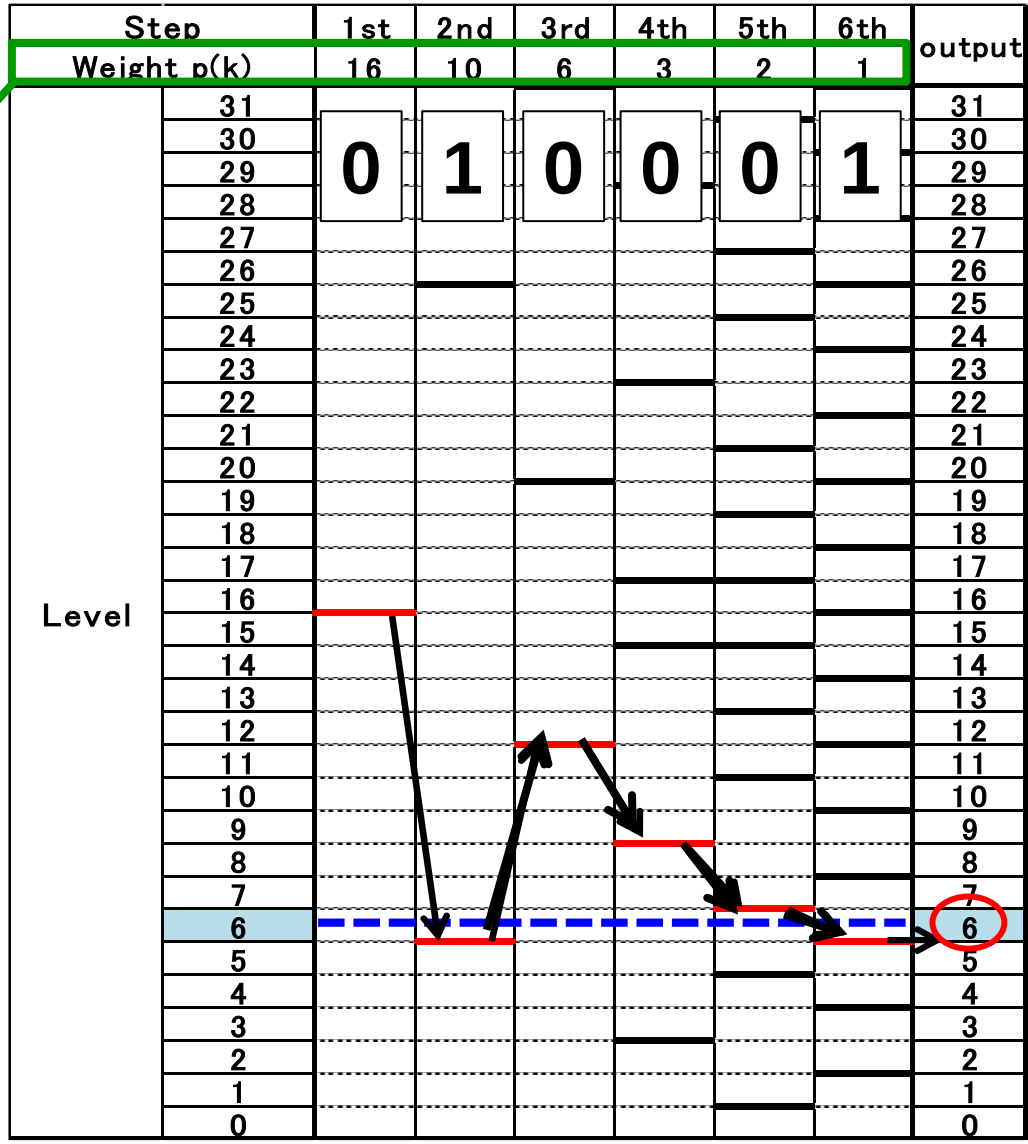
  16, 10, 6, 3, 2, 1

## Correctable expression

**6.3⇒010001⇒6**

$$16 - 10 + 6 - 3 - 2 - 1 + 0.5 - 0.5$$

**=6**



# Redundancy Design Operation(One Error)

## 4bit-5step SAR ADC

- Analog input : 6.3
- Redundant weight :
  16, 10, 6, 3, 2, 1

## Correctable expression

**6.3⇒010001⇒6**

## Another expression

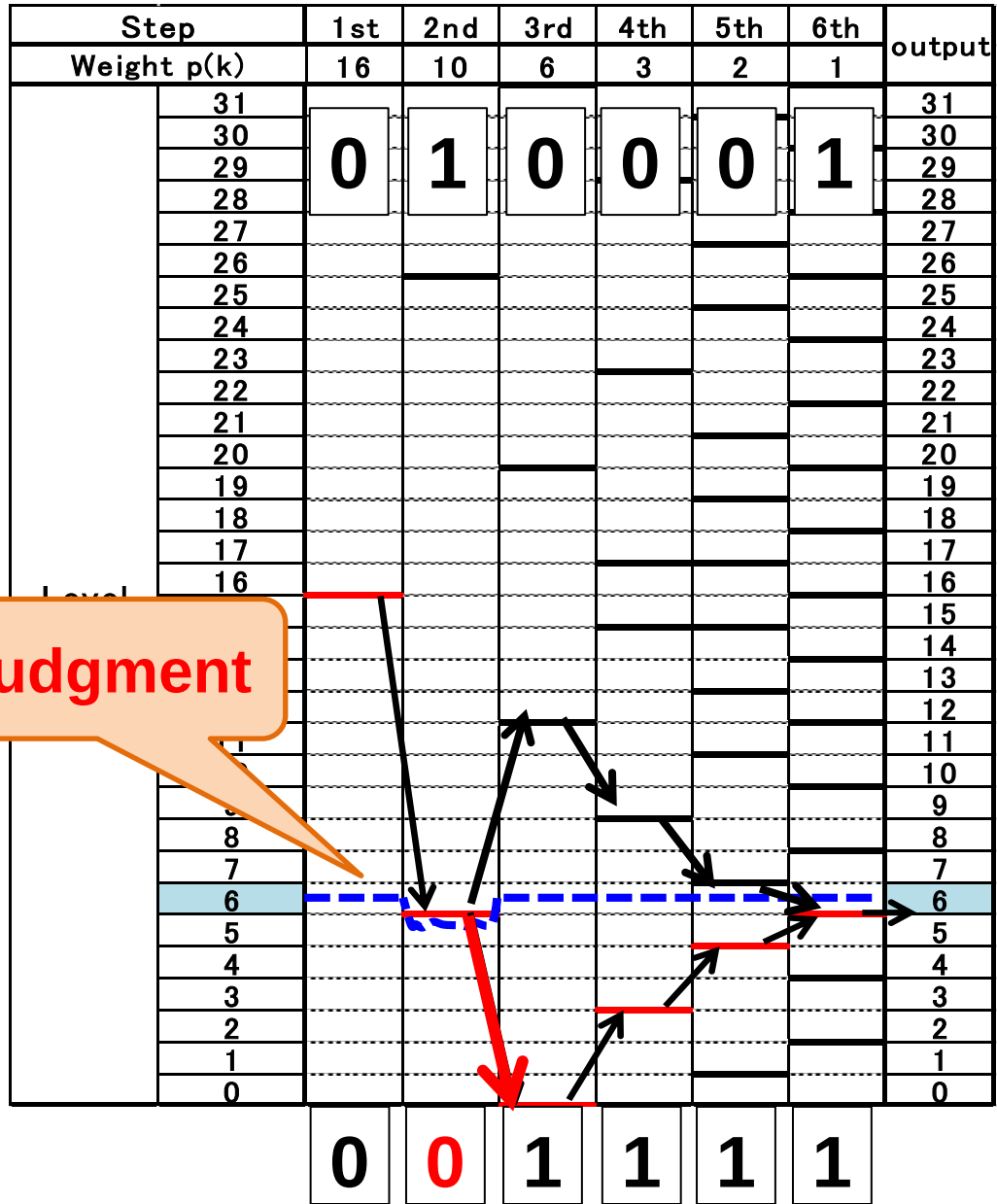
**6.3⇒001111⇒6**

$16 - 10 - 6 + 3 + 2 + 1 + 0.5 - 0.5$

$= 6$

**Error correction**

**High-Reliability**



# Issues of Conventional Method

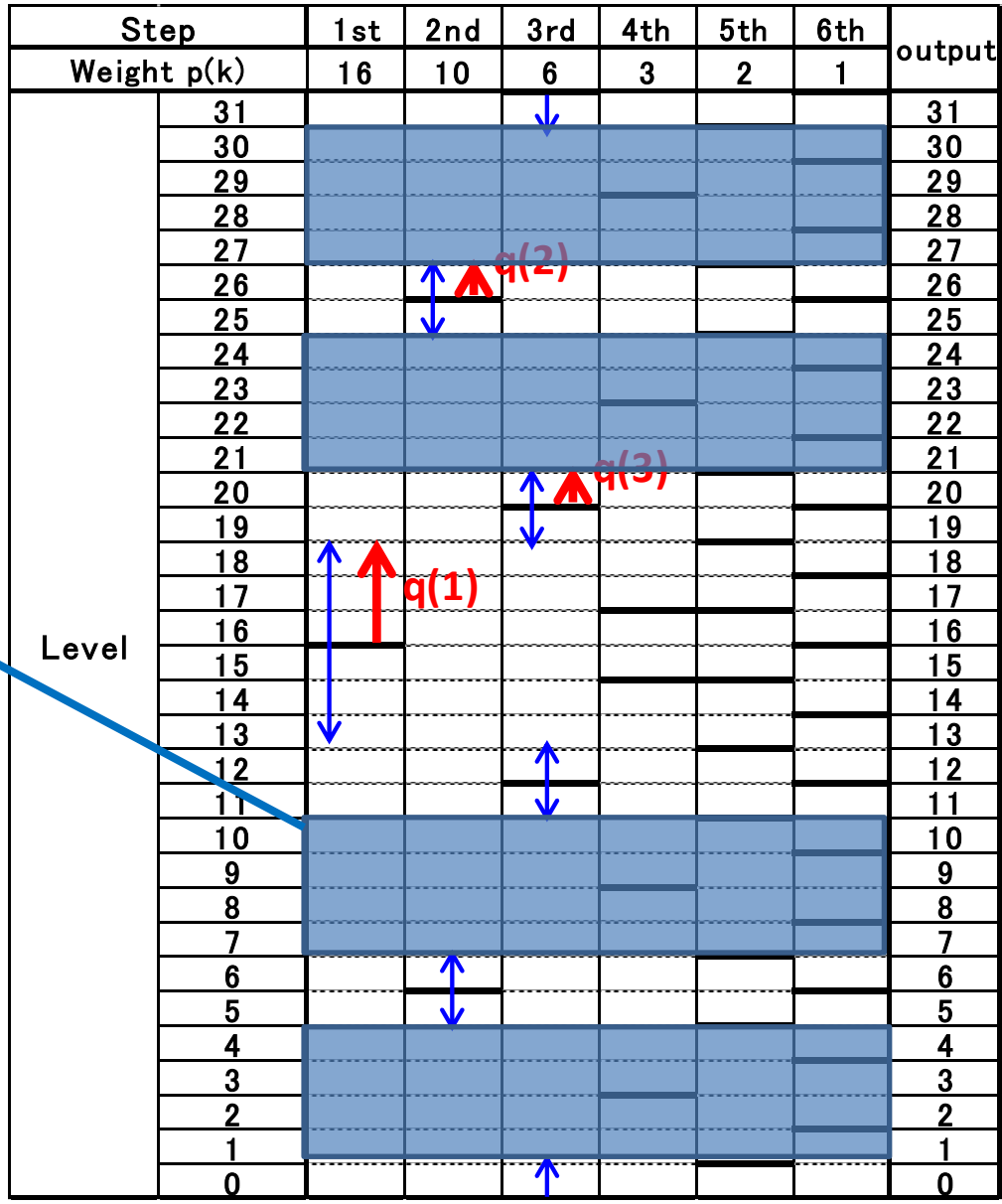
## Selection Reference Voltages

1. ***Difficult to select good reference voltages***
2. ***q(k) must be fraction***

**Uncorrectable Range**

Not effective redundancy design

Good selection method is needed !



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# Fibonacci Sequence

## Fibonacci Definition

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1} \qquad \text{(n=0,1,2…)}$$

**Example of Fibonacci number**

$$0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55 \ldots$$

**Leonardo Fibonacci**
**(Italy:1170-1250)**

## Property

**The closest terms ratio :** ***"Golden Ratio"***

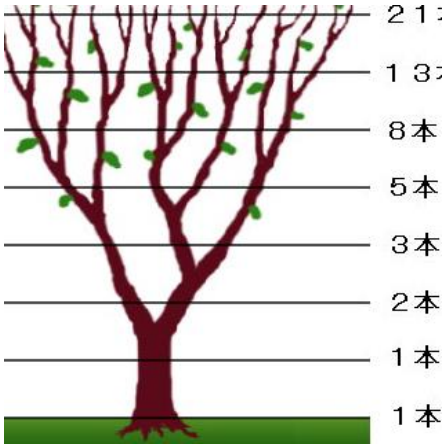
*(about 1.62)*

$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895$$

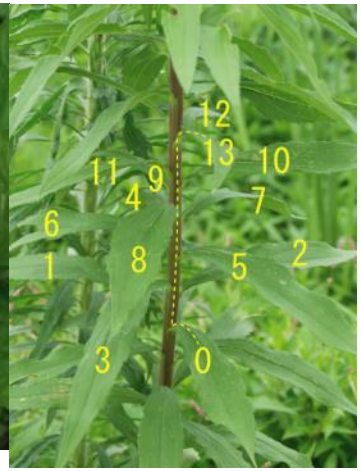
# Fibonacci Numbers

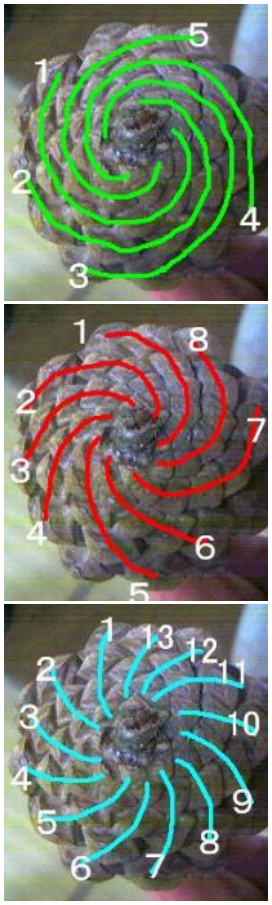
**0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144…**

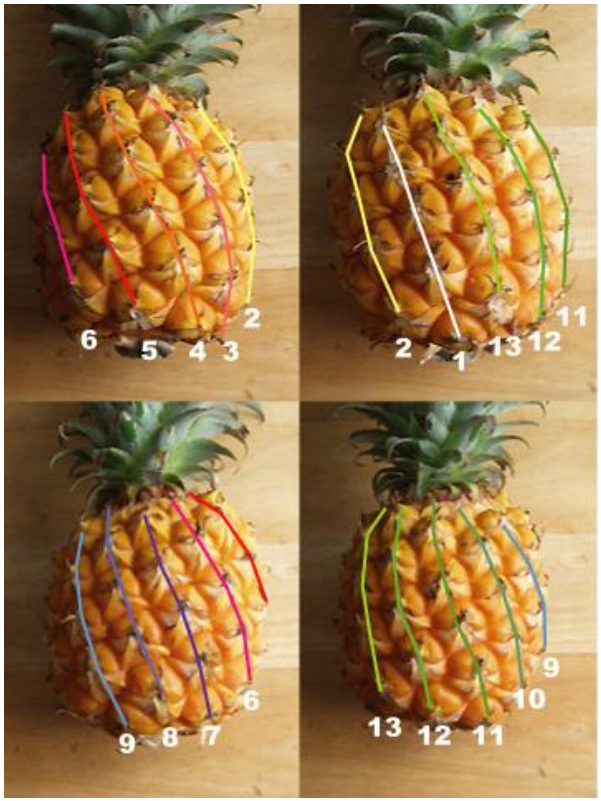
**We can see Fibonacci numbers in nature, especially in plants.**





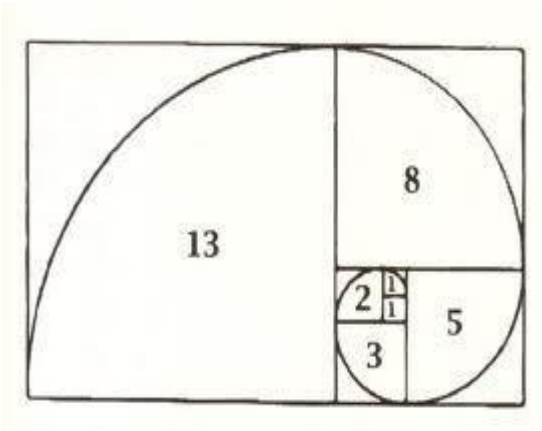



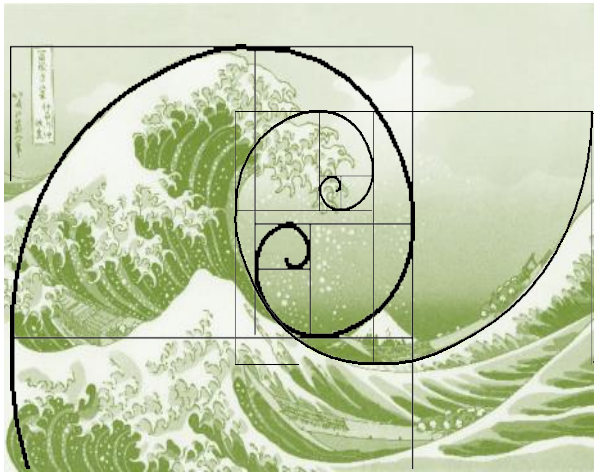
# Golden Ratio

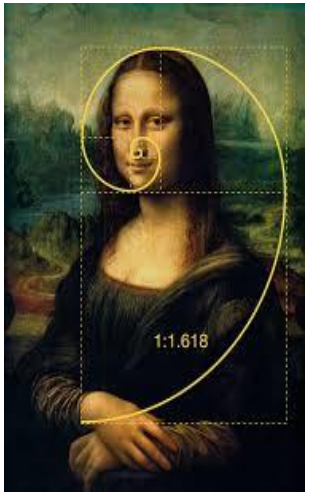
**Golden Ratio :** $\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895 = \varphi$

The most beautiful ratio



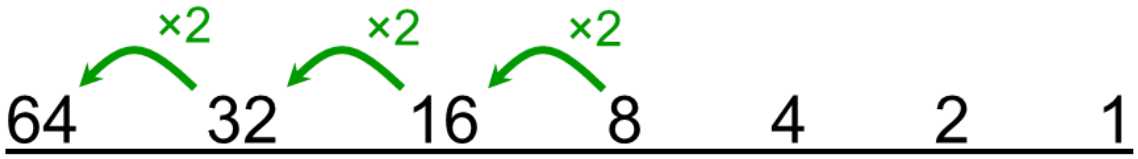




# Use of Fibonacci Sequence

## Use of **Binary**



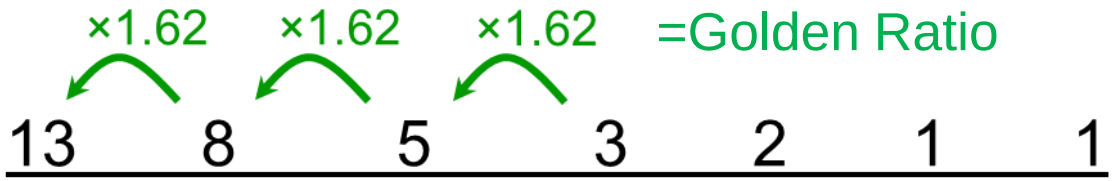


**Binary Weighted** (Radix=2)

Radix：Decision weighted number

Change weighted

## Use of **Fibonacci**





**Fibonacci Weighted** (Radix=1.62)

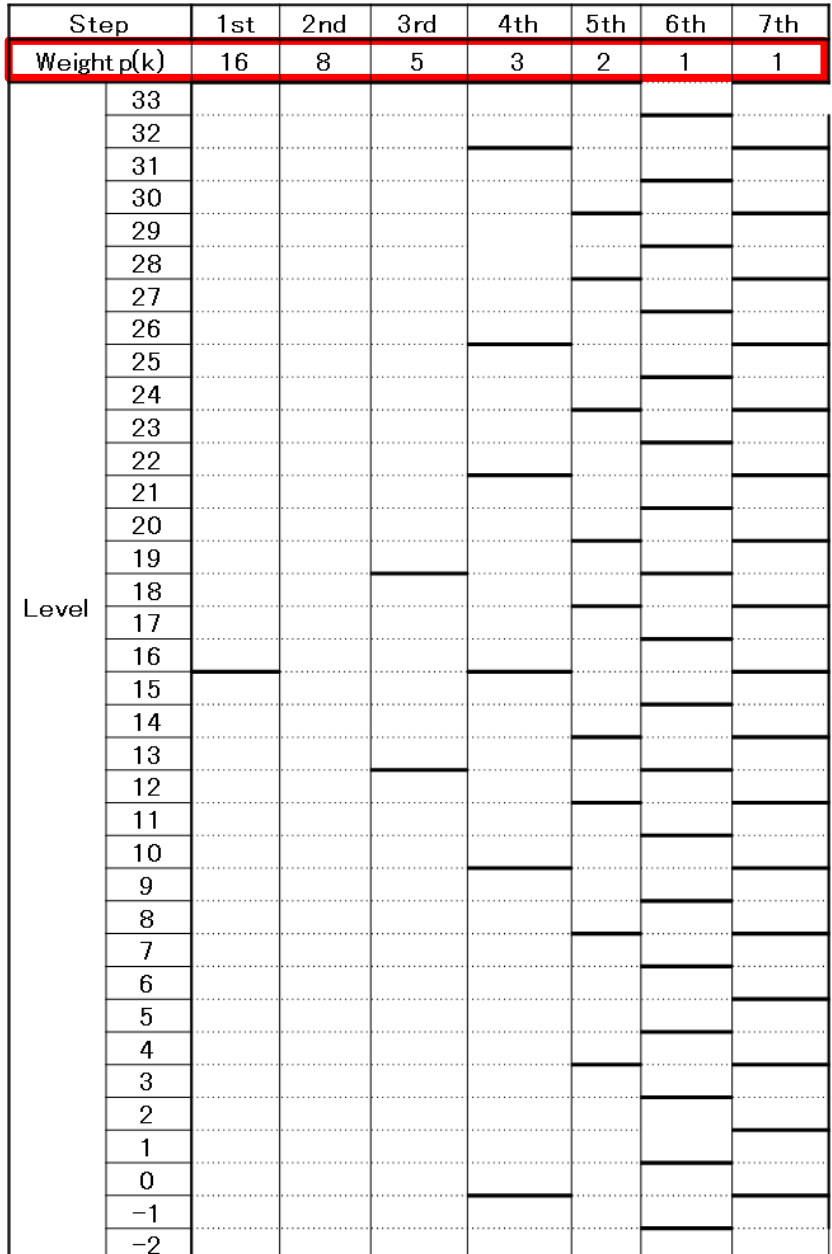
Realize 1.62 weighted by using only integer

# Correction of Fibonacci Redundant Design

## Fibonacci sequence SAR ADC

**Detect new natures of two points !**

1. ***Correctable range q(k) is always Fibonacci number*** $F_{M-k-1}$.
2. ***q(k) is exactly in contact q(k+1) without overlap.***



# Correction of Fibonacci Redundant Design

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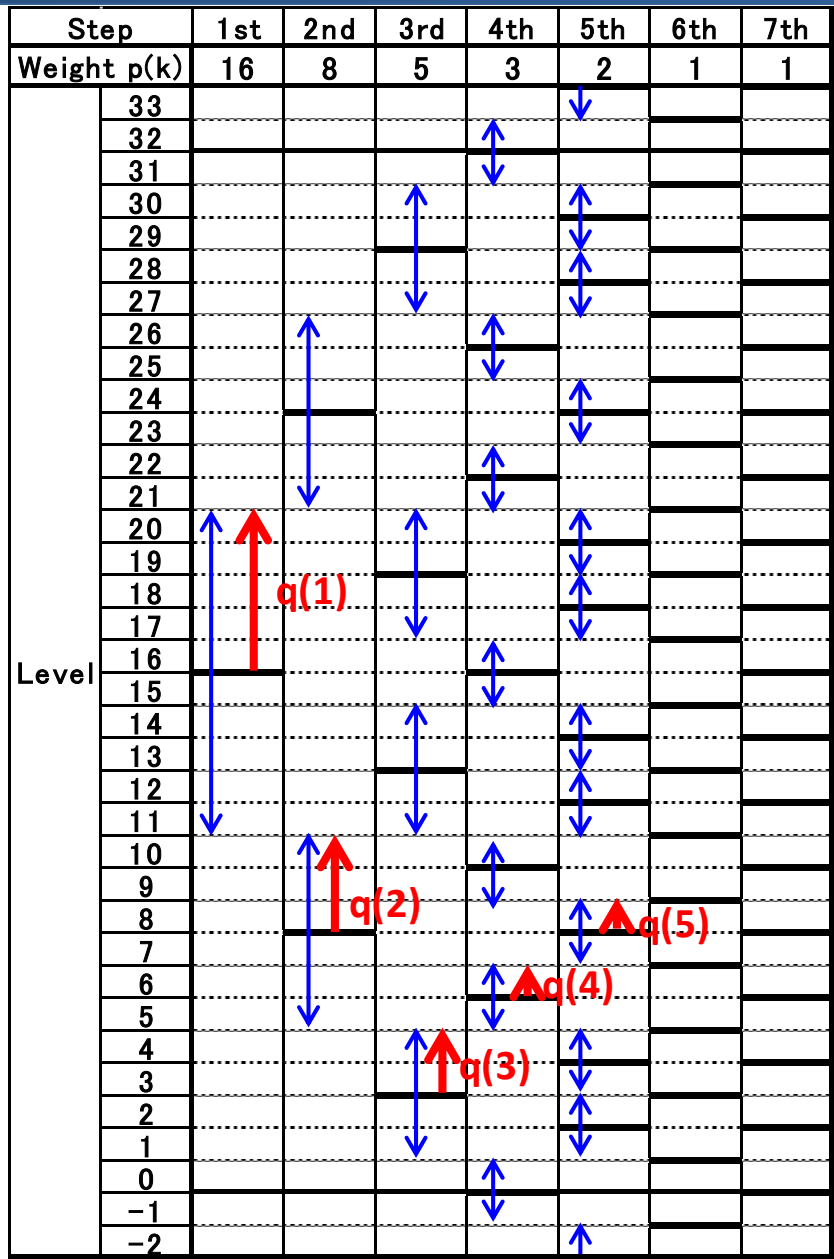

# Correction of Fibonacci Redundant Design

## Fibonacci sequence SAR ADC

**Detect new natures of two points !**

1. *Correctable range q(k) is always Fibonacci number $F_{M-k-1}$.*
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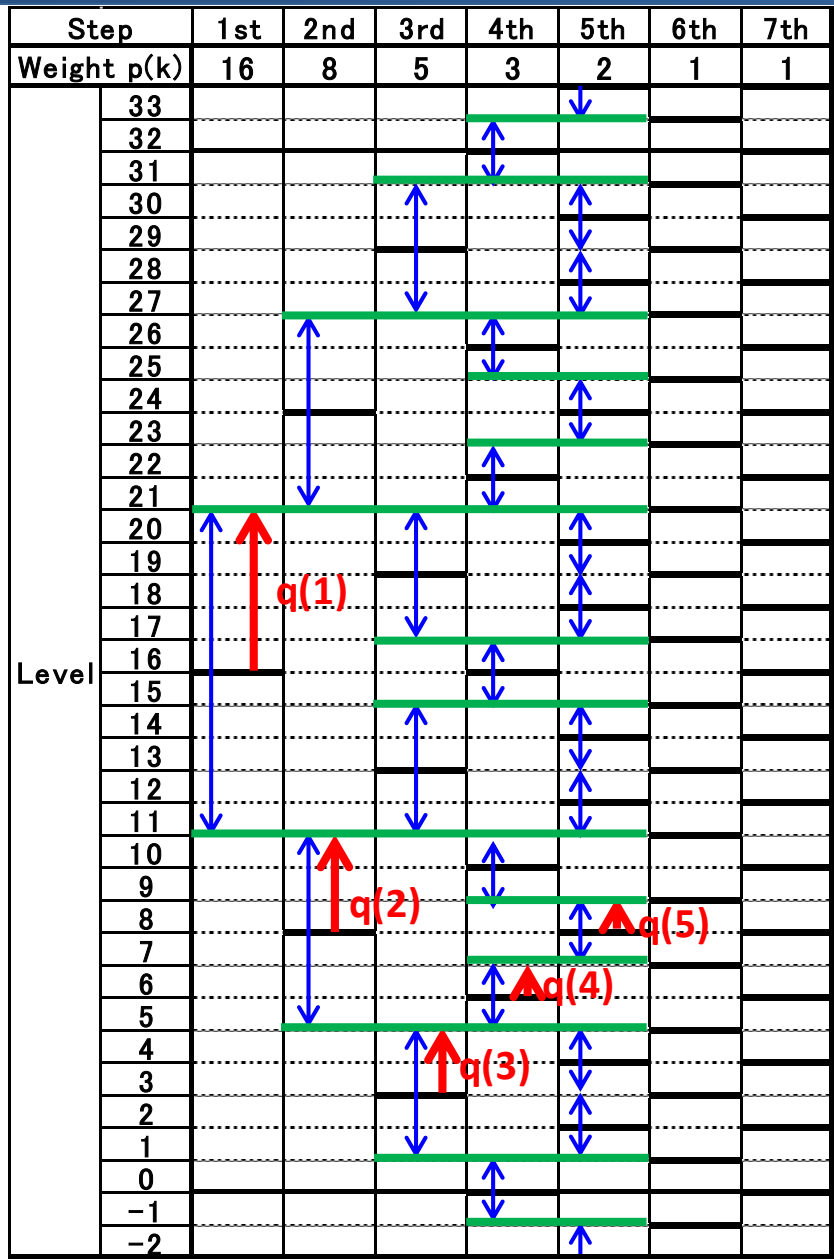


# Correction of Fibonacci Redundant Design

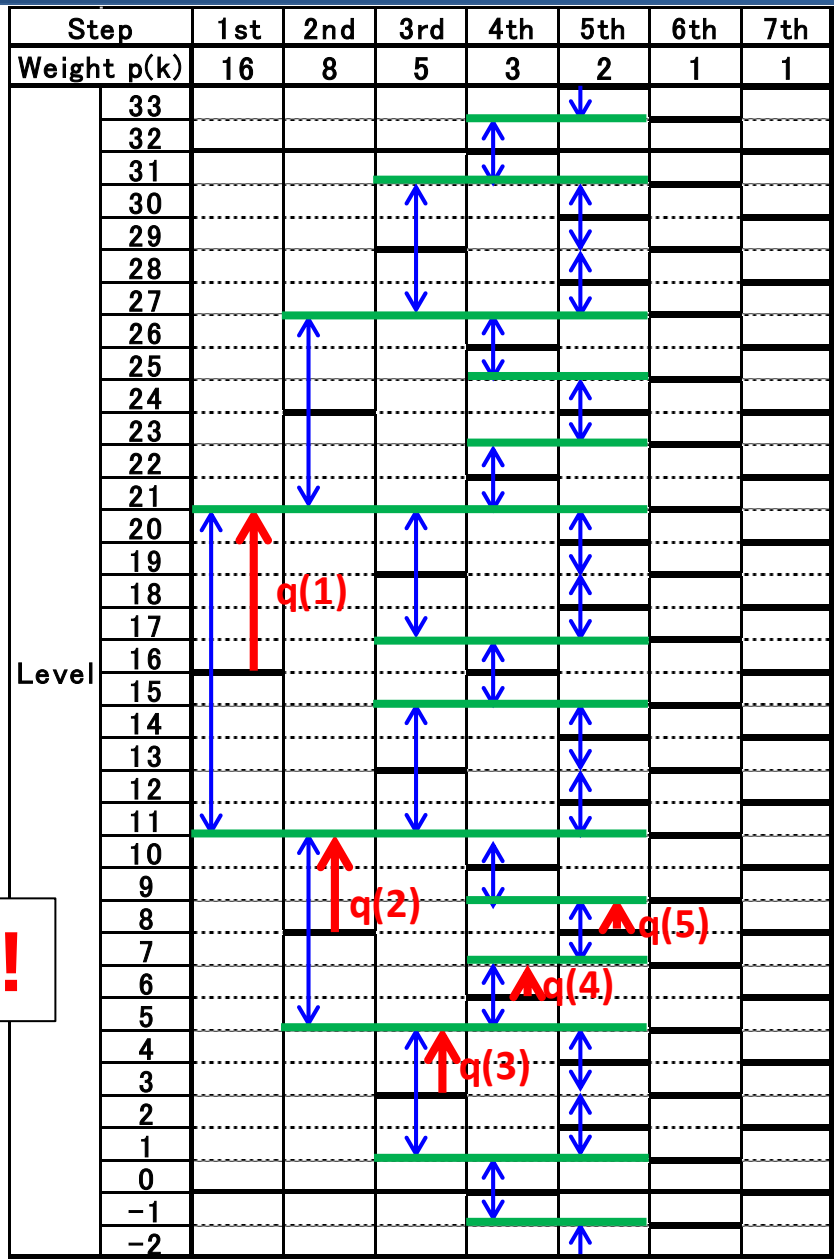
## Fibonacci sequence SAR ADC

**Detect new natures of two points !**

1. ***Correctable range q(k) is always Fibonacci number*** $F_{M-k-1}$.
2. ***q(k) is exactly in contact q(k+1) without overlap.***

Golden ratio covers wide input range by minimum extra comparison steps.

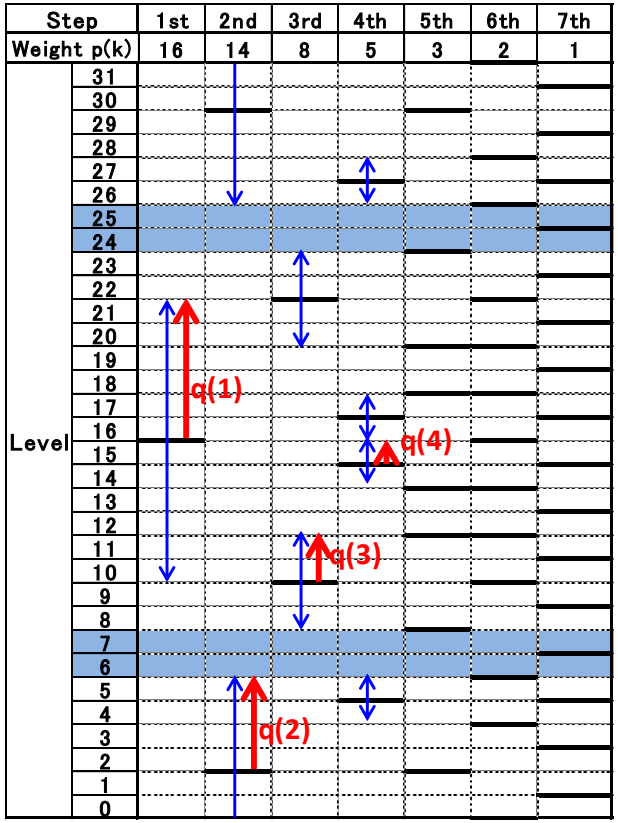
**The most efficient design !**

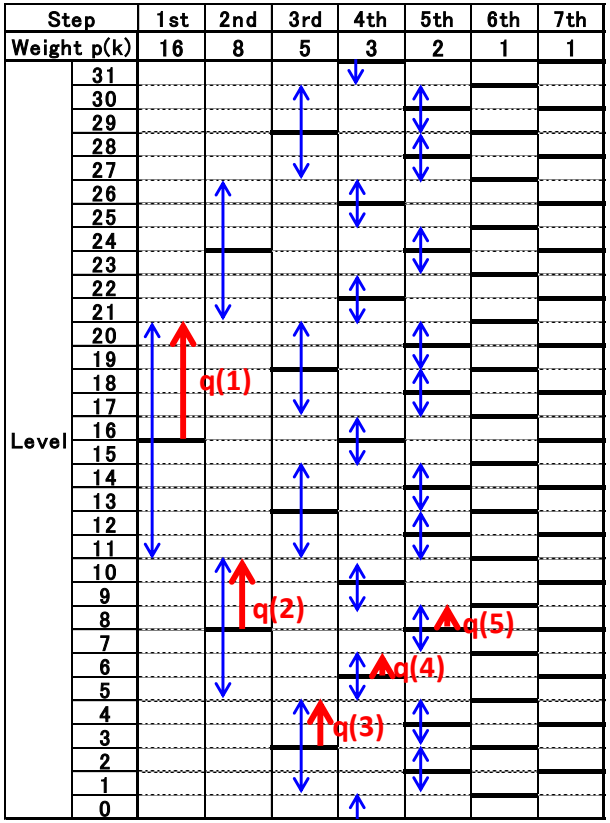


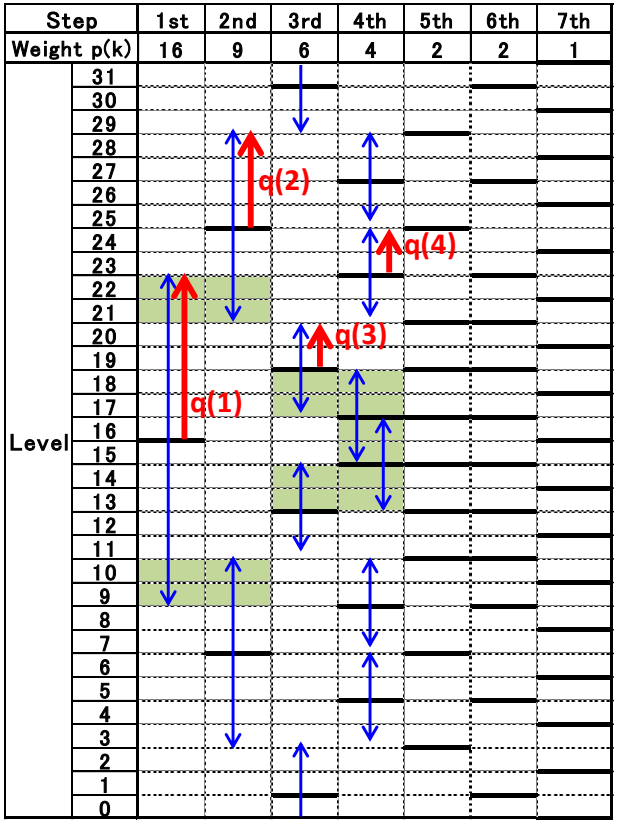
# Comparison with Conventional Method

**5bit SAR ADC**

| Conventional method | Proposed method | Conventional method |
|---|---|---|
| Radix=**1.7** | **1.62** | **1.55** |
| Radix is **bigger** than 1.62 | **Standard !** | Radix is **smaller** than 1.62 |
| ⇨ **separated** | | ⇨ **overlapped** |



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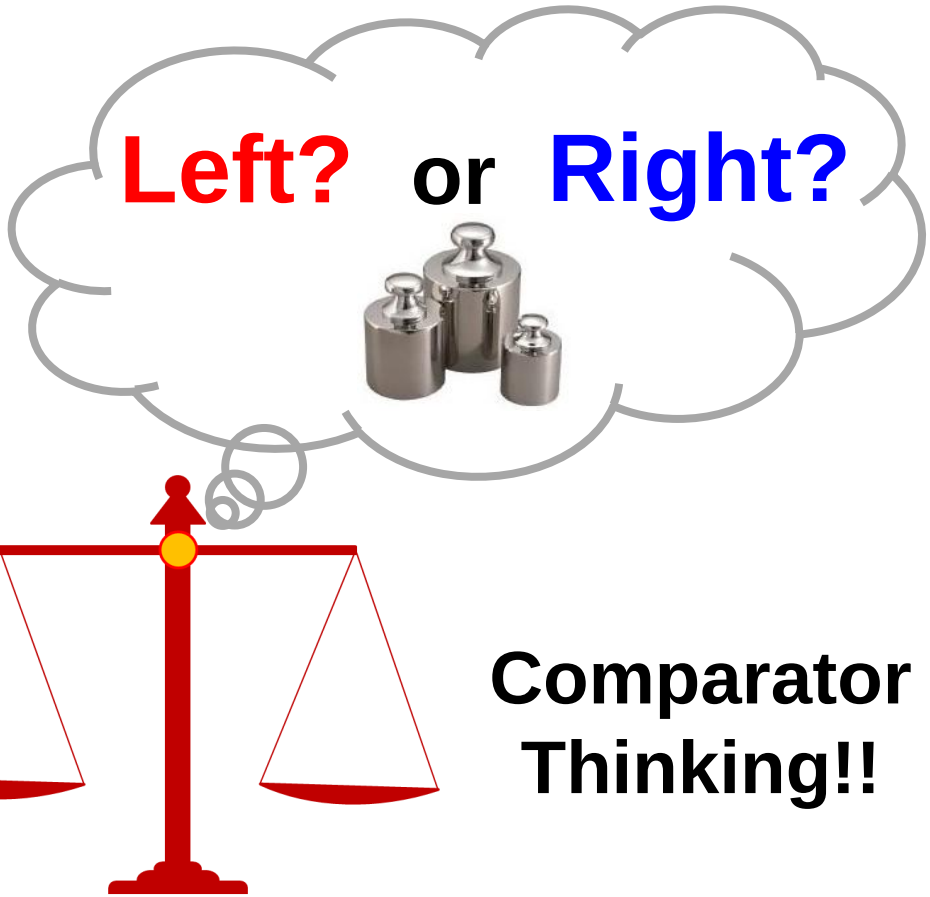
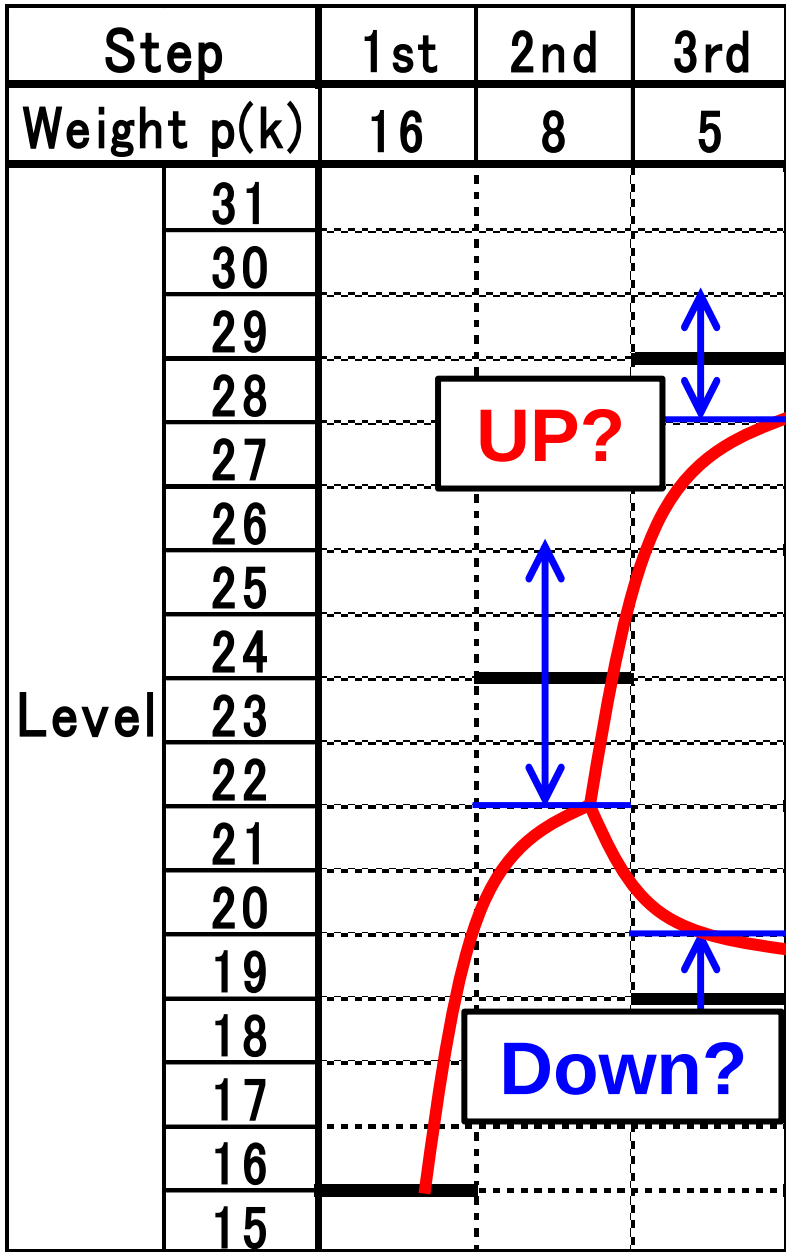
# DAC Output Settling Time

## Settling Time

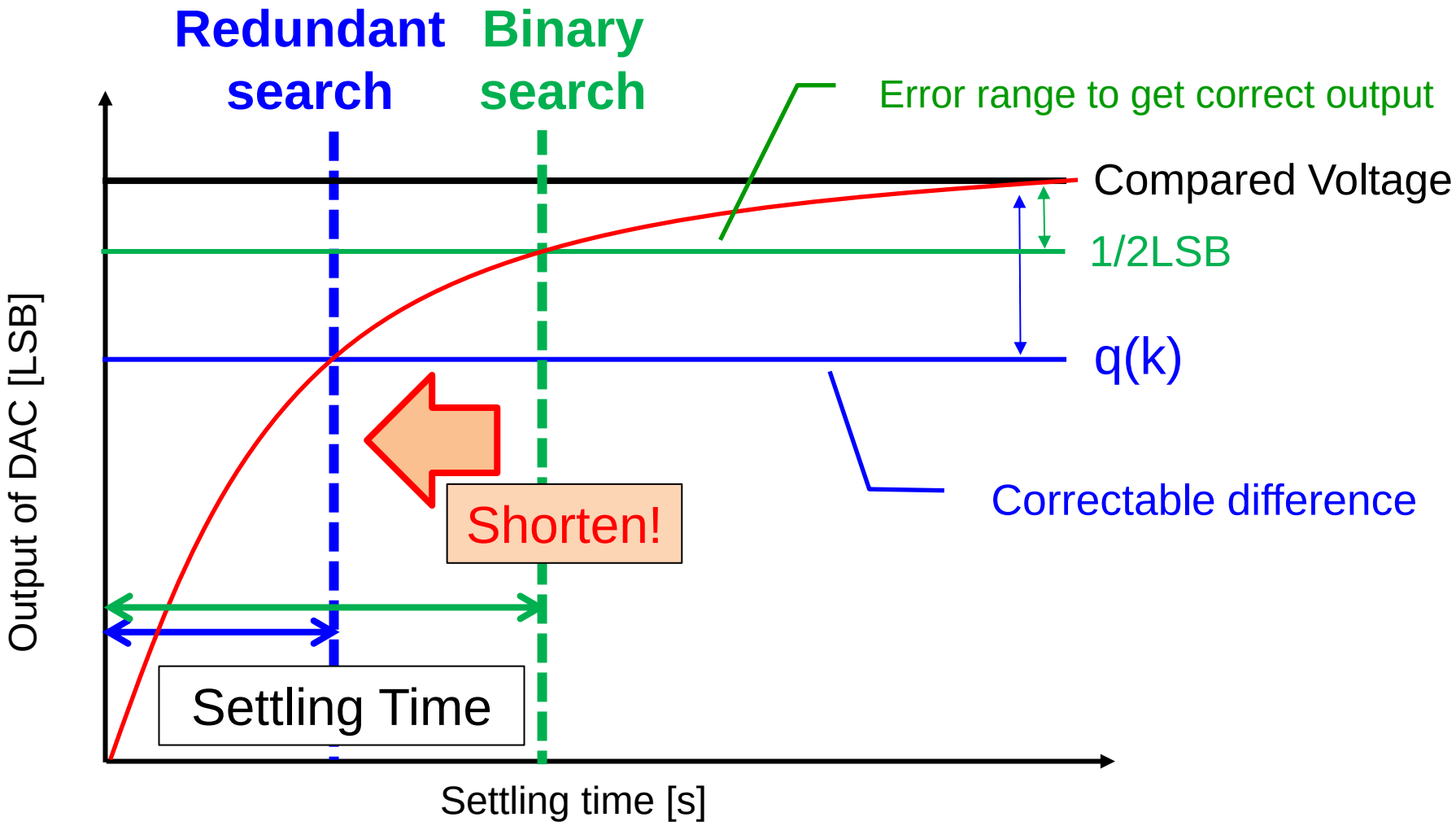
***Transition time from kth step voltage to next step voltage***



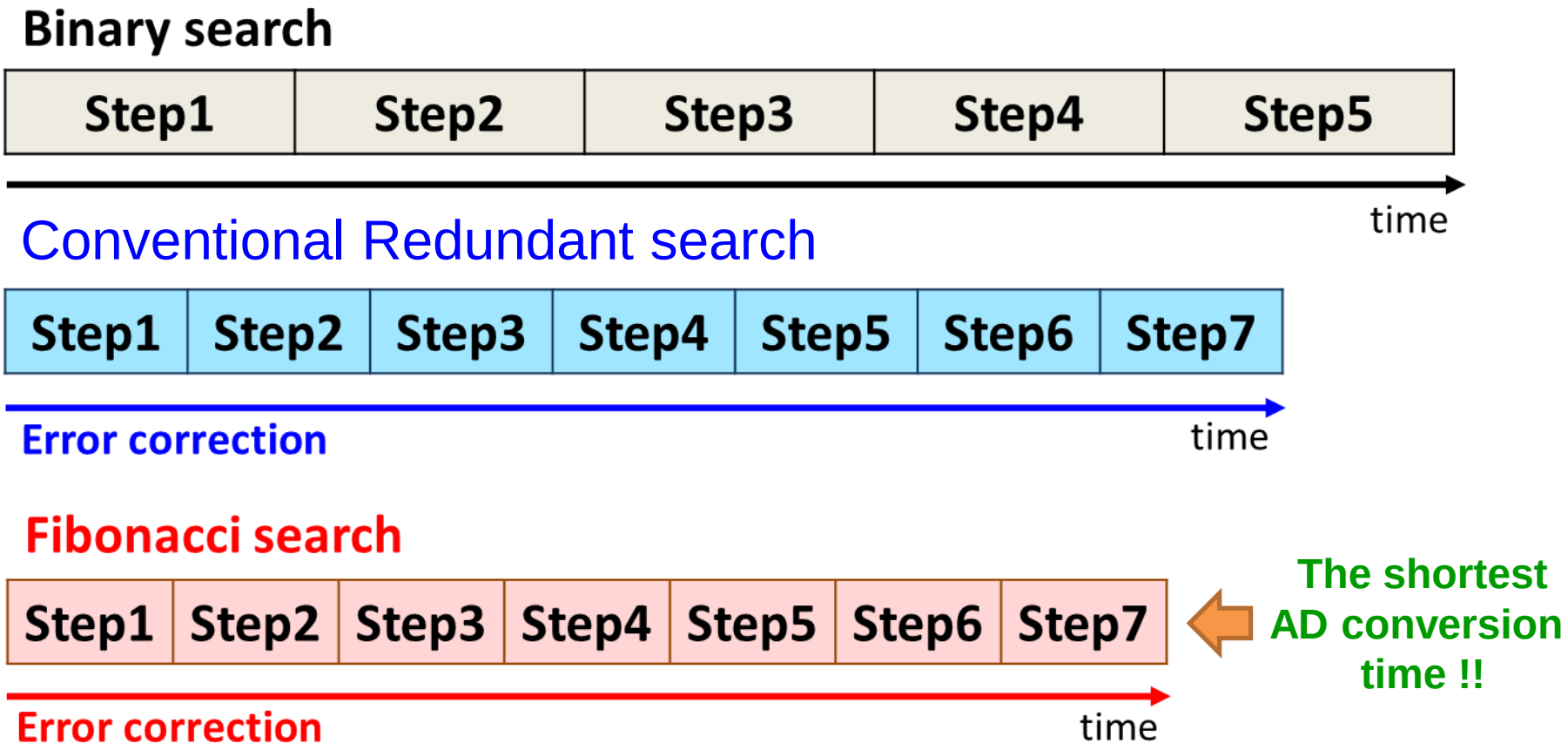
# DAC Settling Time at Every Step

## Shorten Conversion time

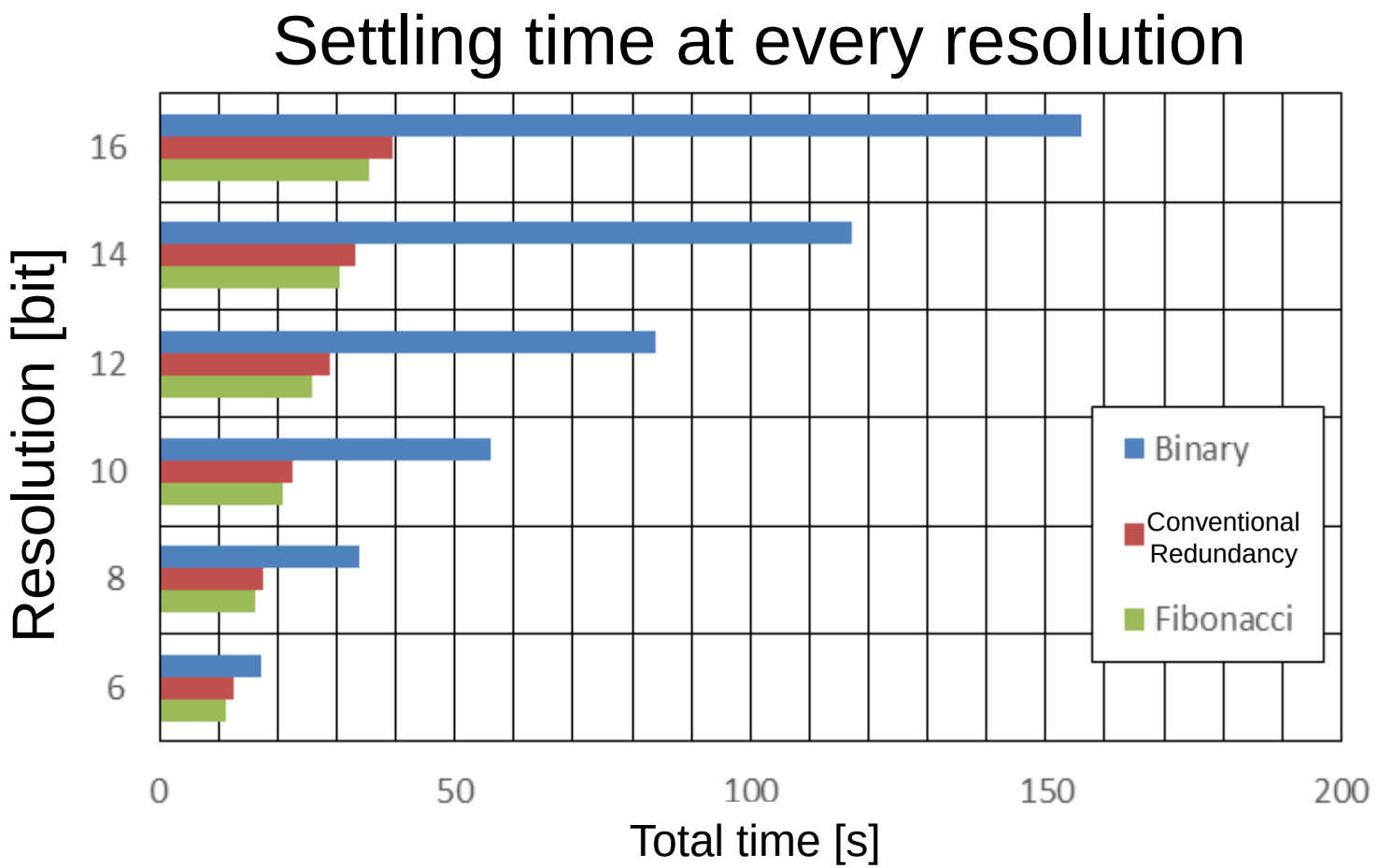


# Reduction of Settling Time

5bit SAR ADC



# Comparison of Incomplete Settling Time




At fixed clock,

**Fibonacci ⇨ the shortest AD conversion time !!**

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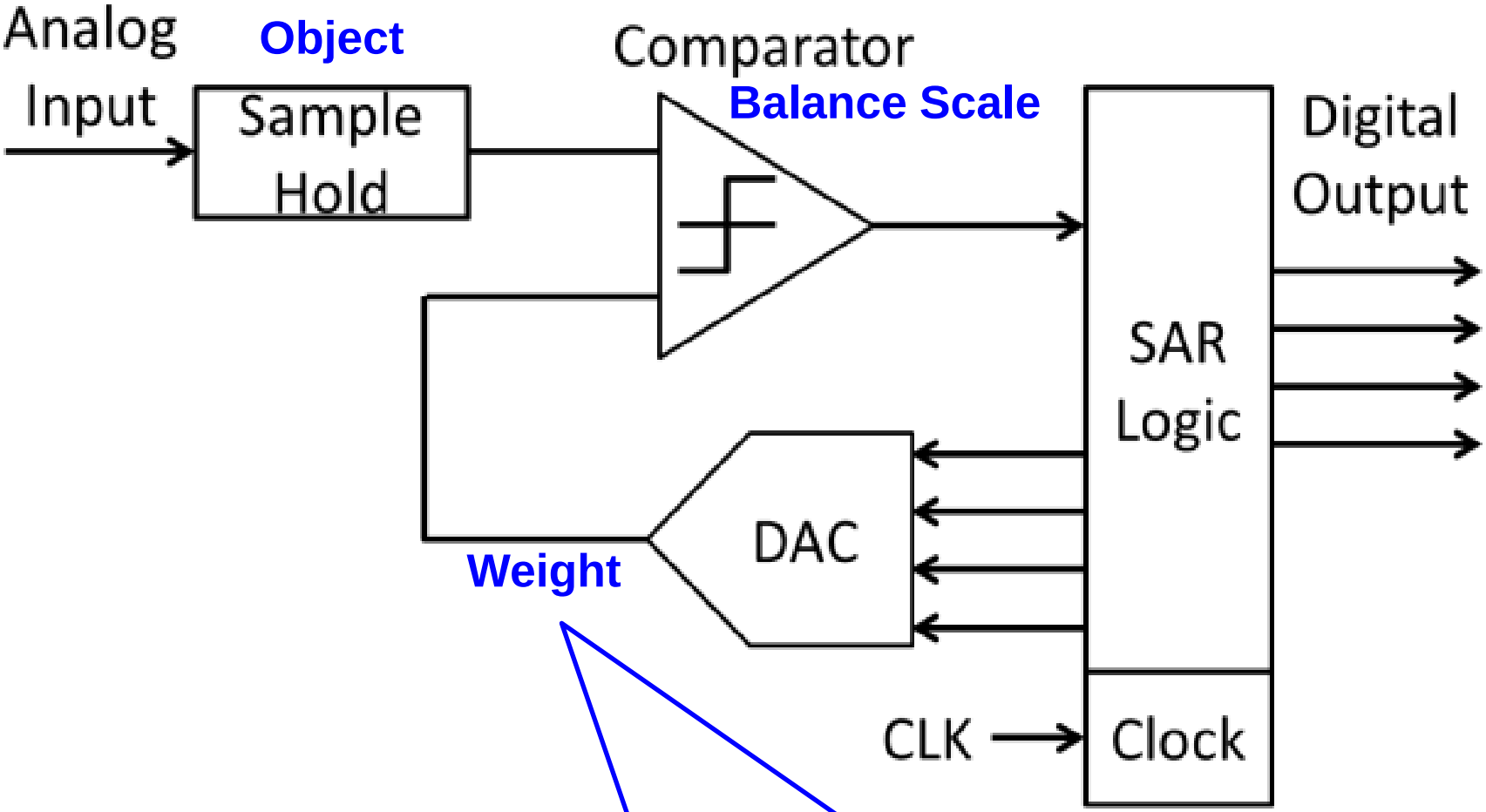
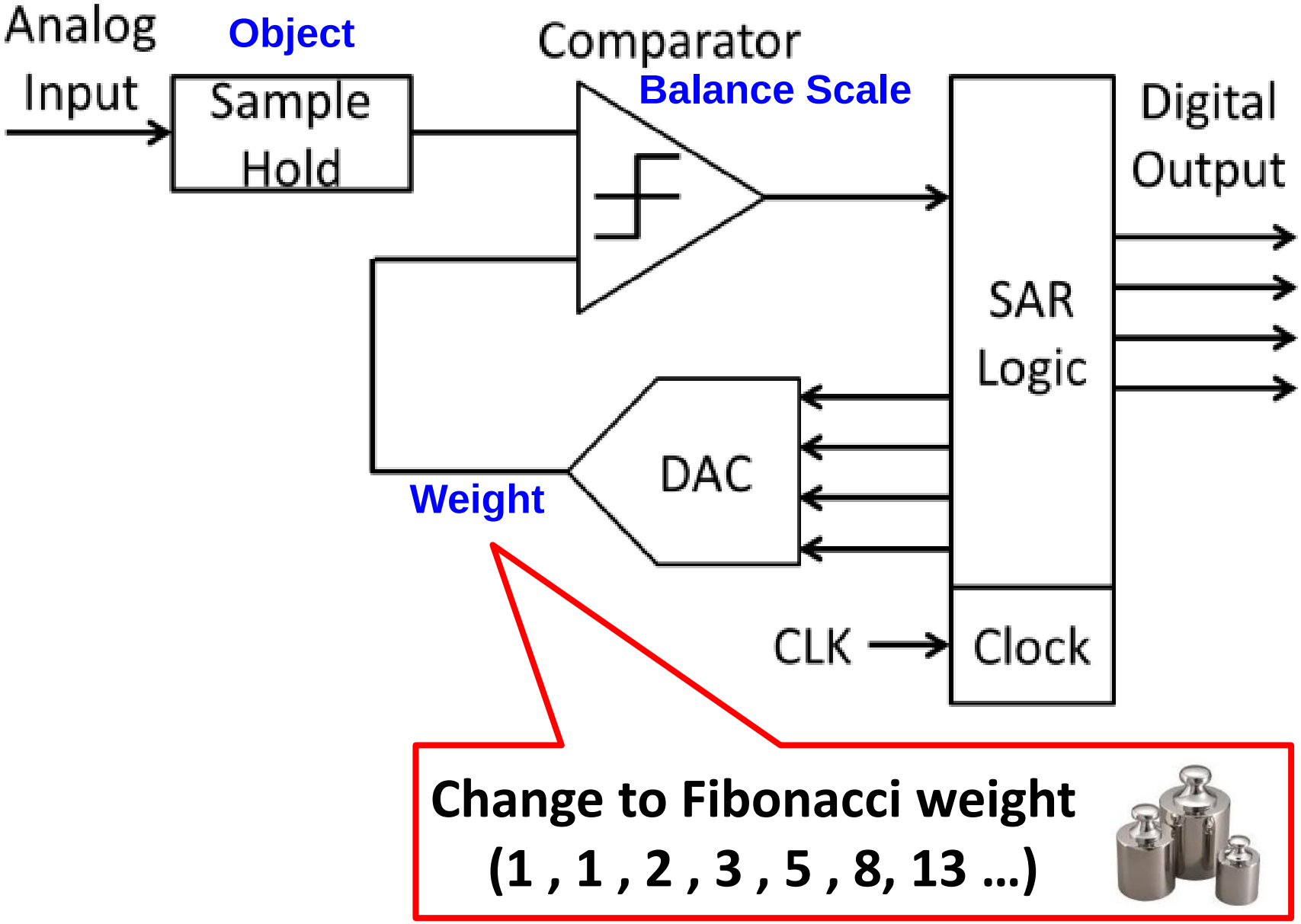
# Binary SAR ADC Configuration

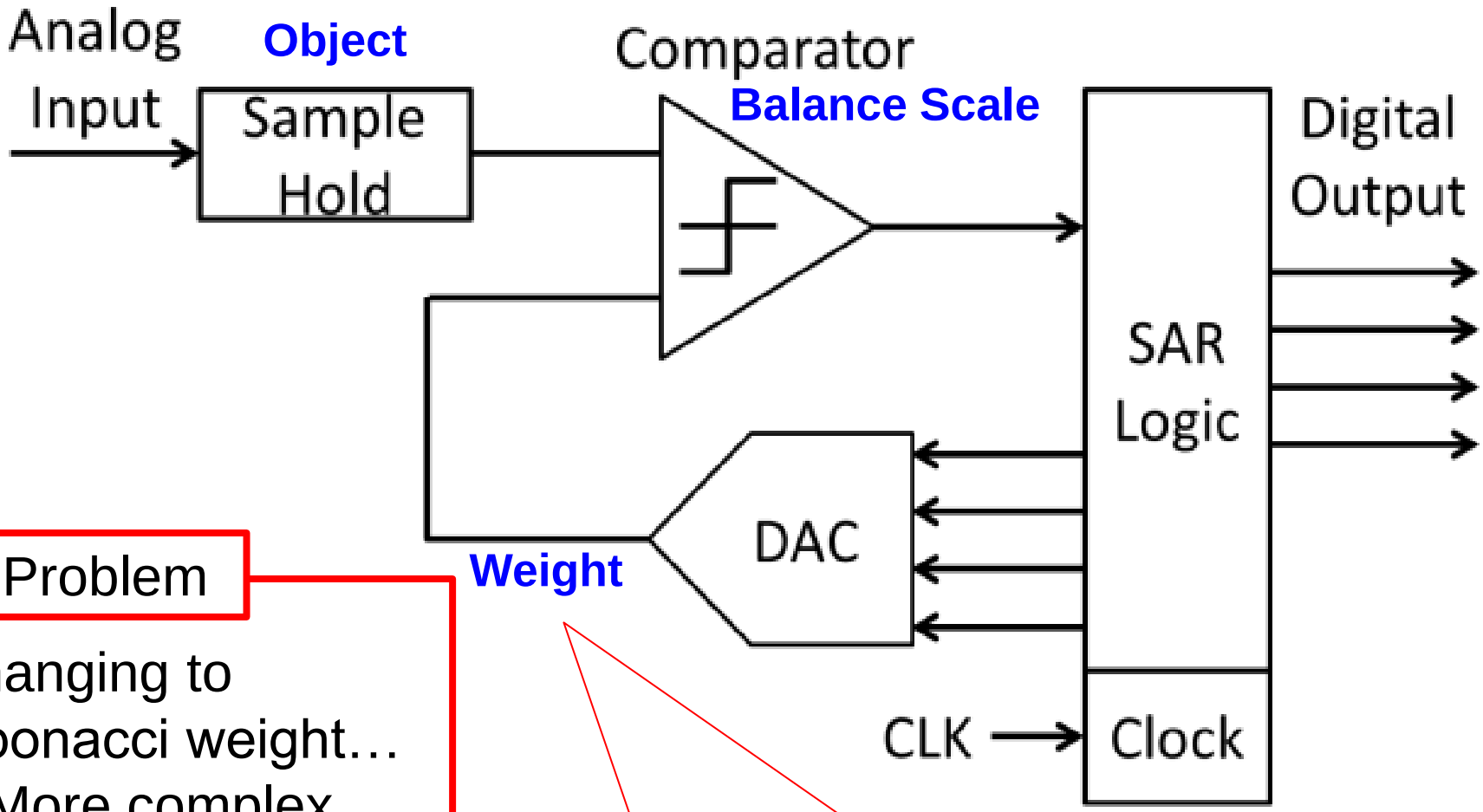



**Generally use binary weight**
**(1 , 2 , 4 , 8 , 16 , 32, 64 …)**

# Fibonacci SAR ADC Configuration



# Fibonacci SAR ADC Configuration




**Problem**

Changing to Fibonacci weight…

- More complex
- More large-scale

than conventional.

**Change to Fibonacci weight**

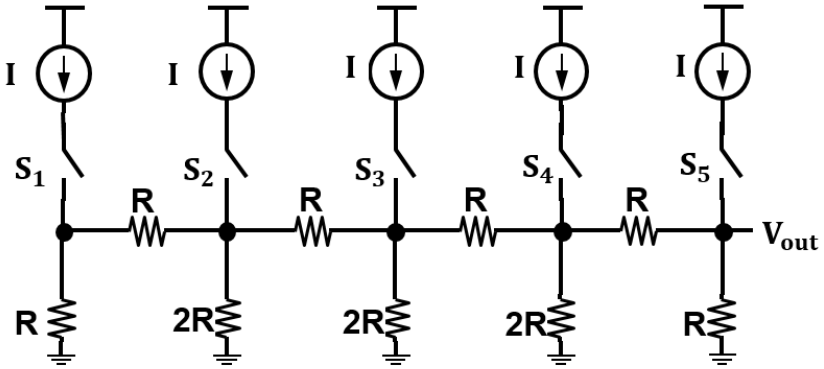
**(1 , 1 , 2 , 3 , 5 , 8, 13 …)**

# Conventional and Proposal DAC

## Conventional

R-2R resistor ladder

⇒Generate **binary** voltage



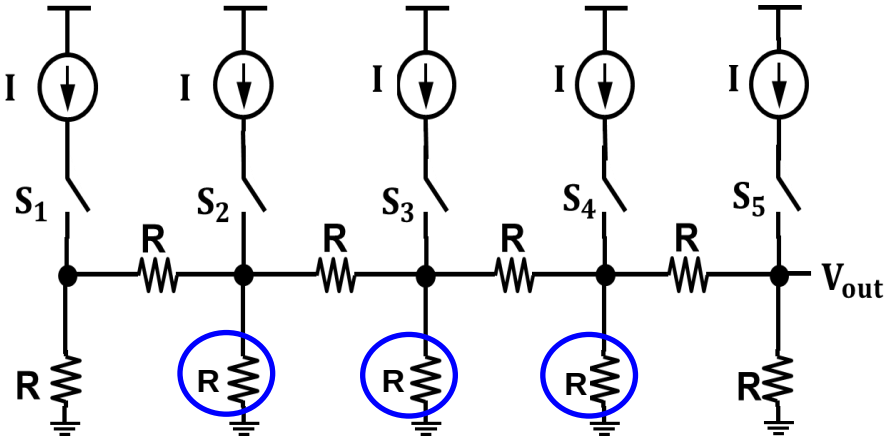

R-2R resistor ladder

Change all resistors to R

## Proposal

R-R resistor ladder

⇒Generate **Fibonacci** voltage



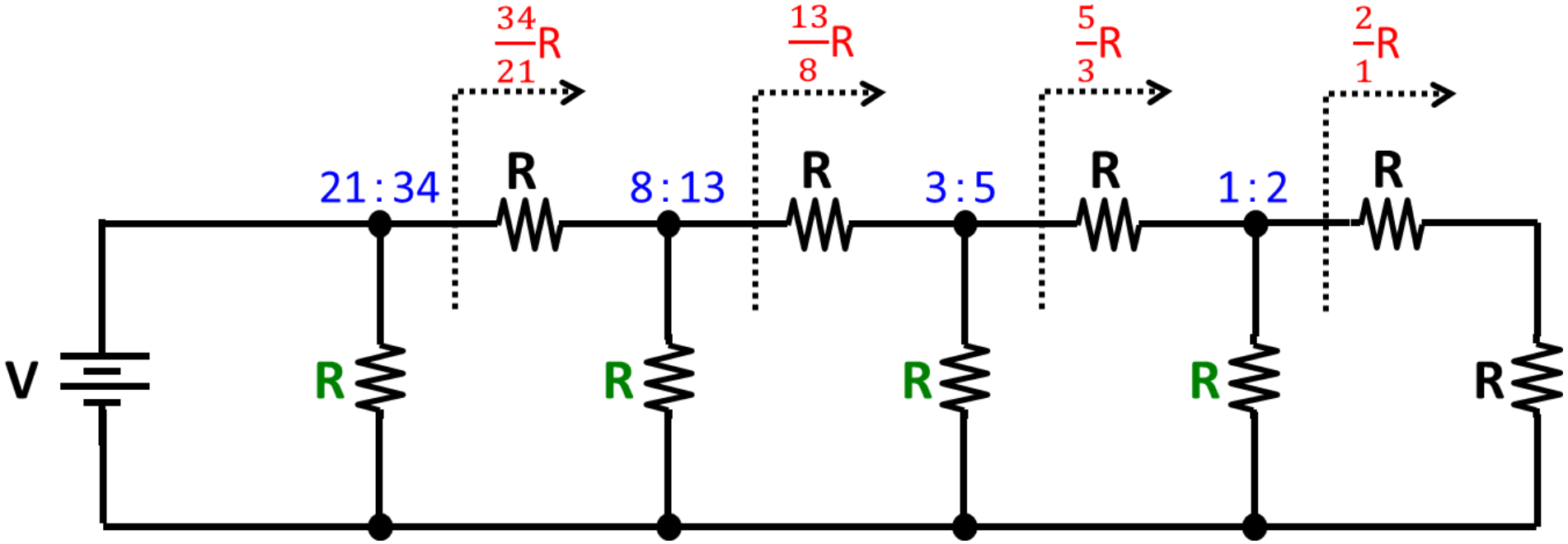

R-R resistor ladder

Realize Fibonacci DAC
by using simple circuit !

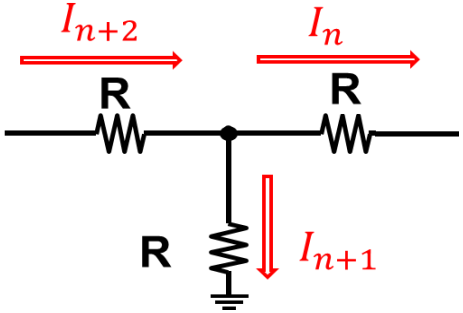
# Principle of Fibonacci Voltage

## New property

Divides current into **Fibonacci ratio** in each node




Principle




$$I_{n+2} = I_{n+1} + I_n$$

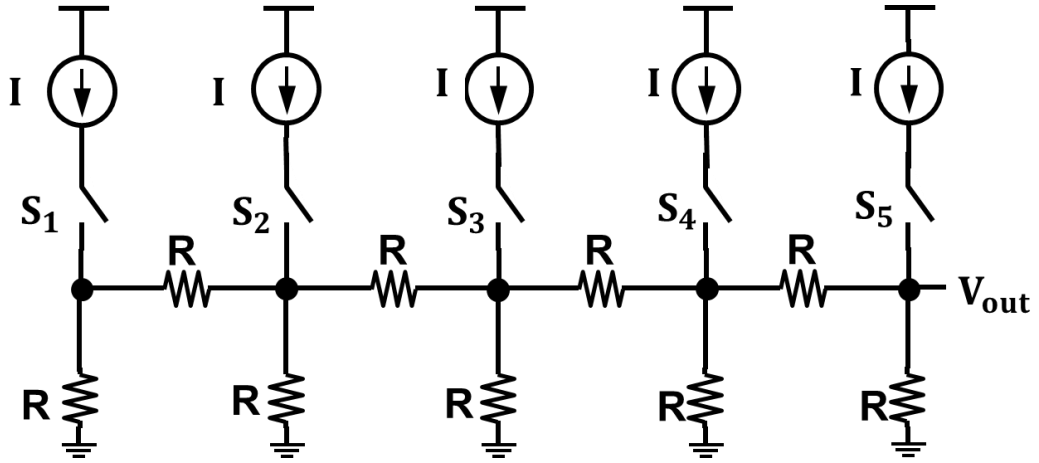
$$\Updownarrow$$

$$F_{n+2} = F_{n+1} + F_n$$

# Proposal of R//R Fibonacci DAC

**R-R resistor ladder**

Generate
Fibonacci voltage
of **odd** term

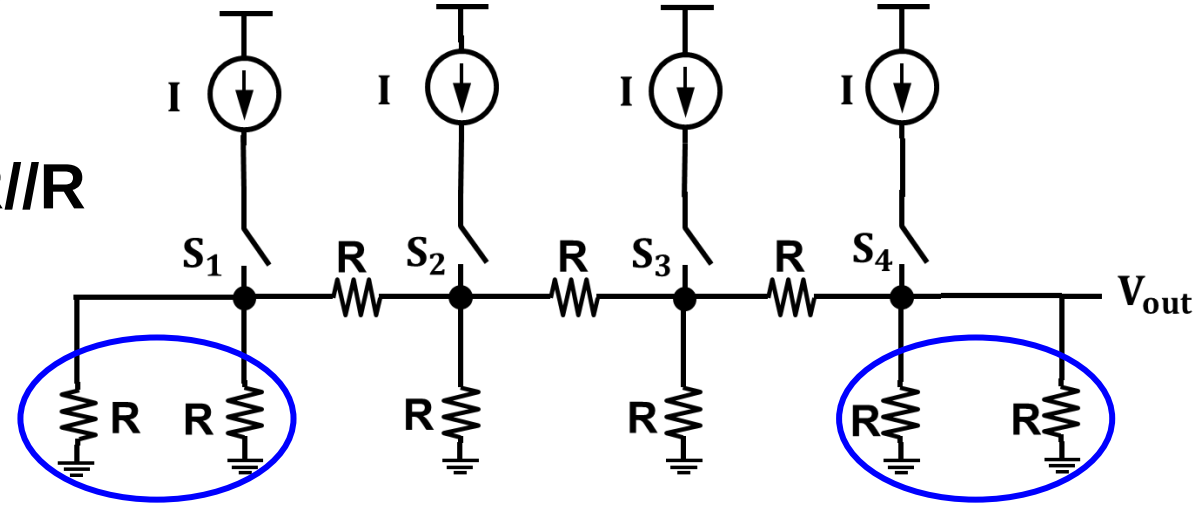



Change terminal resistors to
parallel resistors

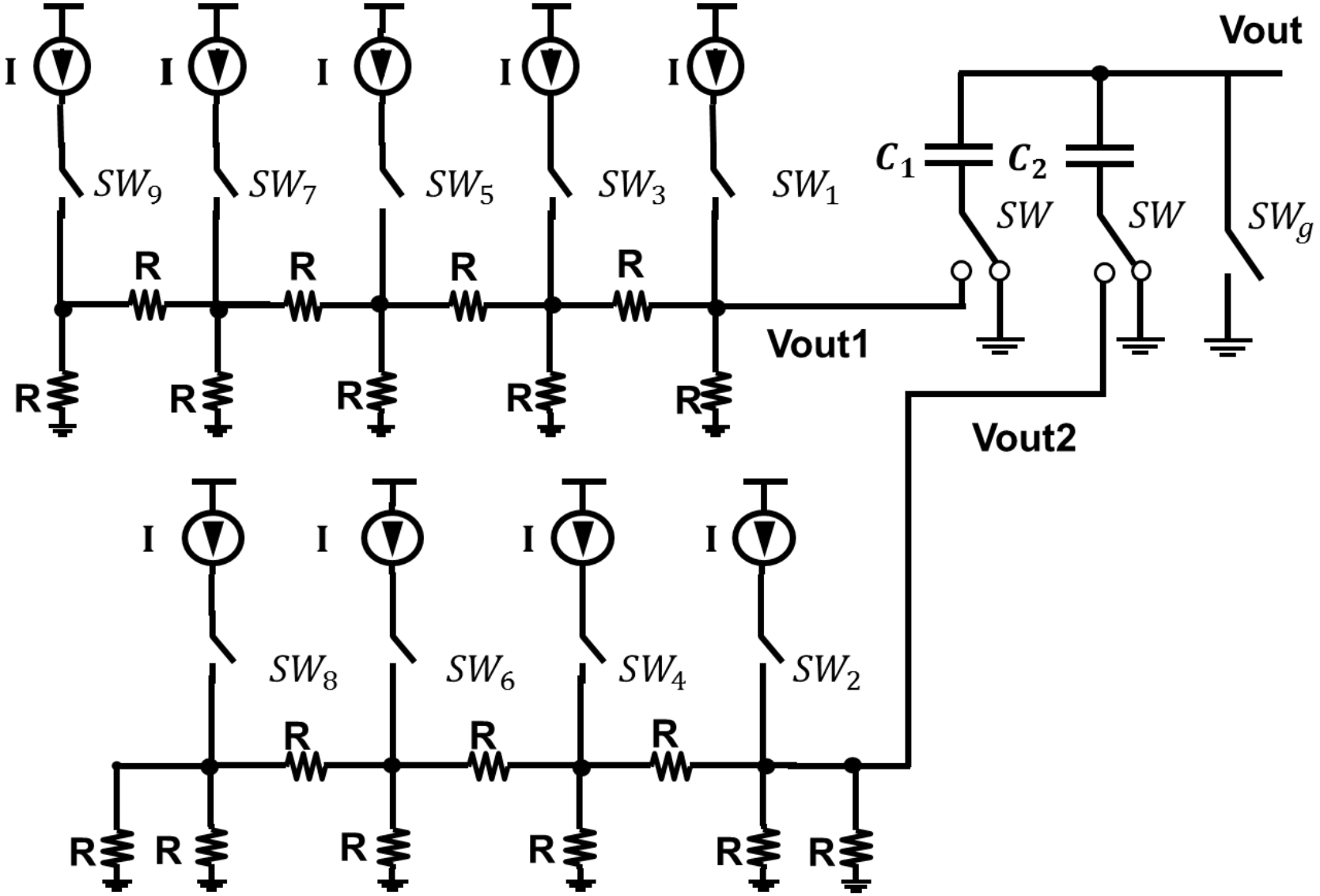
**Proposal**

**R-R resistor ladder**
**with terminations of R//R**

Generate
Fibonacci voltage
of **even** term



# Fibonacci DAC Architecture



# Outline

- Objective
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Error Correction Range
  - Settling Time
- Realization of Fibonacci DAC
- **Conclusion**

# Conclusion

- Propose redundant SAR ADC design methods

- Get important properties by using Fibonacci sequence
  - **Reliable**
    Correctable difference covers wide input range
  - **Shortest-Conversion**
    Conversion time is shortest in a fixed clock
  - **Radix-Standard**
    Golden ratio $\varphi$ establish radix standard

- Propose beautiful DAC structures
  which generate Fibonacci voltages.

Hope that these will contribute to automotive applications !

# Number theory for Engineering

Carolus Fridericus Gauss
(1777-1855)

*"Number theory is the queen of mathematics"*

*Carolus Fridericus Gauss*

## Past Number theory

Beautiful and Mysterious
was NEVER practical

## Current Number theory

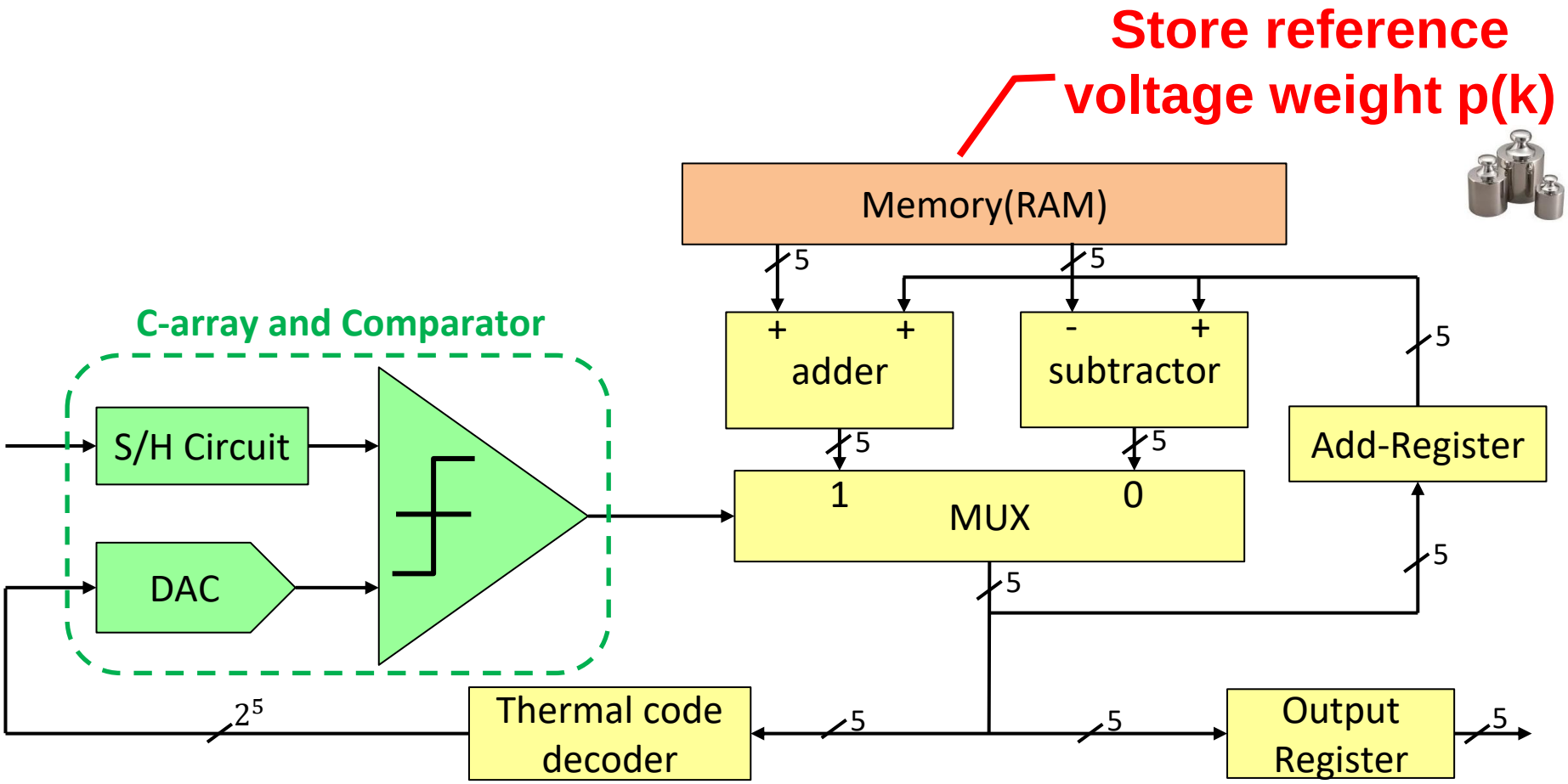
used information communication processing

➡ good match to digital technology

**Number theory application for ADC/DAC is a frontier.**
**There are great chances for new discovering !**

# Appendix

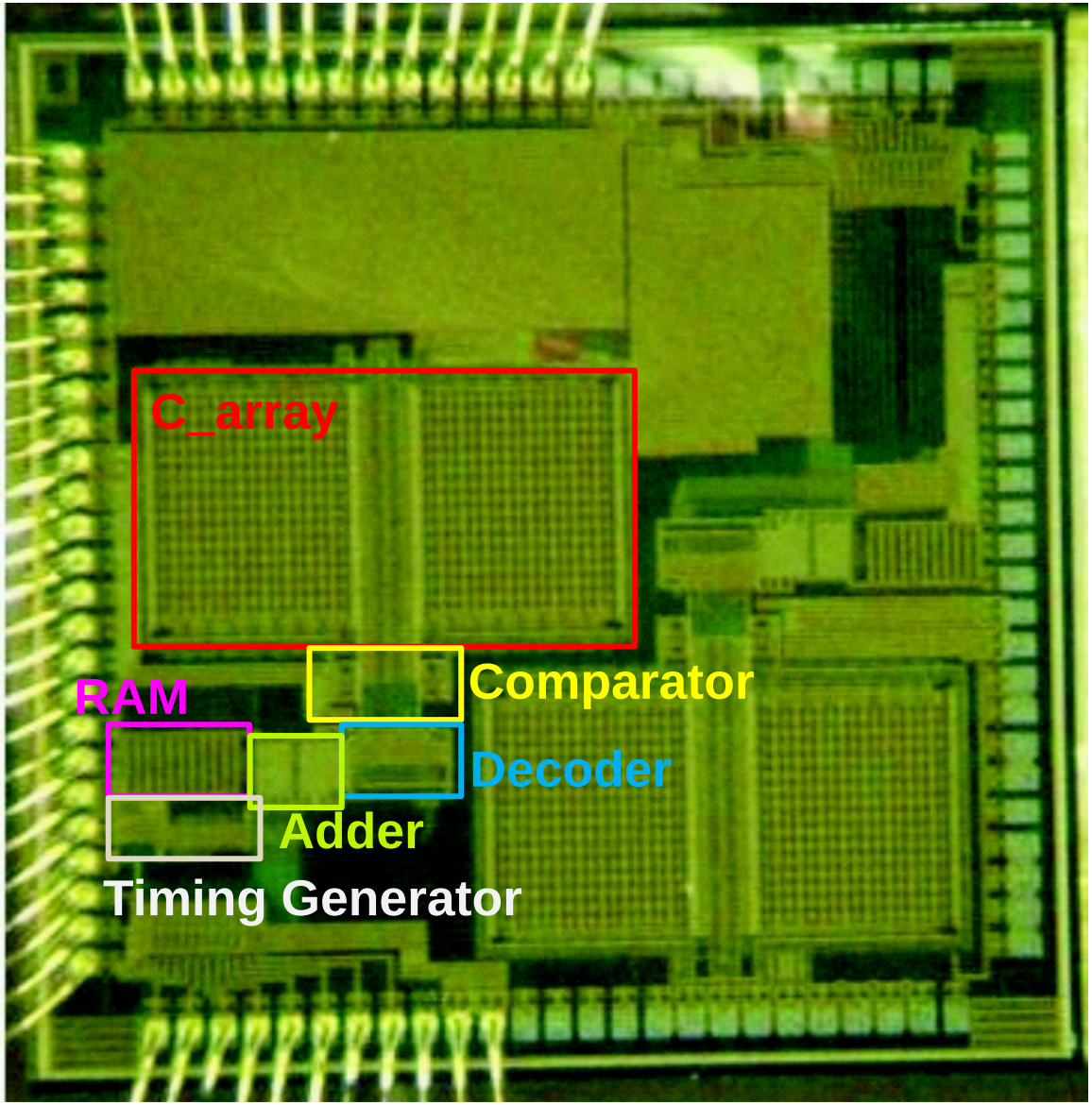
# Configuration Block of redundant SARADC




**SAR ADC circuits consist of mostly digital circuit.**

# Chip of redundant SAR ADC

**(0.18um CMOS 2.5mm x 2.5mm)**




**Additional circuits**

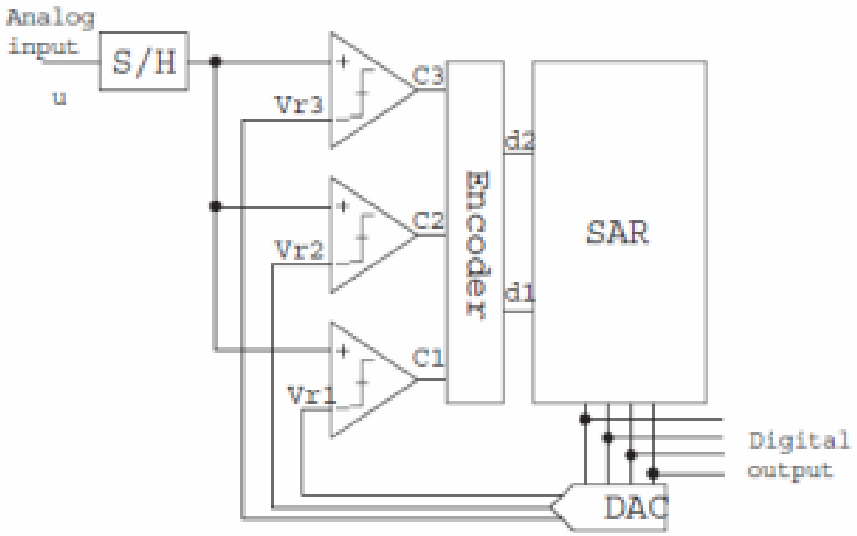
**are very small !!**

# Temporal vs Spatial Redundancy

- Temporal redundancy
- Spatial redundancy

  SAR ADC

  with 3 comparators [1]




- I have a feeling

  temporal redundancy is more effective.

[1] M. Hotta, M. Kawakami, H. Kobayashi, et. al.,
"SAR ADC Architecture with Digital Error Correction",
IEEJ Trans. Electrical and Electronic Eng. (Nov. 2010).

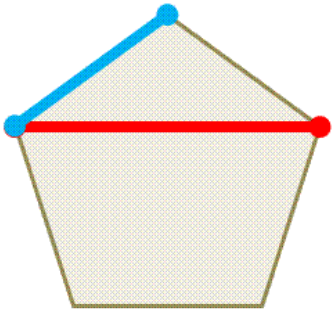
# Redundancy vs Testing

- Robust design makes its testing difficult.
- Redundancy hides defects in DUT.

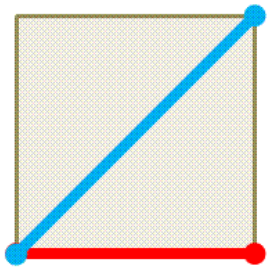
Testing of redundant systems is a challenge.

# Silver Ratio

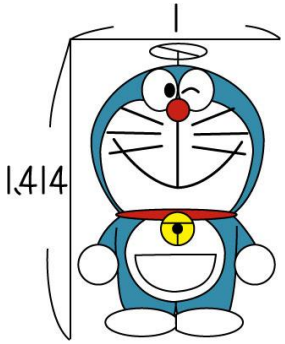
**Silver Ratio : $\frac{\sqrt{2}}{1} = 1.414\ldots$**



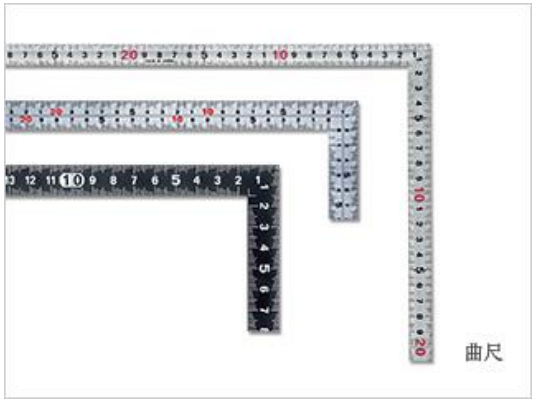
Golden ratio
1 : 0.618



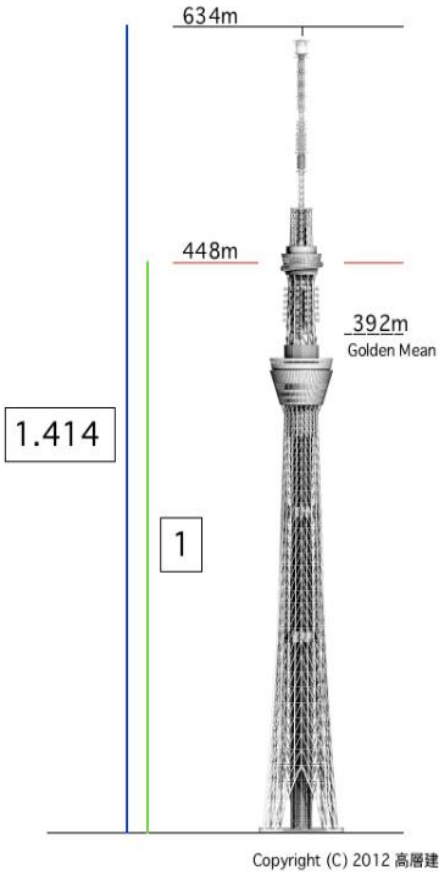
Silver ratio
1 : 1.414




1 : 1.414

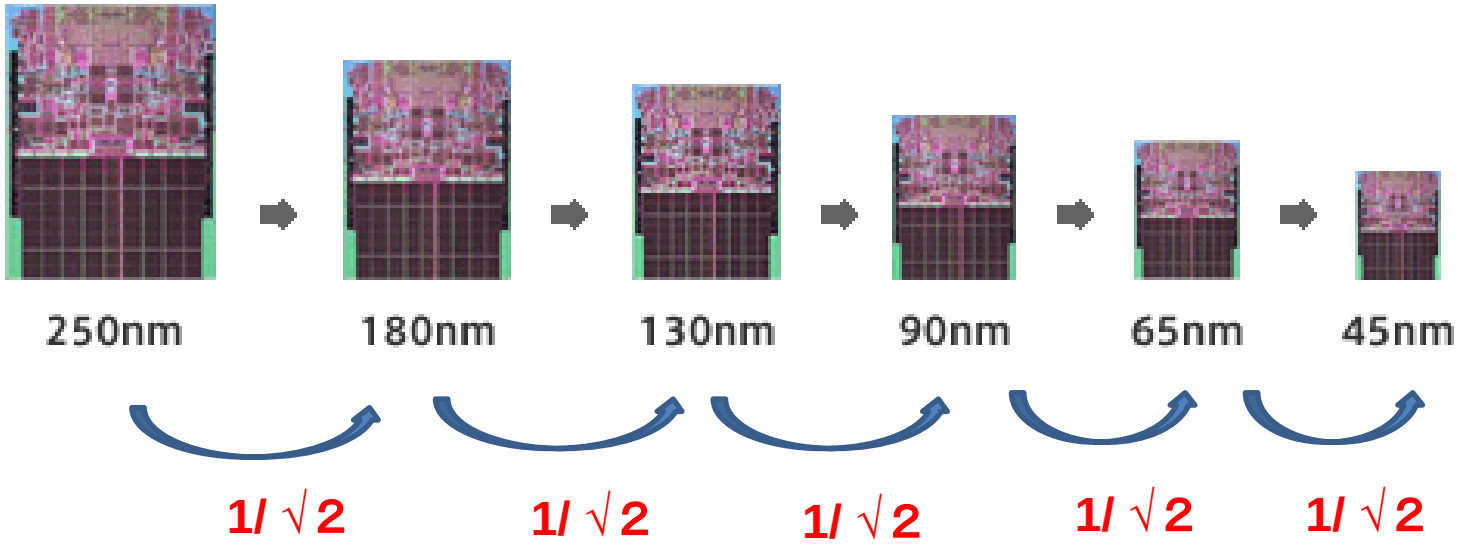






# LSI Scaling vs. Silver Ratio

## LSI Scaling Rule



# Silver Ratio Weight

**N bit M step SAR ADC**

**Weights p(k)**

| | | | |
|---|---|---|---|
| **p(M)** | **=1** | | |
| **p(M-1)** | **=1** | | |
| **p(M-2)** | **=1** | **×1** | $\times\sqrt{2}$ |
| **p(M-3)** | **=2** | **×2** | $\times\sqrt{2}$ |
| **p(M-4)** | **=2** | **×1** | $\times\sqrt{2}$ |
| **p(M-5)** | **=4** | **×2** | $\times\sqrt{2}$ |
| **p(M-6)** | **=4** | **×1** | $\times\sqrt{2}$ |
| **p(M-7)** | **=8** | **×2** | $\times\sqrt{2}$ |
| **p(M-8)** | **=8** | | |
| **p(M-9)** | **=16** | | |
| **p(M-10)** | **=16** | | |

For 2 steps, 2 times ($r^2 = 2$)

**II**

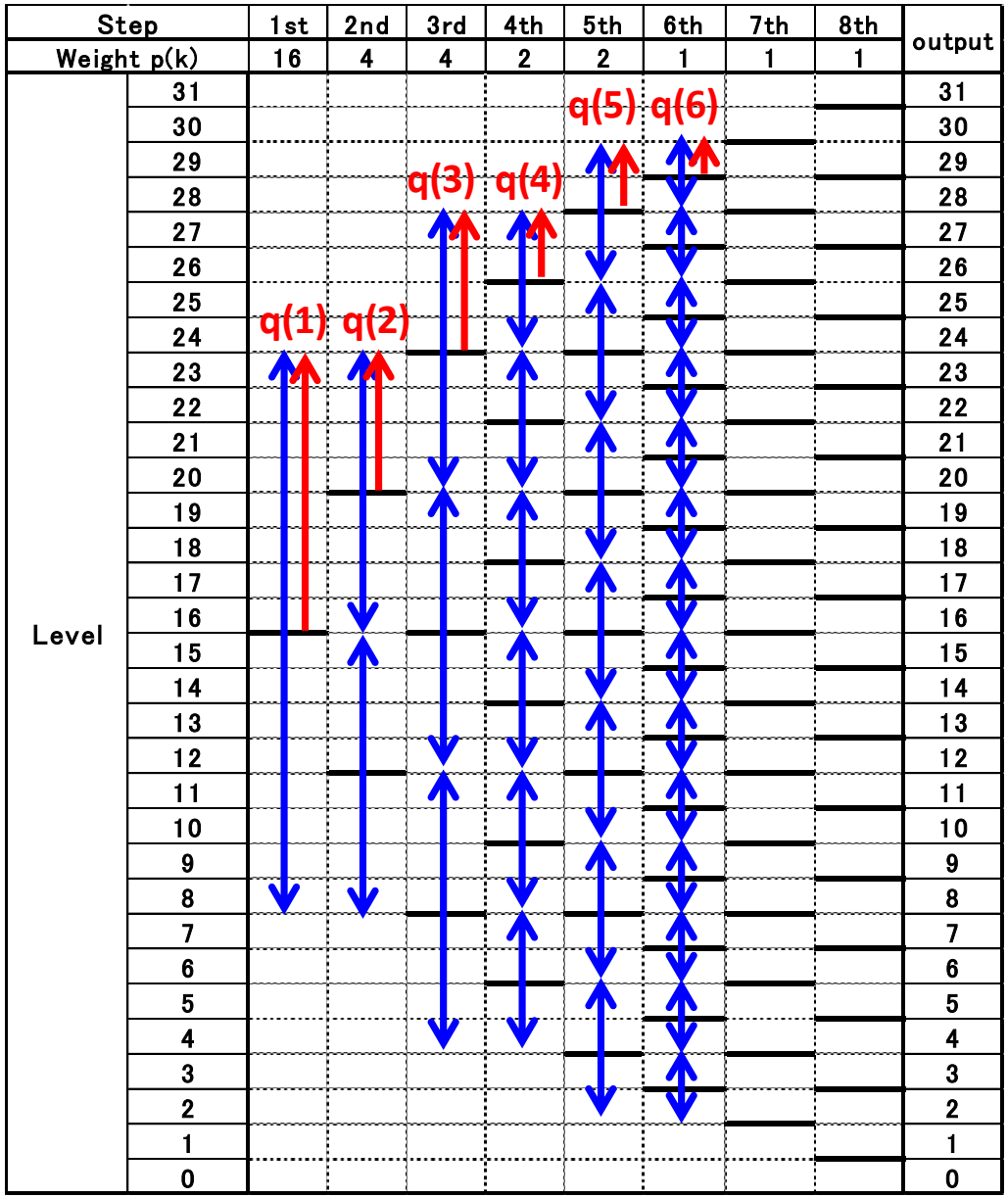
For 1 step, $\sqrt{2}$ times ($r = \sqrt{2}$)

**Peudo radix $\sqrt{2}$ weight**

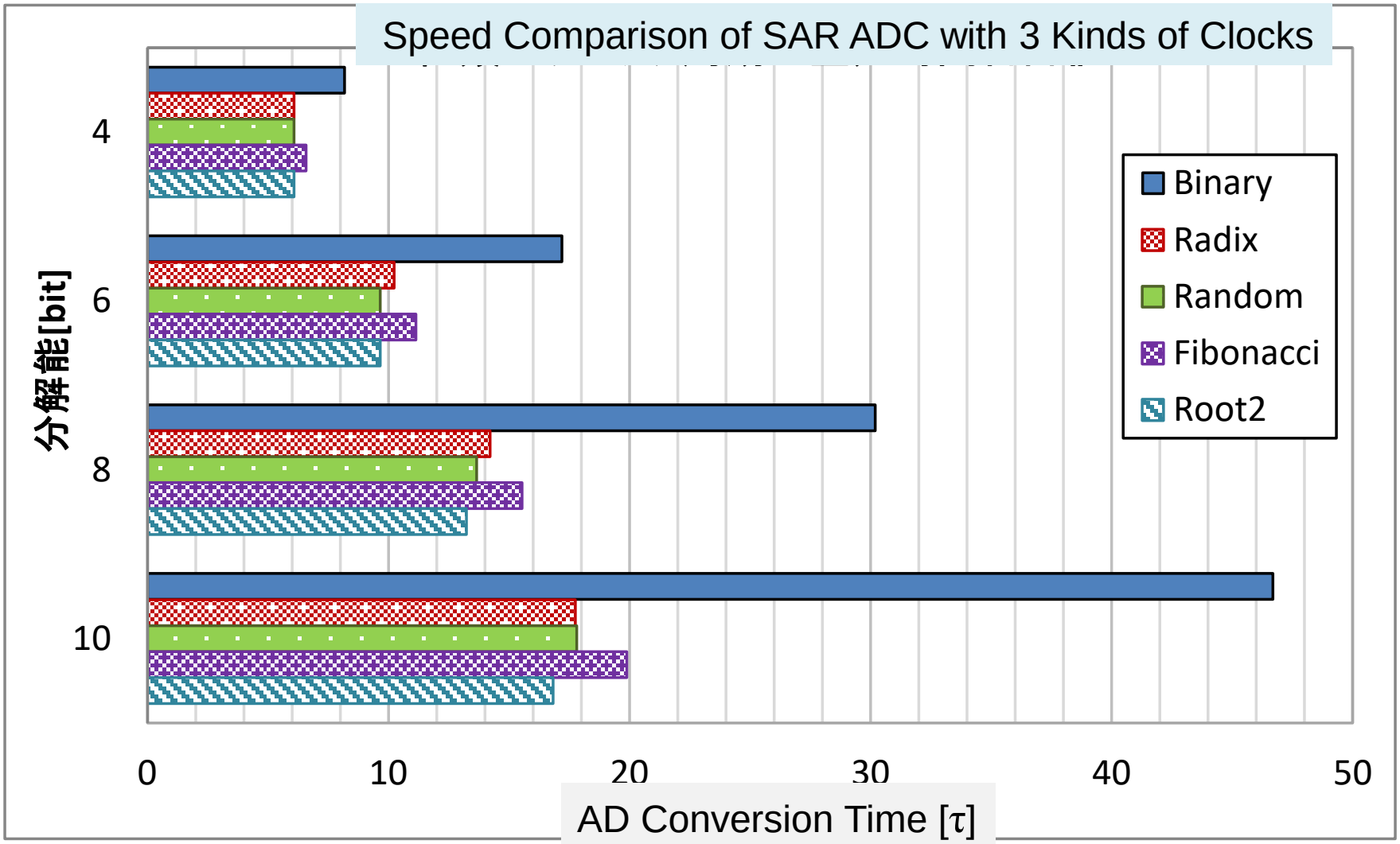
**“Silver ratio”**

# Silver Ratio Weight SAR ADC

## 5bit 8step　SAR ADC



# SAR ADC Speed Comparison




**Silver ratio SAR ADC is the fastest !**

Kobayashi
Laboratory