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Low Power LSI Design

-- Featuring low power ADC design --

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Abstract

- I will discuss low power LSI design featuring low power ADC design.
- Power break through often made new applications and markets, such as watch-like cellular phone, handy digital camera, and on-board DVD in note PC. Current and future big market must be the IoT systems.
- Logic circuit has progressed from fast but power hungry CML to CMOS that doesn't consume any static power and no relation between speed and consumed energy. Small capacitance and low voltage operation are the key.
- ADC plays an important role for all electrical systems, however unlike logic circuits; accuracy, distortion, and noise should be considered. Furthermore, these factors have tough tradeoff against low energy operation and conventionally uses OPamps that need static current.
- CMOS technology that had been regarded as not suitable for ADC application due to large mismatch, however conquered it by using capacitance to realize S/H and to absorb mismatch voltage.
- Recent advanced ADC uses dynamic CMOS circuit and more aggressively replaces conventional amplifier.

Contents

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- Low power digital LSI design
- Progress of video-rate ADC
  - History of video-rate ADC
- Advanced ADC design
  - Mismatch limited ADC: Flash ADC
  - Thermal noise limited ADC
    SAR ADC and SAR+Delta-Sigma ADC

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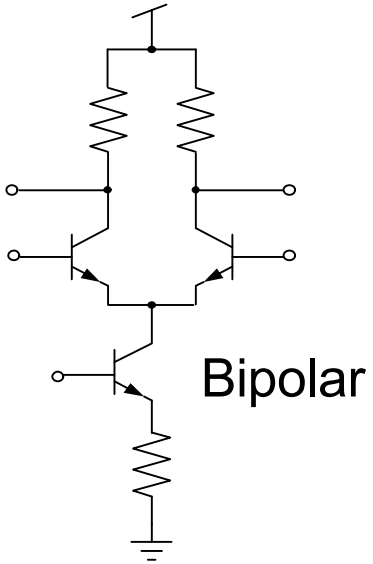
Low power digital LSI design

Progress of logic circuit and devices

Logic circuit and device have been progressed to no static current for low power consumption

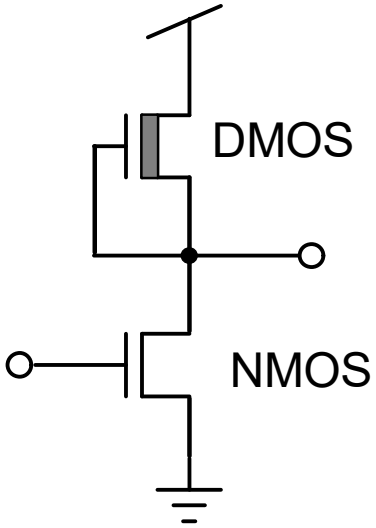
CML



Static current

Main frame
1960-1990

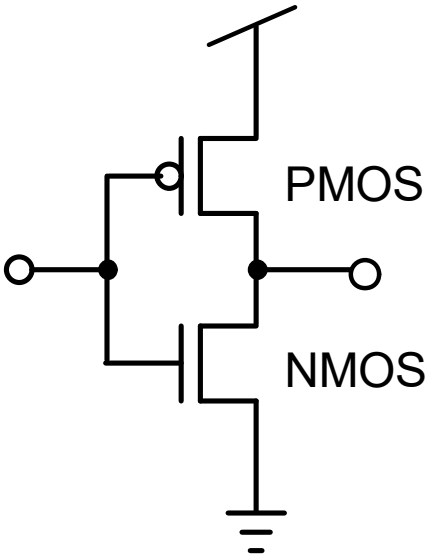
E/D NMOS



Static current

PC
1970-1985

CMOS



No static current

Watch, Calculator,
PC, Every thing
1970-Present

Feature of CMOS logic circuit

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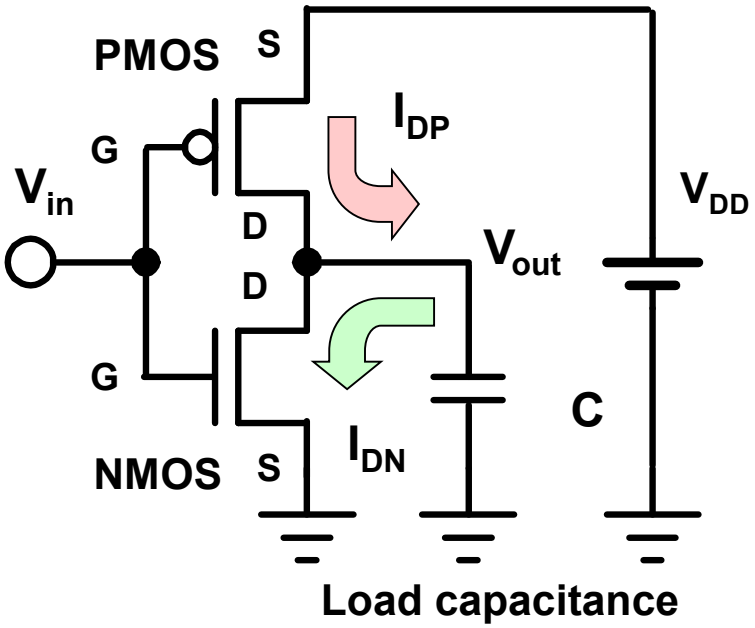
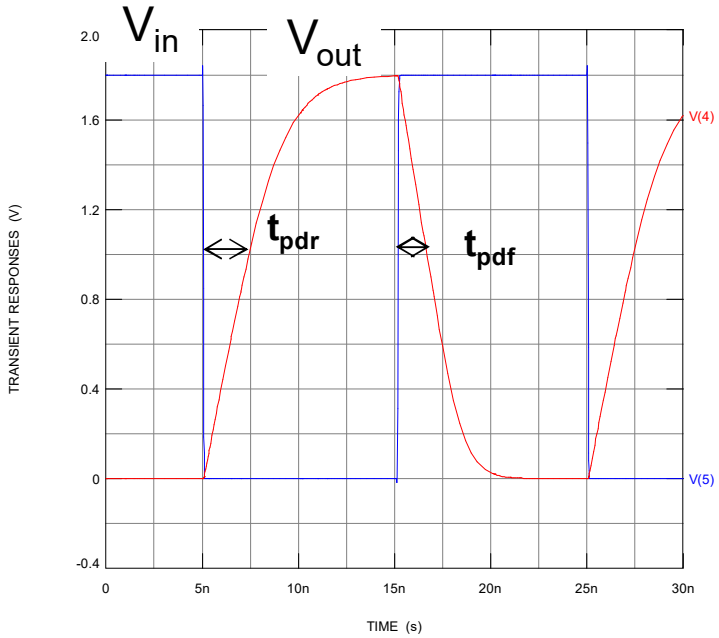
Large dynamic current is needed to reduce logic delay.
However lost energy is not determined by the current, but electrical energy.
This means CMOS can realize high speed and low energy circuit.

No static current can realize low power circuit, basically.





Delay time

$$t_{pdr} = \frac{CV_{DD}}{2I_{DP}}, t_{pdf} = \frac{CV_{DD}}{2I_{DN}}$$

Consumed energy

$$E_d = CV_{DD}^2$$

$$P_d = fCV_{DD}^2$$

Low power digital LSI design

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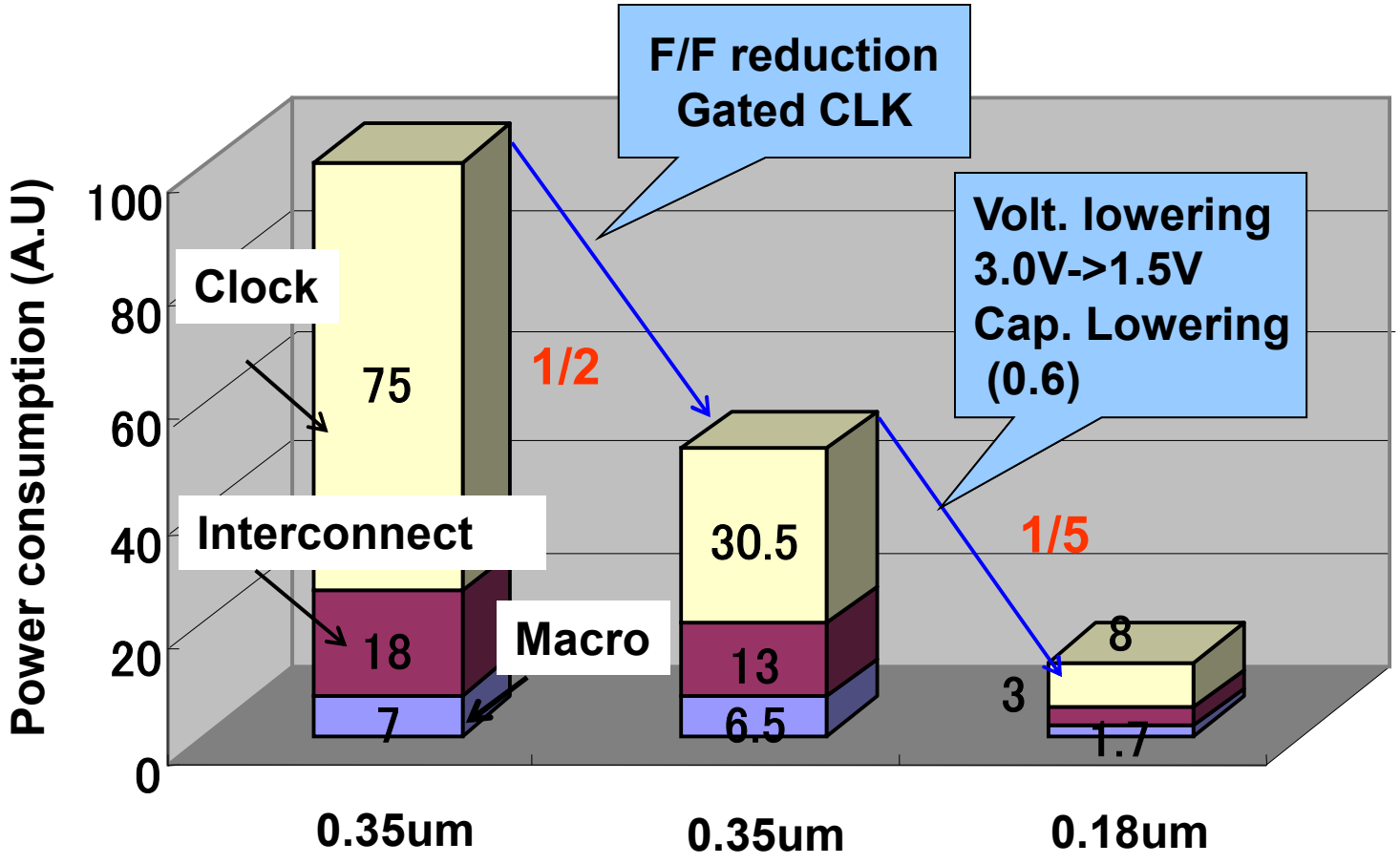
Power dissipation can be reduced to 1/10

Clock circuit (Flip Flop) consumes power of 75% of total P_d in this LSI.



Reconsider Flip Flop circuits

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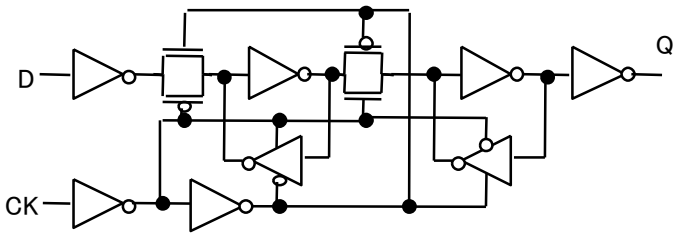
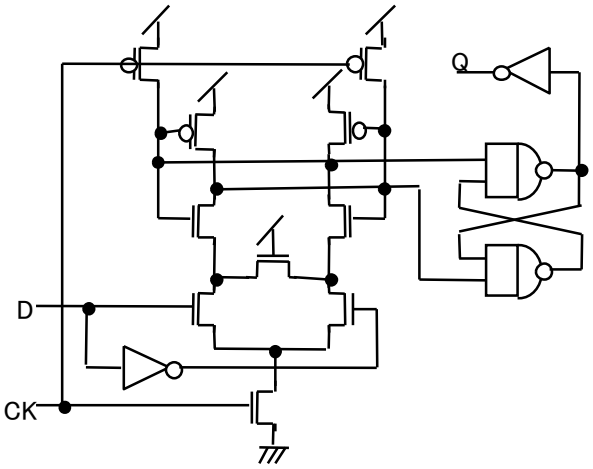
We can reduce power consumption by reconsidering F/F circuit.

P_d of 1/2 or 1/3 is possible

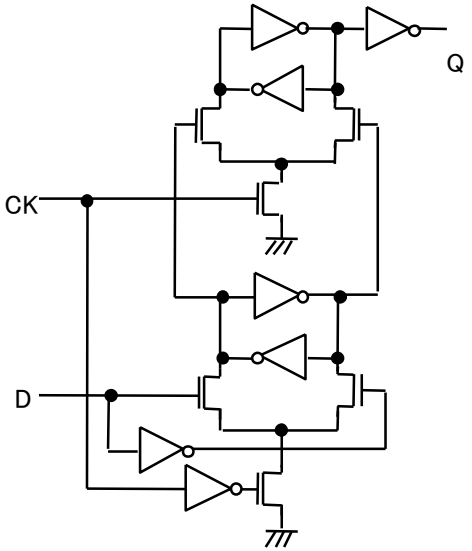
By reducing gate capacitance to the clock



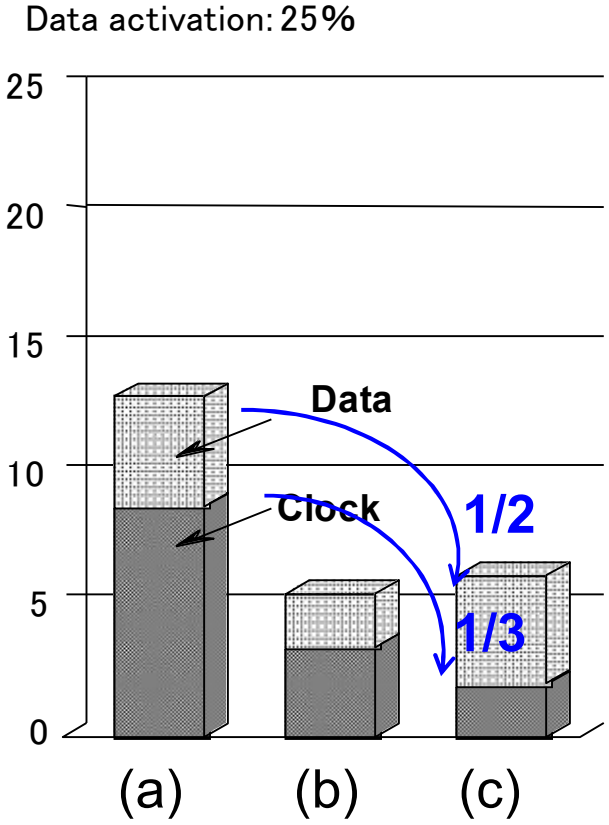
(a) Conventional type



(b) Differential type



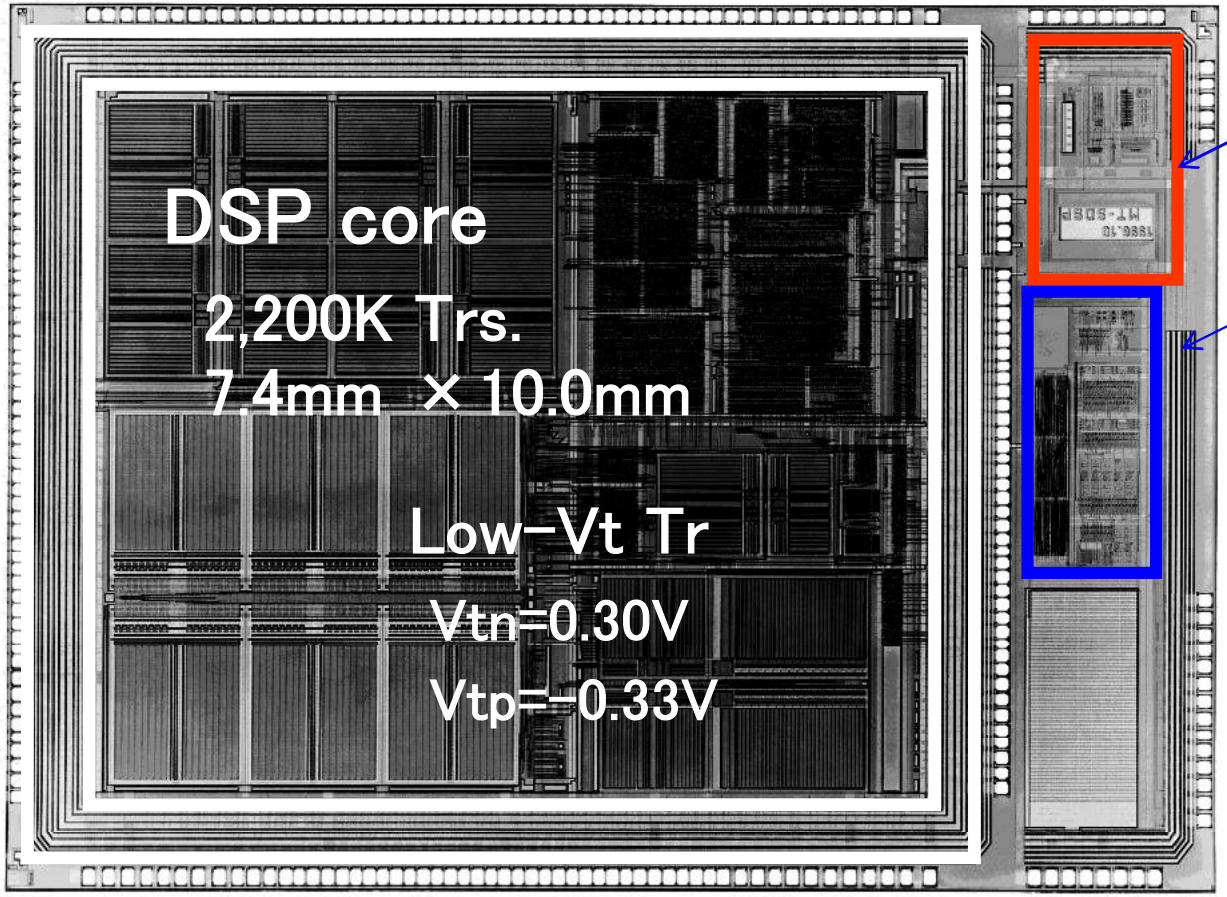
(c) Memory type



DSP with adaptive supply voltage control

We developed low power DSP using adaptive supply voltage control technique that was early work of DVFS technique

S. Sakiyama and A. Matsuzawa, Symp. on VLSI Circuits 1997



Adaptive supply voltage control circuits

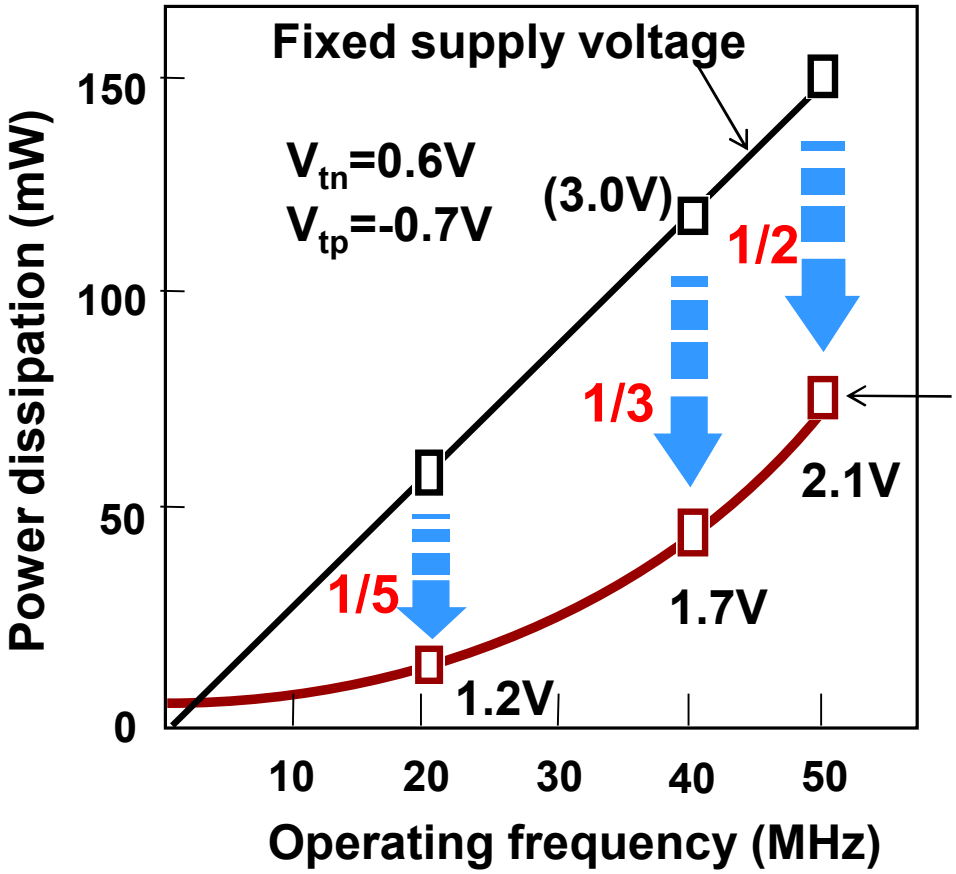
On chip DC/DC

0.35umCMOS
2.2M Tr
20MIPS
12mW (1.2V, internal)

leakage current
500uA: active
1uA: standby

Adaptive supply voltage

Supply voltage can be reduced with the reduction of clock freq.
This makes more aggressive power reduction.



$$E_d = CV_{DD}^2$$

$$P_d = fCV_{DD}^2$$

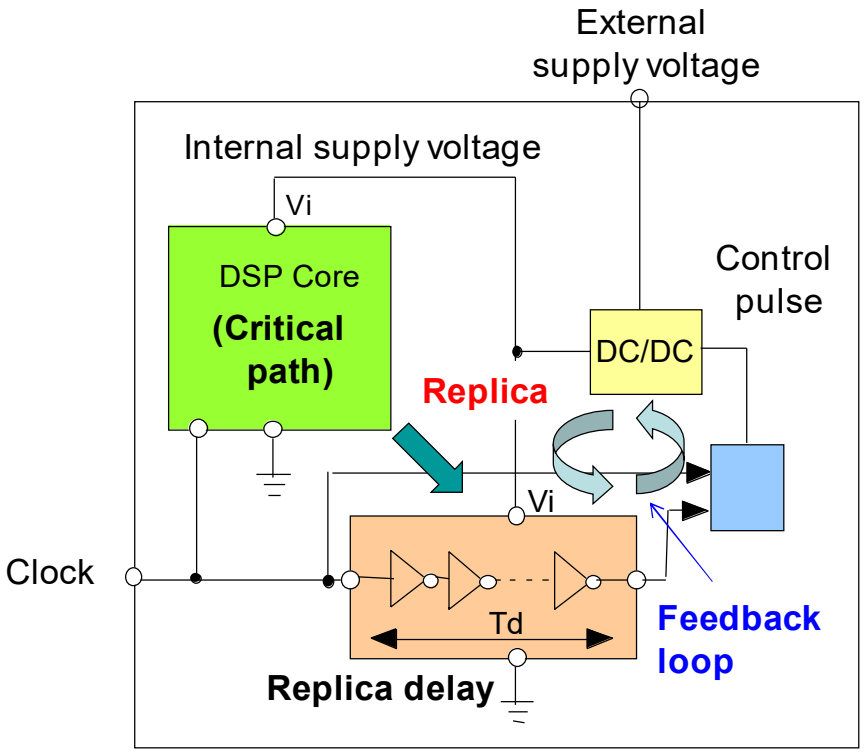
Adaptive supply voltage +Low VT transistors

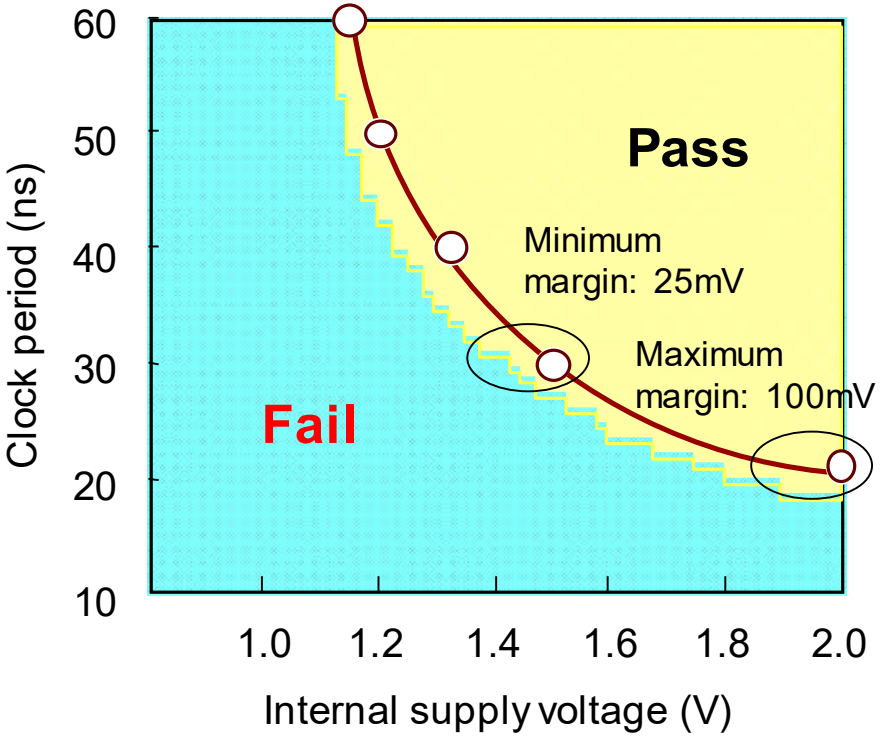
(1.0V-- 2.2V)

V_{tn}=0.30V
V_{tp}=-0.33V

Find minimum operating voltage

Feedback loop can find minimum operating voltage by using replica delay that satisfies required T_{pd} for critical path in the DSP.



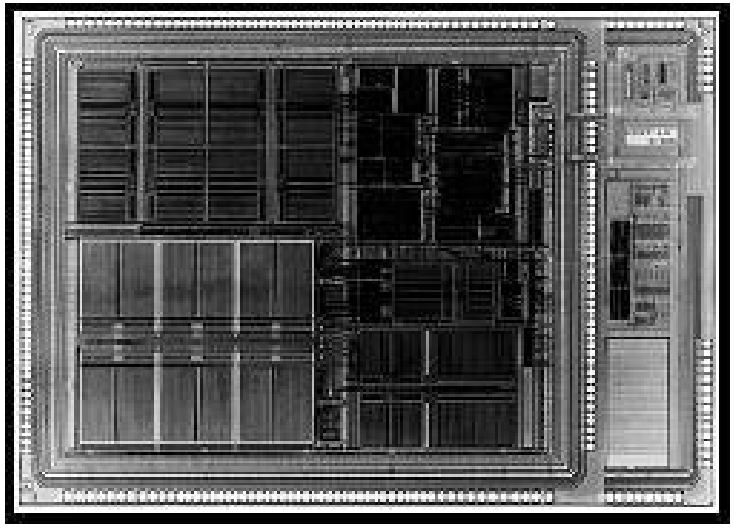


World's first watch-like cellular phone

We developed the world's first watch-like cellular phone using developed low power DSP

This cellular phone was used in Nagano winter Olympic game (1998)

12mW @20MHz 0.35um DSP



World's first watch-like cellular phone

Wireless PDA with ambient energy

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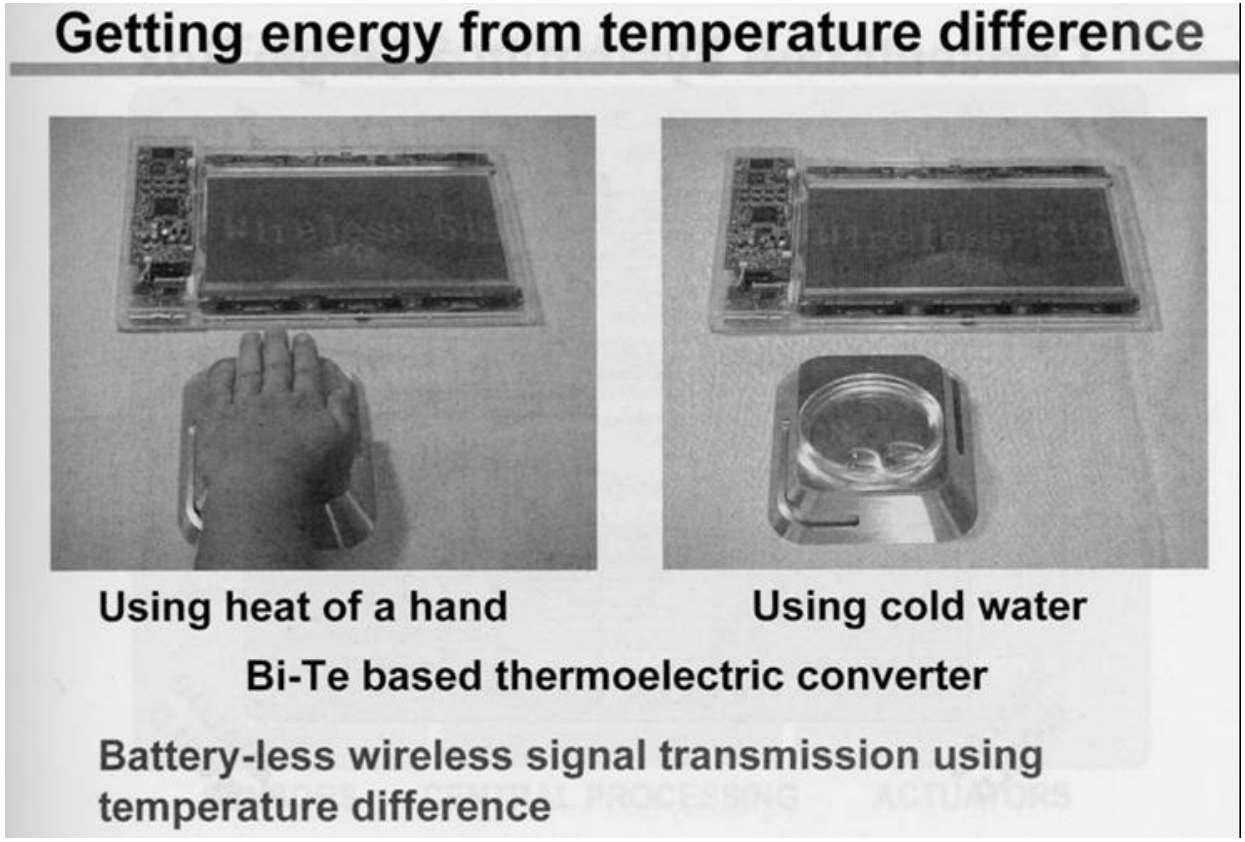
We developed wireless PDA using FD-SOI that can operate with ambient energy. This is an early work for IoT.

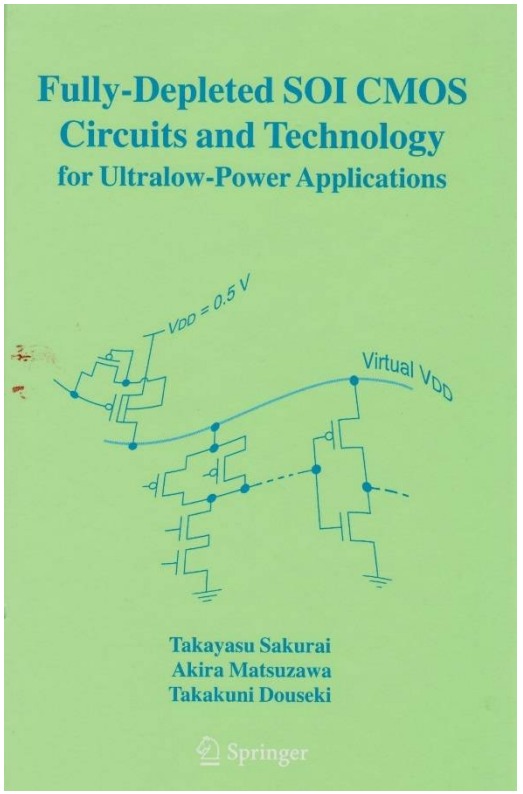


Douseki, A. Matsuzawa, ISSCC2003,

Generate1.7mW/ 0.7V

A. Matsuzawa

Technology is described in this book



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Progress of video-rate ADC

History of video-rate ADC

Progress of video-rate ADC

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- **Module**
  - NO precision monolithic IC technology
- Flash: **Bipolar** technology
  - Only bipolar has low mismatch voltage
  - CMOS has large mismatch voltage
- Two-step flash: **Bi-CMOS** technology
  - Two-step flash can reduce power, but needs S/H
  - CMOS S/H + Bipolar comparator
- Two-step flash: **CMOS** technology
  - Chopper inverter comparator can realize high precision comparator and also S/H circuit
  - Capacitive interpolation method reduce error and power more
- Gate-weighted interpolated flash: **CMOS** technology
  - Gate-weighted linear region MOS + dynamic flip/flop (No static current)

Development start for digital TV&VTR

In 1979, Panasonic (松下電器）succeeded in development of 6 hour VHS and became world's No.1 VTR supplier.
The video equipment used high level analog technology.
The development project for digital TV& VTR has started.

With my friends in 1979, Central research Lab. In Panasonic

Panasonic VHS Video NV-6000, 1979

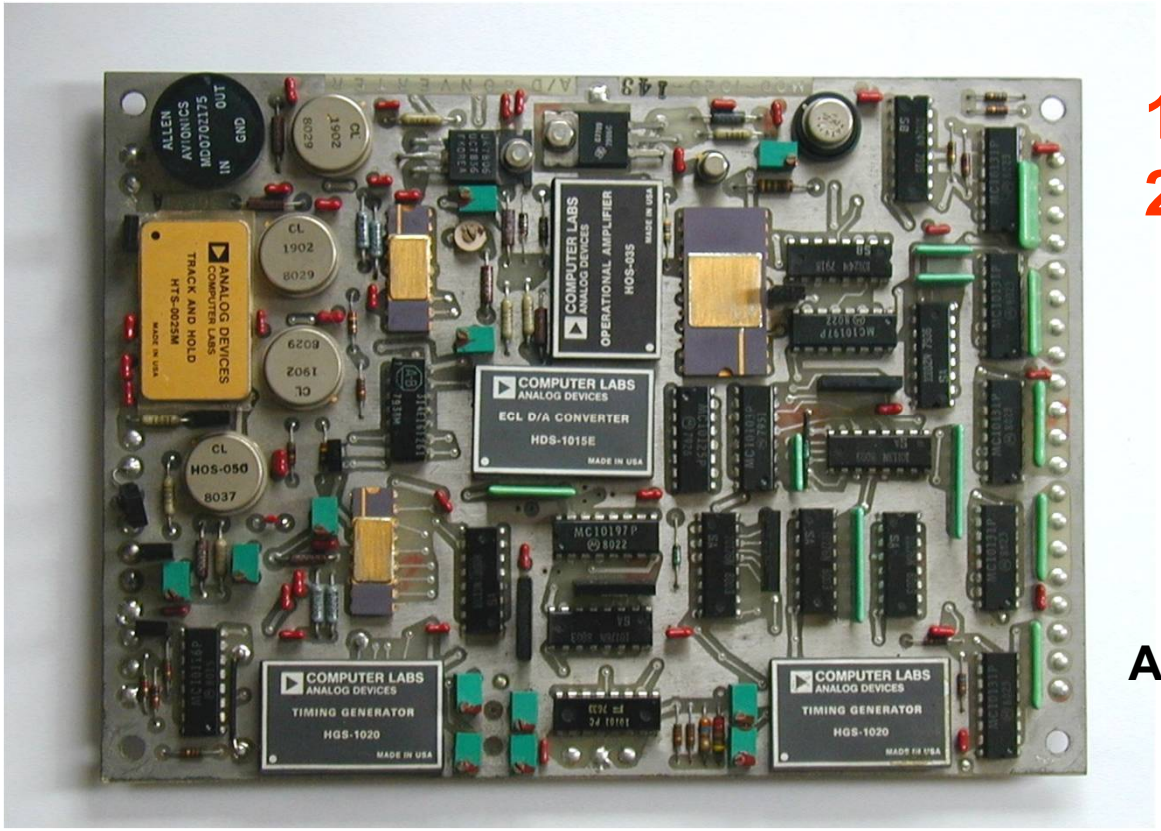
Video-rate ADC at 40 year before

Video-rate ADC was very expensive and power hungry module when I started development of video-rate ADC IC in 1980.

There was no monolithic video-rate 10b ADC at that time

10bit 14.3MHz ADC

Almost same price as a small car!



10,000 USD
20W

Analog Devices Inc.

The world's first video-rate 10bit ADC

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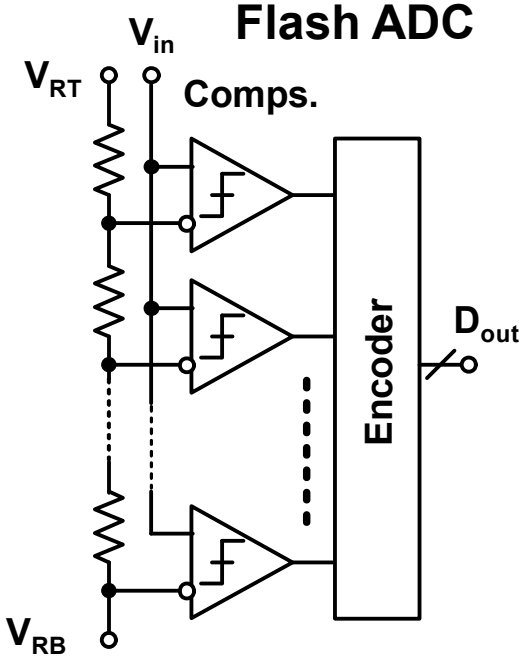
We developed the world's first video-rate 10bit ADC IC using bipolar technology

Price and lower dissipation are reduced by **1/10**

The ADC was used in professional digital TV and video systems

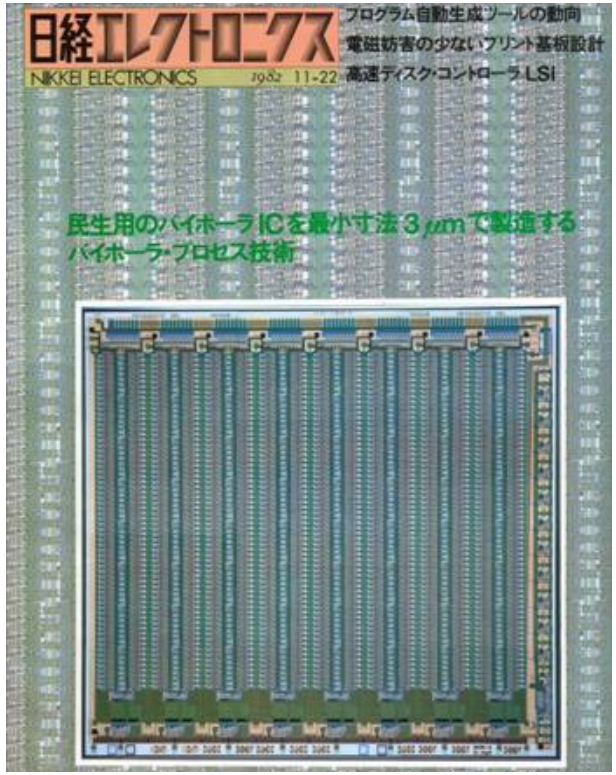
T. Takemoto and A. Matsuzawa,
JSC, pp.1133-1138, 1982.

Flash ADC



Bipolar (3um)
10b, 20MS/s,
2W
$ 800

IR100 Award



Why Bipolar, not CMOS?

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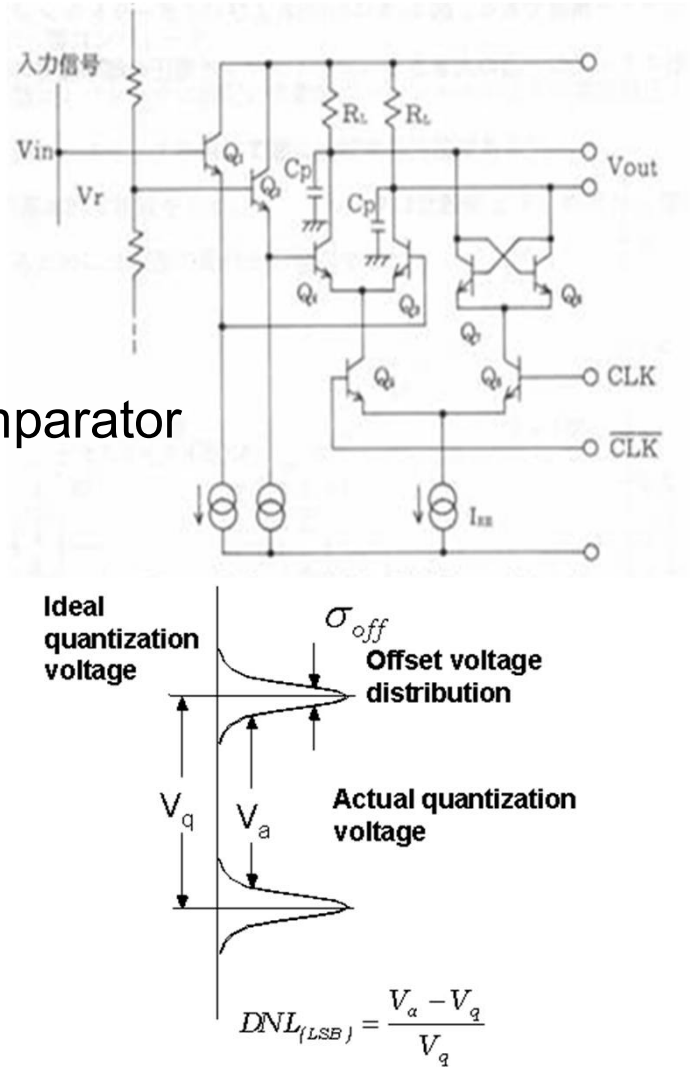
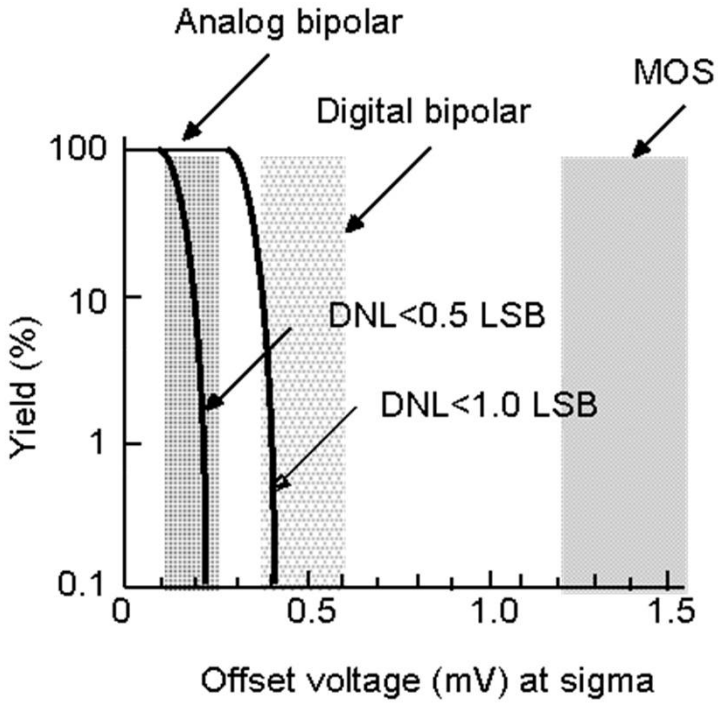
Only bipolar can satisfy the target of mismatch voltage.

Comparator



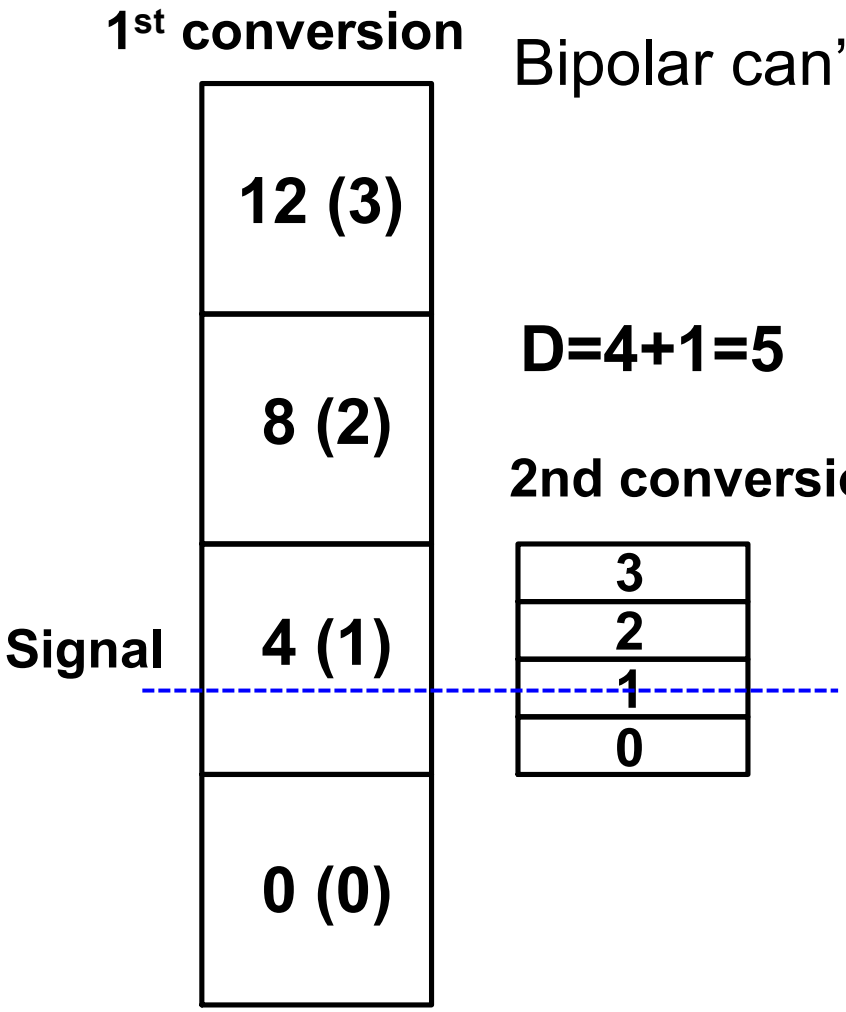
Mismatch voltage should be L.T. 0.2mV

MOS: several mV to several 10mV



Two step flash ADC

Can be reduced by **1/16, but needs S&H**



Bipolar can't realize S&H, due to base current

D=4+1=5

Circuit size

$$n = 2^{M} + 2^{N-M} \rightarrow 2^{\left(1+\frac{N}{2}\right)} @ M = \frac{N}{2}$$

10bit Flash ADC: 2^{10}=1024

10bit two step ADC: 2^{6}=64

Bi-CMOS two step ADC

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Bi-CMOS technology can realize MOS input OPamp for sample and hold to realize two step flash ADC.

10b, 30MSps, 800mW

Bi-CMOS S&H

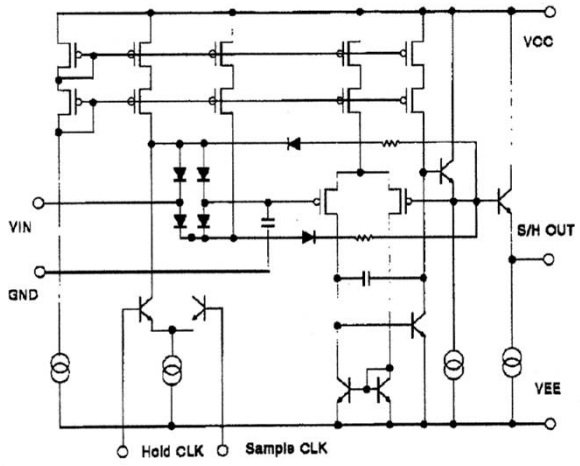
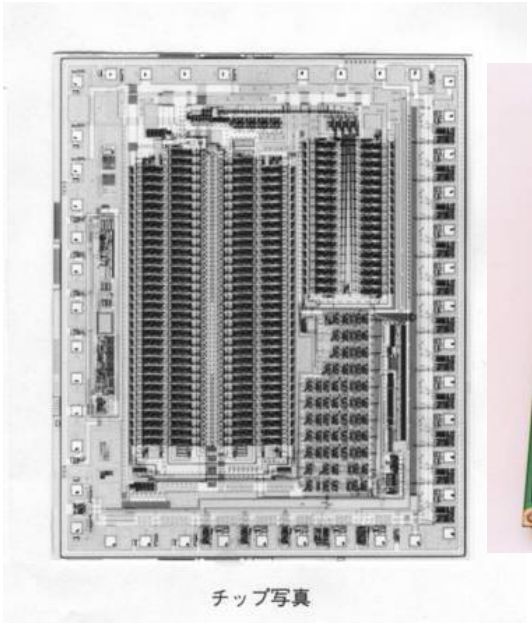


FIGURE 4—BiCMOS S/H circuit.

A. Matsuzawa, ISSCC 1990.



チップ写真

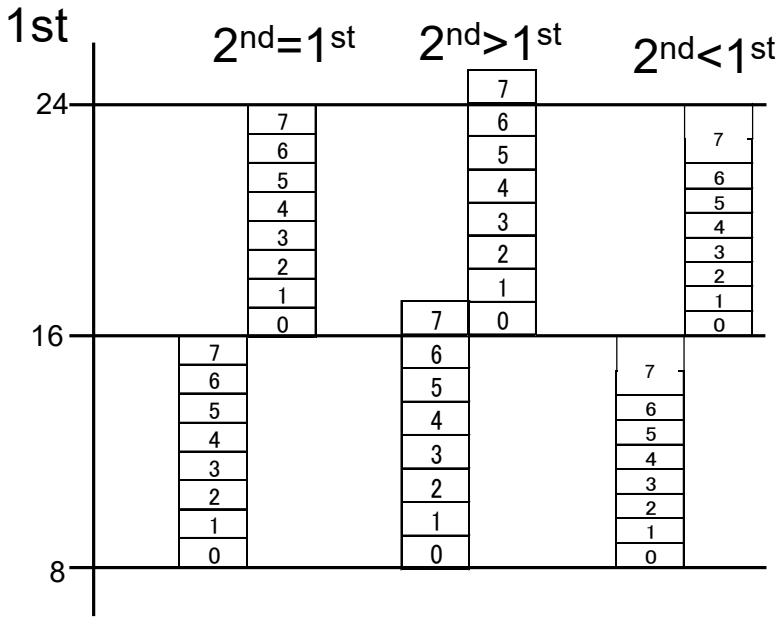
World first's home HDTV

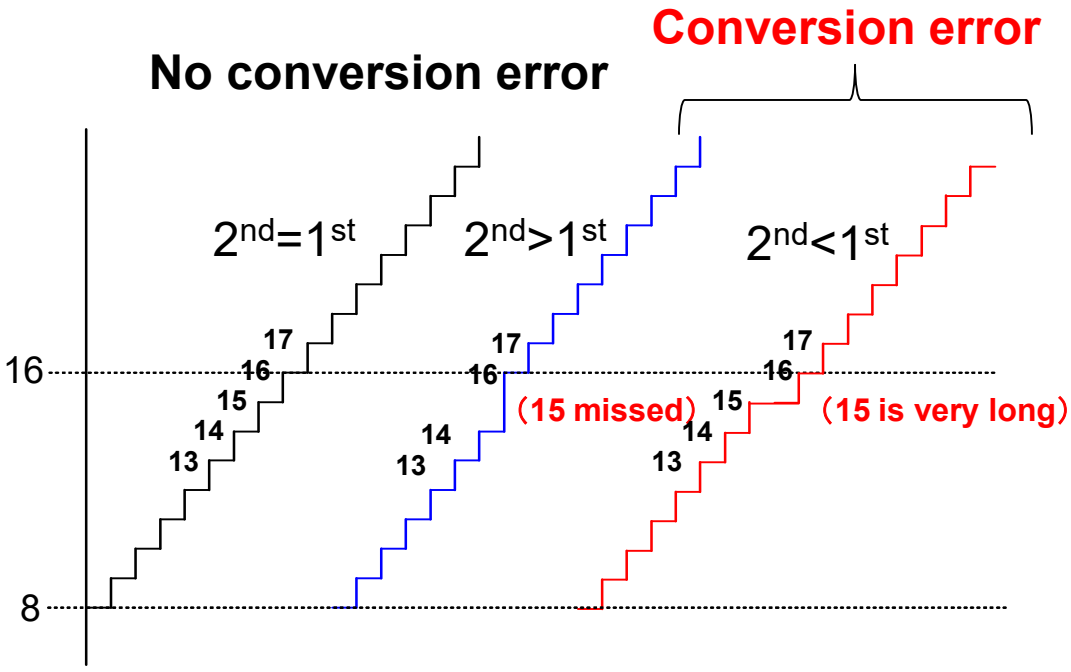
Original AD conversion technique: Interpolation

Multi-step conversion can reduce circuit size and power consumption
However, apt to cause large conversion error, due to stringent matching between the coarse conversion and fine conversion.

1st: Coarse conversion
2nd: Fine conversion

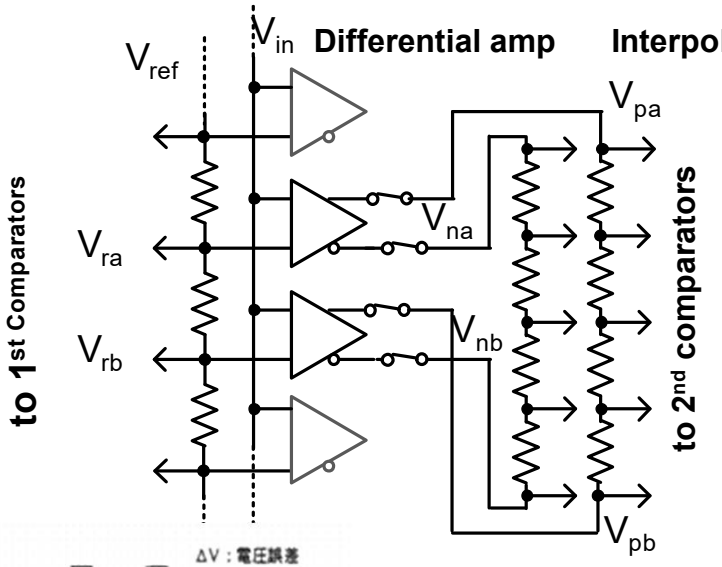
Fixed scale causes conversion error

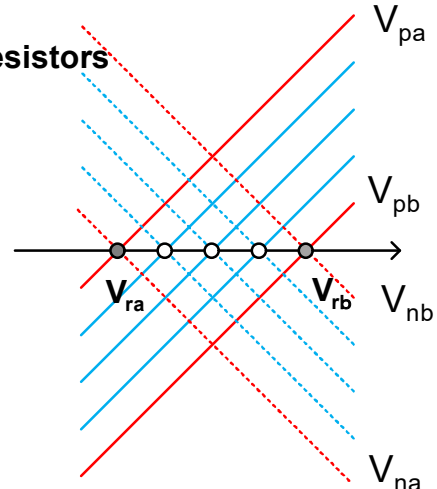




Interpolation

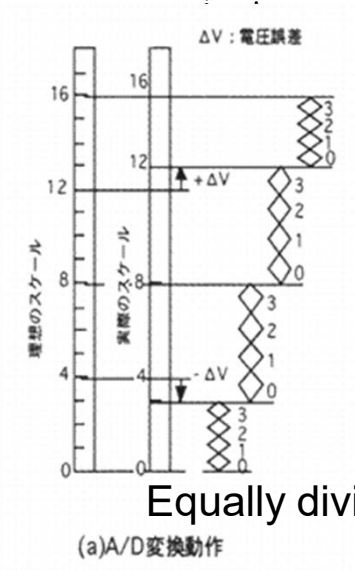
Interpolation can realize smooth connection between 1st and 2nd conversion area, as a result, small DNL can be achieved.



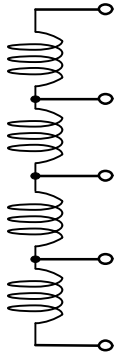


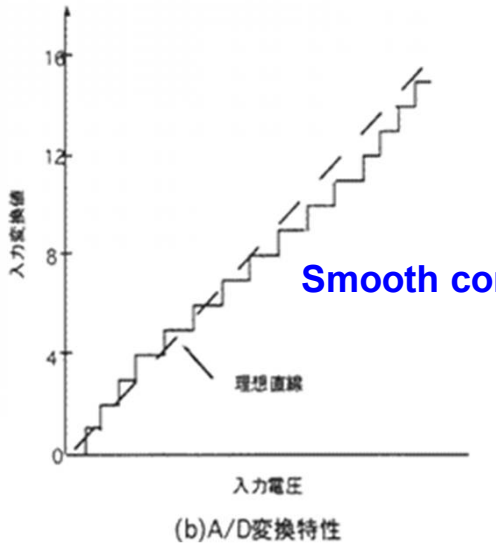
1994 Remarkable invention award

Output voltages are divided equally by resistors



As if spring coil





Smooth connection

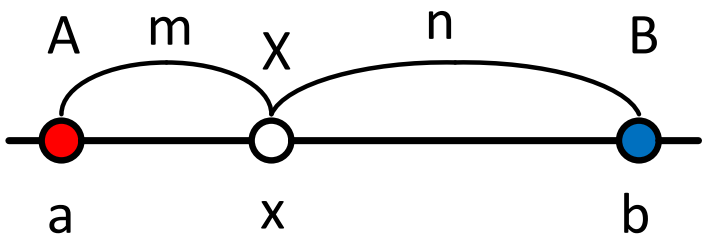
Equally divide of 1st conversion area

A. Matsuzawa

Mathematical expression of interpolation

Addition of weighted two signal makes internal division point.
Using this method, we can realize A/D conversion without reference voltage

Internal division



$$x = \frac{na + mb}{m + n}$$

Weight of $\frac{n}{m+n}$ for signal a weight of $\frac{m}{m+n}$ for signal b

And sum them

Our proposed interpolation techniques

- **Resistive interpolation: using resistors**
- **Capacitive interpolation : using capacitors**
- **Gate weighed interpolation: conductance of linear region**
- **Time interpolation : using delay elements**

CMOS comparator

CMOS comparator (33 year ago) had not good performance to the bipolar comparator. Mismatch was 20 times larger and consumed large power. Conventionally larger size is needed to reduce the mismatch.

Yukawa, et al., JSC, 1986.

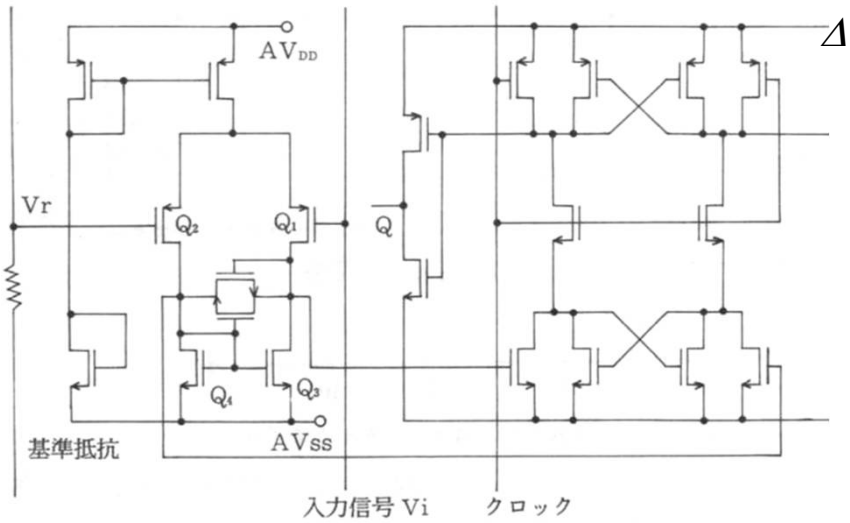
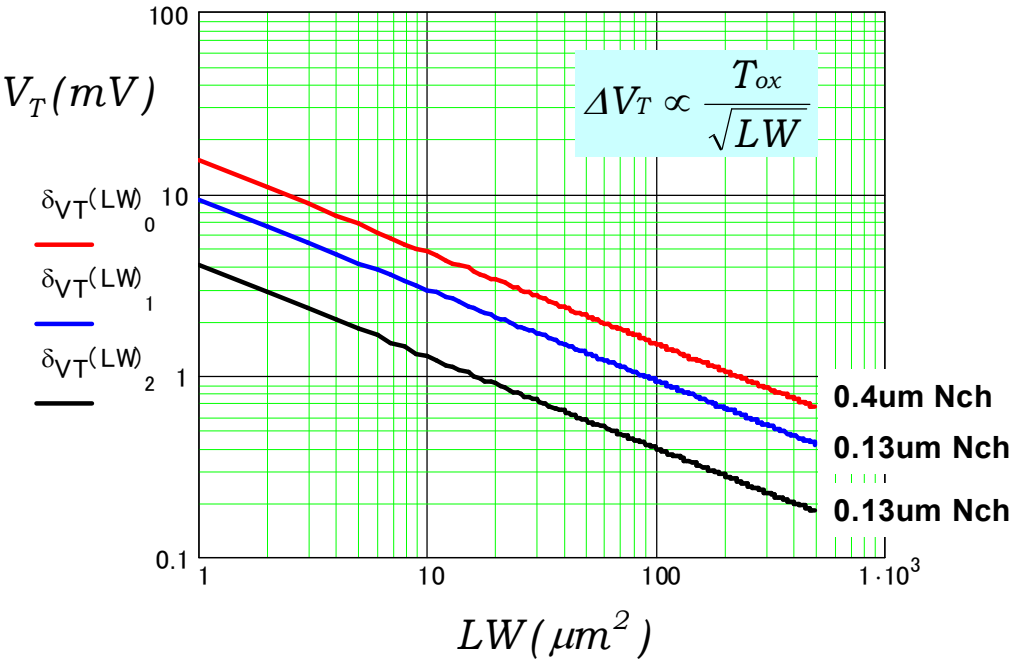


図5-5（b） MOS差動型コンパレータ

Gate area vs. mismatch



Chopper CMOS comparator

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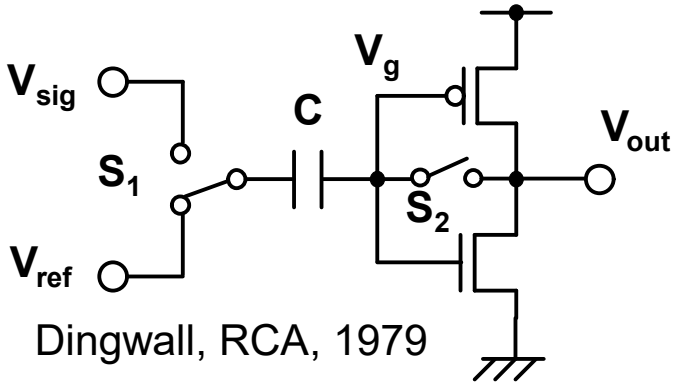
Invention of CMOS chopper inverter comparator realized high resolution and low power CMOS ADC.



Dingwall, RCA, 1979

Capacitor

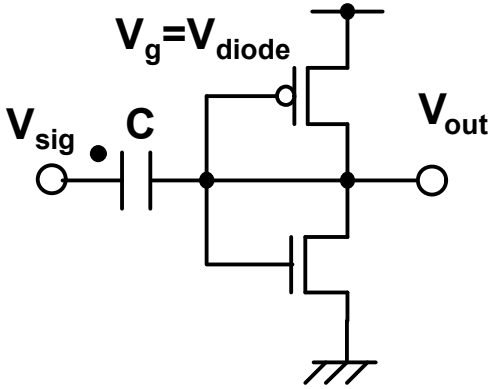
1) absorbs mismatch voltage
2) Sample & Hold
3) Auto level shift

Inverter

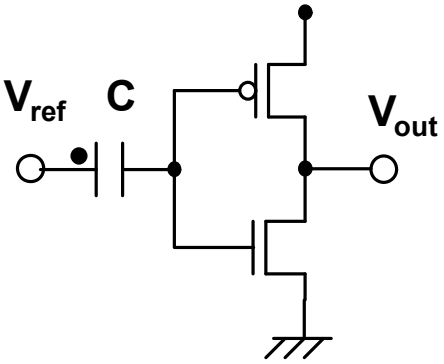
1) Amplifier
2) Self bias
3) Simple and low voltage

Chopper inverter comparator

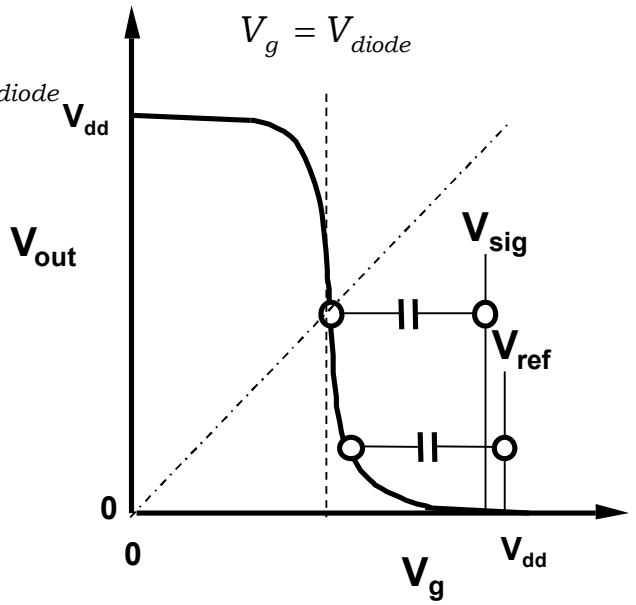
$$V_{out} = G\left(V_{sig} - V_{ref}\right) + V_{diode}$$



Signal tracking



Sample and amplify



Ultra low power Video-rate 10b CMOS ADC

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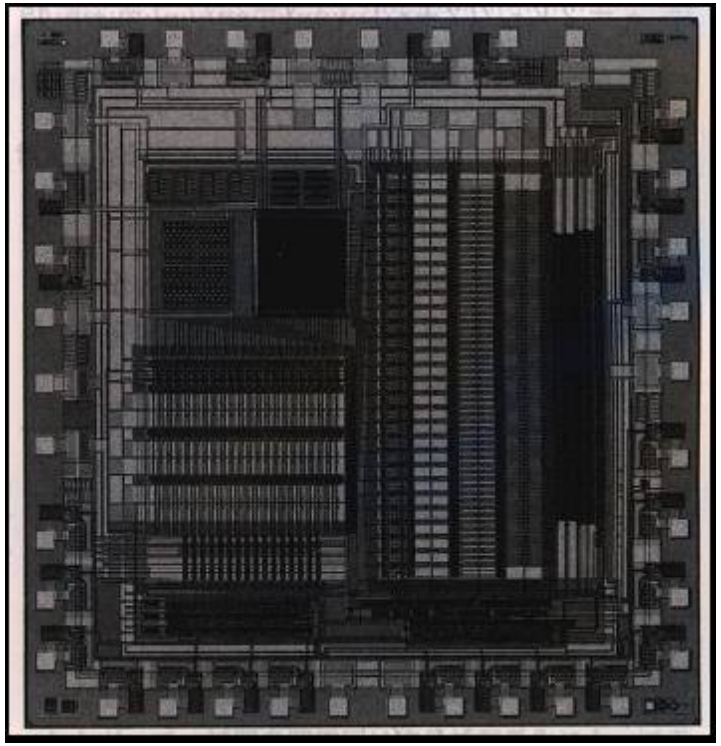
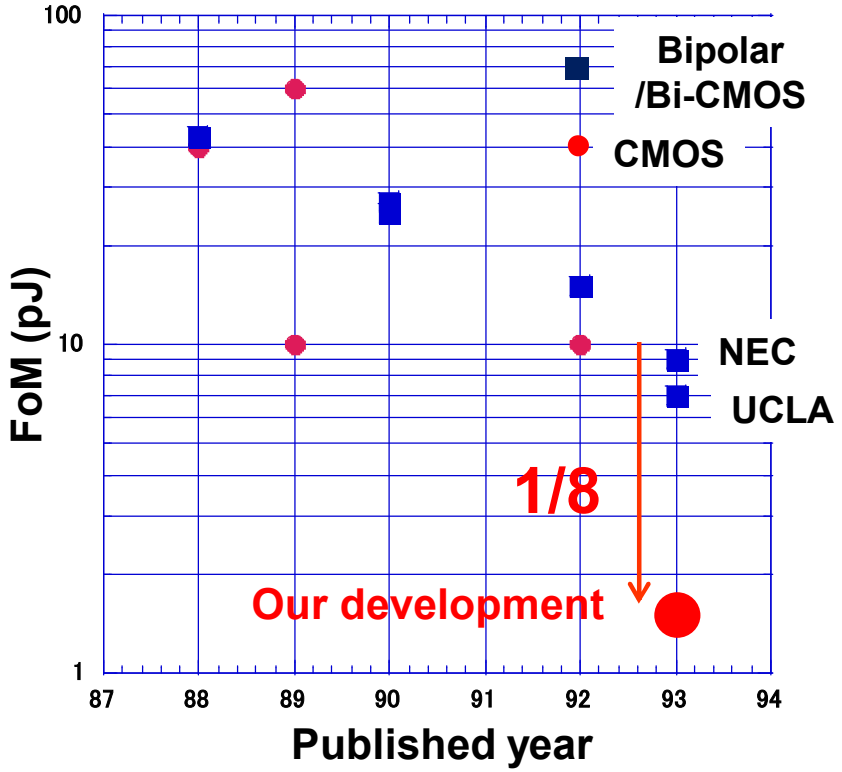
The ADC demonstrated superiority of CMOS technology in ADC.
Since then, all ADCs use CMOS technology and no use of bipolar.
Consumed energy is **1/8** to other ADCs.
FoM of ADC was invented to show the significance of this development.

K. Kusumoto and A. Matsuzawa
ISSCC '93, JSC 1993.



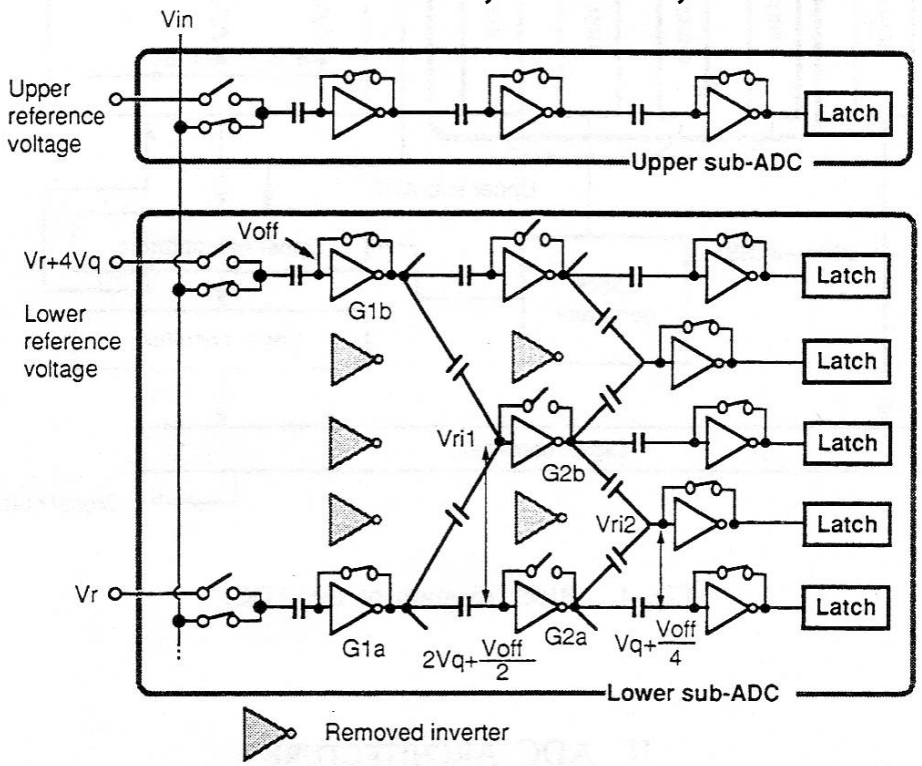
CMOS 10b, 20MS/s, **30mW**



Capacitive interpolation

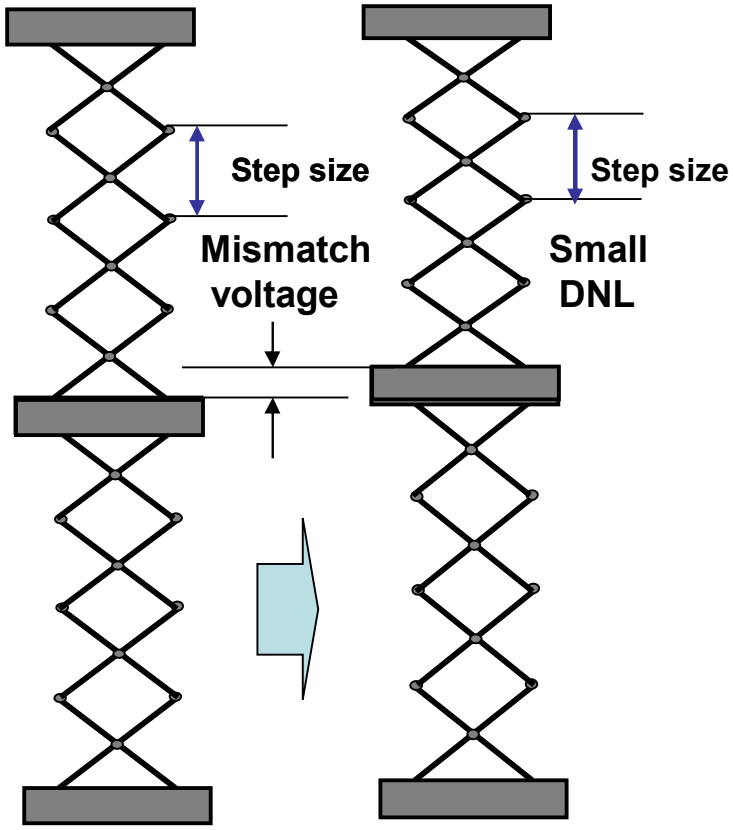
Chopper comparator had a accuracy limitation of **8bit**.
We invented capacitive interpolation and realized ultra low power CMOS video-rate **10bit** ADC

CMOS 10b, 20MS/s, 30mW



K. Kusumoto and A. Matsuzawa
JSC, pp. 1200-1206, 1993.

Absorb mismatch by interpolation



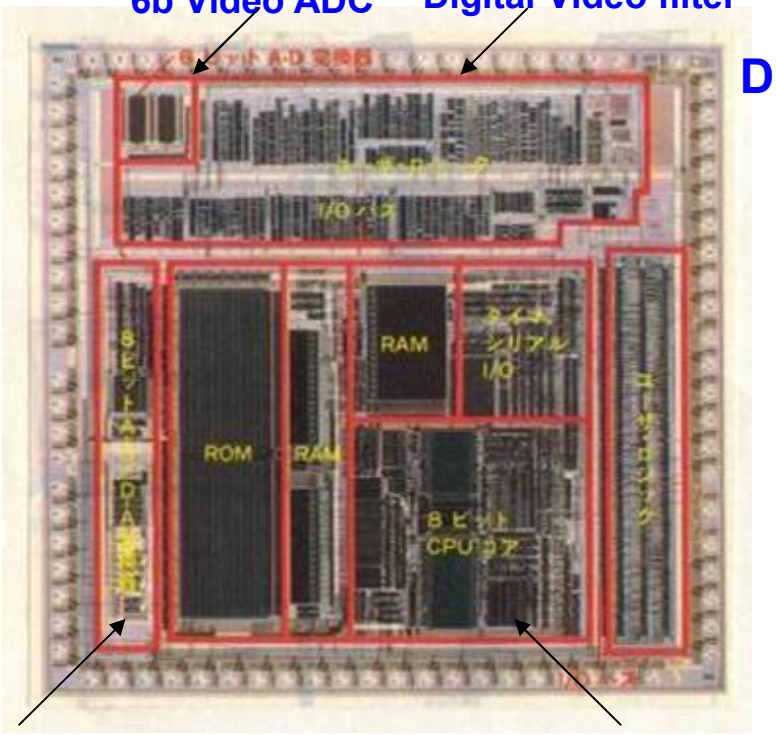
Early stage mixed signal LSI

TOKYO TECH Pursuing Excellence

Success of CMOS video-rate ADC triggered the development of mixed signal LSI for portable AV equipment; Handy digital video.

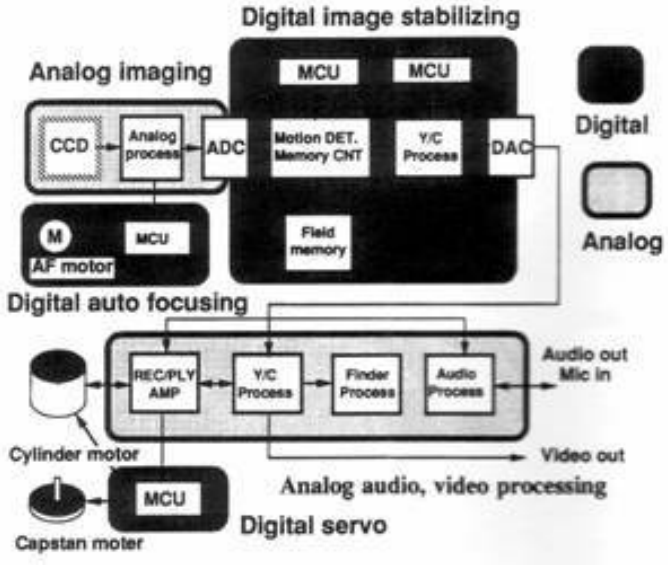
This paper triggered the low power electronics

A. Matsuzawa, "Low-Voltage and Low-Power Circuit Design for mixed Analog/Digital Systems in Portable Equipment," IEEE Journal of Solid-State Circuits, Vol.29, No.4, pp.470-480, 1994.



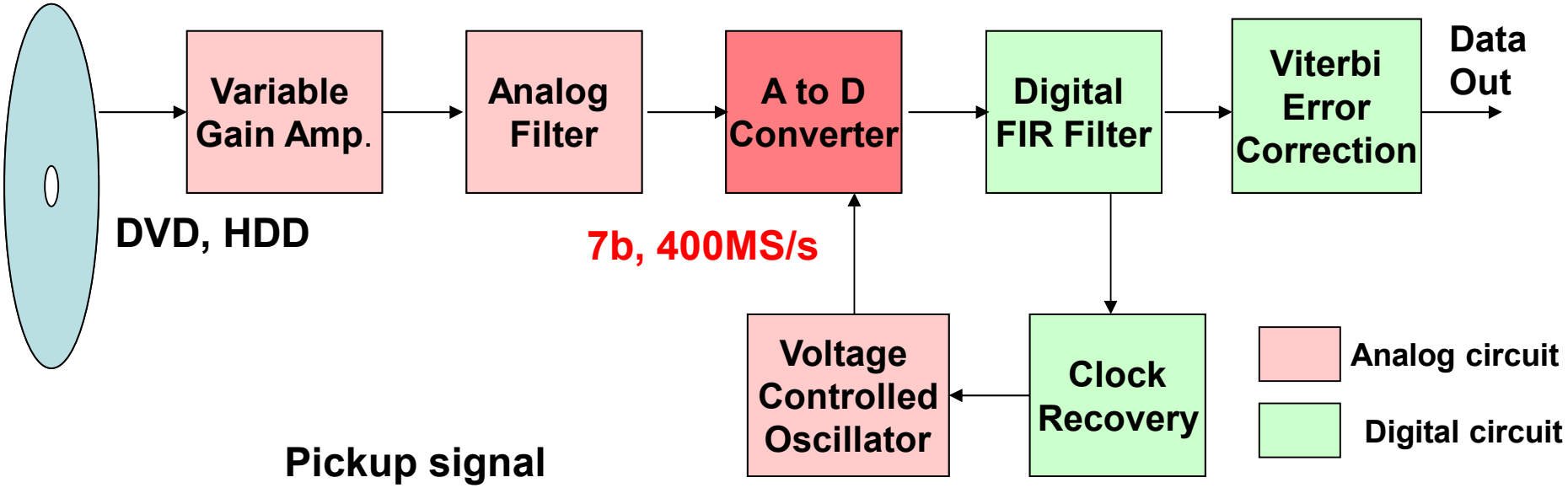
Digital image stabilizer

System block diagram

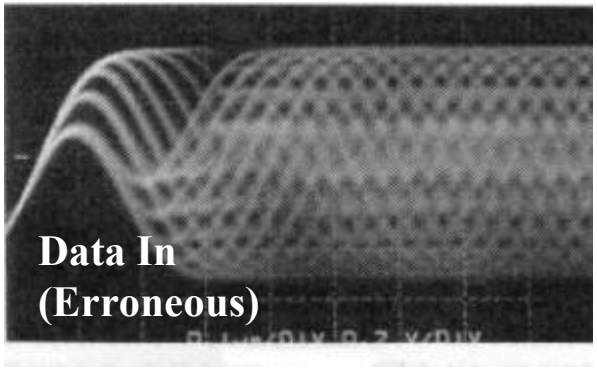


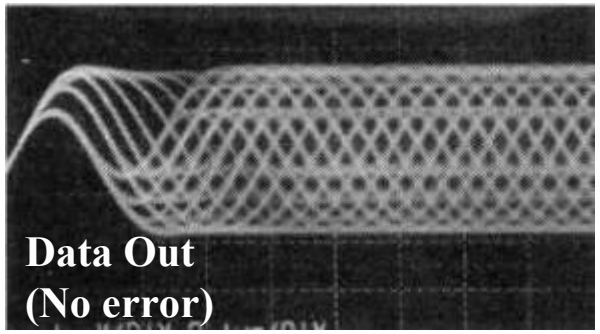
High speed digital signal processing for DVD

Error rate in DVD recorder is quite high due to low SNR
High speed DSP is needed for waveform equalizer and error correction
This means an ultra-high speed (400MS/s) ADC is required.



Pickup signal

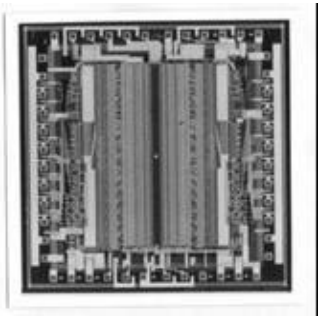




Development of high speed CMOS ADC

TOKYO TECH Pursuing Excellence

Huge power reduction is needed to realize consumer products



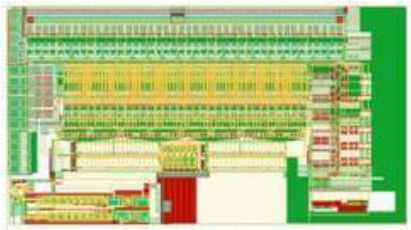
World's fastest 6b ADC at 1991, Bipolar

6b, 1GHz ADC
2W,
1.5um Bipolar

A. Matsuzawa, ISSCC 1991

World's fastest CMOS ADC at 2000

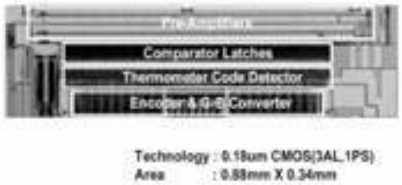
K. Sushihara and A. Matsuzawa, ISSCC 2000.



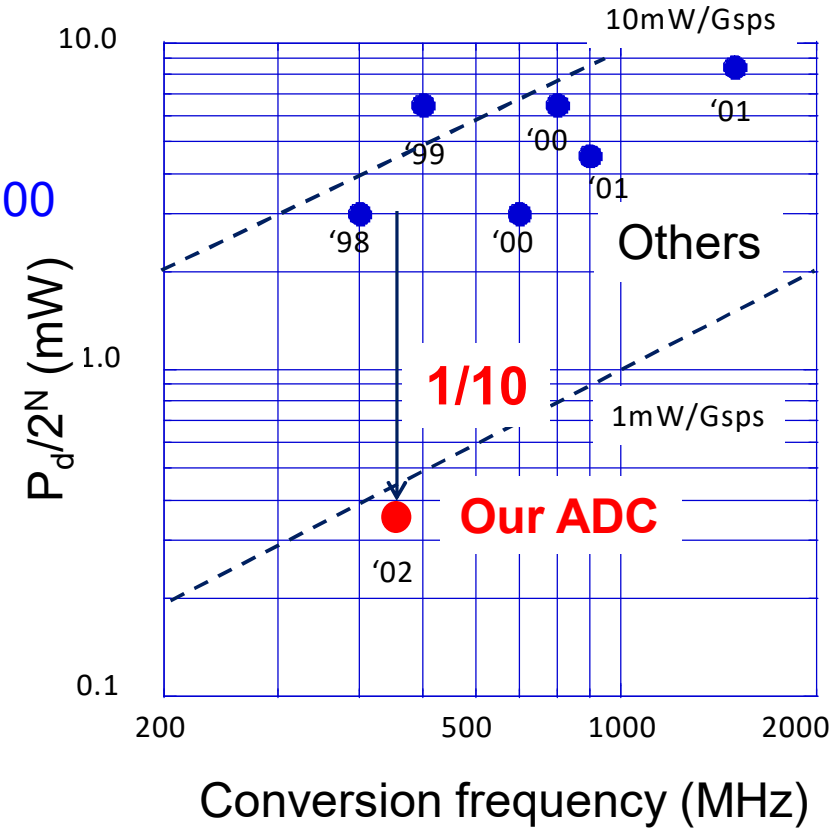
6b, 800MHz ADC
400mW, 2mm^2
0.25umCMOS

P_d is down to 1/8 with keeping speed

K. Sushihara and A. Matsuzawa, ISSCC 2002.



7b, 400MHz ADC
50mW, 0.3mm^2
0.18umCMOS

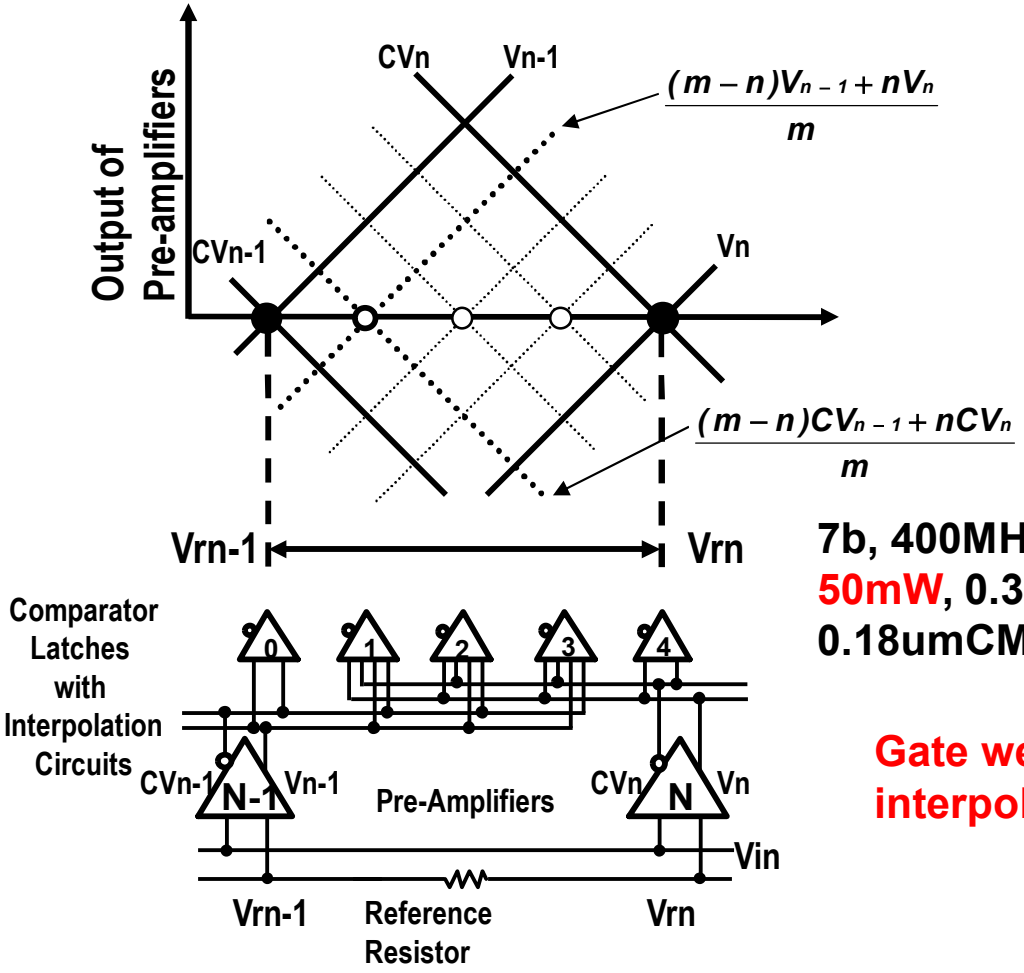


A. Matsuzawa

Gate weighted interpolation with dynamic comparator

TOKYO TECH Pursuing Excellence

Interpolation is realized using the additivity of drain conductance in MOS linear region. Very low power due to dynamic action of MOS Latch. Input referred mismatch can be reduced using distributed pre-amplifiers.



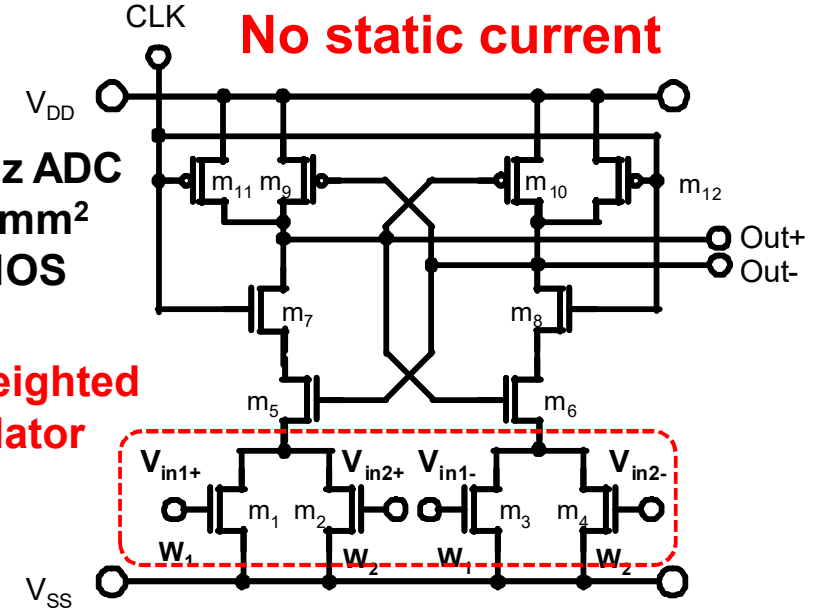
$$G_1 = K_p\left[\frac{W_1}{L}(V_{in1+} - V_{th}) + \frac{W_2}{L}(V_{in2+} + -V_{th})\right]$$

$$G_2 = K_p\left[\frac{W_1}{L}(V_{in1-} - V_{th}) + \frac{W_2}{L}(V_{in2-} + -V_{th})\right]$$

$$if\ W_1 : W_2 = \frac{m-n}{m} : \frac{n}{m}$$

$$then,\ (m-n)V_{in1+} + nV_{in2+} = (m-n)V_{in1-} + nV_{in2-}$$

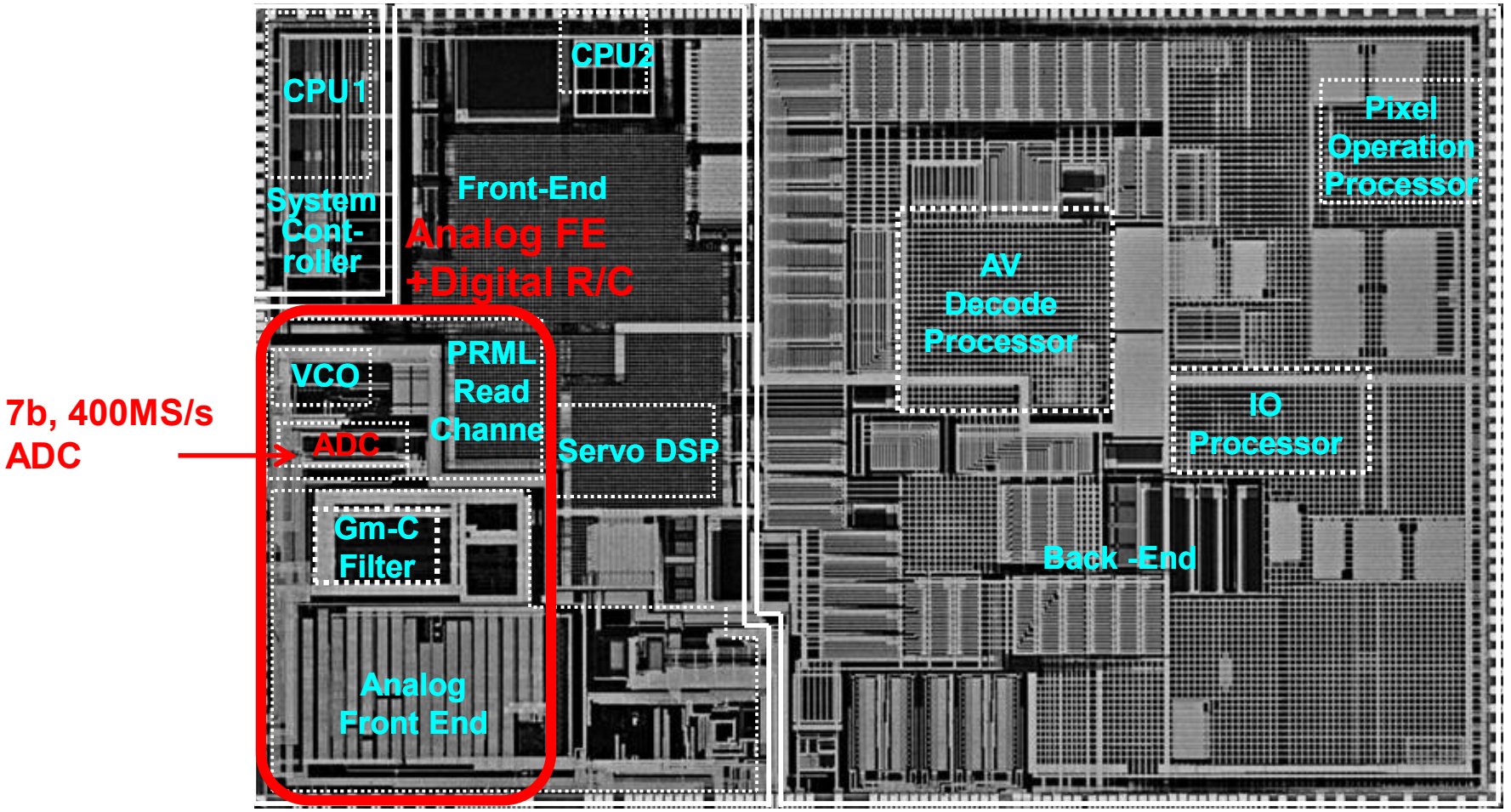
7b, 400MHz ADC
50mW, 0.3mm²
0.18umCMOS



The world's first fully integrated SoC for DVD

We developed the world's first mixed signal SoC for DVD that can integrate full DVD system.

Okamoto,…, A. Matsuzawa., ISSCC 2003, JSC 2003. **0.13um, Cu 6Layer, 24MTr**



The effect of Fully integrated SoC

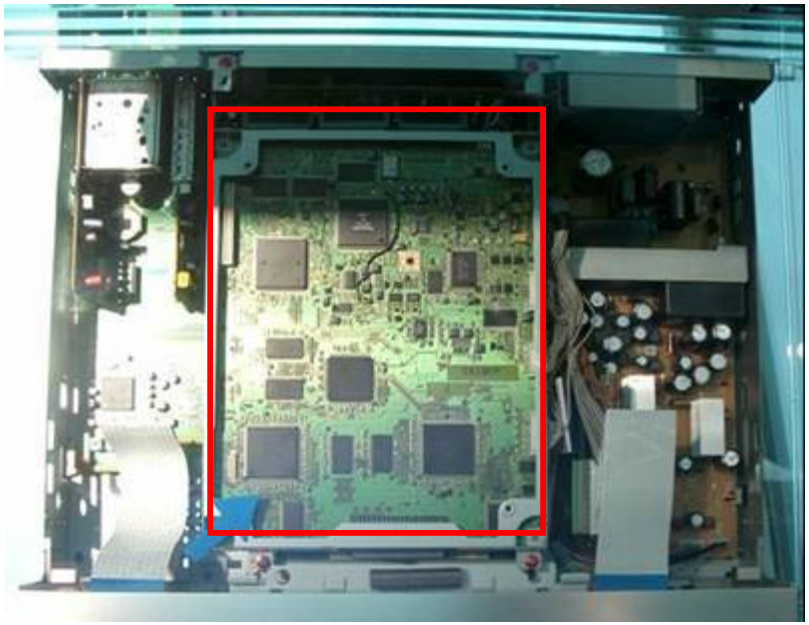
TOKYO TECH Pursuing Excellence

Developed fully integrated SoC can reduce the # of components drastically. It contributed increase of performance and reliability, reduction of product cost and system space. It enabled on-board DVD system in note PC.

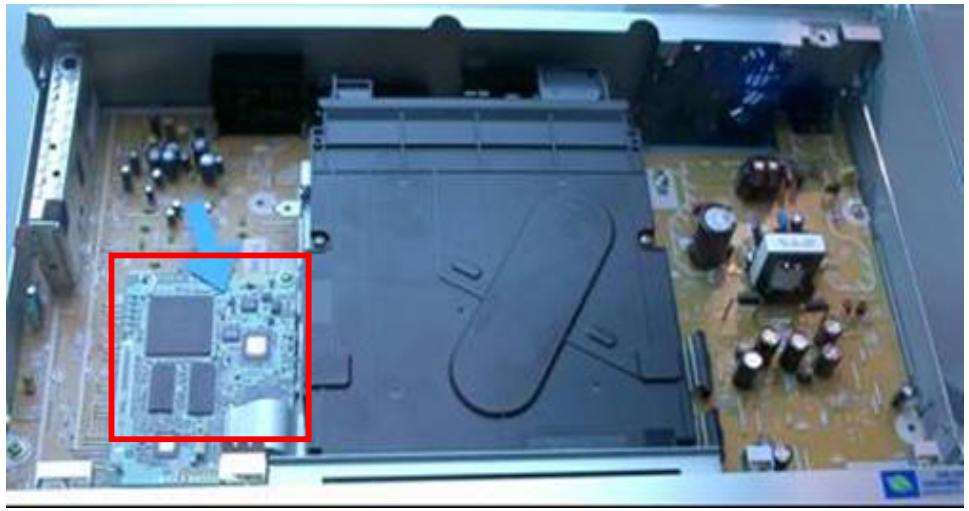
SoCs for DVD shipped **520 M chips** and the total sales is **2.5 Billion USD.**

DVD Recorder SoC: System on a Chip

'2000 Model (before SoC)



'2003 Model (after SoC)



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Advanced ADC design

Discussion in recent low power
and high performance ADC design

Typical ADC architectures

36

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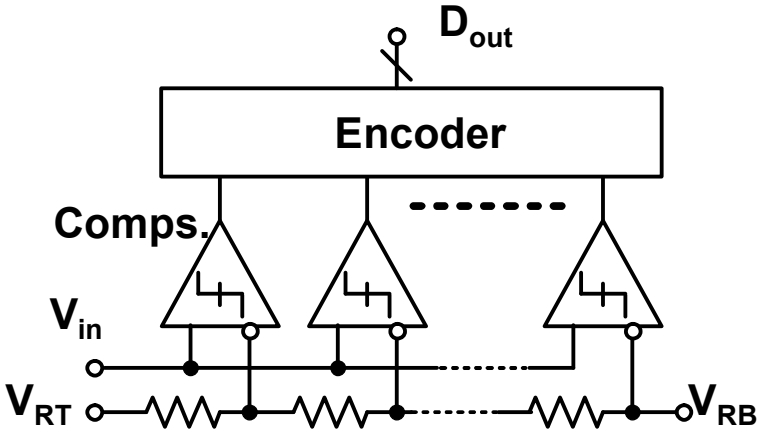
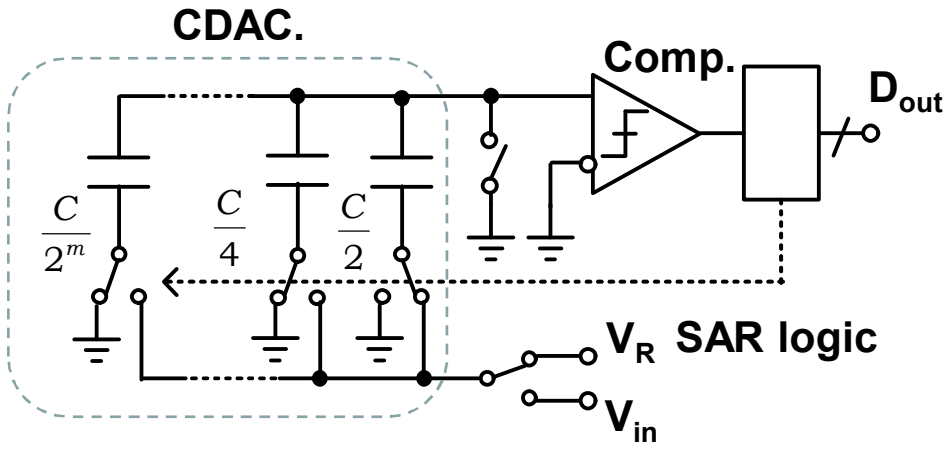
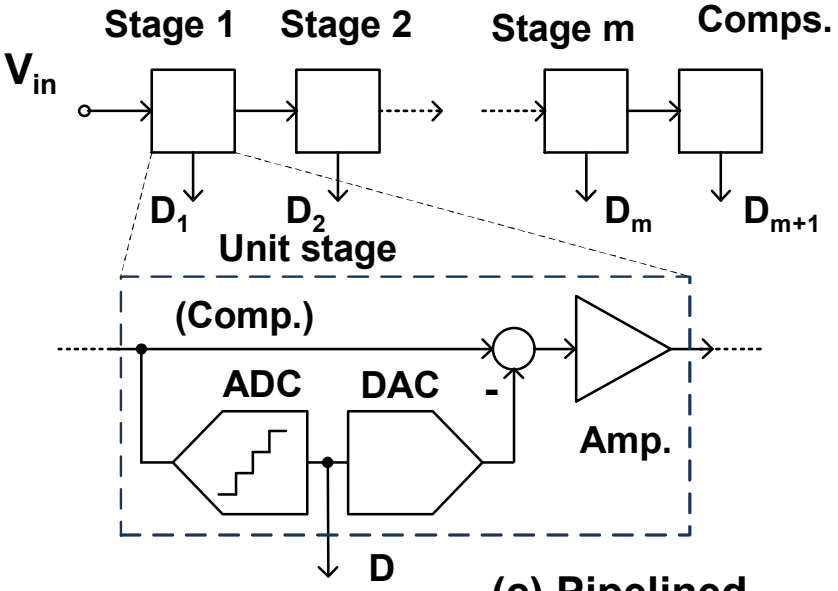
Flash, SAR, Pipelined, and ΔΣ are the major ADC architectures



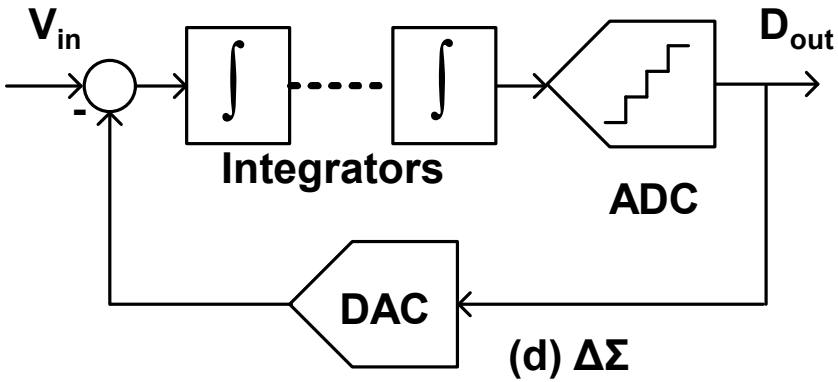
(a) Parallel (Flash)



(b) Successive Approximation Register (SAR)



(c) Pipelined



(d) ΔΣ

ADC architecture and performance

37

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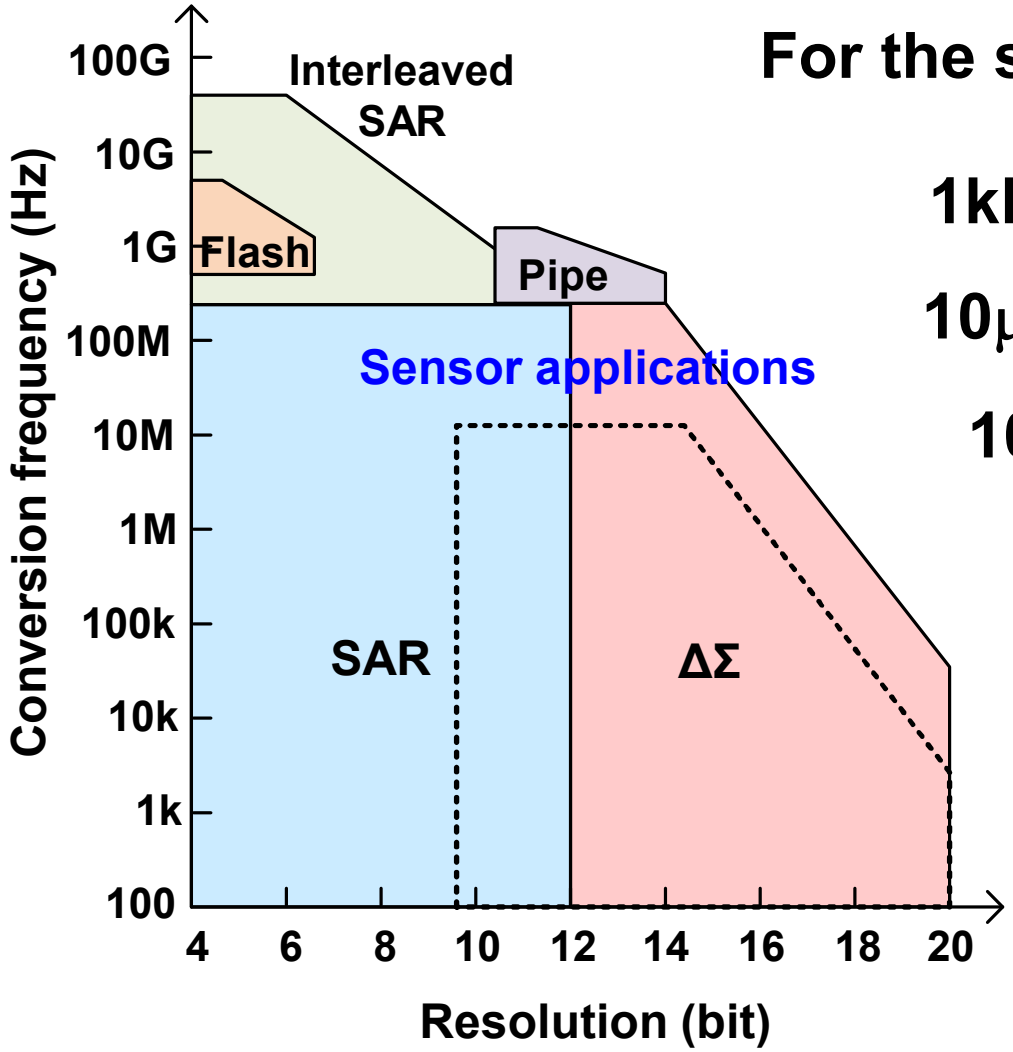
SAR ADC and ΔΣ ADC are the dominant architecture



For the sensor applications

$1kHz<f_c<10MHz$

$10\mu V<V_n<200\mu V$

$10bit<N<18bit$

A. Matsuzawa, Tech Idea

Basic idea for advanced ADC design

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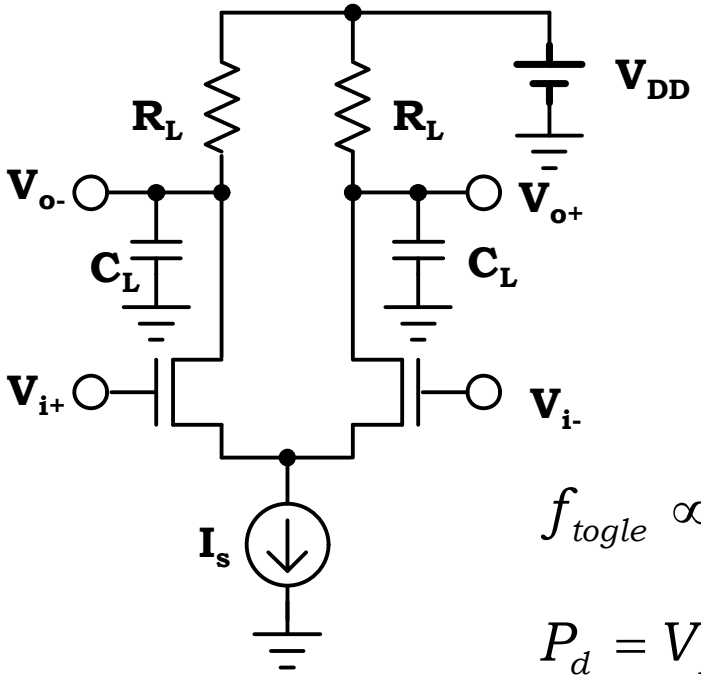
Challenge to design of ADC circuit like CMOS logic

No or less static current, minimum capacitance.
Power should be proportional to clock frequency.

CML logic and conventional amplifier



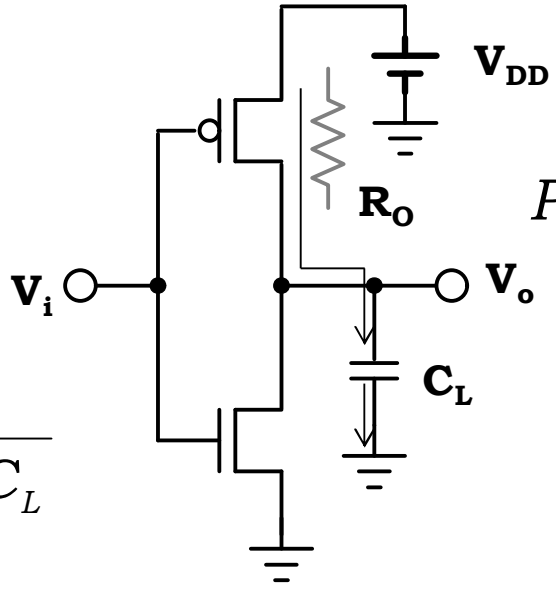
$$f_{togle} \propto \frac{I_s}{V_{DD} C_L}$$

$$P_d = V_{DD} I_s$$

Consume static current

Should increase current
to increase speed.

CMOS logic



$$E_d = C_L V_{DD}^2$$

$$P_d = f E_d = f C_L V_{DD}^2$$

$$f_{togle} \propto \frac{1}{R_o C_L}$$

No static current

No need to increase current
to increase speed.

Advanced ADC design

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- Mismatch limited ADC architecture: flash ADC
  - Use dynamic comparator
  - Transistor and circuit should be small as possible
  - Mismatch increase with decreasing transistor size
  - Compensate mismatch by digital calibration method

- Thermal noise limited ADC architecture: SAR
  - Use minimum capacitance determined by thermal noise
  - Use no or less static current circuit
  - Compensate capacitance and MOS mismatch by digital calibration
  - Use low-noise dynamic comparator
  - Delta-sigma method should be used for further noise reduction
  - Open-loop integrator with dynamic amplifier can realize low energy and high speed complete integrator

Mismatch limited ADC: Flash ADC

Developing baseband SoC

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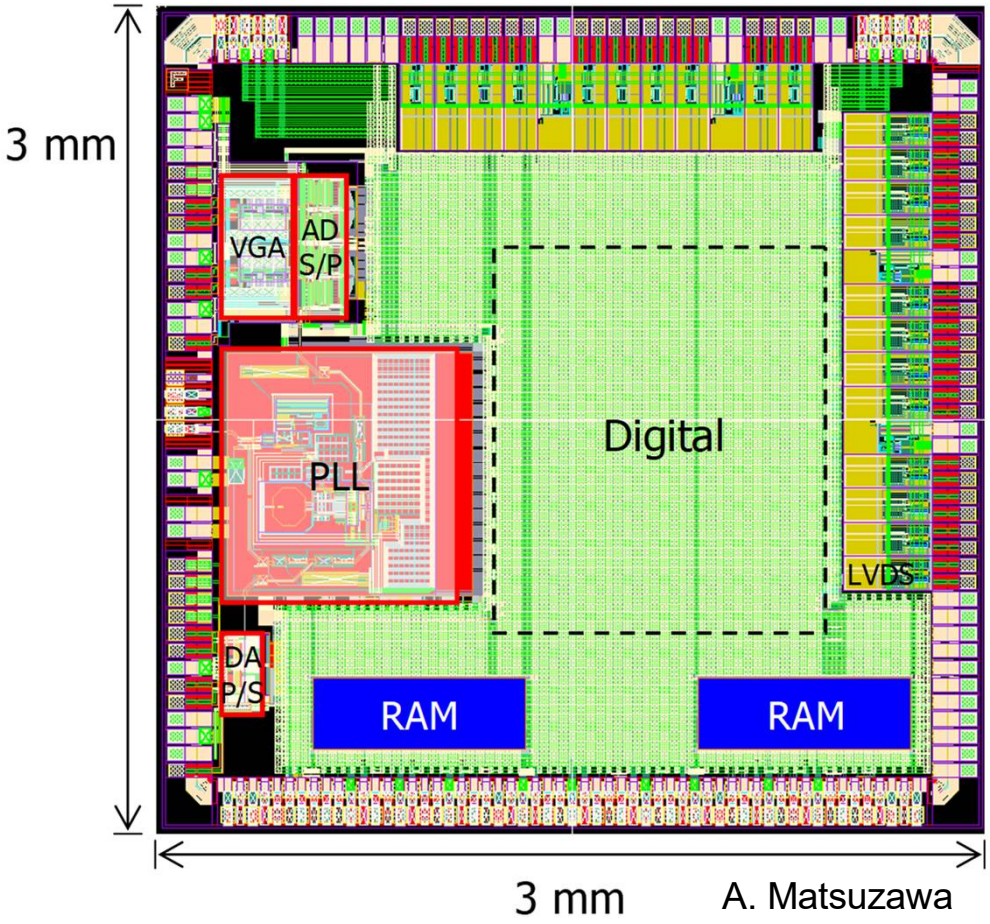
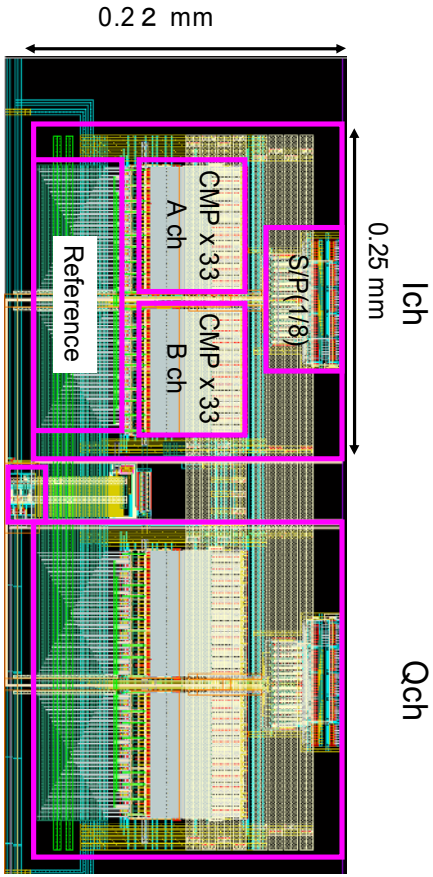
Developed chip for 60GHz transceiver integrating ADC, DAC, VGA, and PLL, using 40nm CMOS technology.

RX: 300mW, TX: 110mW
40nm CMOS technology



K. Okada and A. Matsuzawa, et al., ISSCC 2012.

ADC 5b, 2.3GSps, 12mW/ch



Analog Baseband : ADC

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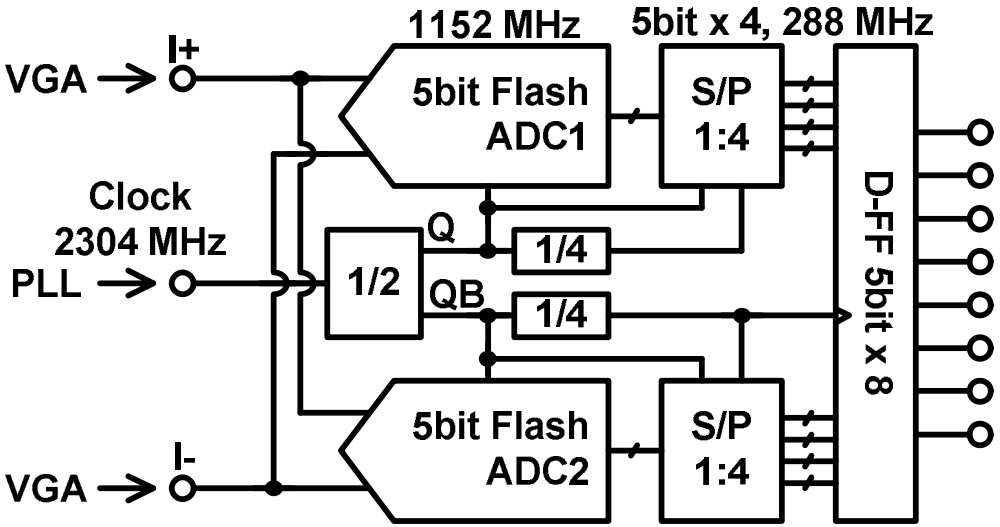
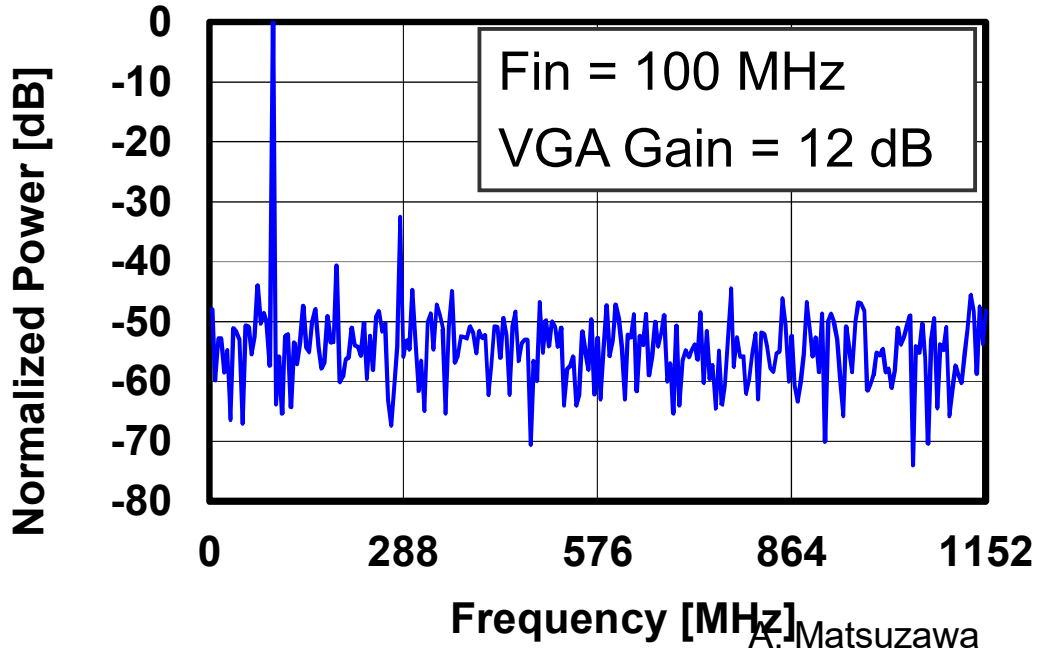


On-chip foreground calibration

M. Miyahara and A. Matsuzawa, et al., RFIC 2012.



VGA Gain range	0-40 dB
ADC Resolution	5 bit
Sampling rate	2304 MS/s
Power Consumption	VGA : 9 mW ADC : 12 mW*
DNL, INL	< 0.8 LSB
SNDR	26.1 dB
FoM of ADC	316 fJ/conv.-s

*single channel inc. S/P

Flash ADC design

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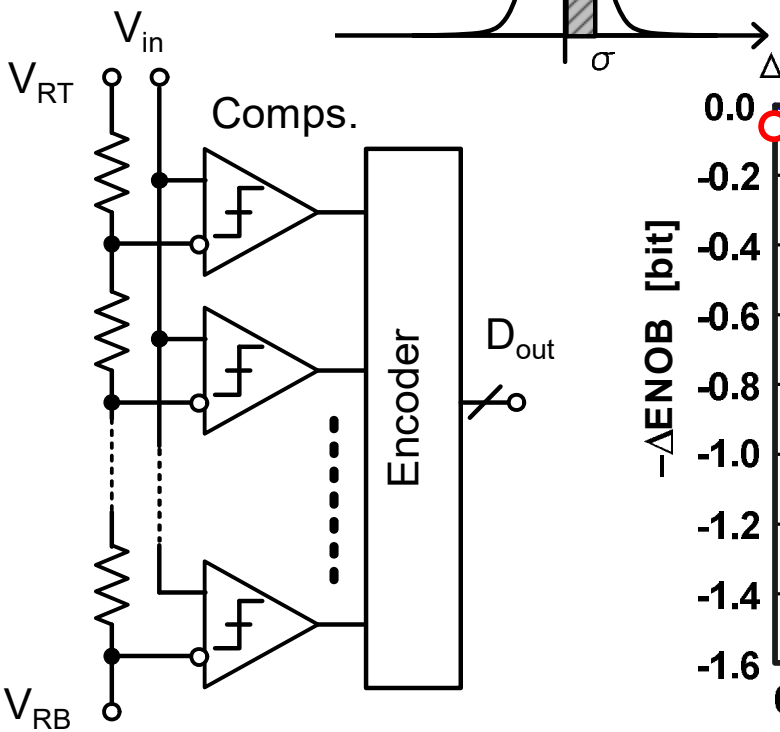
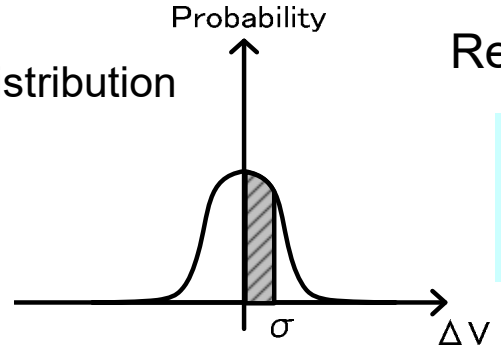
Offset mismatch determines the effective resolution.

Thermal noise can be neglected because of low resolution.

Flash ADC

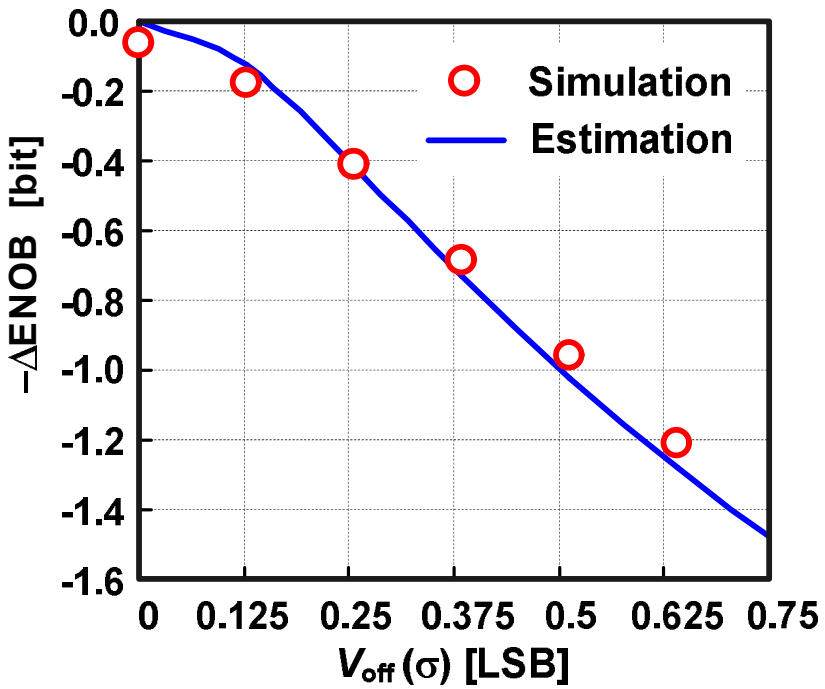




Reduction of ENOB by mismatch

$$\Delta ENOB = \frac{1}{2}\log_2\left(1 + 12\left(\frac{V_{\text{off}}(\sigma)}{V_{\text{q}}}\right)^2\right)$$

Effective Number of Bit



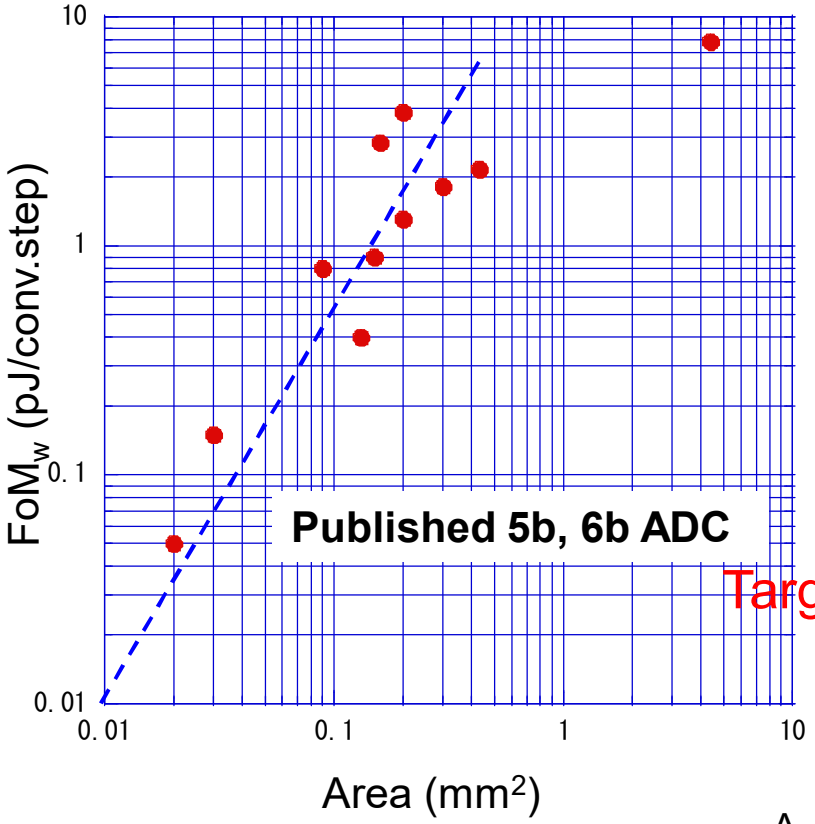
Strategy for low energy flash ADC

Small area is required to educe energy, but increases mismatch.
Therefor, (digital) mismatch reduction technique should be applied

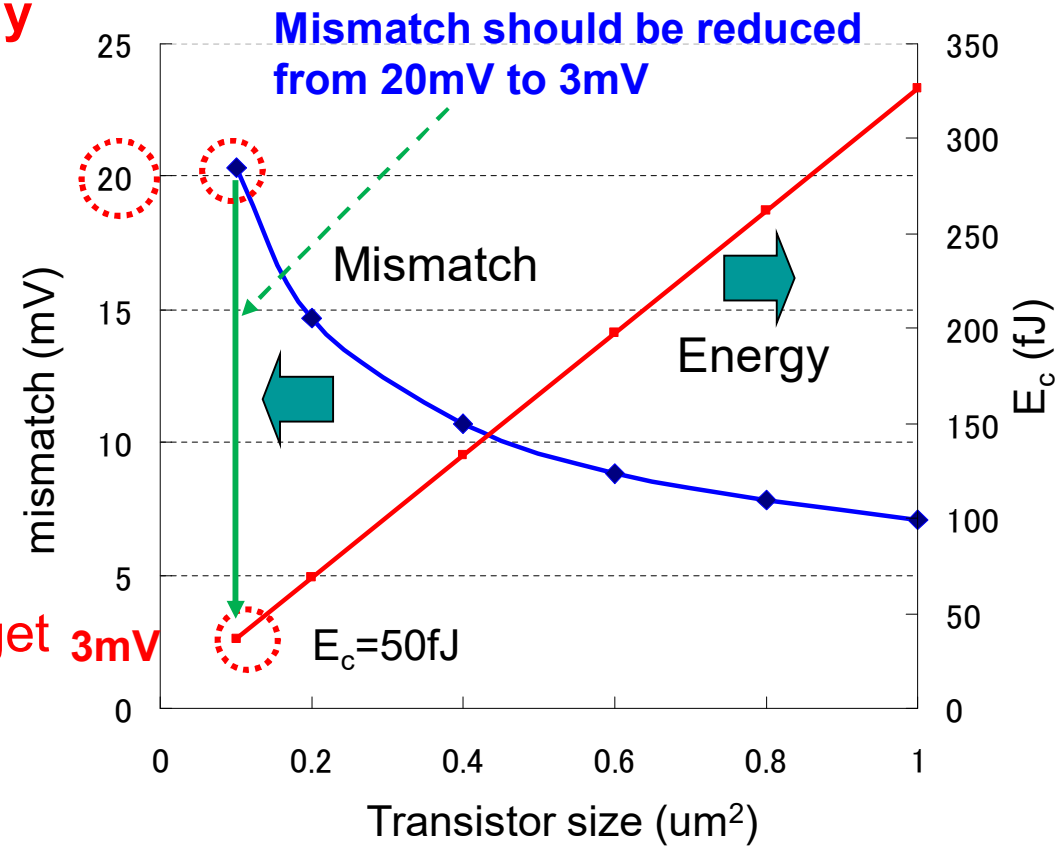
$$FoM_w = \frac{P_d \cdot 2^{\Delta ENOB}}{f_c \cdot 2^N}$$

$$V_{\text{offset}}(\sigma) \propto \frac{1}{\sqrt{LW}} \qquad E_c \propto C_c \propto LW$$

Small area realizes low energy



Small transistor increases mismatch

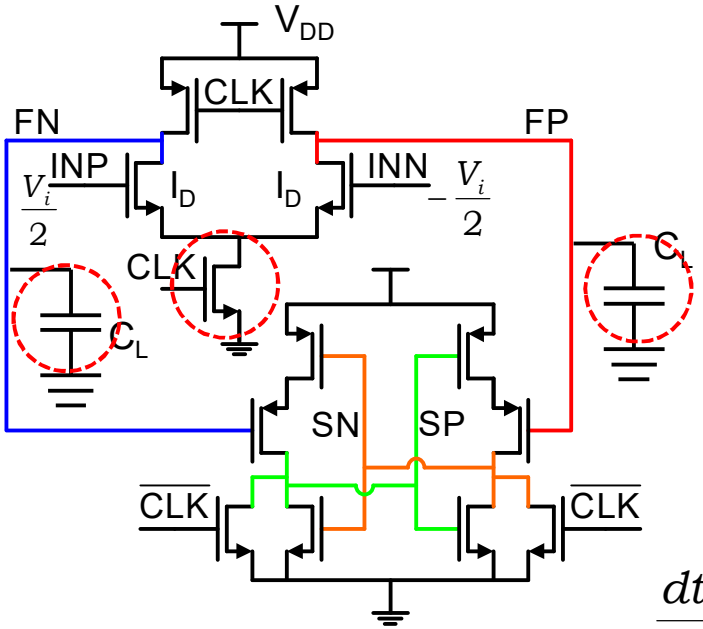


A. Matsuzawa

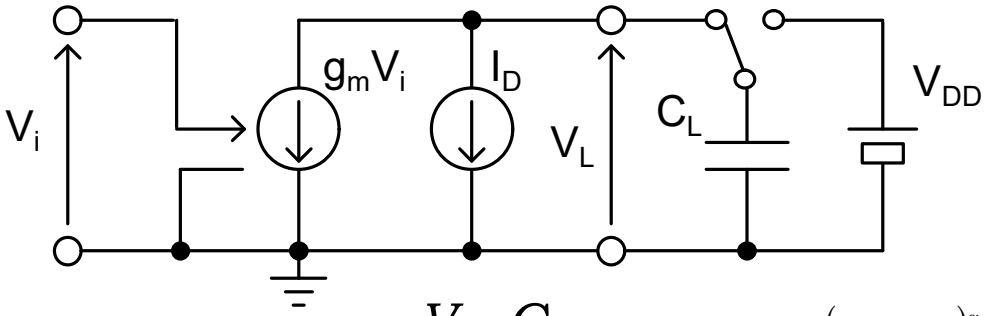
Mismatch compensation for the dynamic comparator

TOKYO TECH Pursuing Excellence

Mismatch can be compensated by capacitance or current



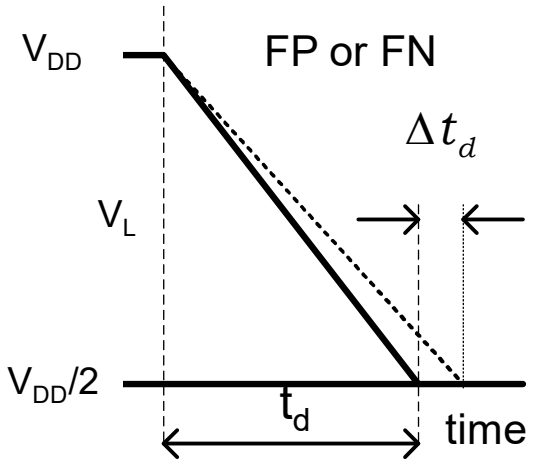
Equivalent circuit for the fist stage



Delay time $t_d = \frac{V_{DD} C_L}{2 I_D}$

$$I_D \propto (V_{gs} - V_T)^{\alpha} = V_{eff}^{\alpha}$$

$$g_m = \frac{dI_D}{V_{eff}} = \alpha \frac{I_D}{V_{eff}}$$



$$\frac{dt_d}{dV_i} = \frac{dt_d}{dI_D} \cdot \frac{dI_D}{dV_i} = -\frac{V_{DD} C_L}{2 I_D} \frac{g_m}{I_D} = -t_d \frac{\alpha}{V_{eff}} \quad \therefore \frac{g_m}{I_D} = \frac{\alpha}{V_{eff}}$$

$$\therefore \frac{\Delta t_d}{t_d} = \alpha \frac{\Delta V_i}{V_{eff}} \qquad \frac{\Delta t_d}{t_d} = \left(\frac{\Delta C_L}{C_L} - \frac{\Delta I_D}{I_D} \right)$$

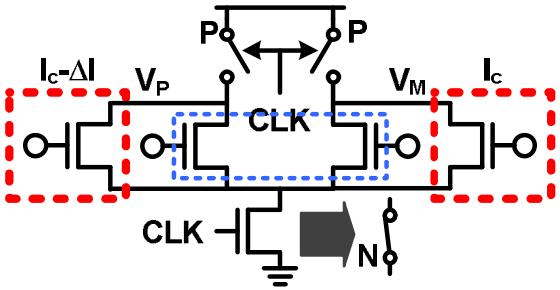
$$\therefore \frac{\Delta t_d}{t_d} = \alpha \frac{\Delta V_i}{V_{eff}}$$

$$\Delta V_i = \frac{V_{eff}}{\alpha} \left(\frac{\Delta C_L}{C_L} - \frac{\Delta I_D}{I_D} \right)$$

A. Matsuzawa

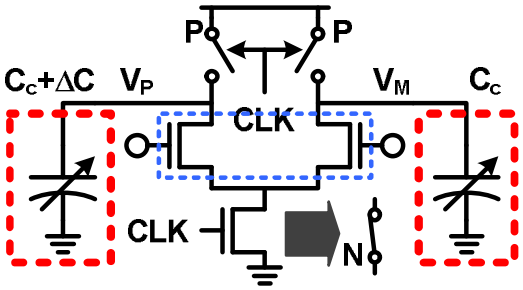
Digital calibration methods for mismatch

Resistor ladder type

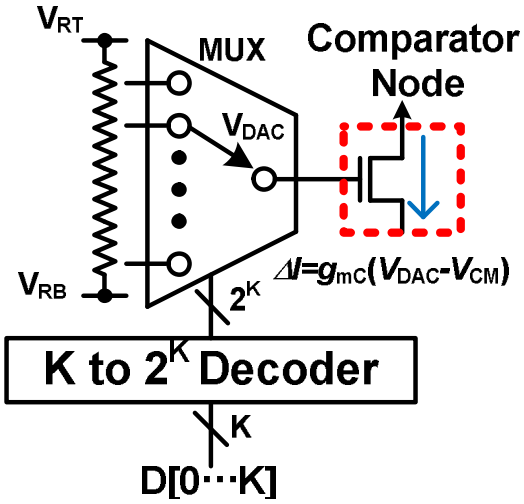


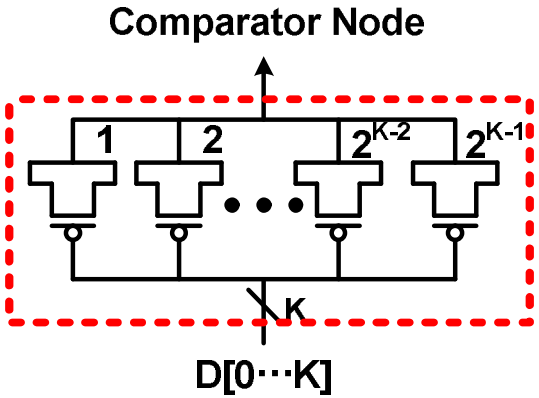
Current calibration

Capacitor array type



Capacitance calibration





Binary weighted capacitor array

Y. Asada, K. Yoshihara,T. Urano, M. Miyahara and A. Matsuzawa,

"A 6bit, 7mW, 250fJ, 700MS/s Sub-ranging ADC" A-SSCC, pp. 141-144, Nov. 2009.

Comparator with digital mismatch compensation

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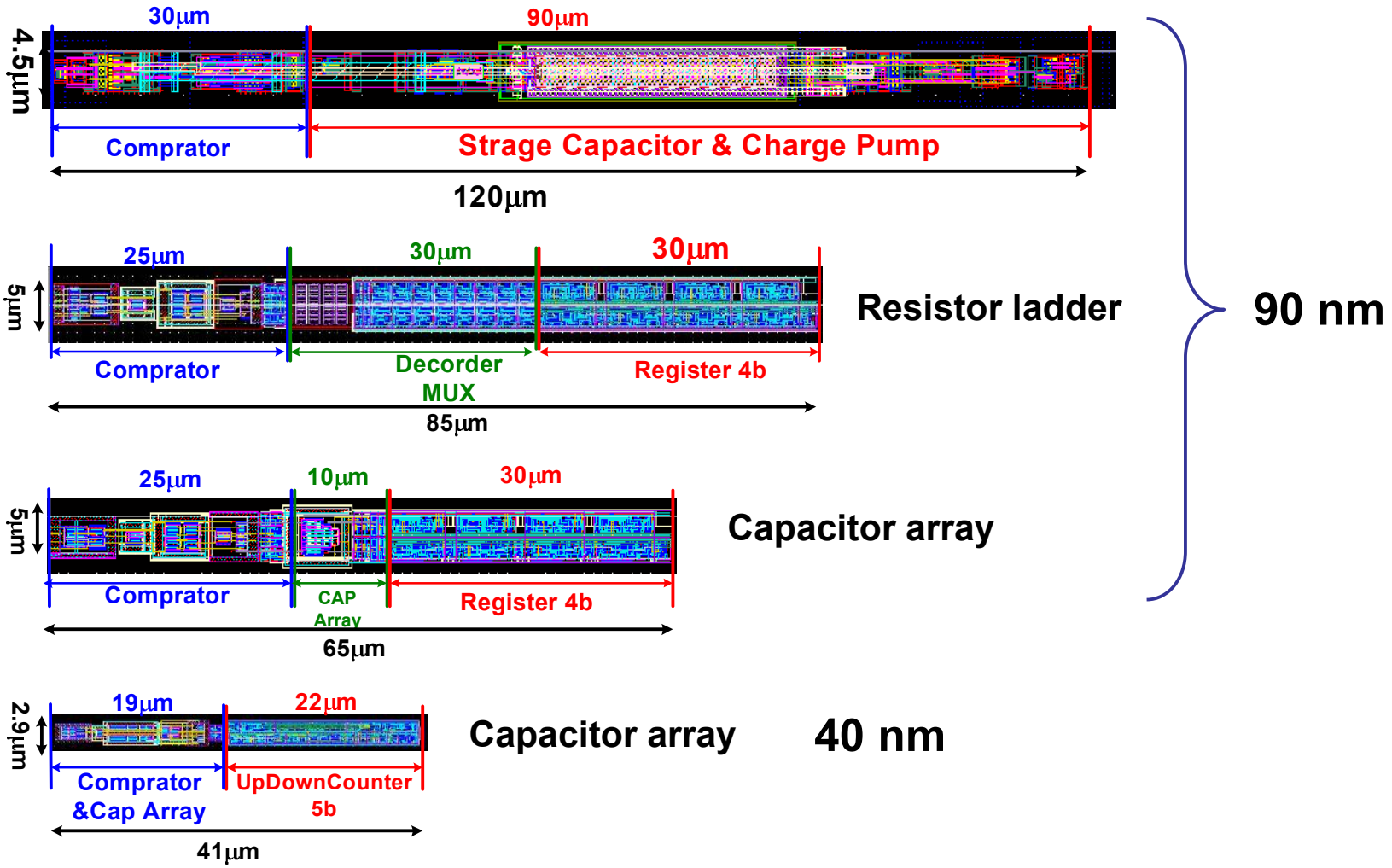
Area for digital compensation can be reduced by tech. scaling.



Effect of digital mismatch compensation

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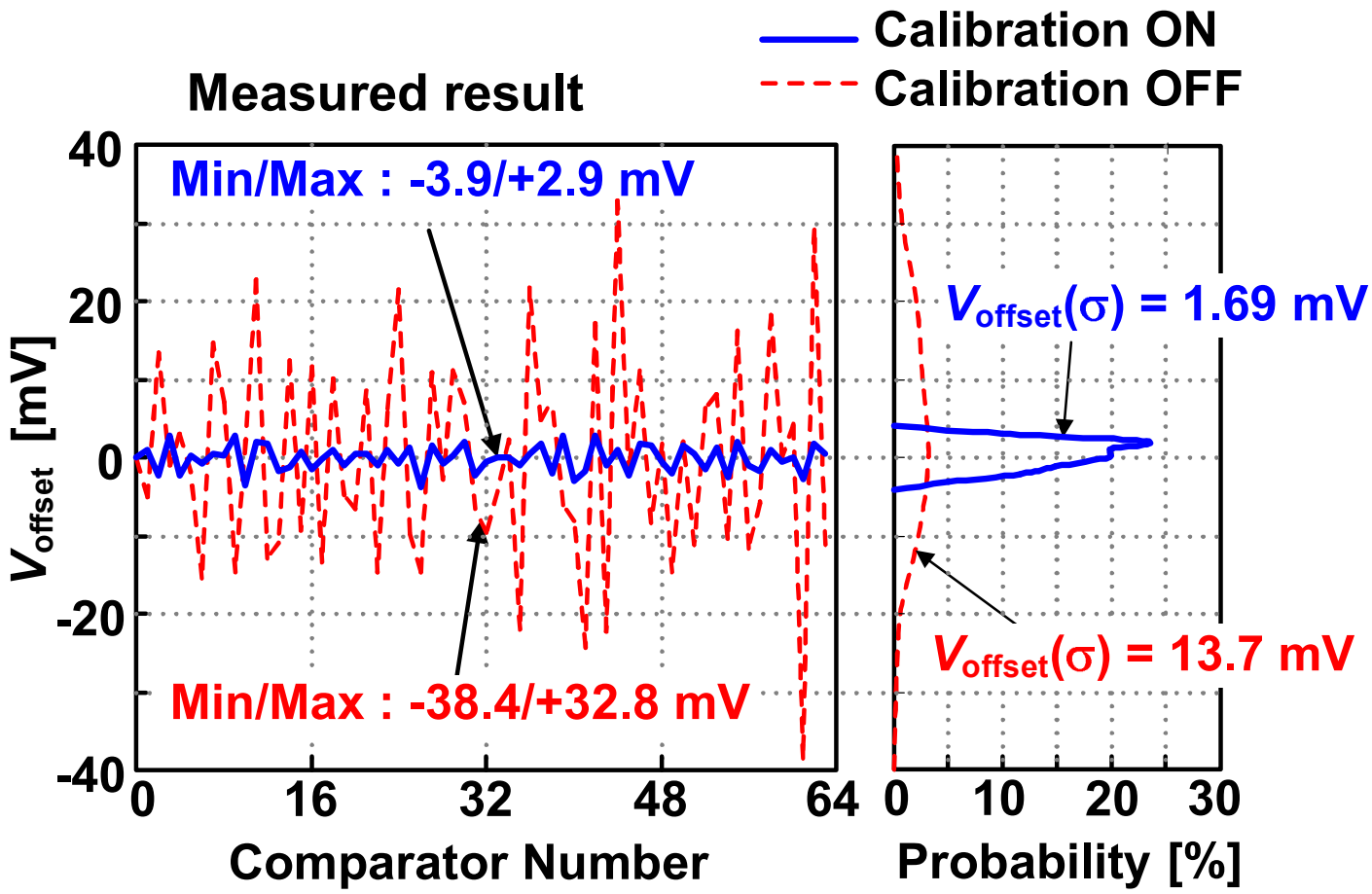
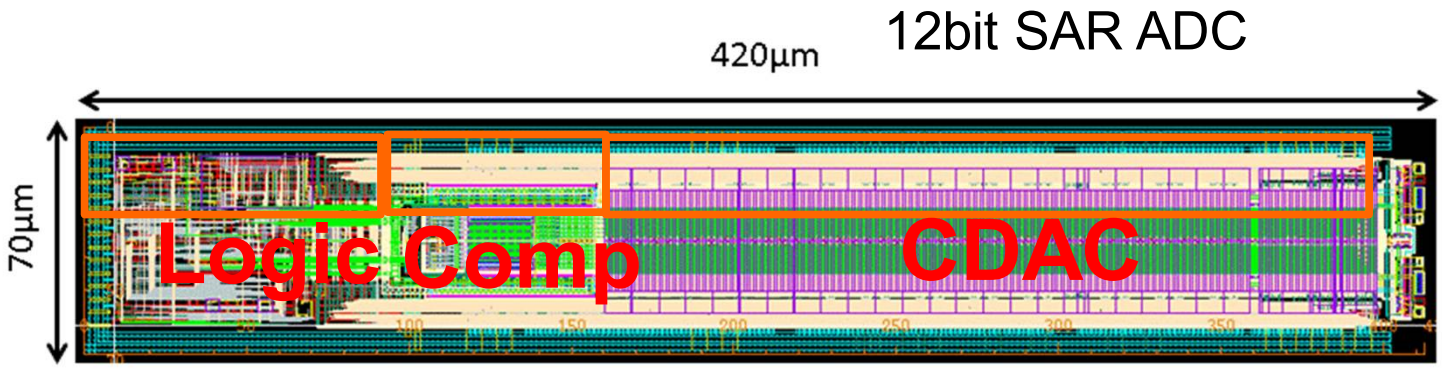
The mismatch voltage can be reduced from 14mV to 1.7mV.



M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Thermal noise limited ADC: SAR ADC



S. Lee, A. Matsuzawa, et al., SSDM 2013

Sampling rate vs. power dissipation

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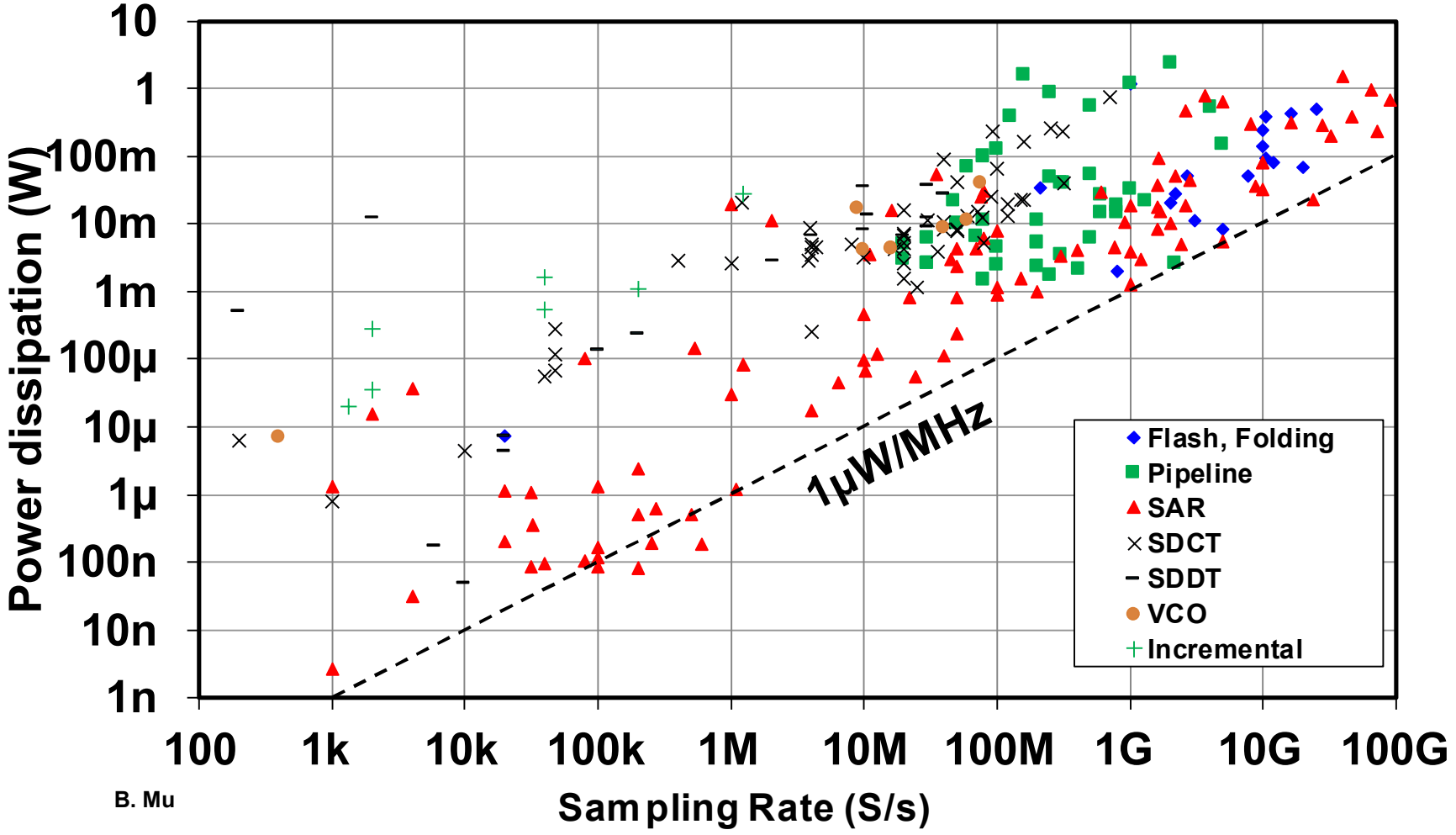
SAR ADC is the lowest energy ADC architecture



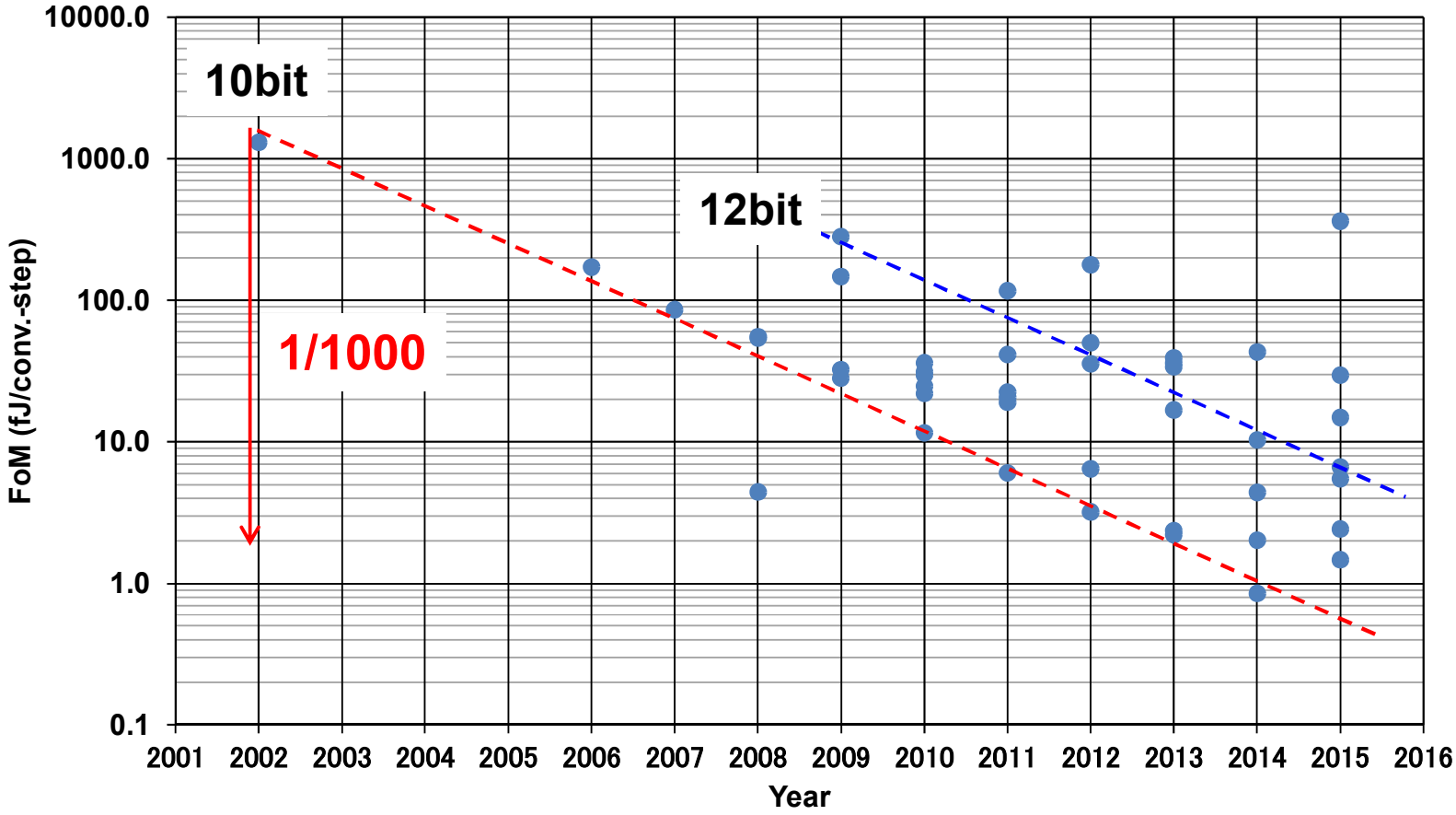
Rapid energy decrease of SAR ADC

Conversion energy of SAR ADC has decreased rapidly.
1/1000 has been achieved in recent 12 years.

$$FoM = \frac{P_d}{f_s \times 2^{N'}}$$ (Jour)

1/1000 in 12 years

N': Effective # of bit



Theory: SNR and consumed energy

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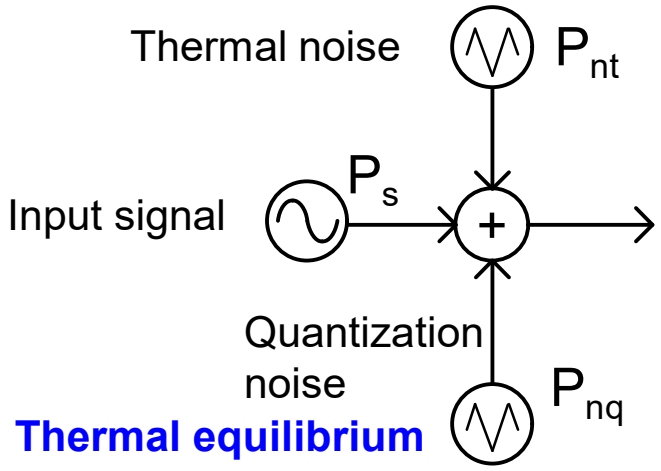
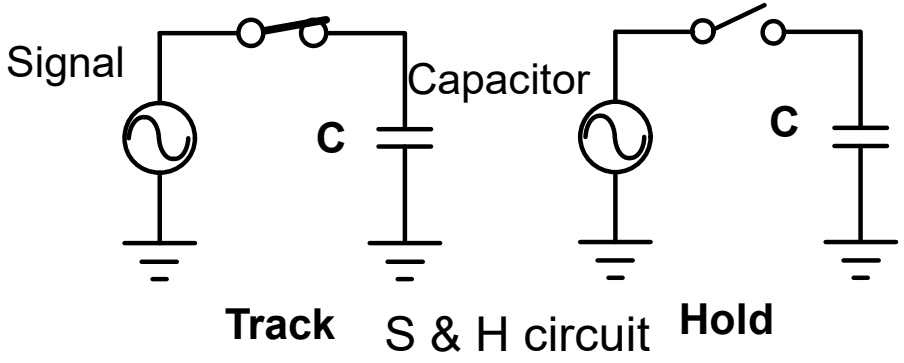
Signal and noise in ADC



Thermal equilibrium

$$\frac{1}{2}CV_n^2 = \frac{1}{2}kT$$

Electrical energy=Thermal energy



$$E_w = 10^{\left(\frac{SNR(dB)-190}{10}\right)}(J)$$

Quantization voltage $V_q = \frac{V_{FS}}{2^N}$ V_{FS}: Full scale voltage, N: Resolution

Quantization noise $P_{nq} = \frac{1}{3}\left(\frac{V_q}{2}\right)^2 = \frac{V_{FS}^2}{12 \cdot 2^{2N}}$

Thermal noise $P_{nt} = m\frac{kT}{C}$ m: # of noise source

Required capacitance $C = 12mkT\frac{2^{2N}}{V_{FS}^2}$ $P_{nq} = P_{nt}$

Consumed energy

$$E_w = 2C\left(\frac{V_{FS}}{2}\right)^2 = 6mkT \cdot 2^{2N} \approx 5\times10^{-20} \times 2^{2N}\ (J)$$

$$E_w = 10^{\left(\frac{SNR(dB)-190}{10}\right)}(J)$$

SNDR vs. Ew

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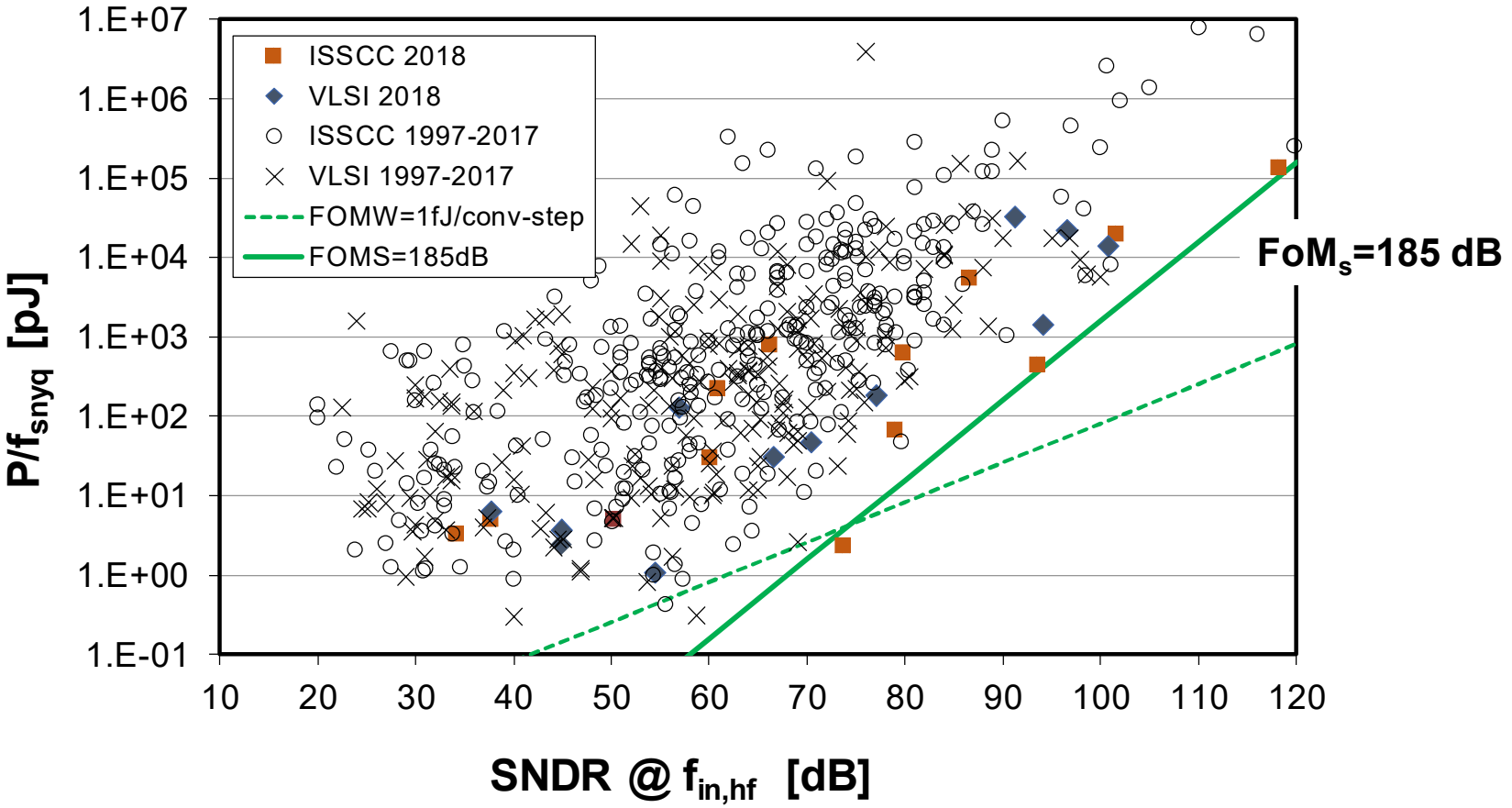
Theoretical trend has good agreement with experimental data

Consumed energy is proportional to SNR

$$E_w = 10^{\left(\frac{SNR(dB)-190}{10}\right)}(J)$$



SAR ADC

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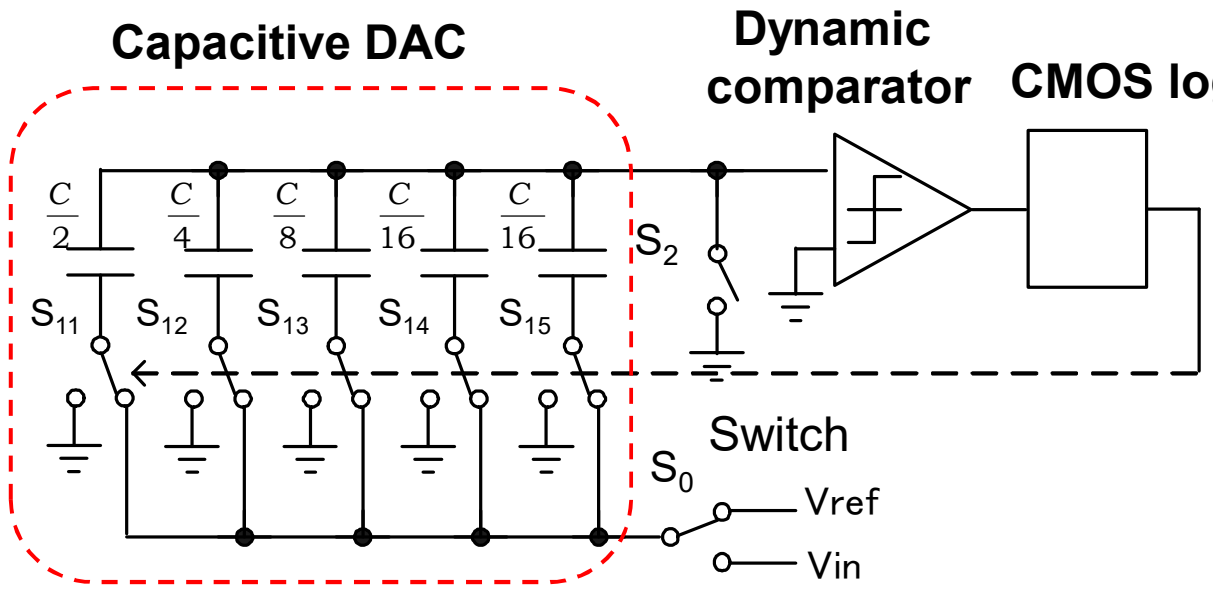
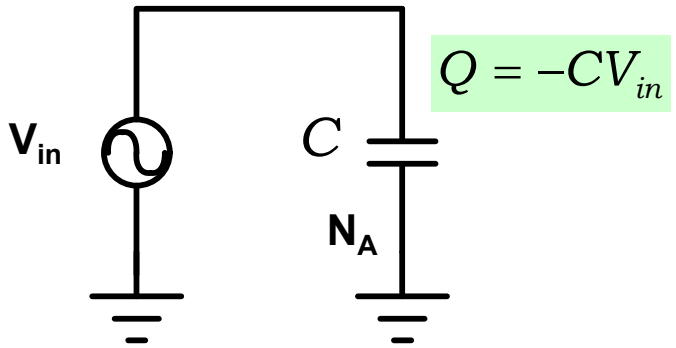
SAR ADC can be composed with no circuit that flows static current



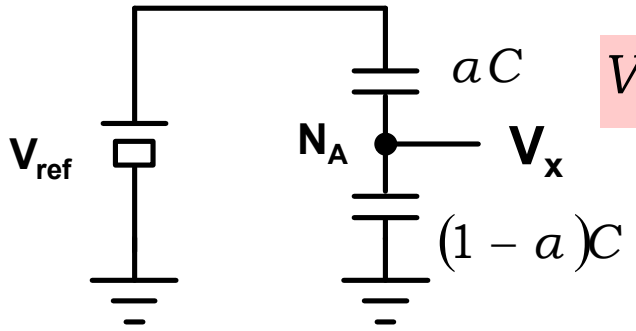
- No resistance
- No OPamp
- No static current

Sample



$$Q = -CV_{in}$$

Voltage generation by CDAC

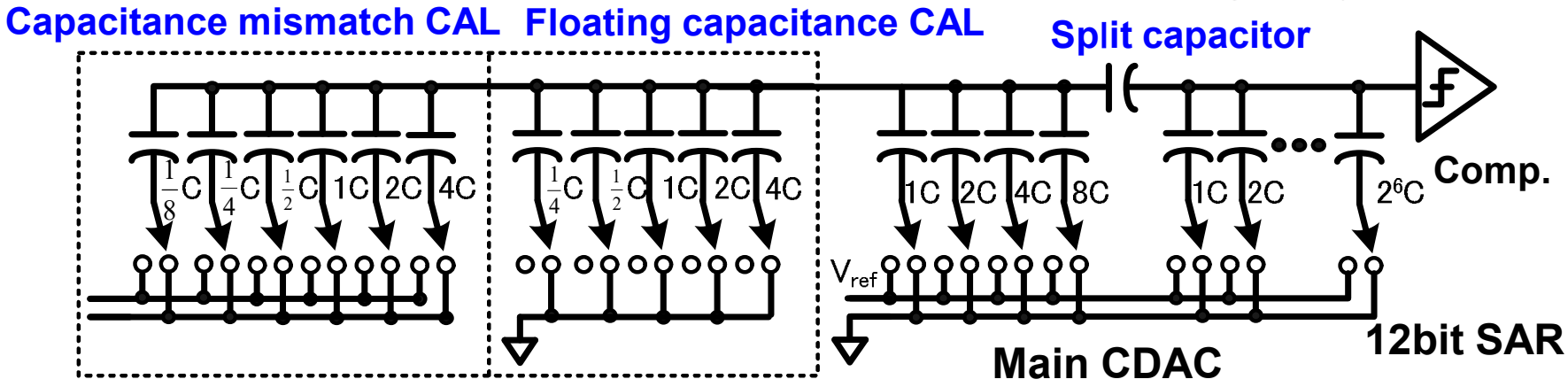


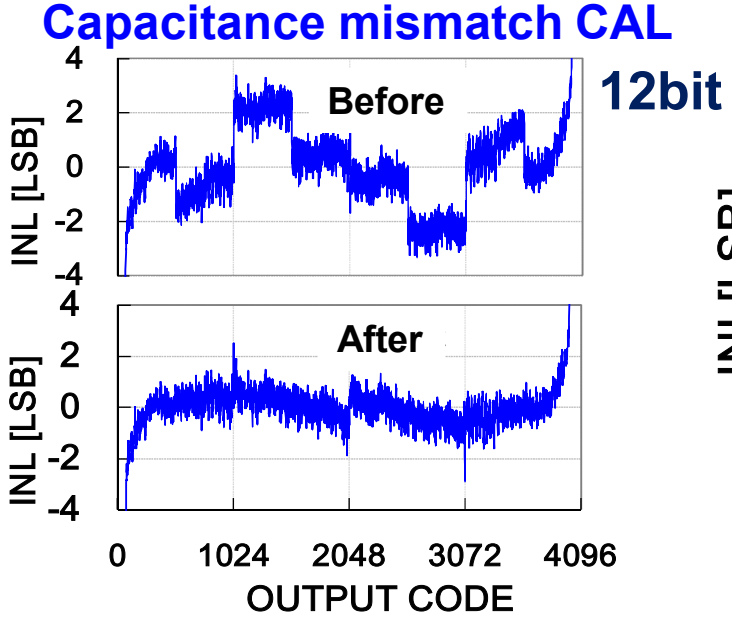
$$V_x = -\left(V_{sig} - a \cdot V_{ref}\right)$$

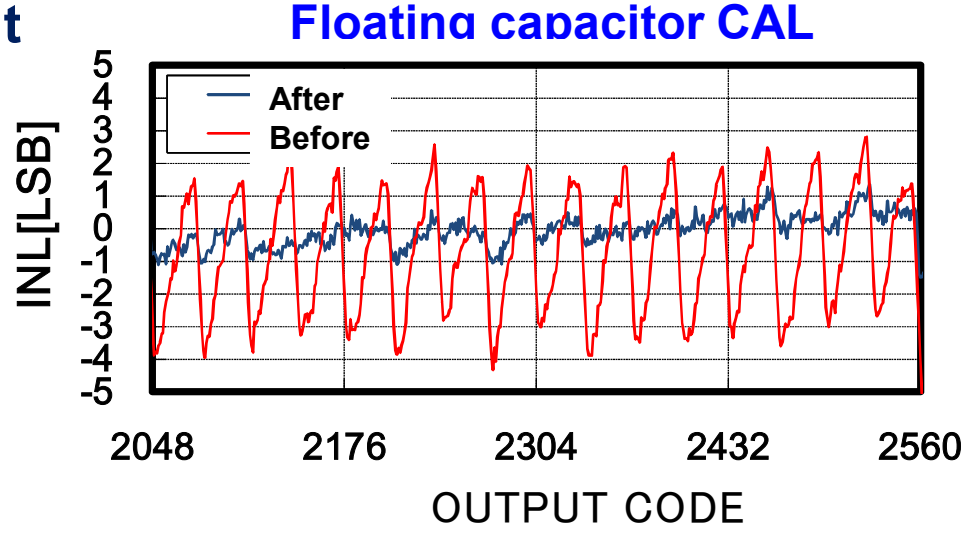
$$0 < a < 1$$

To address capacitor mismatch

Use small capacitor that satisfies the thermal noise limit.
Capacitor mismatch should be compensated digitally.

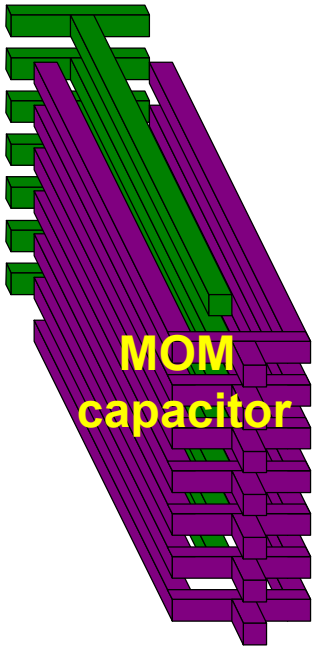


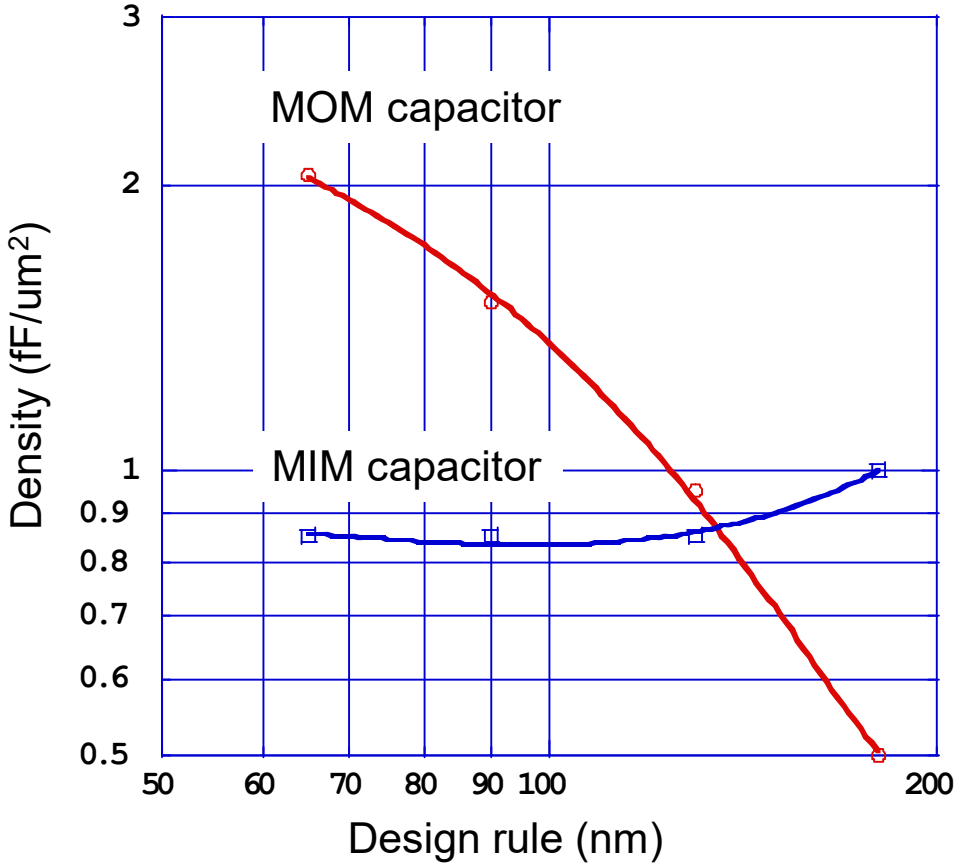




Use of MOM capacitor

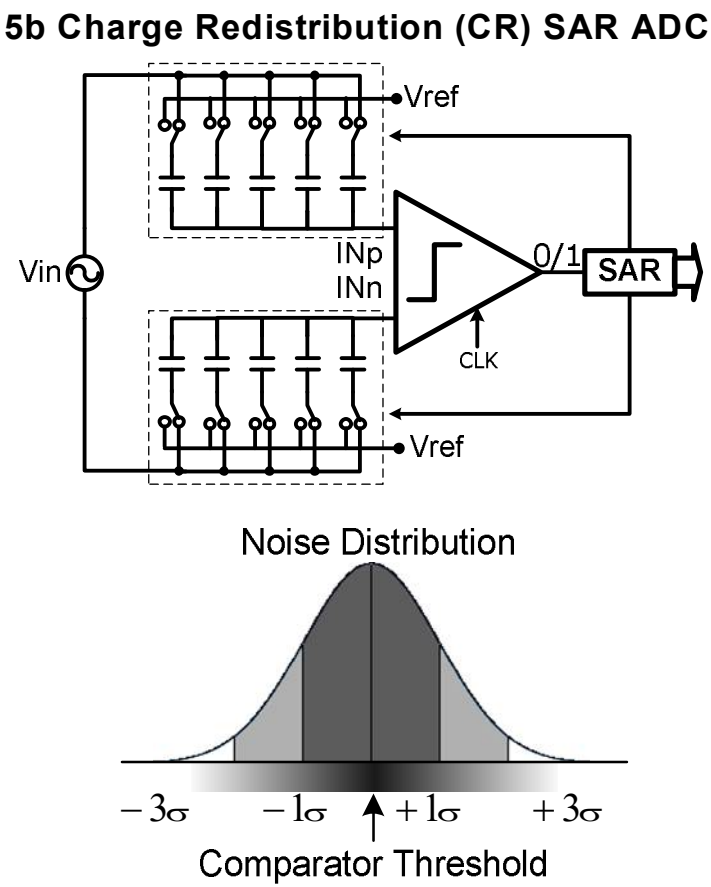
MOM capacitor uses the capacitance between the lateral interconnection.
The capacitor density can be increased by technology scaling.
Smaller occupied area (same C) can be expected by technology scaling.
Furthermore, parasitic capacitance can be controlled.

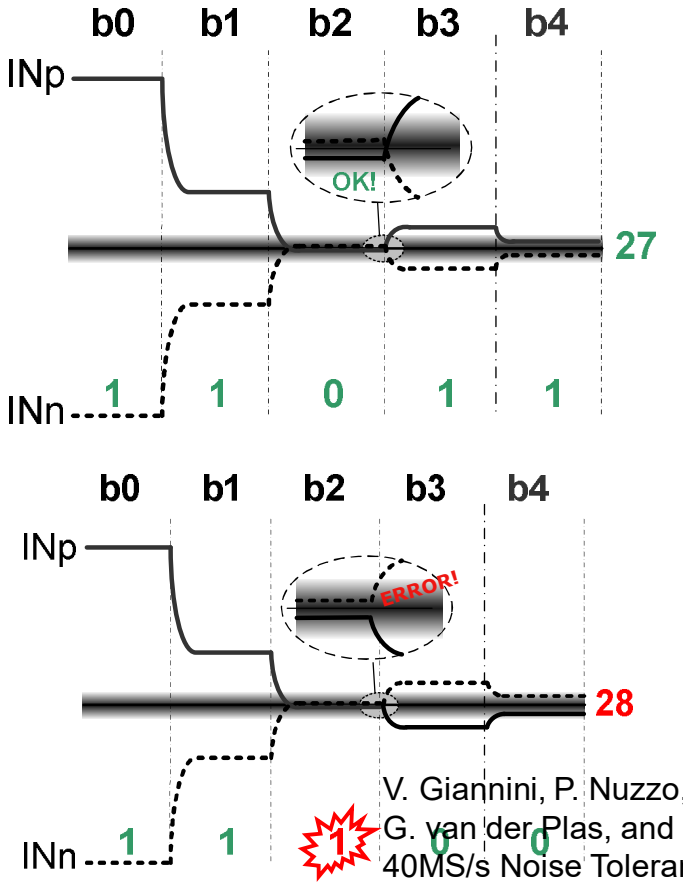




Effect of comparator noise to SAR ADCs

A comparator has noise and this results in conversion error.
Comparator noise determines SNR of SAR ADC





V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, “An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS,” IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.

Invention of low noise dynamic comparator

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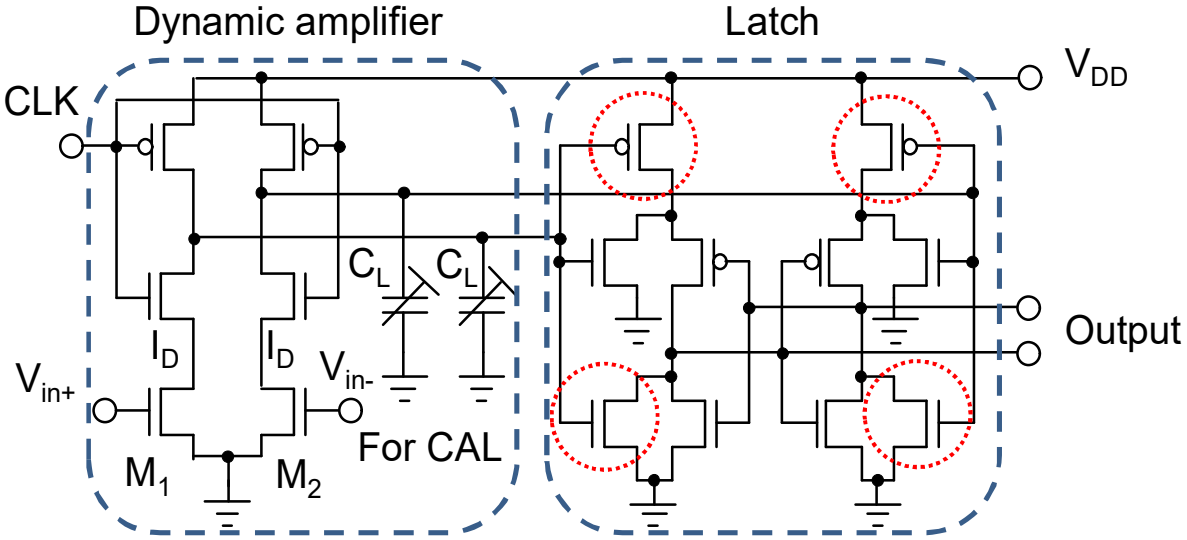
We invented low noise dynamic comparator.

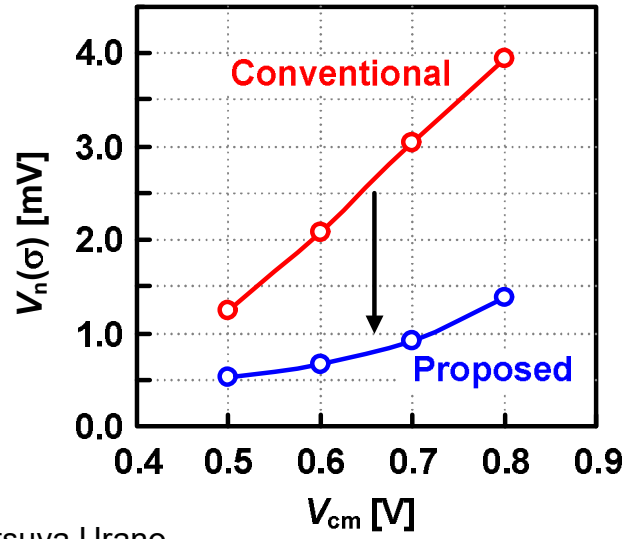
10 bit is a max. resolution when using conventional comparator

But this comparator can realize 12 bit resolution.

This paper has been cited more than 200 and becomes major comparator

$$\overline{v_{ni}^2} = \frac{kT\gamma}{C_L}\frac{V_{eff}}{V_{os}}$$





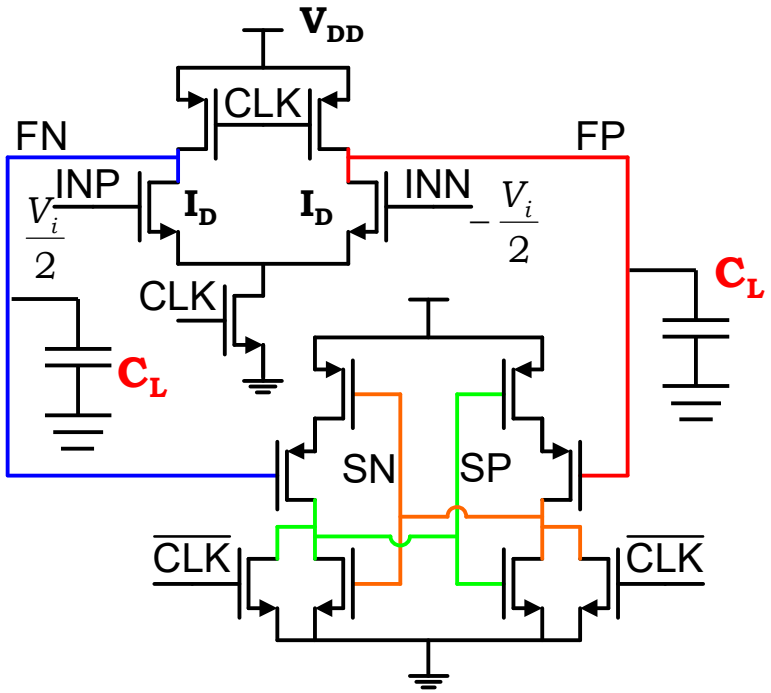
M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

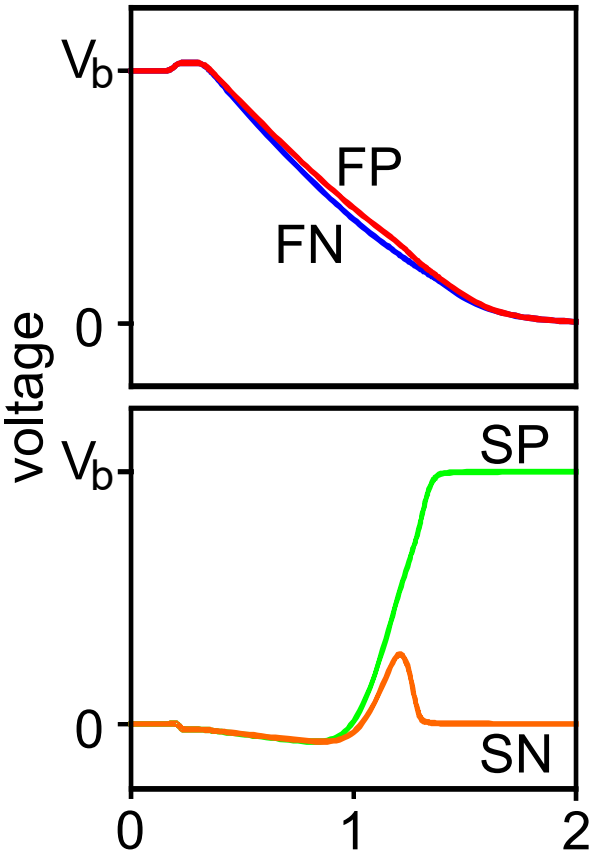
Yusuke Asada, Kei Yoshihara, Tatsuya Urano, Masaya Miyahara, and Akira Matsuzawa, "A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC," A-SSCC, 5-3, pp. 141-144, Taiwan, Taipei, Nov. 2009.

Dynamic comparator

A dynamic comparator is widely used to reduce static power.

The difference in input voltages causes a difference in discharging speed.

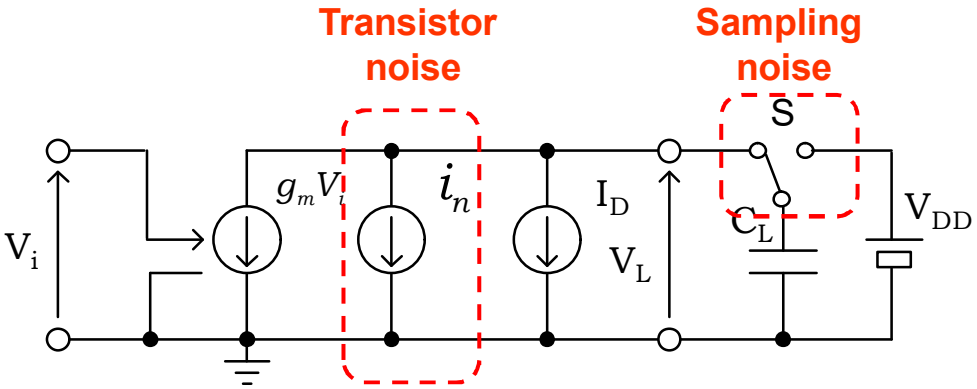




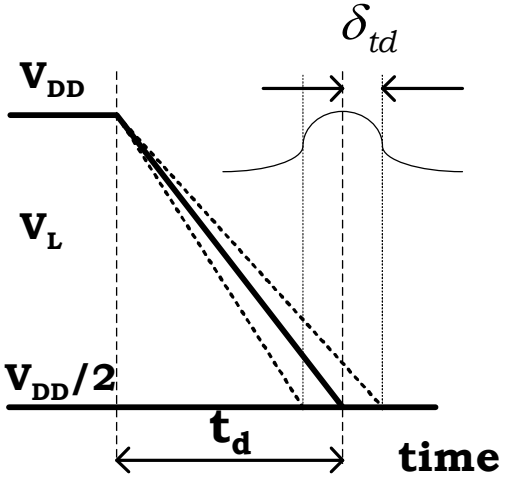
D. Schinkel, E. Mensink, E. Klumperink, Ed Van Tuijl, B. Nauta,

"A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup-Hold Time," ISSCC Dig. of Tech. Papers, pp.314-315, Feb., 2007.

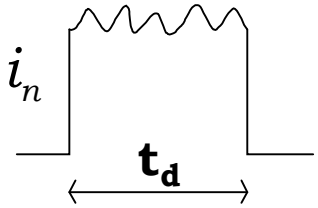
Deriving noise equation



Equivalent circuit



Voltage and timing



TR noise

1) Sampling noise of Switch

$$\left\langle v_n^2 \right\rangle = \frac{kT}{C_L}, \quad \delta_{t_d}^2 = \frac{\left\langle v_n^2 \right\rangle}{\left(\frac{I_D}{C_L}\right)^2} = \frac{kTC_L}{I_D^2}$$

2) Transistor noise

$$\delta t = \frac{C_L}{I_D}\delta v$$

Noise voltage of output by current noise

$$v_n = \frac{1}{C_L}\int_0^{t_d} i_n dt \qquad \delta_{t_d}^2 = \frac{C_L^2}{I_D^2}\delta_{vn}^2 = \frac{1}{I_D^2}\left\langle \left(\int_0^{t_d} i_n dt \right)^2 \right\rangle$$

$$\delta_{t_d}^2 = \frac{kTC_L}{I_{ds}^2}\left(\alpha\gamma\frac{V_{dd}}{V_{eff}} + 1\right)$$

$$\delta V_{in}^2 = \left(\frac{V_{eff}}{a}\frac{\delta_{td}}{t_d}\right)^2 = \frac{4kTV_{eff}^2}{a^2 C_L V_{dd}^2}\left(\alpha\gamma\frac{V_{dd}}{V_{eff}} + 1\right)$$

A. Matsuzawa," IEEE 8th International Conference on ASIC(ASICON), pp. 218-221, Oct. 2009.

Match with noise simulation

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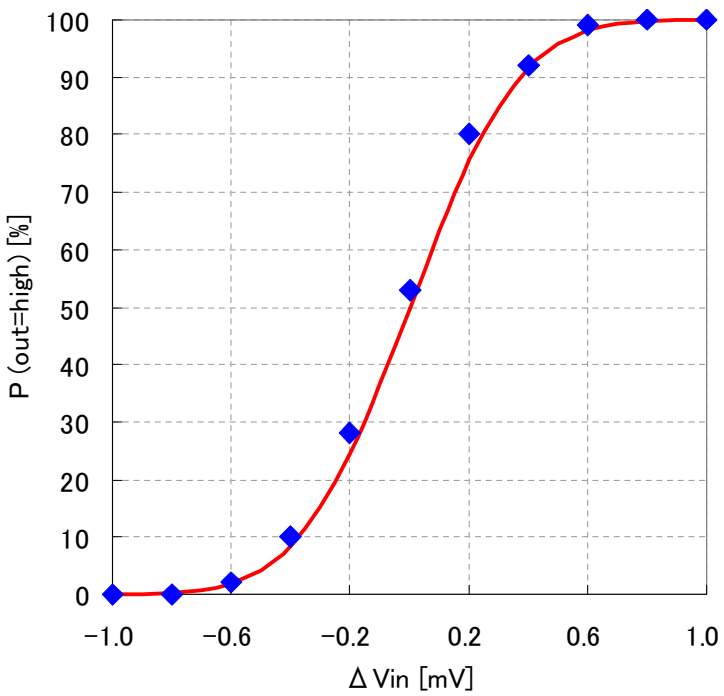
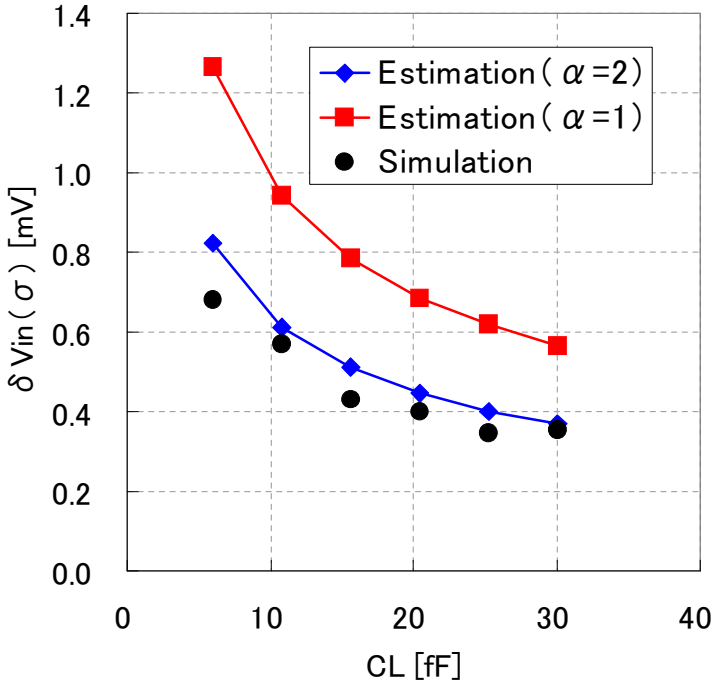
The derived equation has a good match with simulation.

$$\delta V_{in}^2 = \frac{4kTV_{eff}^2}{a^2 C_L V_{dd}^2}\left(a\gamma\frac{V_{dd}}{V_{eff}}+1\right)$$

Noise in comparator





Scalable P_d of SAR ADC

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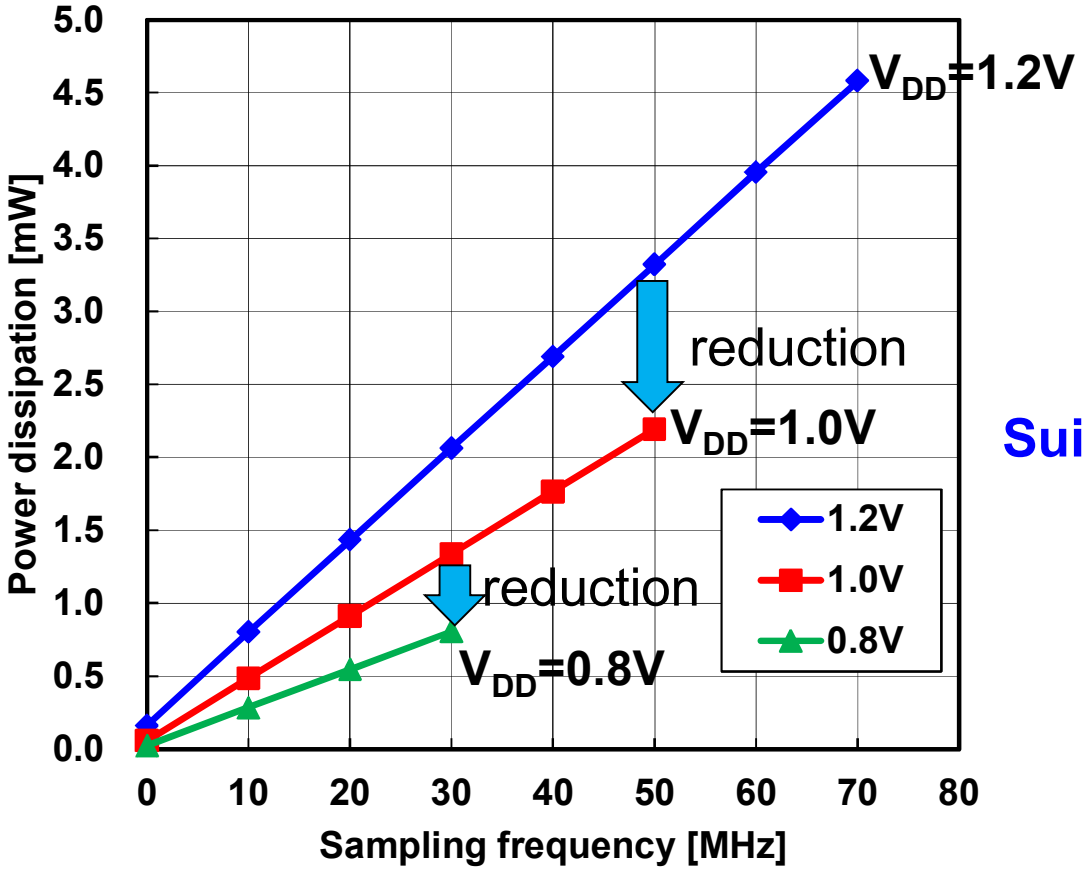
Pd of SAR ADC is proportional to the sampling frequency.
This nature is very suitable for IoT applications.
Very low power when the sampling frequency is low.



$$P_d \propto f_{clk} \cdot C V_{DD}^2$$

Like CMOS logic

Further Pd reduction
by low voltage operation

Suitable for IoT applications

50MSps: 2mW
5MSps: 200uW
500KSps: 20uW
50KSps: 2uW
5kSps: 0.2uW

S. Lee, A. Matsuzawa, et al., SSDM 2013

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Thermal noise limited ADC: SAR+DS ADC

SAR+DS ADC
using open-loop complete integrator
with dynamic amplifiers

M. Miyahara, A. Matsuzawa, CICC, 2-1, May. 2017.

Hybrid ADCs

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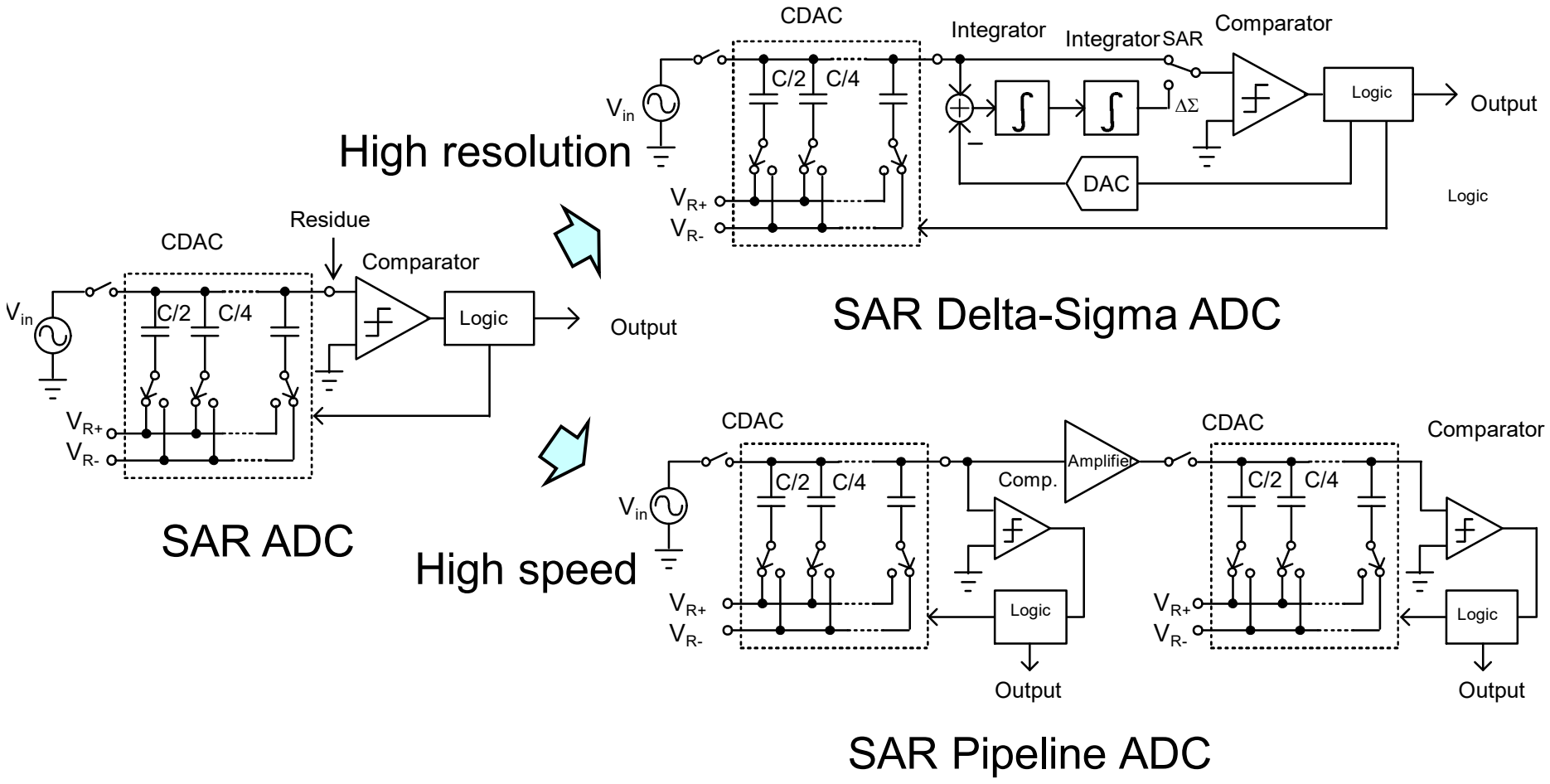
Recent ADC development trend is a hybrid architecture based on SAR ADC



SAR + Delta-Sigma ADC

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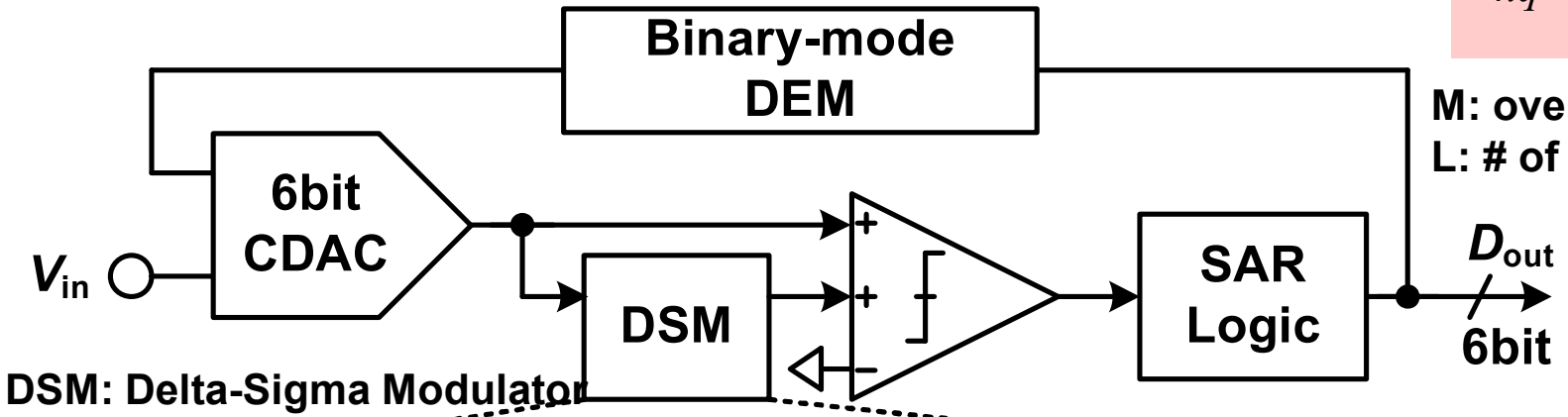
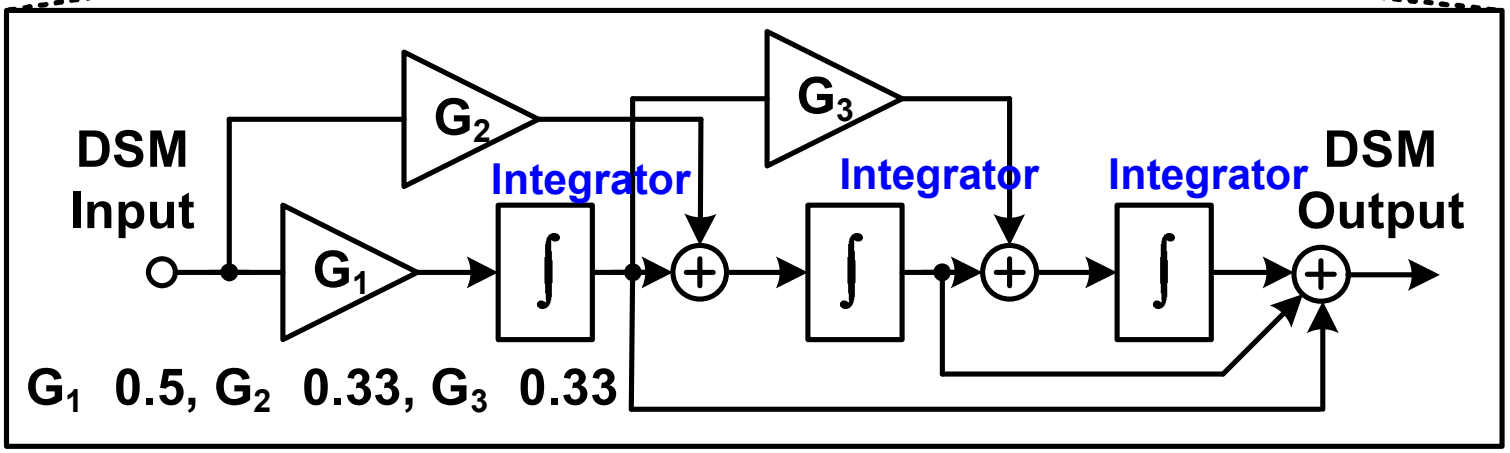
Further noise reduction is possible by delta-sigma modulation that uses integrators

However, integrator needs power hungry OPamp

$$v_{nq}^2 \propto \frac{1}{M^{2L+1}}$$

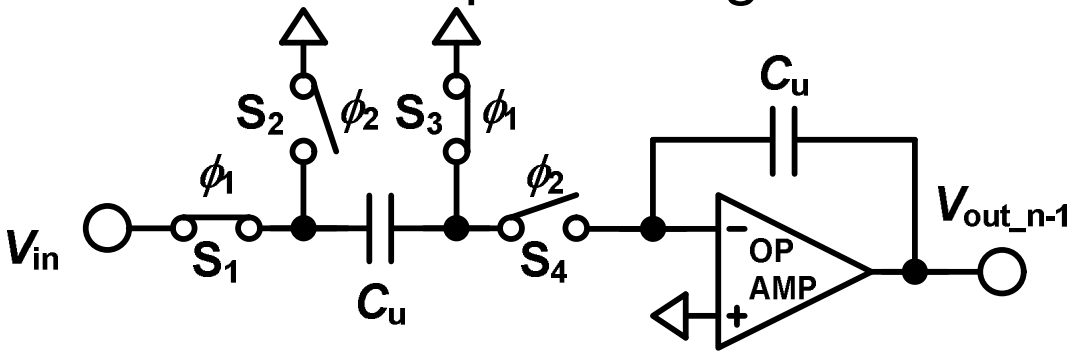
M: oversampling ratio
L: # of integrator





Proposed open-loop Integrator

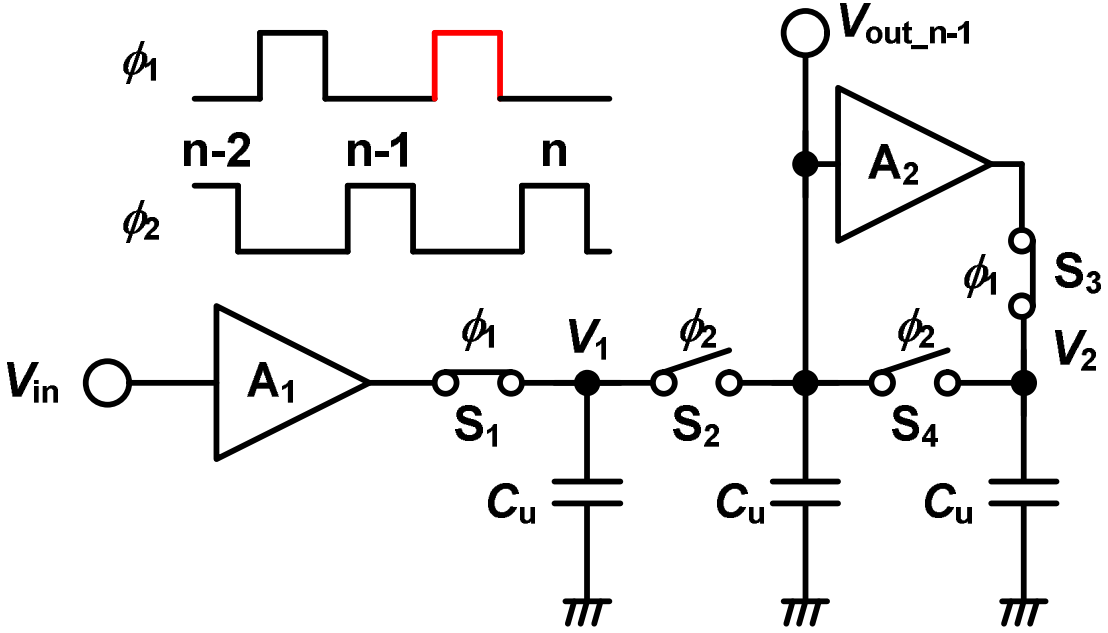
It can realize complete integration with minimum energy



Conventional closed-loop integrator

Phase: ϕ_1

$V_{out} = V_{out\_n-1}$



Proposed open-loop integrator

Phase: ϕ_1

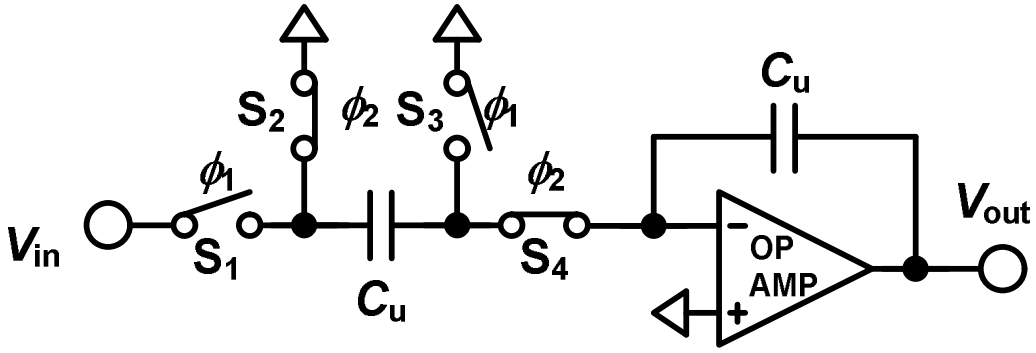
$V_{out} = V_{out\_n-1}$

$V_1 = A_1 V_{in}$

$V_2 = A_2 V_{out\_n-1}$

Proposed Open-loop Integrator

Open-loop integrator can realize complete integration with minimum energy



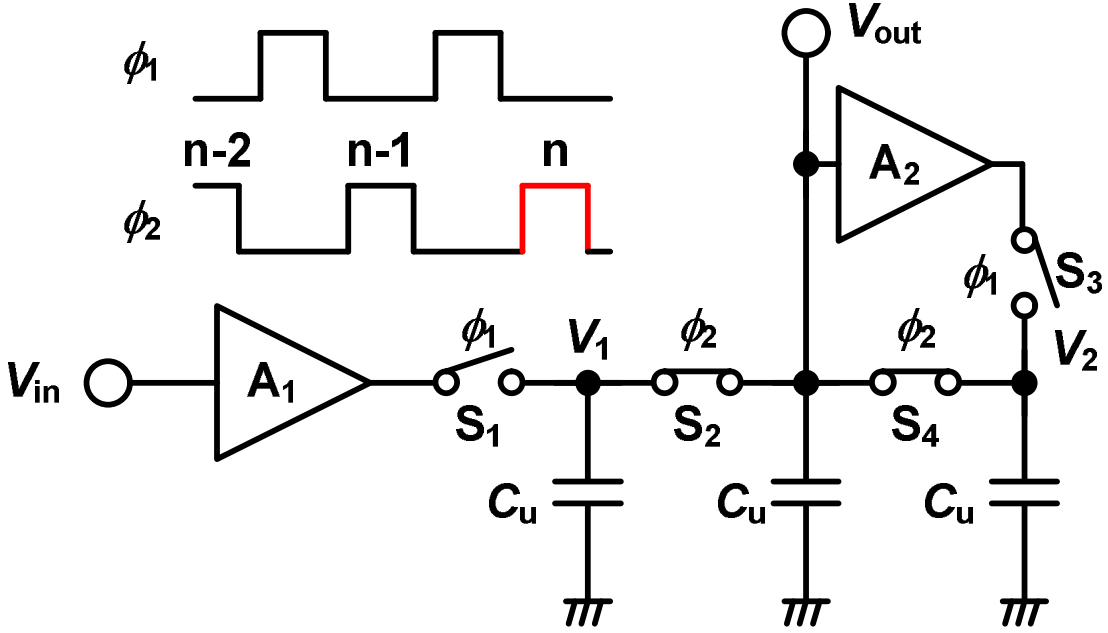
Conventional closed-loop integrator

Phase: ϕ_1

$V_{out} = V_{out\_n-1}$

Phase: ϕ_2

$V_{out} = V_{out\_n-1} + V_{in}$



Proposed open-loop integrator

Phase: ϕ_1

$V_{out} = V_{out\_n-1}$

$V_1 = A_1 V_{in}$

$V_2 = A_2 V_{out\_n-1}$

Phase: ϕ_2

$V_{out} = (V_{out\_n-1} + V_1 + V_2)/3$

$A_1 = 3$, $A_2 = 2$,

$V_{out} = V_{out\_n-1} + V_{in}$

Proposed dynamic amplifier

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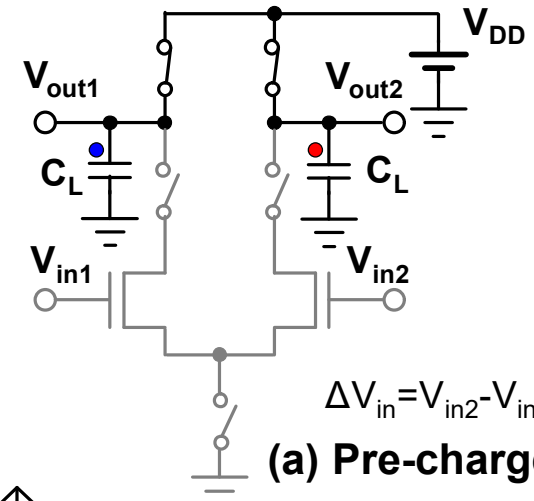
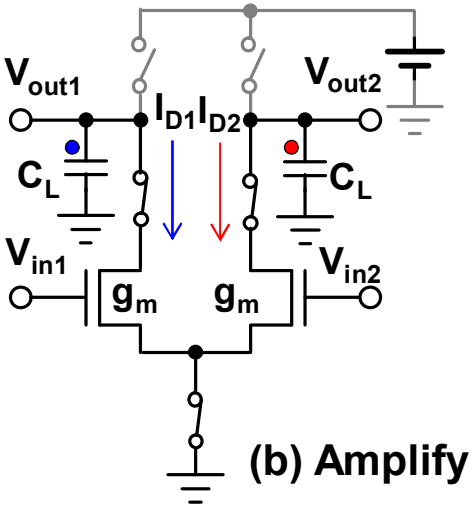
Dynamic amplifier does not require static current

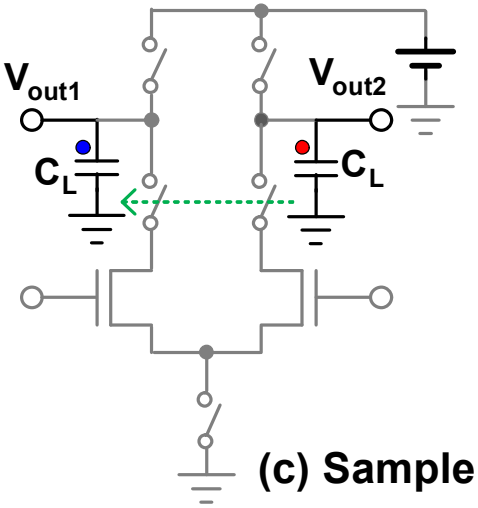
Ultimate low power, it consumes just wasted charge



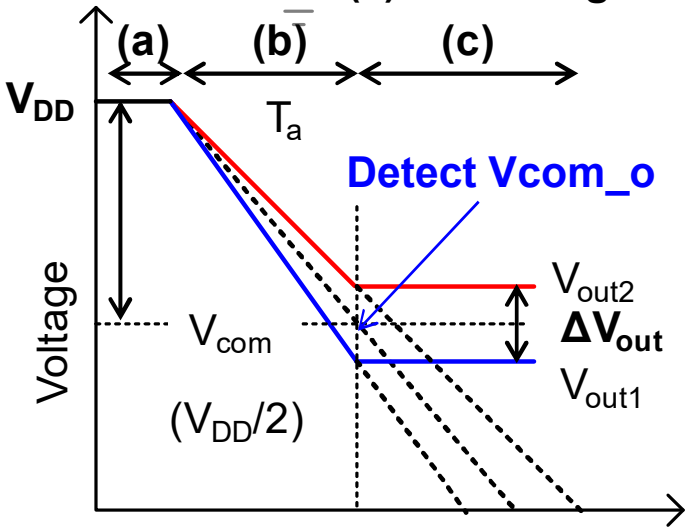
(a) Pre-charge



(b) Amplify



(c) Sample and hold



$$\Delta V_{out} = \frac{\Delta Q}{C_L} = \frac{\Delta I_D \cdot T_a}{C_L} = -\frac{g_m \Delta V_{in} \cdot T_a}{C_L}$$

$$T_a = \frac{C_L (V_{DD} - V_{com})}{I_{DA}} \qquad G_v \equiv \frac{\Delta V_{out}}{\Delta V_{in}} = -\frac{g_m \cdot T_a}{C_L} = -\frac{g_m \cdot (V_{DD} - V_{com})}{I_{DA}}$$

$$G_v = -\frac{2(V_{DD} - V_{com})}{V_{eff}}$$

Gain is almost determined by V_{DD}

J. Lin, A. Matsuzawa, ISCAS 2011.

Dynamic Amplifier Design

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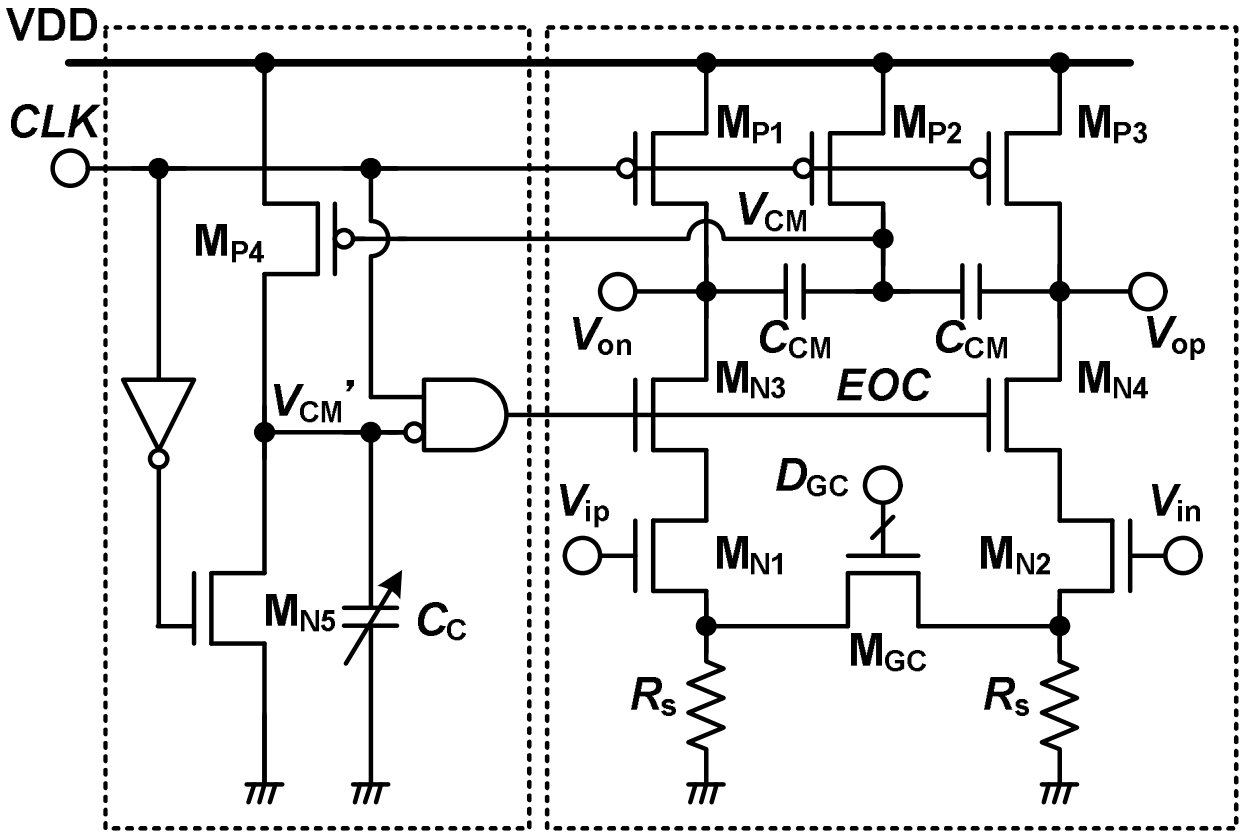
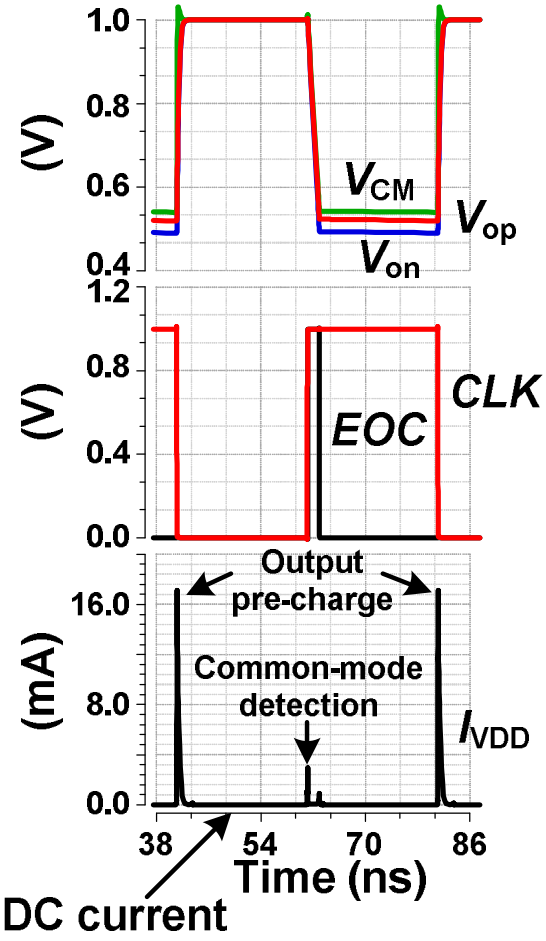
- No DC current and No timer
- Gain controllable 1.5x～4.5x, 5bit resolution





Dynamic amp. vs. OPamp.

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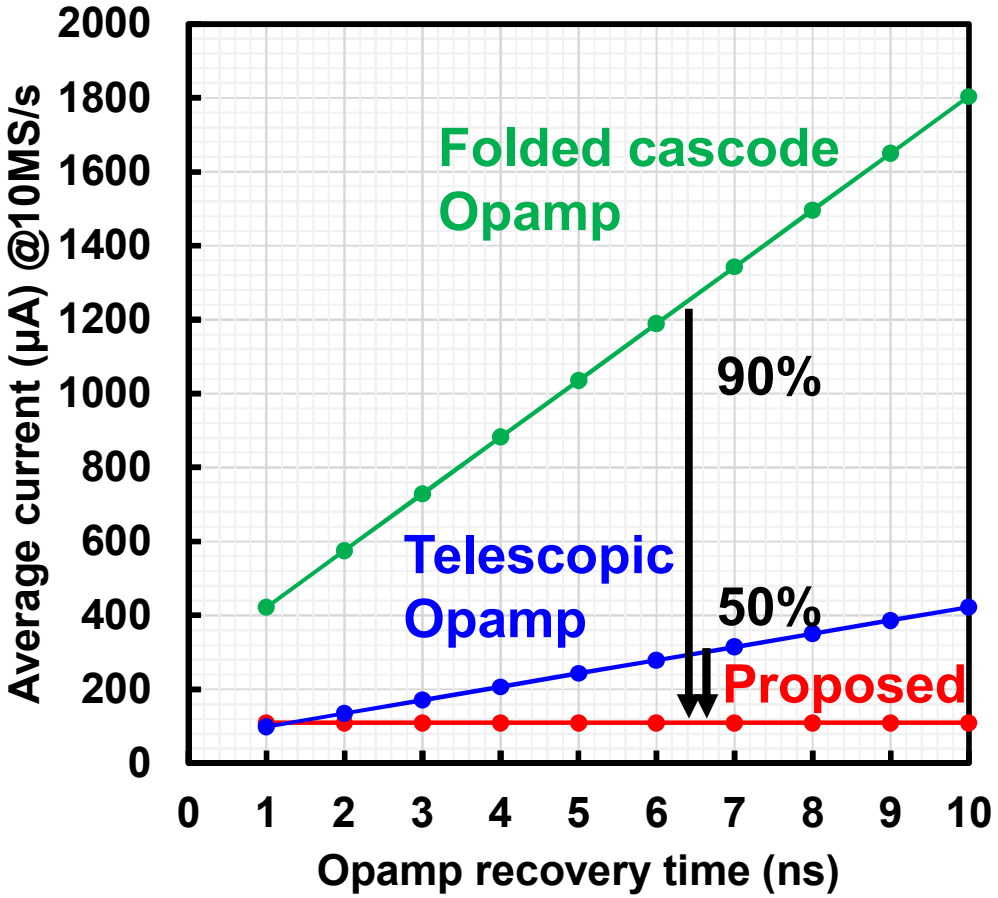
An OPamp-less integrator achieves 50~90% power reduction



	Proposed	Opamp
DC Gain(V/V)	3	100
# of unit	2	1
Integrator Type	Open	Closed
Integrator Output noise	100μV RMS	
Settling error	-	1%
Settling time	1.8ns	
Clock Freq.	150MHz	
Recovery time	None	1 CLK (6.7ns)

A. Matsuzawa, Tech Idea

Chip photo

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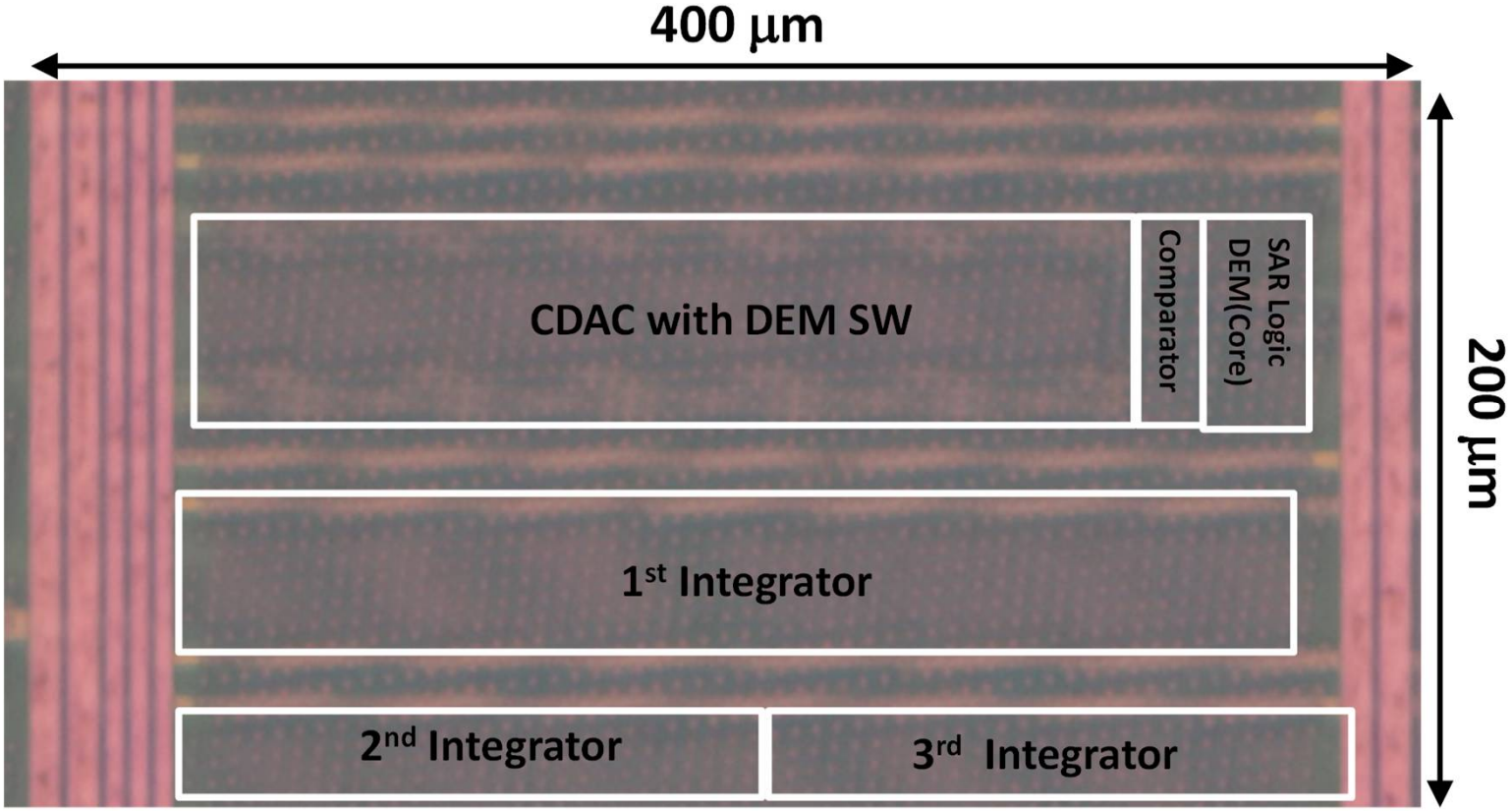
- 65nm 9M1P CMOS technology
- Chip area of 0.08mm^2



FFT Spectrum

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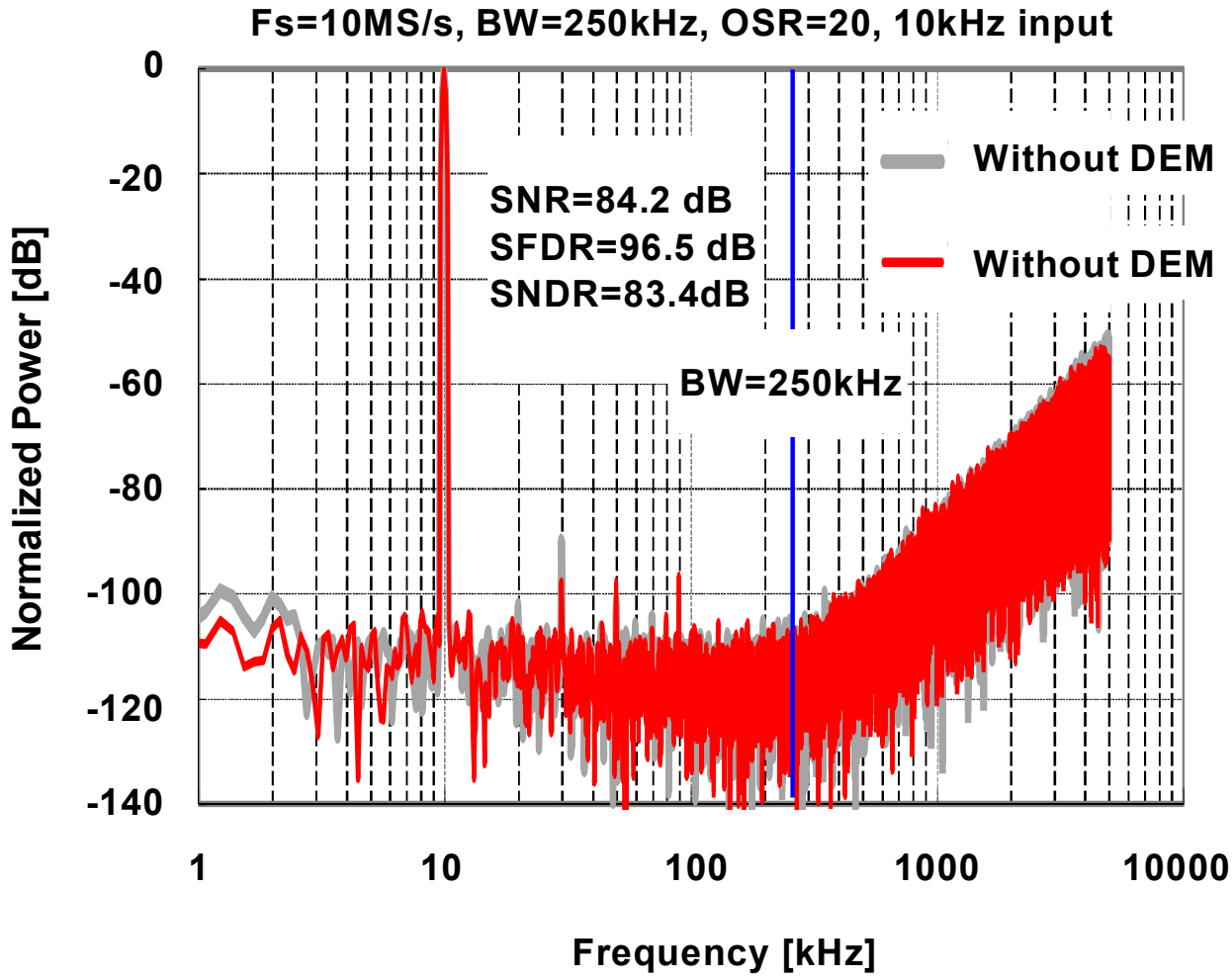
High SNDR of 84dB (V_n=24μV) is achieved



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Clock scalability

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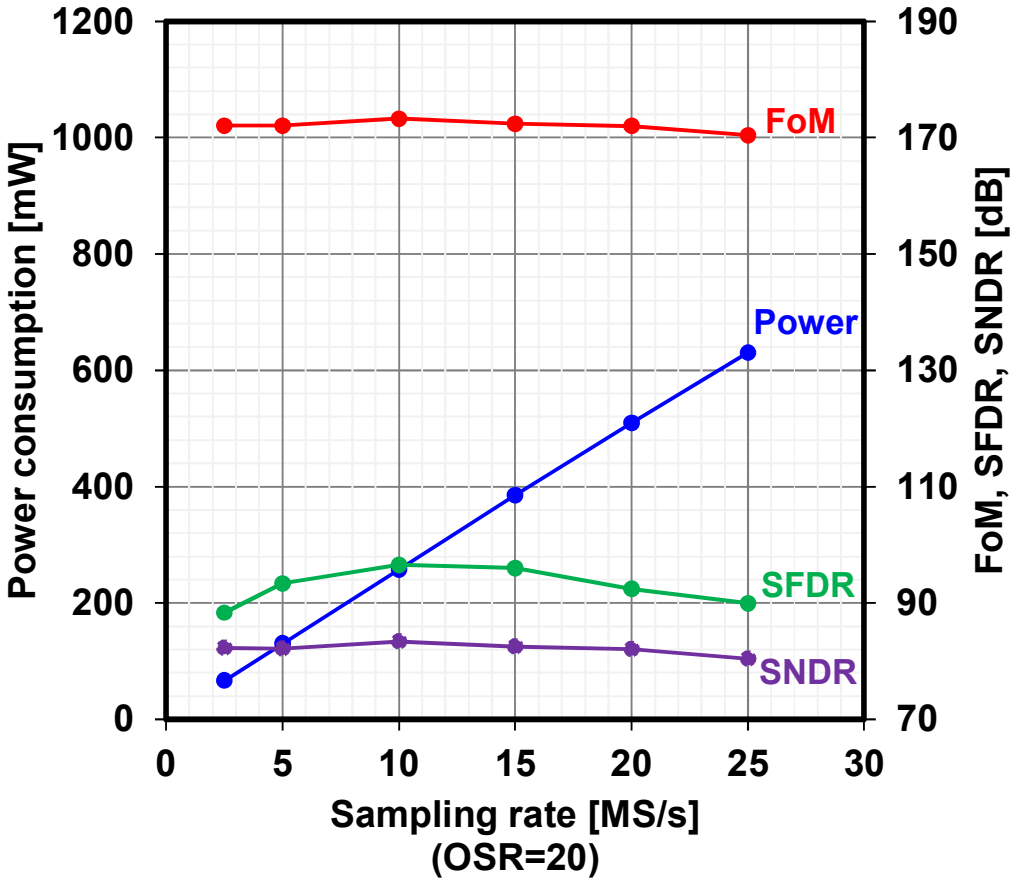
FoMs > 170 dB for different sampling rates of 2.5 - 25 MS/s.

Power of the dynamic amplifier is clock scalable

n=20

f_c=125kHz- 1.25MHz



P_c @ 10MS/s
Analog : 60.0μW (23.3%)
Ref : 35.1μW (13.6%)
Digital : 162.7μW (63.1%)

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Performance Summary

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The ADC has achieved high FoMs at the highest sampling rat

Recent noise shaping SAR ADC

	This Work			VLSI 2016 [3]		ISSCC 2016 [1]	ISSCC 2014 [2]
Architecture	NS SAR			NS SAR		NS SAR	NS SAR
Process [nm]	65			28		55	65
Active Area [mm^2]	0.08			0.116		0.072	0.18
Supply [V]	1.0			1.55/0.75	1.8/1.1	1.2	0.8
Sampling rate [MS/s]	2.5	10	25	0.1	1.0	1.0	0.128
BW [kHz]	62.5	250	625	2	20	4	16
SFDR [dB]	88.3	96.5	89.9	111.8	108.0	105.1	86.9
SNR [dB]	84.3	84.2	82.2	98.57	94.44	96.8	-
SNDR [dB]	82.3	83.4	80.4	97.99	93.95	96.1	76.1
Power [μW]	66.3	257.8	630.2	37.1	493.1	15.7	1.37
FoM [dB]	172.0	173.3	170.4	175.3	170.0	180.0	176.8

Performance

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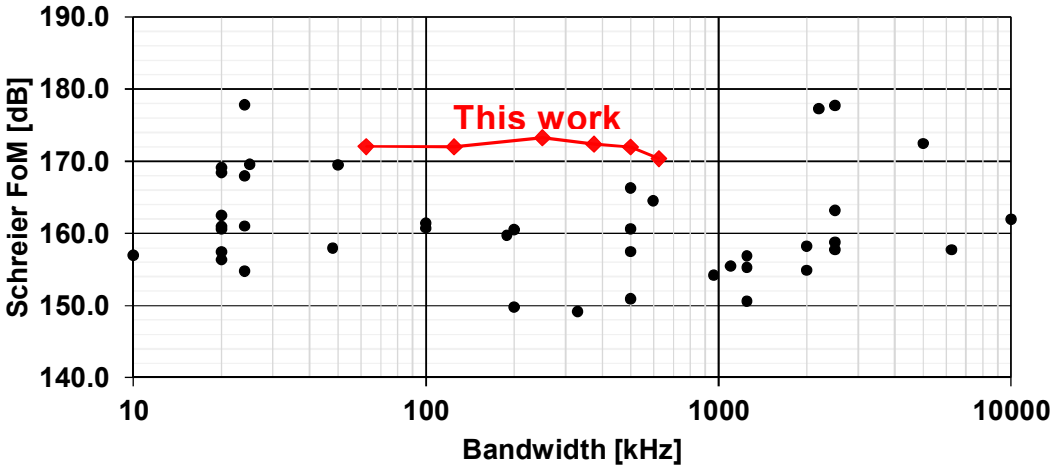
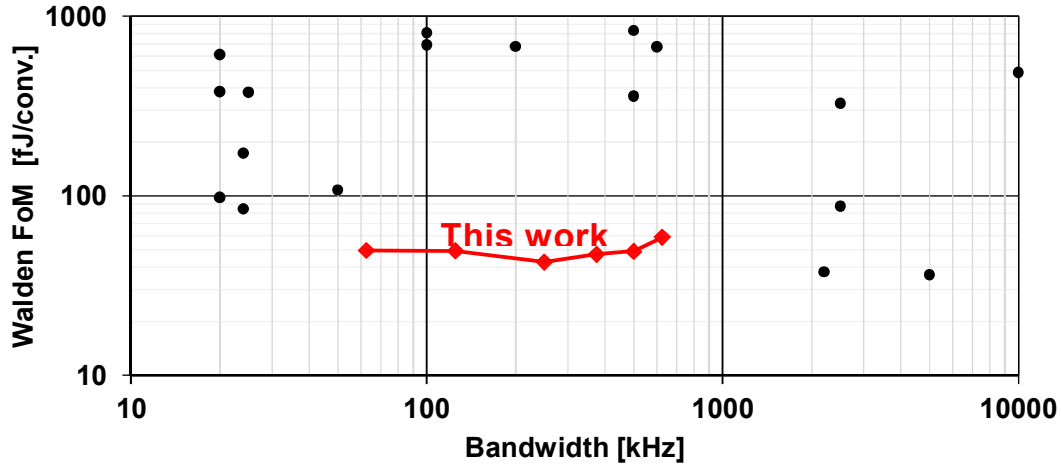
Highest FoMs and lowest FoMw from 50kS/s to 500kS/s

High SNDR of 83dB at 625KS/s P_d of 630uW was obtained



$$FoM_s(dB) = SNDR(dB) + 10\log\left(\frac{f_s/2}{P}\right)$$



$$FoM_W(J) = \frac{P_d}{f_s \times 2^{ENOB}}$$

Summary

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- Power break through often made new applications and markets. Current and future big market must be IoT systems.
- CMOS is ultimate logic circuit that doesn't consume any static power and no relation between speed and consumed energy.
  Small capacitance and low voltage operation are the key.
- ADC should consider accuracy, distortion, and noise. Furthermore, these factors essentially have tough tradeoff against low energy operation.
- CMOS technology conquered many drawbacks by using capacitance to realize S/H and to absorb mismatch voltage. Furthermore, CMOS enables use of digital compensation.
- Recent advanced ADC uses dynamic CMOS circuit more aggressively replaces conventional amplifier.