Low Power LSI Design
-- Featuring low power ADC design --

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A. Matsuzawa
Abstract

• I will discuss low power LSI design featuring low power ADC design.

• Power breakthrough often made new applications and markets, such as watch-like cellular phone, handy digital camera, and on-board DVD in notebook PC. Current and future big market must be the IoT systems.

• Logic circuit has progressed from fast but power hungry CML to CMOS that doesn't consume any static power and no relation between speed and consumed energy. Small capacitance and low voltage operation are the key.

• ADC plays an important role for all electrical systems, however unlike logic circuits; accuracy, distortion, and noise should be considered. Furthermore, these factors have tough tradeoff against low energy operation and conventionally uses OPamps that need static current.

• CMOS technology that had been regarded as not suitable for ADC application due to large mismatch, however conquered it by using capacitance to realize S/H and to absorb mismatch voltage.

• Recent advanced ADC uses dynamic CMOS circuit and more aggressively replaces conventional amplifier.

A. Matsuzawa
Contents

- Low power digital LSI design
- Progress of video-rate ADC
  - History of video-rate ADC
- Advanced ADC design
  - Mismatch limited ADC: Flash ADC
  - Thermal noise limited ADC
    SAR ADC and SAR+Delta-Sigma ADC
Low power digital LSI design
Progress of logic circuit and devices

Logic circuit and device have been progressed to no static current for low power consumption

CML

E/D NMOS

CMOS

Bipolar

DMOS

PMOS

Static current

Static current

No static current

Main frame
1960-1990

PC
1970-1985

Watch, Calculator, PC, Every thing
1970-Present

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Feature of CMOS logic circuit

Large dynamic current is needed to reduce logic delay. However, lost energy is not determined by the current, but electrical energy. This means CMOS can realize high speed and low energy circuit.

No static current can realize low power circuit, basically.

Delay time

\[ t_{pdr} = \frac{C V_{DD}}{2 I_{DP}} \]

\[ t_{pdf} = \frac{C V_{DD}}{2 I_{DN}} \]

Consumed energy

\[ E_d = C V_{DD}^2 \]

\[ P_d = f C V_{DD}^2 \]

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Low power digital LSI design

Power dissipation can be reduced to 1/10

Clock circuit (Flip Flop) consumes power of 75% of total $P_d$ in this LSI.

- F/F reduction
- Gated CLK
- Volt. lowering 3.0V->1.5V
- Cap. Lowering (0.6)

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Reconsider Flip Flop circuits

We can reduce power consumption by reconsidering F/F circuit.

\[ P_d \text{ of } 1/2 \text{ or } 1/3 \text{ is possible} \]

By reducing gate capacitance to the clock

Data activation: 25%

(a) Conventional type

(b) Differential type

(c) Memory type

A. Matsuzawa
DSP with adaptive supply voltage control

We developed low power DSP using adaptive supply voltage control technique that was early work of DVFS technique

S. Sakiyama and A. Matsuzawa, Symp. on VLSI Circuits 1997

A. Matsuzawa

Adaptive supply voltage control circuits

On chip DC/DC

0.35umCMOS
2.2M Tr
20MIPS
12mW (1.2V, internal)

leakage current
500uA: active
1uA: standby
Adaptive supply voltage

Supply voltage can be reduced with the reduction of clock freq. This makes more aggressive power reduction.

\[ E_d = CV_{DD}^2 \]
\[ P_d = fCV_{DD}^2 \]

![Graph showing power dissipation vs. operating frequency for fixed and adaptive supply voltages.](image)

- Fixed supply voltage
  - \( V_{tn} = 0.6V \)
  - \( V_{tp} = -0.7V \)
  - Operating frequency (MHz)
  - Power dissipation (mW)
- Adaptive supply voltage
  - Low VT transistors
  - (1.0V -- 2.2V)
  - \( V_{tn} = 0.30V \)
  - \( V_{tp} = -0.33V \)

A. Matsuzawa
Find minimum operating voltage

Feedback loop can find minimum operating voltage by using replica delay that satisfies required $T_{pd}$ for critical path in the DSP.
World’s first watch-like cellular phone

We developed the world’s first watch-like cellular phone using developed low power DSP

This cellular phone was used in Nagano winter Olympic game (1998)

12mW @20MHz 0.35um DSP
We developed wireless PDA using FD-SOI that can operate with ambient energy. This is an early work for IoT.

Douseki, A. Matsuzawa, ISSCC2003,

Generate 1.7mW/0.7V

A. Matsuzawa
Progress of video-rate ADC

History of video-rate ADC

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Progress of video-rate ADC

- **Module**
  - NO precision monolithic IC technology

- **Flash: Bipolar technology**
  - Only bipolar has low mismatch voltage
  - CMOS has large mismatch voltage

- **Two-step flash: Bi-CMOS technology**
  - Two-step flash can reduce power, but needs S/H
  - CMOS S/H + Bipolar comparator

- **Two-step flash: CMOS technology**
  - Chopper inverter comparator can realize high precision comparator and also S/H circuit
  - Capacitive interpolation method reduce error and power more

- **Gate-weighted interpolated flash: CMOS technology**
  - Gate-weighted linear region MOS + dynamic flip/flop (No static current)

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Development start for digital TV&VTR

In 1979, Panasonic (松下電器) succeeded in development of 6 hour VHS and became world’s No.1 VTR supplier. The video equipment used high level analog technology. The development project for digital TV& VTR has started.
Video-rate ADC at 40 year before

Video-rate ADC was very expensive and power hungry module when I started development of video-rate ADC IC in 1980.

There was no monolithic video-rate 10b ADC at that time

10bit 14.3MHz ADC

Almost same price as a small car!

10,000 USD
20W

Analog Devices Inc.

A. Matsuzawa
The world’s first video-rate 10bit ADC

We developed the world’s first video-rate 10bit ADC IC using bipolar technology.

Price and lower dissipation are reduced by 1/10

The ADC was used in professional digital TV and video systems.

T. Takemoto and A. Matsuzawa,

IR100 Award

Flash ADC

Bipolar (3um)
10b, 20MS/s,
2W
$ 800

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Why Bipolar, not CMOS?

Only bipolar can satisfy the target of mismatch voltage.

Mismatch voltage should be L.T. 0.2mV

MOS: several mV to several 10mV

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Two step flash ADC

Can be reduced by \(1/16\), but needs S&H

<table>
<thead>
<tr>
<th>Signal</th>
<th>1st conversion</th>
<th>2nd conversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 (3)</td>
<td>12 (3)</td>
<td>12 (3)</td>
</tr>
<tr>
<td>8 (2)</td>
<td>8 (2)</td>
<td>8 (2)</td>
</tr>
<tr>
<td>4 (1)</td>
<td>4 (1)</td>
<td>4 (1)</td>
</tr>
<tr>
<td>0 (0)</td>
<td>0 (0)</td>
<td>0 (0)</td>
</tr>
</tbody>
</table>

Bipolar can’t realize S&H, due to base current

Circuit size

\[
n = 2^M + 2^{N-M} \rightarrow 2^{\left(1+\frac{N}{2}\right)} \quad @ \quad M = \frac{N}{2}
\]

10bit Flash ADC: \(2^{10} = 1024\)

10bit two step ADC: \(2^6 = 64\)

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Bi-CMOS two step ADC

Bi-CMOS technology can realize MOS input OPamp for sample and hold to realize two step flash ADC.

10b, 30MSps, 800mW

Bi-CMOS S&H

A. Matsuzawa, ISSCC 1990.

World first’s home HDTV

A. Matsuzawa
Multi-step conversion can reduce circuit size and power consumption. However, apt to cause large conversion error, due to stringent matching between the coarse conversion and fine conversion.

1st: Coarse conversion
2nd: Fine conversion

Fixed scale causes conversion error

No conversion error

Conversion error

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Interpolation can realize smooth connection between 1\textsuperscript{st} and 2\textsuperscript{nd} conversion area, as a result, small DNL can be achieved.

Output voltages are divided equally by resistors

As if spring coil

Equally divide of 1\textsuperscript{st} conversion area

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Addition of weighted two signal makes internal division point. Using this method, we can realize A/D conversion without reference voltage.

**Internal division**

\[ x = \frac{na + mb}{m + n} \]

Weight of \( \frac{n}{m + n} \) for signal a  
weight of \( \frac{m}{m + n} \) for signal b

And sum them

**Our proposed interpolation techniques**

- Resistive interpolation: using resistors
- Capacitive interpolation: using capacitors
- Gate weighed interpolation: conductance of linear region
- Time interpolation: using delay elements

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CMOS comparator (33 year ago) had not good performance to the bipolar comparator. **Mismatch was 20 times larger** and consumed large power. Conventionally larger size is needed to reduce the mismatch.


Gate area vs. mismatch

$$\Delta V_T(mV)$$

$$\delta_{VT(LW)}$$

$$\Delta V_T \propto \frac{T_{ox}}{\sqrt{LW}}$$

$$LW(\mu m^2)$$

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Chopper CMOS comparator

Invention of CMOS chopper inverter comparator realized high resolution and low power CMOS ADC.

V_{dd}

0

V_{sig}

\( V_{g} = V_{\text{diode}} \)

\( V_{\text{out}} \)

1) absorbs mismatch voltage
2) Sample & Hold
3) Auto level shift

1) Amplifier
2) Self bias
3) Simple and low voltage

Signal tracking

Sample and amplify

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Chopper inverter comparator

\( V_{\text{out}} = G(V_{\text{sig}} - V_{\text{ref}}) + V_{\text{diode}} \)
Ultra low power Video-rate 10b CMOS ADC

The ADC demonstrated superiority of CMOS technology in ADC. Since then, all ADCs use CMOS technology and no use of bipolar. Consumed energy is $1/8$ to other ADCs. FoM of ADC was invented to show the significance of this development.

K. Kusumoto and A. Matsuzawathe.

ISSCC '93, JSC 1993.

A. Matsuzawa
Capacitive interpolation

Chopper comparator had a accuracy limitation of 8bit. We invented capacitive interpolation and realized ultra low power CMOS video-rate 10bit ADC

Absorb mismatch by interpolation

K. Kusumoto and A. Matsuzawa

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Early stage mixed signal LSI

Success of CMOS video-rate ADC triggered the development of LSI for portable AV equipment; Handy digital video.


This paper triggered the low power electronics
Error rate in DVD recorder is quite high due to low SNR. High speed DSP is needed for waveform equalizer and error correction. This means an ultra-high speed (400MS/s) ADC is required.
Development of high speed CMOS ADC

Huge power reduction is needed to realize consumer products

World’s fastest 6b ADC at 1991, Bipolar

- 6b, 1GHz ADC
- 2W
- 1.5um Bipolar

A. Matsuzawa, ISSCC 1991

World’s fastest CMOS ADC at 2000

- 6b, 800MHz ADC
- 400mW, 2mm²
- 0.25umCMOS


Pd is down to 1/8 with keeping speed

- 7b, 400MHz ADC
- 50mW, 0.3mm²
- 0.18umCMOS


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Gate weighted interpolation with dynamic comparator

Interpolation is realized using the additivity of drain conductance in MOS linear region. Very low power due to dynamic action of MOS Latch. Input referred mismatch can be reduced using distributed pre-amplifiers.

\[
G_1 = K_p \left[ \frac{W_1}{L} (V_{in1+} - V_{th}) + \frac{W_2}{L} (V_{in2+} + V_{th}) \right]
\]

\[
G_2 = K_p \left[ \frac{W_1}{L} (V_{in1-} - V_{th}) + \frac{W_2}{L} (V_{in2-} + V_{th}) \right]
\]

if \( W_1 : W_2 = \frac{m-n}{m} : \frac{n}{m} \)

then, \( (m-n)V_{in1+} + nV_{in2+} = (m-n)V_{in1-} + nV_{in2-} \)

No static current

7b, 400MHz ADC
50mW, 0.3mm\(^2\)
0.18um CMOS

Gate weighted interpolator

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The world’s first fully integrated SoC for DVD

We developed the world’s first mixed signal SoC for DVD that can integrate full DVD system.


We developed the world’s first mixed signal SoC for DVD that can integrate full DVD system.
The effect of Fully integrated SoC

Developed fully integrated SoC can reduce the # of components drastically. It contributed increase of performance and reliability, reduction of product cost and system space. It enabled on-board DVD system in note PC.

SoCs for DVD shipped **520 M chips** and the total sales is **2.5 Billion USD.**
Advanced ADC design

Discussion in recent low power and high performance ADC design
Typical ADC architectures

Flash, SAR, Pipelined, and $\Delta\Sigma$ are the major ADC architectures.

(a) Parallel (Flash)

(b) Successive Approximation Register (SAR)

(c) Pipelined

(d) $\Delta\Sigma$

A. Matsuzawa, Tech Idea
ADC architecture and performance

SAR ADC and $\Delta\Sigma$ ADC are the dominant architecture

For the sensor applications

$1kHz < f_c < 10MHz$

$10\mu V < V_n < 200\mu V$

$10\text{bit} < N < 18\text{bit}$

A. Matsuzawa, Tech Idea
Basic idea for advanced ADC design

Challenge to design of ADC circuit like CMOS logic

No or less static current, minimum capacitance.
Power should be proportional to clock frequency.

CML logic and conventional amplifier

\[ V_{DD} \]
\[ R_L \]
\[ V_{i+} \]
\[ V_{o-} \]
\[ C_L \]
\[ I_s \]

Consume static current
Should increase current to increase speed.

CMOS logic

\[ E_d = C_L V_{DD}^2 \]
\[ P_d = fE_d = fC_L V_{DD}^2 \]

\[ f_{togle} \propto \frac{1}{R_o C_L} \]

No static current
No need to increase current to increase speed.

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Advanced ADC design

• Mismatch limited ADC architecture: flash ADC
  – Use dynamic comparator
  – Transistor and circuit should be small as possible
  – Mismatch increase with decreasing transistor size
  – Compensate mismatch by digital calibration method

• Thermal noise limited ADC architecture: SAR
  – Use minimum capacitance determined by thermal noise
  – Use no or less static current circuit
  – Compensate capacitance and MOS mismatch by digital calibration
  – Use low-noise dynamic comparator
  – Delta-sigma method should be used for further noise reduction
  – Open-loop integrator with dynamic amplifier can realize low energy and high speed complete integrator

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Mismatch limited ADC: Flash ADC

A. Matsuzawa
Developing baseband SoC

Developed chip for 60GHz transceiver integrating ADC, DAC, VGA, and PLL, using 40nm CMOS technology.

RX: 300mW, TX: 110mW
40nm CMOS technology


ADC 5b, 2.3GSps, 12mW/ch

A. Matsuzawa
Analog Baseband : ADC

M. Miyahara and A. Matsuzawa, et al., RFIC 2012.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VGA Gain range</td>
<td>0-40 dB</td>
</tr>
<tr>
<td>ADC Resolution</td>
<td>5 bit</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>2304 MS/s</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>VGA : 9 mW, ADC : 12 mW*</td>
</tr>
<tr>
<td>DNL, INL</td>
<td>&lt; 0.8 LSB</td>
</tr>
<tr>
<td>SNDR</td>
<td>26.1 dB</td>
</tr>
<tr>
<td>FoM of ADC</td>
<td>316 fJ/conv.-s</td>
</tr>
</tbody>
</table>

*single channel inc. S/P
Flash ADC design

Offset mismatch determines the effective resolution. Thermal noise can be neglected because of low resolution.

Reduction of ENOB by mismatch

\[ \Delta \text{ENOB} = \frac{1}{2} \log_2 \left( 1 + 12 \left( \frac{V_{\text{off}}(\sigma)}{V_q} \right)^2 \right) \]

Effective Number of Bit

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Strategy for low energy flash ADC

Small area is required to reduce energy, but increases mismatch. Therefore, (digital) mismatch reduction technique should be applied.

\[ FoM_w = \frac{P_d \cdot 2^{\Delta ENOB}}{f_c \cdot 2^N} \]

Small transistor increases mismatch

Mismatch should be reduced from 20mV to 3mV

\[ V_{\text{offset}}(\sigma) \propto \frac{1}{\sqrt{LW}} \quad E_c \propto C_c \propto LW \]

Small area realizes low energy

Published 5b, 6b ADC

Target 3mV

\[ E_c = 50\text{fJ} \]
Mismatch compensation for the dynamic comparator

Mismatch can be compensated by capacitance or current

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Digital calibration methods for mismatch

Resistor ladder type

Capacitor array type

Current calibration

Capacitance calibration

K to $2^K$ Decoder

Y. Asada, K. Yoshihara, T. Urano, M. Miyahara and A. Matsuzawa,


A. Matsuzawa
Comparator with digital mismatch compensation

Area for digital compensation can be reduced by tech. scaling.

A. Matsuzawa
The mismatch voltage can be reduced from 14mV to 1.7mV.


A. Matsuzawa
Thermal noise limited ADC: SAR ADC

S. Lee, A. Matsuzawa, et al., SSDM 2013

A. Matsuzawa
SAR ADC is the lowest energy ADC architecture.
Conversion energy of SAR ADC has decreased rapidly. 1/1000 has been achieved in recent 12 years.

\[ FoM = \frac{P_d}{f_s \times 2^{N'}} \]

(Jour)

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1/1000 in 12 years

N': Effective # of bit

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Theory: SNR and consumed energy

Signal and noise in ADC

Thermal noise

Input signal

Quantization noise

Thermal equilibrium

Electrical energy=Thermal energy

Signal

Capacitor

Track

S & H circuit

Hold

Quantization voltage

$$V_q = \frac{V_{FS}}{2^N}$$

V_{FS}: Full scale voltage
N: Resolution

Quantization noise

$$P_{nq} = \frac{1}{3} \left( \frac{V_q}{2} \right)^2 = \frac{V_{FS}^2}{12 \cdot 2^{2N}}$$

Thermal noise

$$P_{nt} = m \frac{kT}{C}$$

m: # of noise source

Required capacitance

$$C = 12mkT \cdot 2^{2N}$$

$$P_{nq} = P_{nt}$$

Consumed energy

$$E_w = 2C \left( \frac{V_{FS}}{2} \right)^2 = 6mkT \cdot 2^{2N} \approx 5 \times 10^{-20} \times 2^{2N} (J)$$

$$E_w = 10 \left( \frac{SNR(dB)-190}{10} \right) (J)$$

A. Matsuzawa
Theoretical trend has good agreement with experimental data.

Consumed energy is proportional to SNR

\[ E_w = 10 \left( \frac{SNR(dB) - 190}{10} \right) (J) \]

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SAR ADC

SAR ADC can be composed with no circuit that flows static current

- No resistance
- No OPamp
- No static current

Sample

\[ Q = -CV_{in} \]

Voltage generation by CDAC

\[ V_x = -(V_{sig} - a \cdot V_{ref}) \]

\[ V_x = (1-a)C \]

0 < a < 1

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Capacitive DAC

Dynamic comparator

CMOS logic

Switch

S_0

V_{ref}

V_{in}

S_11

S_12

S_13

S_14

S_15

S_2

\[ C/2 \]

\[ C/4 \]

\[ C/8 \]

\[ C/16 \]

\[ C/16 \]
To address capacitor mismatch

Use small capacitor that satisfies the thermal noise limit.

Capacitor mismatch should be compensated digitally.

A. Matsuzawa
Use of MOM capacitor

MOM capacitor uses the capacitance between the lateral interconnection. The capacitor density can be increased by technology scaling. Smaller occupied area (same C) can be expected by technology scaling. Furthermore, parasitic capacitance can be controlled.
Effect of comparator noise to SAR ADCs

A comparator has noise and this results in conversion error. Comparator noise determines SNR of SAR ADC.


A. Matsuzawa
Invention of low noise dynamic comparator

We invented low noise dynamic comparator. 10 bit is a max. resolution when using conventional comparator. But this comparator can realize 12 bit resolution.

This paper has been cited more than 200 and becomes major comparator.

\[
\bar{v}_{ni}^2 = \frac{kT\gamma}{C_L} \frac{V_{eff}}{V_{os}}
\]


A. Matsuzawa
A dynamic comparator is widely used to reduce static power.

The difference in input voltages causes a difference in discharging speed.

Deriving noise equation

1) Sampling noise of Switch

\[ \langle v_n^2 \rangle = \frac{kT}{C_L}, \quad \delta_{td}^2 \frac{\langle v_n^2 \rangle}{\langle v_{in}^2 \rangle} = \frac{kTC_L}{I_D^2} \]

2) Transistor noise

\[ \delta_t = \frac{C_L}{I_D} \delta v \]

\[ \delta t_d = \frac{C_L^2}{I_D^2} \delta t_m \]

\[ \delta_{td} = \frac{kTC_L}{I_D^2} \left( \alpha \gamma \frac{V_{dd}}{V_{eff}} + 1 \right) \]

\[ \delta V_{in}^2 = \left( \frac{V_{eff}}{a} \frac{\delta_{td}}{t_d} \right)^2 = \frac{4kTV_{eff}^2}{a^2 C_L V_{dd}^2} \left( \alpha \gamma \frac{V_{dd}}{V_{eff}} + 1 \right) \]

Match with noise simulation

The derived equation has a good match with simulation.

\[ \delta V_{in}^2 = \frac{4kTV_{eff}^2}{\sigma^2 C_L V_{dd}^2} \left( aV \frac{V_{dd}}{V_{eff}} + 1 \right) \]

Noise in comparator
Scalable $P_d$ of SAR ADC

$P_d$ of SAR ADC is proportional to the sampling frequency. This nature is very suitable for IoT applications. Very low power when the sampling frequency is low.

**Like CMOS logic**

Further $P_d$ reduction by low voltage operation

Suitable for IoT applications

- 50MSps: 2mW
- 5MSps: 200uW
- 500KSp: 20uW
- 50KSp: 2uW
- 5kSp: 0.2uW

S. Lee, A. Matsuzawa, et al., SSDM 2013
Thermal noise limited ADC: SAR+DS ADC

SAR+DS ADC
using open-loop complete integrator
with dynamic amplifiers

Recent ADC development trend is a hybrid architecture based on SAR ADC

SAR ADC

High speed

SAR Delta-Sigma ADC

High resolution

SAR Pipeline ADC

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SAR + Delta-Sigma ADC

Further noise reduction is possible by delta-sigma modulation that uses integrators.

However, integrator needs **power hungry OPamp**

\[
V_{nq}^2 \propto \frac{1}{M^{2L+1}}
\]

M: oversampling ratio
L: # of integrator

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Proposed open-loop Integrator

It can realize complete integration with minimum energy

\[ V_{out} = V_{out\_n-1} \]

**Phase:** \( \phi_1 \)

**Conventional closed-loop integrator**

\[ V_{2} = A_2 V_{out\_n-1} \]
\[ V_{1} = A_1 V_{in} \]

**Proposed open-loop integrator**

A. Matsuzawa
Proposed Open-loop Integrator

Open-loop integrator can realize complete integration with minimum energy.

**Proposed Open-loop Integrator**

\[ V_{\text{out}} = V_{\text{out}_{n-1}} + V_{\text{in}} \]

**Phase: \( \phi_1 \)**

\[ V_{\text{out}} = V_{\text{out}_{n-1}} \]

**Phase: \( \phi_2 \)**

\[ V_{\text{out}} = V_{\text{out}_{n-1}} + V_{\text{in}} \]

**Conventional closed-loop integrator**

**Proposed open-loop integrator**

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Proposed dynamic amplifier

Dynamic amplifier does not require static current
Ultimate low power, it consumes just wasted charge

\[
\Delta V_{in} = V_{in2} - V_{in1}
\]

(a) Pre-charge

(b) Amplify

(c) Sample and hold

\[
\Delta V_{out} = \frac{\Delta Q}{C_L} = \frac{\Delta I_D \cdot T_a}{C_L} = g_m \Delta V_{in} \cdot T_a
\]

\[
T_a = \frac{C_L (V_{DD} - V_{com})}{I_{DA}}
\]

\[
G_v = \frac{2 (V_{DD} - V_{com})}{V_{eff}}
\]

Gain is almost determined by \(V_{DD}\)

J. Lin, A. Matsuzawa, ISCAS 2011.
Dynamic Amplifier Design

- No DC current and No timer
- Gain controllable 1.5x ~ 4.5x, 5bit resolution

A. Matsuzawa, Tech Idea
Dynamic amp. vs. OPamp.

An OPamp-less integrator achieves 50~90% power reduction

<table>
<thead>
<tr>
<th></th>
<th>Proposed</th>
<th>Opamp</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain (V/V)</td>
<td>3</td>
<td>100</td>
</tr>
<tr>
<td># of unit</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Integrator Type</td>
<td>Open</td>
<td>Closed</td>
</tr>
<tr>
<td>Integrator Output noise</td>
<td>100μV RMS</td>
<td></td>
</tr>
<tr>
<td>Settling error</td>
<td>-</td>
<td>1%</td>
</tr>
<tr>
<td>Settling time</td>
<td>1.8ns</td>
<td></td>
</tr>
<tr>
<td>Clock Freq.</td>
<td>150MHz</td>
<td></td>
</tr>
<tr>
<td>Recovery time</td>
<td>None</td>
<td>1 CLK (6.7ns)</td>
</tr>
</tbody>
</table>
Chip photo

- 65nm 9M1P CMOS technology
- Chip area of 0.08mm²
High SNDR of 84dB ($V_n=24\mu V$) is achieved

Fs=10MS/s, BW=250kHz, OSR=20, 10kHz input

SNR=84.2 dB
SFDR=96.5 dB
SNDR=83.4dB

A. Matsuzawa, Tech Idea
Clock scalability

FoMs $> 170$ dB for different sampling rates of $2.5 - 25$ MS/s.

Power of the dynamic amplifier is clock scalable $m=2$

$\begin{align*}
    f_c &= 125 \text{kHz} - 1.25 \text{MHz} \\
    P_c @ 10\text{MS/s} & \begin{align*} 
    \text{Analog} & : 60.0 \mu\text{W (23.3\%)} \\
    \text{Ref} & : 35.1 \mu\text{W (13.6\%)} \\
    \text{Digital} & : 162.7 \mu\text{W (63.1\%)}
\end{align*}
\end{align*}$

A. Matsuzawa, Tech Idea
Performance Summary

The ADC has achieved high FoMs at the highest sampling rate.

Recent noise shaping SAR ADC

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<tbody>
<tr>
<td>Architecture</td>
<td>NS SAR</td>
<td>NS SAR</td>
<td>NS SAR</td>
<td>NS SAR</td>
</tr>
<tr>
<td>Process [nm]</td>
<td>65</td>
<td>28</td>
<td>55</td>
<td>65</td>
</tr>
<tr>
<td>Active Area [mm²]</td>
<td>0.08</td>
<td>0.116</td>
<td>0.072</td>
<td>0.18</td>
</tr>
<tr>
<td>Supply [V]</td>
<td>1.0</td>
<td>1.55/0.75</td>
<td>1.8/1.1</td>
<td>1.2</td>
</tr>
<tr>
<td>Sampling rate [MS/s]</td>
<td>2.5</td>
<td>10</td>
<td>25</td>
<td>0.1</td>
</tr>
<tr>
<td>BW [kHz]</td>
<td>62.5</td>
<td>250</td>
<td>625</td>
<td>2</td>
</tr>
<tr>
<td>SFDR [dB]</td>
<td>88.3</td>
<td>96.5</td>
<td>89.9</td>
<td>111.8</td>
</tr>
<tr>
<td>SNR [dB]</td>
<td>84.3</td>
<td>84.2</td>
<td>82.2</td>
<td>98.57</td>
</tr>
<tr>
<td>SNDR [dB]</td>
<td>82.3</td>
<td>83.4</td>
<td>80.4</td>
<td>97.99</td>
</tr>
<tr>
<td>Power [µW]</td>
<td>66.3</td>
<td>257.8</td>
<td>630.2</td>
<td>37.1</td>
</tr>
<tr>
<td>FoM [dB]</td>
<td>172.0</td>
<td>173.3</td>
<td>170.4</td>
<td>175.3</td>
</tr>
</tbody>
</table>

A. Matsuzawa, Tech Idea
Performance

Highest FoMs and lowest FoMw from 50kS/s to 500kS/s

High SNDR of 83dB at 625KS/s  $P_d$ of 630uW was obtained

$$FoM_s (dB) = SNDR (dB) + 10 \log \left( \frac{f_s / 2}{P} \right)$$

$$FoM_w (J) = \frac{P_d}{f_s \times 2^{ENOB}}$$
Summary

• Power break through often made new applications and markets. Current and future big market must be IoT systems.

• CMOS is ultimate logic circuit that doesn't consume any static power and no relation between speed and consumed energy. Small capacitance and low voltage operation are the key.

• ADC should consider accuracy, distortion, and noise. Furthermore, these factors essentially have tough tradeoff against low energy operation.

• CMOS technology conquered many drawbacks by using capacitance to realize S/H and to absorb mismatch voltage. Furthermore, CMOS enables use of digital compensation.

• Recent advanced ADC uses dynamic CMOS circuit more aggressively replaces conventional amplifier.

A. Matsuzawa