Dynamics of Parallel-Type and Serial-Type Charge Pump Circuits for High Voltage Generation

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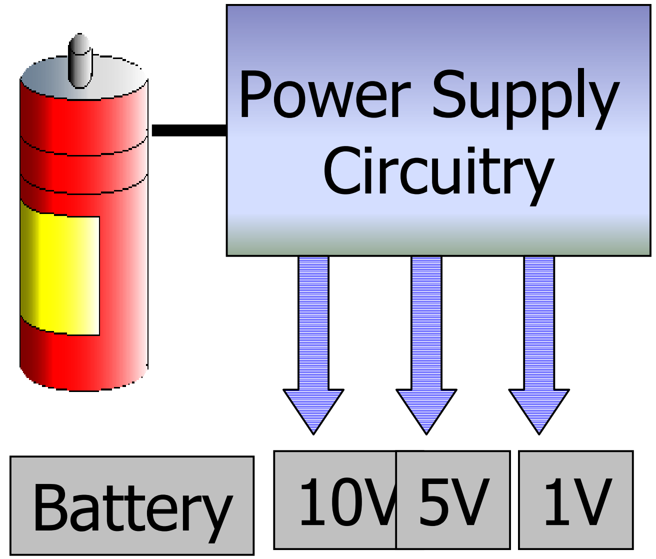
Contents

1. Research Background & Goal

Research Background

- Mobile equipment prevails everywhere.
- Mobile phone, Digital still camera, PDA

- Small size, High efficiency
- High- and low-voltage multiple supplies



Switching Regulator

- Merit
  - High efficiency
  - Continuously varying output voltage
  - Large output current

- Demerit
  - Coils are required. ⇒ bulky and costly
  - Switching noise

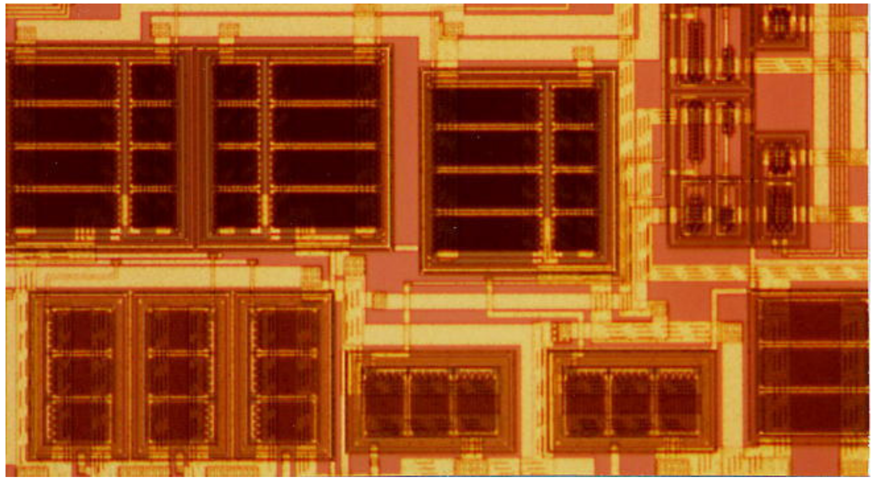
Charge Pump Circuit

- Merit
  - No coils
  - Less noise

- Demerit
  - Low efficiency
  - Small output current
  - Output voltage = 2Vdd, 3Vdd, 4Vdd, …

Our Charge Pump Circuit Implementation

- Fabricated
  in Sanyo Process.
- Commercialization
  has started.



Chip photo: 3.99mm × 4.35mm

- Applications:
  - PDA (Personal Digital Assistance)
  - DSC (Digital Still Camera)
  - Mobile Phone

Research Goal

- To establish the design methodology of charge pump circuits

- To compare two types of charge pump circuits:
  - Parallel-type (Dickson-type)
  - Serial-type (Switched-capacitor type)

2. Parallel-type Charge Pump Circuit

2.1 Transient Analysis

- Node Voltage
- Energy Flow

2.2 Steady State Analysis

- Output Voltage
- Efficiency

2. Parallel-type Charge Pump Circuit

2.1 Transient Analysis

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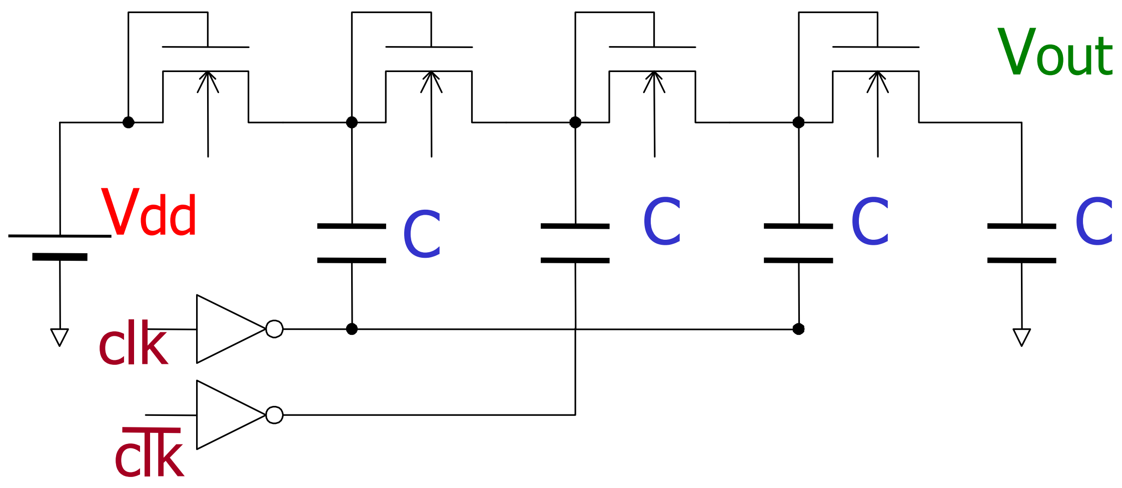
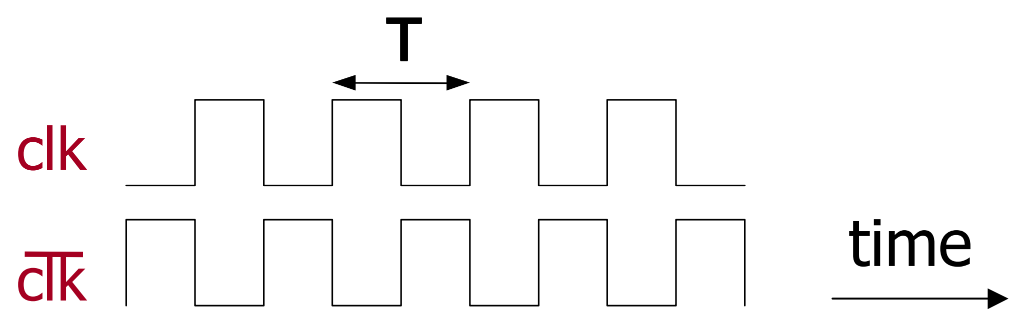
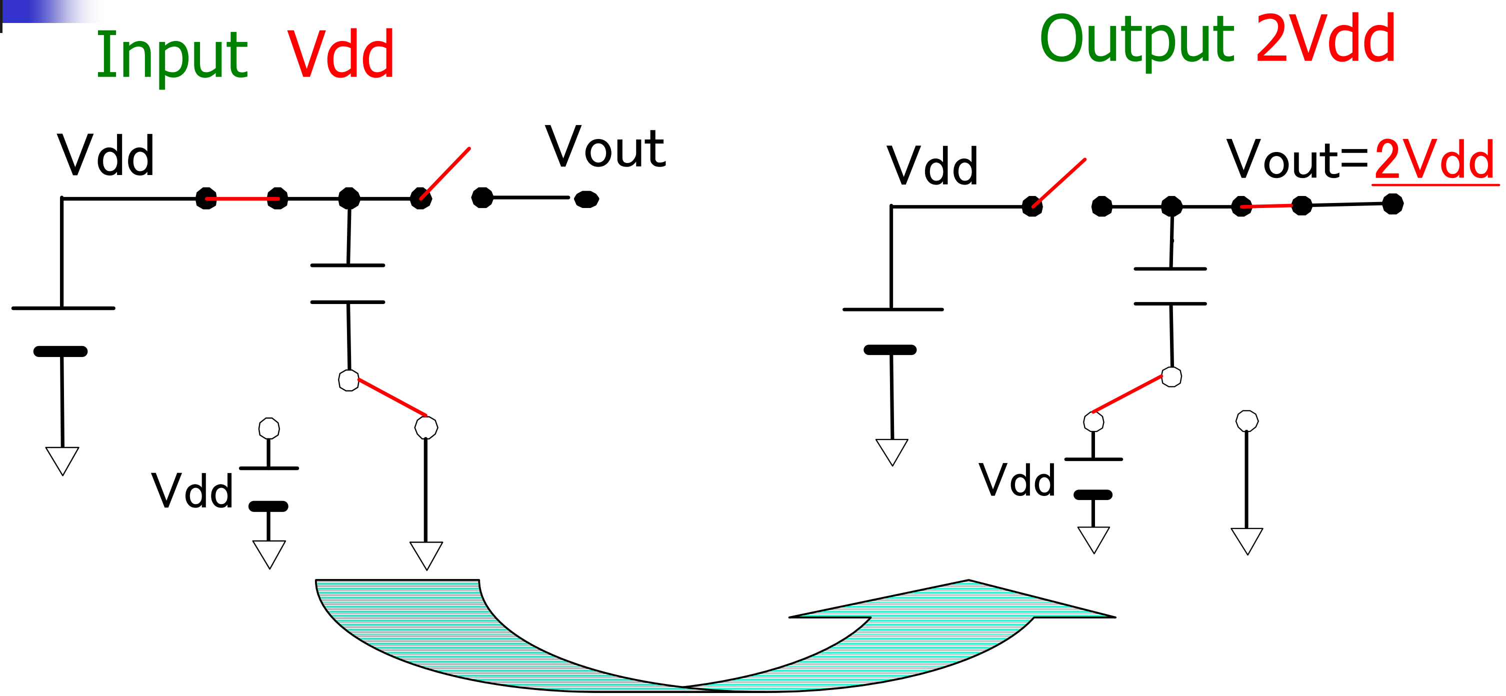
Parallel-type (Dickson-type) Charge Pump Circuit

- Input Vdd
- Output Vout
- Diode-connected MOSFETs
- Capacitors C
- Clock clk, $\overline{\text{clk}}$



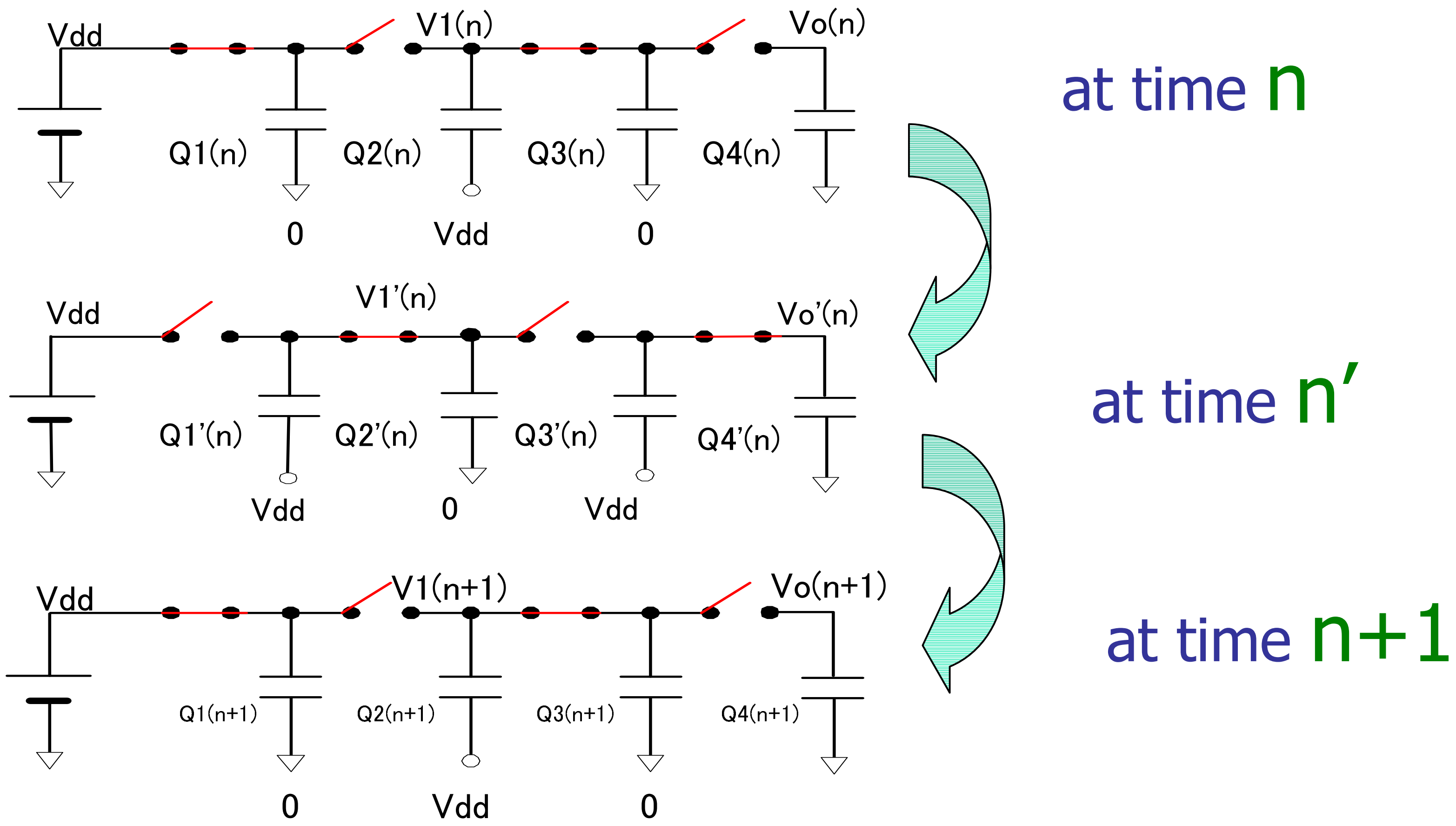


Principle of Parallel-type Charge Pump Circuit

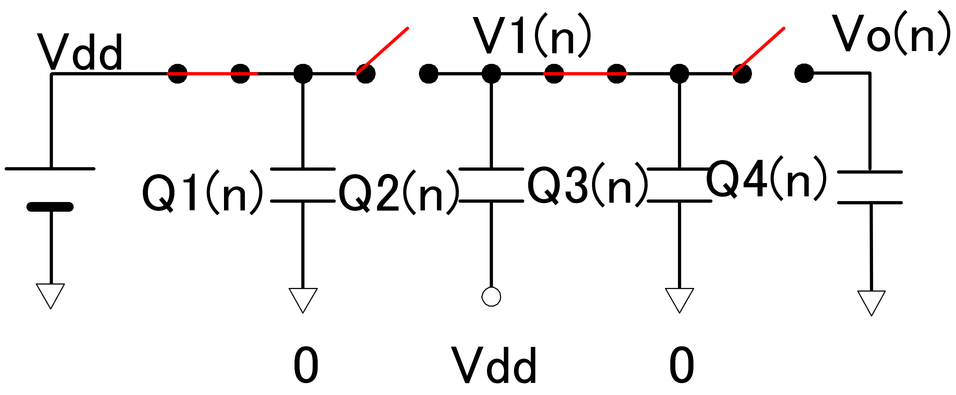


- A parallel-type charge pump circuit is cascade of the above circuit.

State Transition of 3-stage Charge Pump Circuit



Time n vs. Time n′



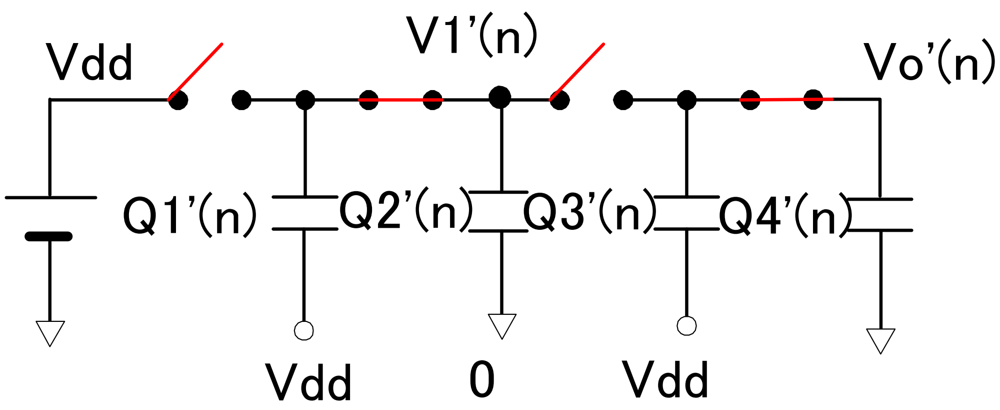
At time n

$Q1(n)=CV_{dd}$

$Q2(n)=C[V1(n)-Vdd]$

$Q3(n)=CV1(n)$

$Q4(n)=CVo(n)$



At time n′

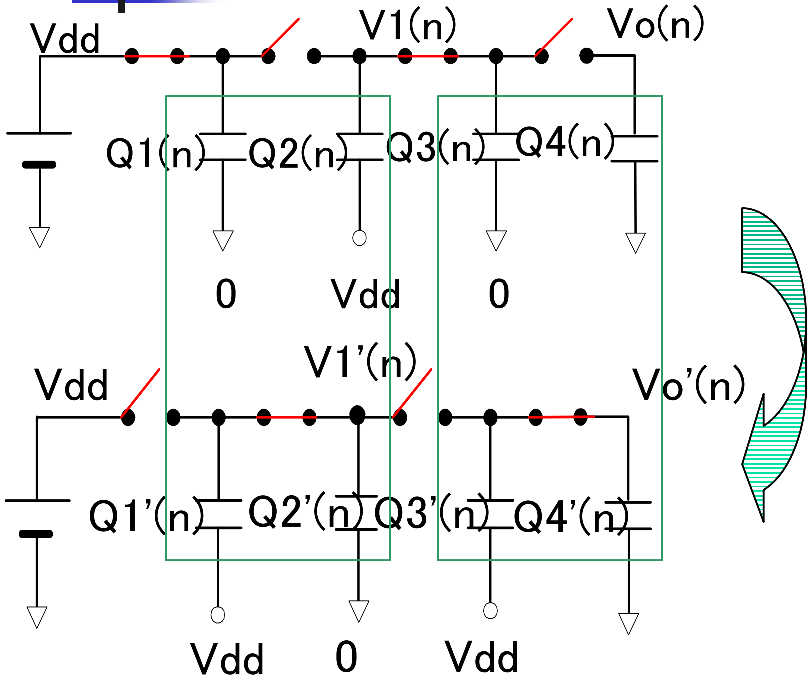
$Q1'(n)=C[V1'(n)-Vdd]$

$Q2'(n)=CV1'(n)$

$Q3'(n)=C[Vo'(n)-Vdd]$

$Q4'(n)=CVo'(n)$

Time n vs. Time n’



From charge conservation law

Q1(n)+Q2(n)= Q1′(n)+Q2′(n)

Q3(n) +Q4(n)= Q3′(n)+Q4′(n)

∴ CVdd+C[V1(n)-Vdd]=

C[V1′(n)Vdd]+CV1′(n)

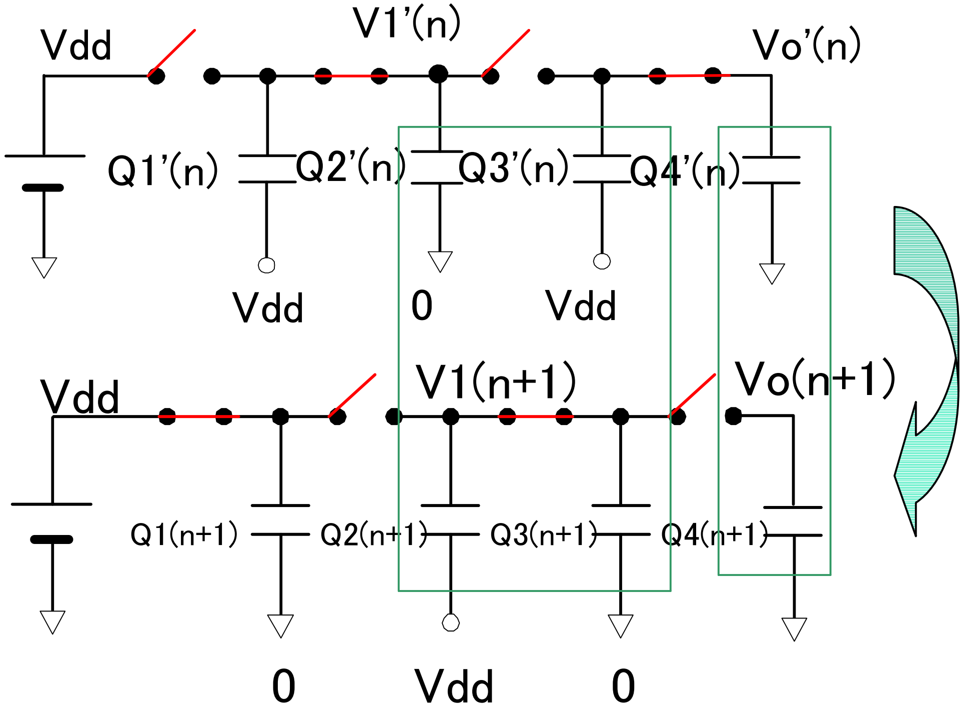
CV1(n) +Cvo(n)=

C[Vo′(n)-Vdd]+ Cvo′(n)

V1′ (n) = [V1(n)+Vdd] / 2

Vo′ (n) = [V1(n) + Vo(n) + Vdd] / 2

Time n vs. Time n+1



From charge conservation law

Q2(n+1)+Q3(n+1)=

Q2′(n) +Q3′(n)

∴C[V1(n+1)-Vdd]+CV1(n+1)=

CV1′(n) +C[Vo′(n)-Vdd]

Vo(n+1) = [V1(n)+Vo(n)+Vdd] / 2

V1(n+1) = [2V1(n)+Vo(n)+2Vdd] / 2

State-Space Approach

- State equation

$$\begin{bmatrix} Vo(n+1) \\ V1(n+1) \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & \frac{1}{2} \\ \frac{1}{4} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} Vo(n) \\ V1(n) \end{bmatrix} + \begin{bmatrix} \frac{1}{2}Vdd \\ \frac{1}{2}Vdd \end{bmatrix}$$

- This state-space approach can be used for a general N-stage charge pump circuit.

Node Voltage Formula

$$Vo(n) = \frac{1}{2}\left(\lambda_1^n + \lambda_2^n\right)Vo(0) + \frac{1}{\sqrt{2}}\left(\lambda_1^n - \lambda_2^n\right)V1(0)$$

$$+ \left(\frac{-2\sqrt{2}-3}{\sqrt{2}}\lambda_1^n - \frac{2\sqrt{2}-3}{\sqrt{2}}\lambda_2^n + 4\right)Vdd \quad \cdots ⑦$$

$$V1(n) = \frac{1}{\sqrt{2}}\left(\lambda_1^n - \lambda_2^n\right)Vo(0) + \frac{1}{2}\left(\lambda_1^n + \lambda_2^n\right)V1(0)$$

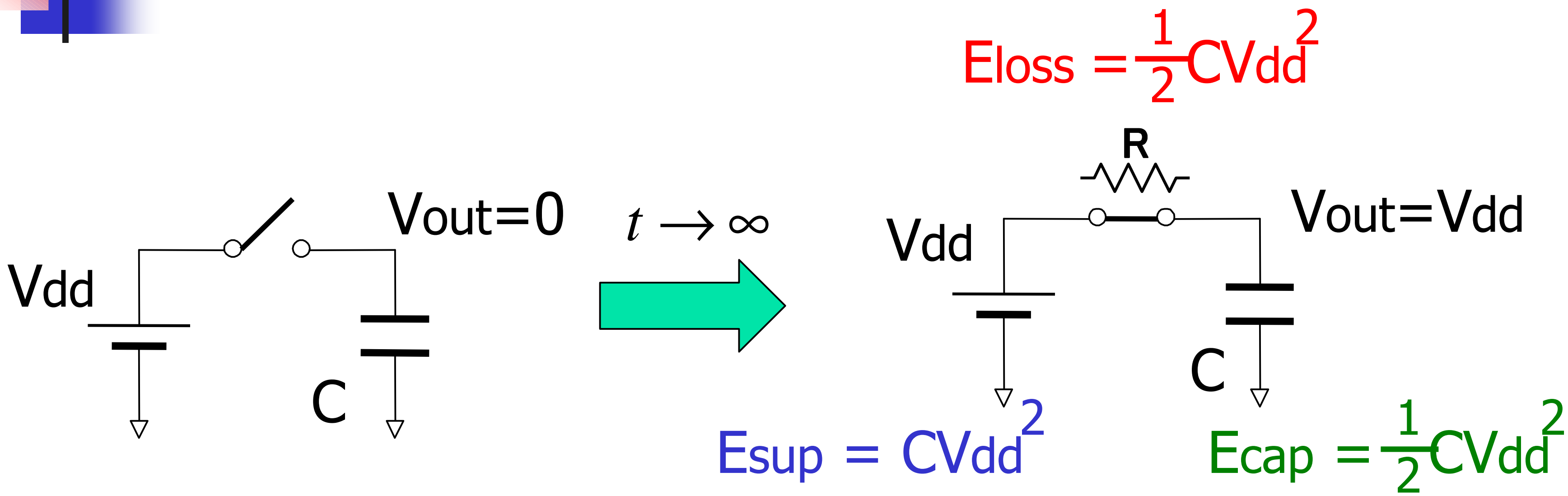
$$+ \left(\frac{-3-2\sqrt{2}}{2}\lambda_1^n + \frac{2\sqrt{2}-3}{2}\lambda_2^n + 3\right)Vdd \quad \cdots ⑧$$

Where $\lambda_1=(2+\sqrt{2})/4<1$、$\lambda_2=(2-\sqrt{2})/4<1$.

∴ as $n \to \infty$, $\lambda_1^n \to 0$, $\lambda_2^n \to 0$,

$Vo(\infty)=4Vdd$, $V1(\infty)=3Vdd$.

Energy Flow
When Charging Capacitor



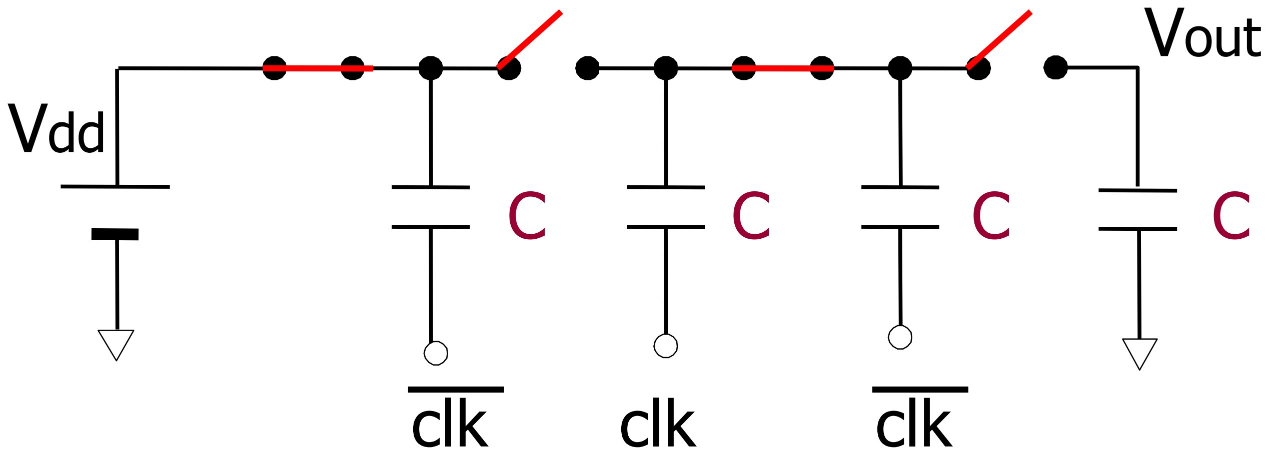
Esup: Total supplied energy from Vdd

Eloss: Total dissipated energy through R

Ecap: Stored energy in C

Esup = Eloss + Ecap, Eloss = Ecap

Ideal Parallel-type Charge Pump in Transient State



At t=0, charges in all capacitors are zero.

$t \rightarrow \infty$

Esup: Total supplied energy from Vdd, clock drivers

Eloss: Total dissipated energy through switches

Ecap: Stored energy in capacitors

Esup = Eloss + Ecap, Eloss = Ecap (= $15CV_{dd}^{2}$)

2. Parallel-type Charge Pump Circuit

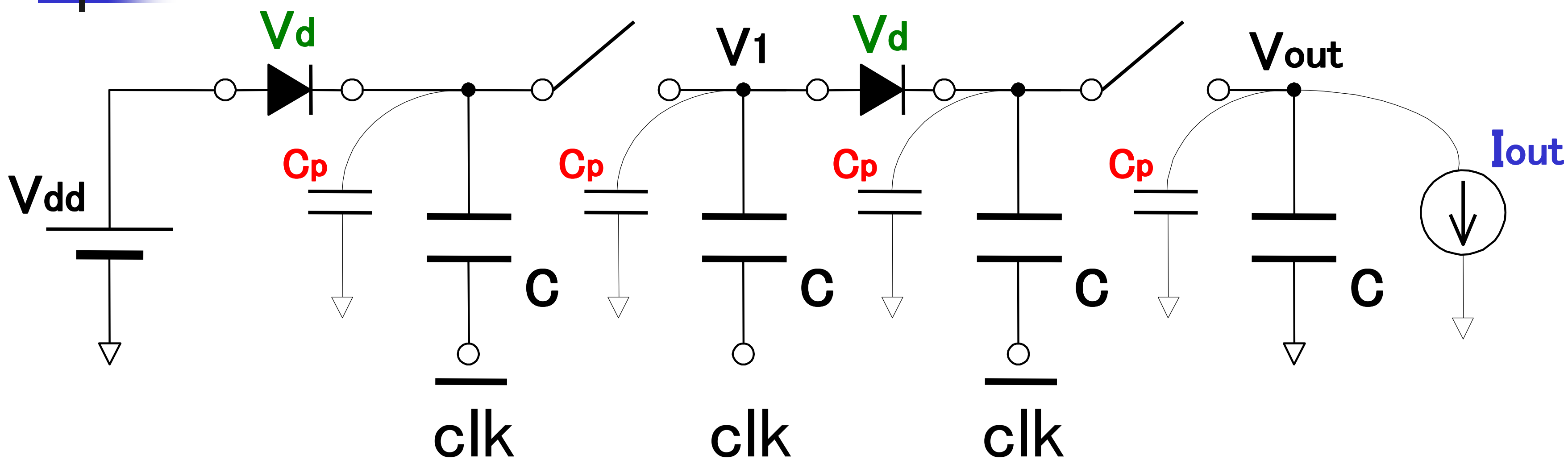
2.1 Transient Analysis

- Node Voltage
- Energy Flow

2.2 Steady State Analysis

- Output Voltage
- Efficiency

Parallel-type Charge Pump Circuit with Non-idealities



Vd: Voltage drop across switch

Cp: Parasitic capacitance to ground

Iout: Output load current

Parallel-type Charge Pump Node Voltage in Steady State

As $n \Rightarrow \infty$

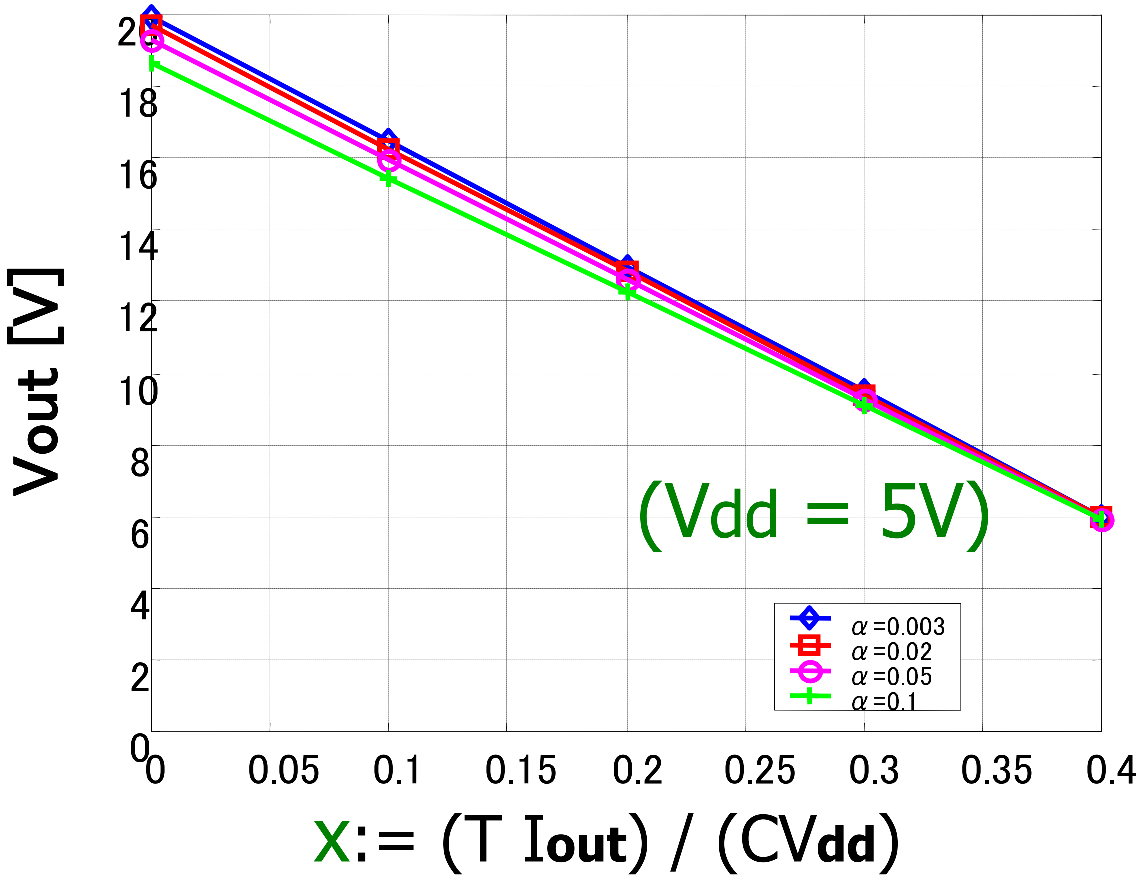
- Output voltage

$$V_{out}(n) \Rightarrow \left[4 - \frac{3\,C_p}{C+C_p}\right] V_{dd} - 4V_d - \frac{7\,T\,I_{out}}{C + C_p}$$

- Internal node voltage

$$V_1(n) \Rightarrow \left[2 - \frac{3\,C_p}{2\,(C+C_p)}\right] V_{dd} - 2V_d - \frac{7\,T\,I_{out}}{2\,(C + C_p)}$$

Parallel-type Charge Pump Output Voltage from Formula



3-stage charge pump (N=3), β := Vd/Vdd = 0.0

α : = Cp/C = 0.003, 0.02, 0.05, 0.1

Parallel-type Charge Pump Efficiency η in Steady State

$$\eta := \frac{\text{Output power from Vout}}{\text{Supplied power from Vdd and clock drivers}}$$

$$= 1 - \frac{N\alpha + 2(N+1)(1+\alpha)\beta x + 4Nx}{N\alpha + 2(N+1+\alpha)x}$$

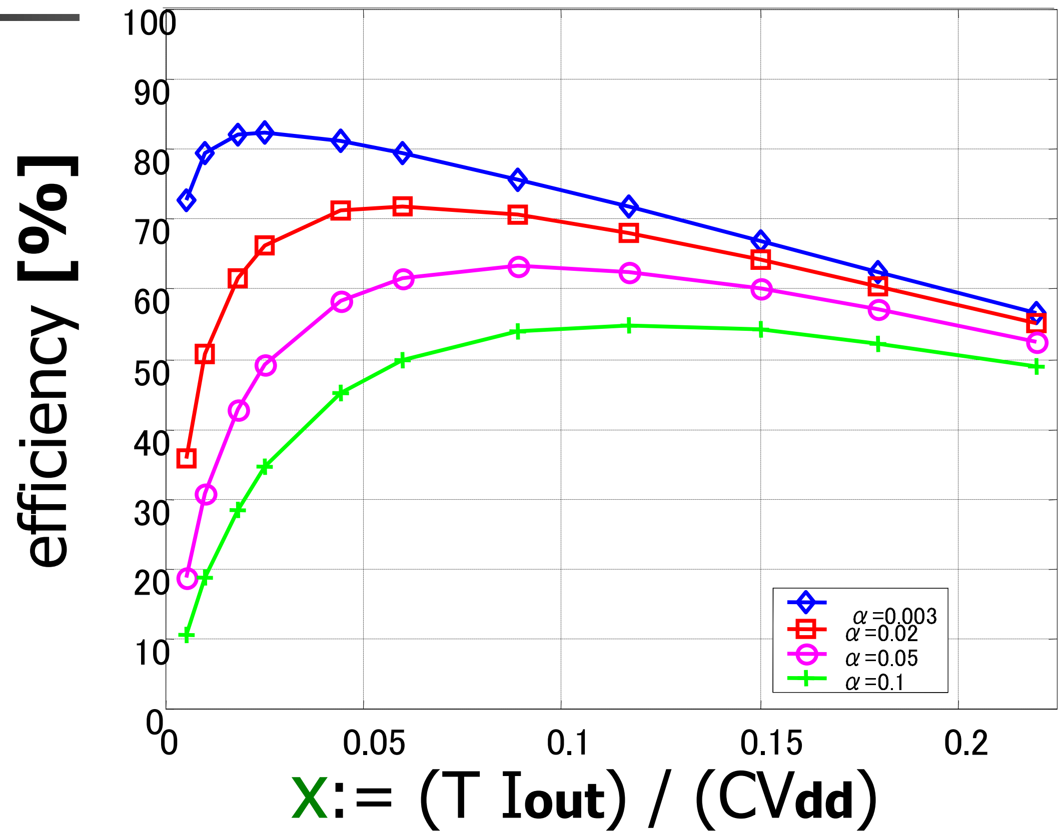
Where

N: number of stages

$x := (T\,I_{out}) / (C\,V_{dd})$,

$\alpha := C_p/C$, $\beta := V_d/V_{dd}$.

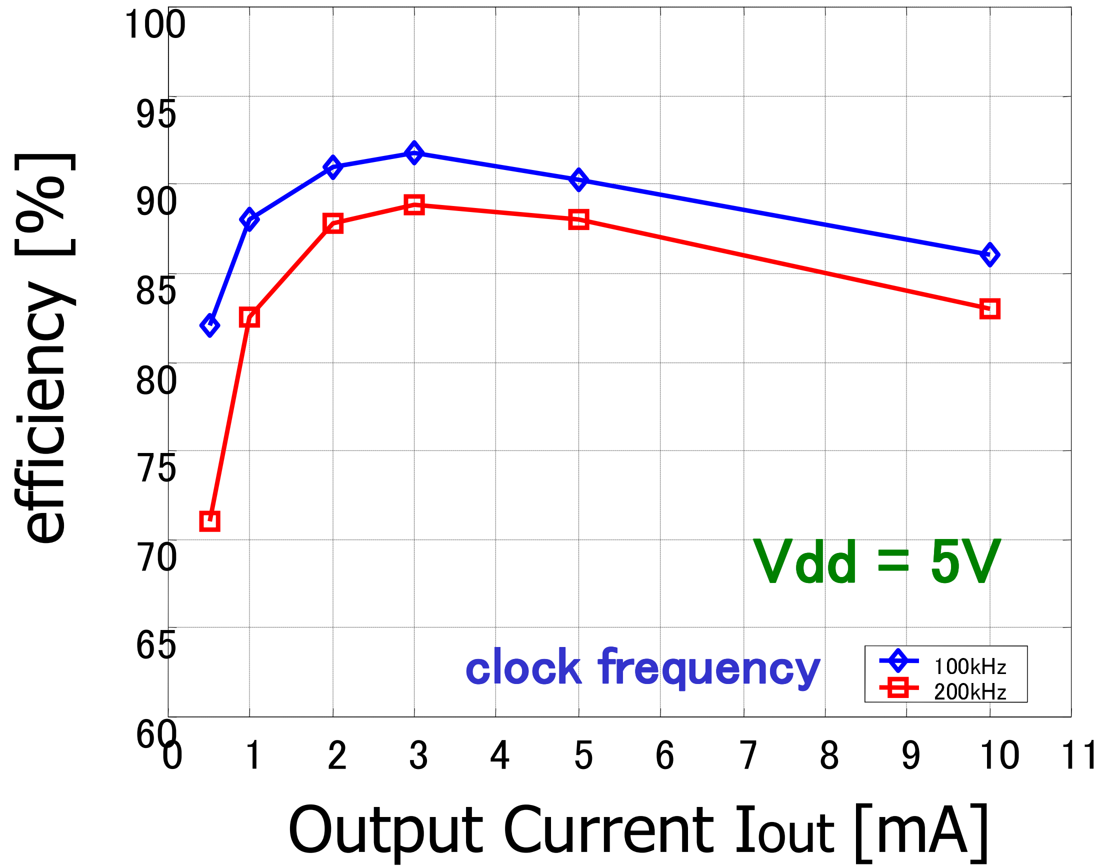
Parallel-type Charge Pump Efficiency from Formula

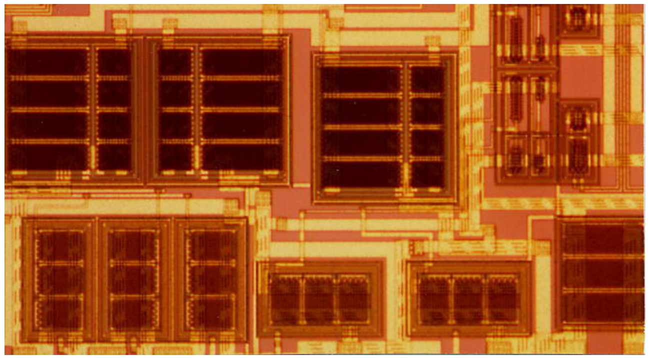


3-stage charge pump (N=3), β := Vd/Vdd = 0.1

α : = Cp/C = 0.003, 0.02, 0.05, 0.1

Measured Parallel-type Charge Pump Efficiency





3-stage charge pump
TEG chip photo

3. Serial-type
Charge Pump Circuit

3.1 Steady State Analysis

- Output Voltage
- Efficiency

3.2 Comparison of Parallel and Serial-type Charge Pump Circuits

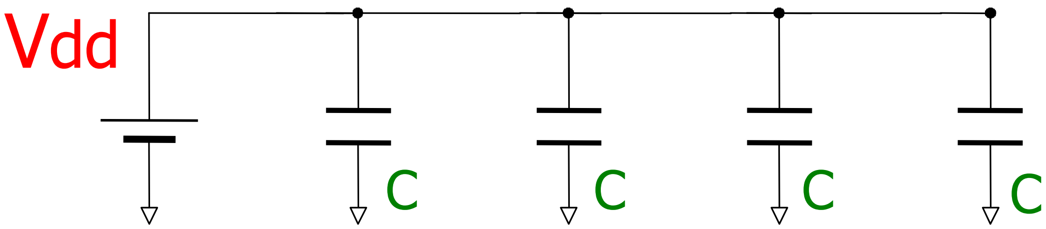
3. Serial-type Charge Pump Circuit

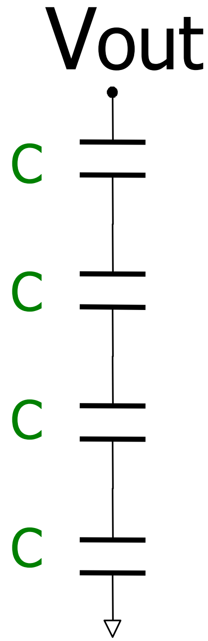
3.1 Steady State Analysis

- Output Voltage
- Efficiency

3.2 Comparison of Parallel and Serial-type Charge Pump Circuits

Principle of Serial-type Charge Pump

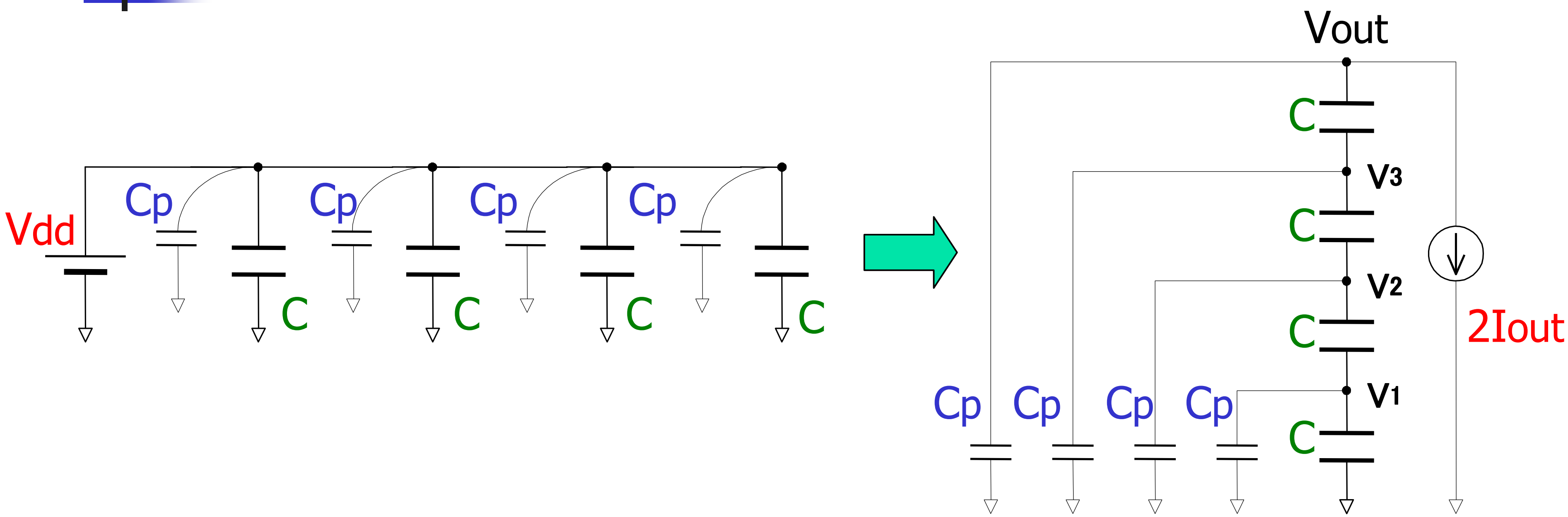




All C's are connected in parallel and charged to Vdd.

All C's are connected in series to produce high output voltage.

Serial-type Charge Pump with Non-idealities



- Cp: Parasitic capacitance to ground
- Iout: Output load current

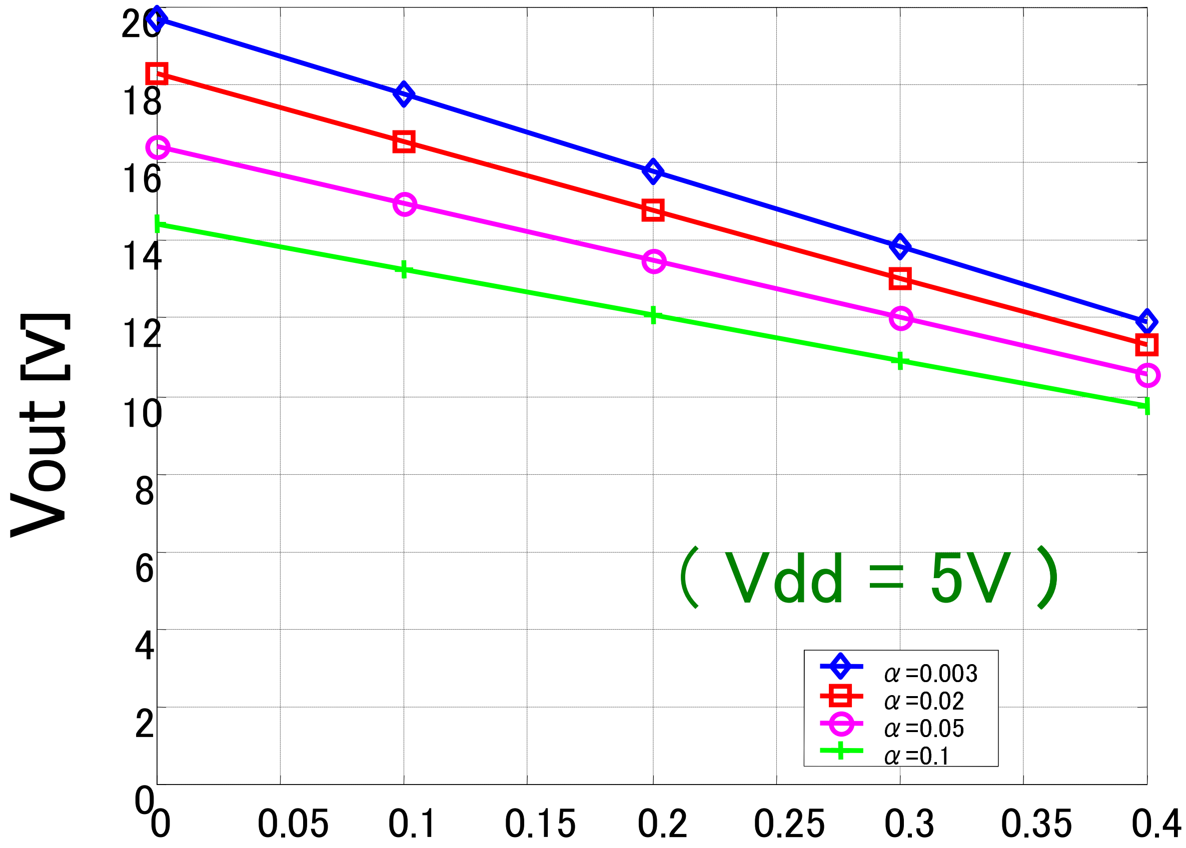
Serial-type Charge Pump Output Voltage in Steady State

$$V_{out} = \frac{V_{dd}}{D}\left[(4 + 20\alpha + 21\alpha^2 + 8\alpha^3 + \alpha^4) - x\,(4 + 10\alpha + 6\alpha^2 + \alpha^3) \right]$$

Where

- $x := (T\,I_{out}) / (C\,V_{dd})$
- $\alpha := C_p / C$
- $D := 1 + 10\alpha + 15\alpha^2 + 7\alpha^3 + \alpha^4$

Serial-type Charge Pump Output Voltage from Formula



X:= (T Iout) / (CVdd)

α : = Cp/C = 0.003, 0.02, 0.05, 0.1

Serial-type Charge Pump Efficiency η in Steady State

$$\eta = \frac{F x - (H x^2 / 2)}{G + 2 F x}$$

Where

$x := (T\ I_{out}) / (C\ V_{dd})$

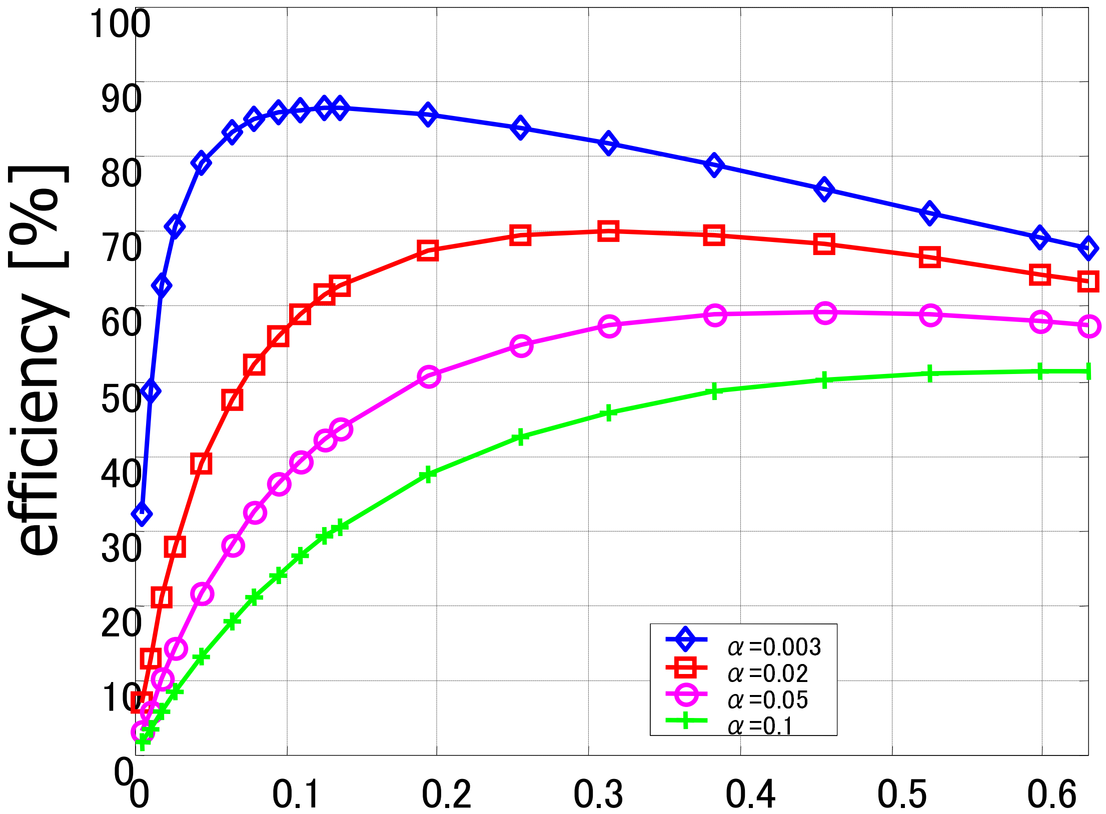
$F := 4 + 20\alpha + 21\alpha^2 + 8\alpha^3 + \alpha^4$

$G := 14\alpha + 34\alpha^2 + 19\alpha^3 + 3\alpha^4$

$H := 4 + 10\alpha + 6\alpha^2 + \alpha^3$

$\alpha := C_p / C$

Serial-type Charge Pump Efficiency from Formula



X:= (T Iout) / (CVdd)

α : = Cp/C = 0.003, 0.02, 0.05, 0.1

3. Serial-type Charge Pump Circuit

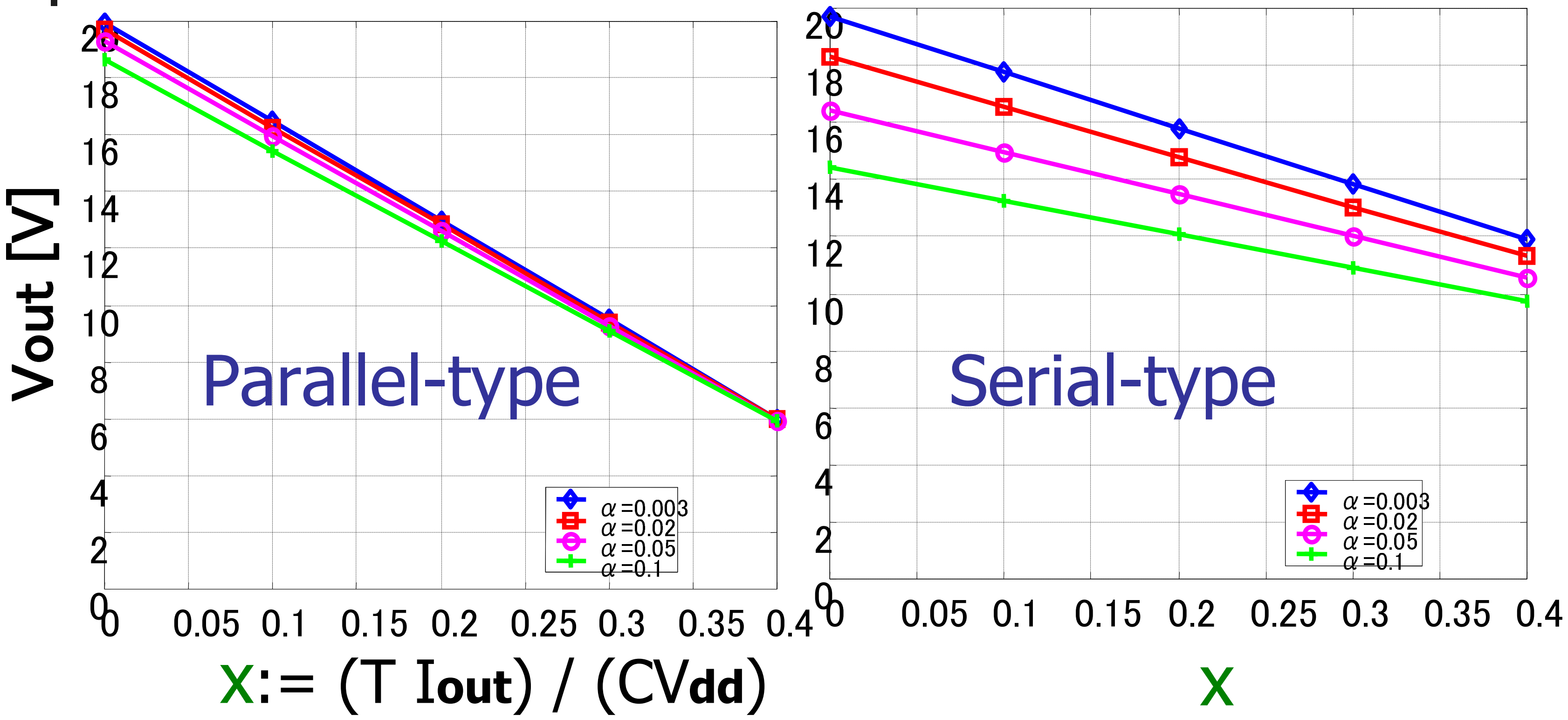
3.1 Steady State Analysis

- Output Voltage
- Efficiency

3.2 Comparison of Parallel and Serial-type Charge Pump Circuits

Output Voltage Comparison of Parallel- and Serial-types

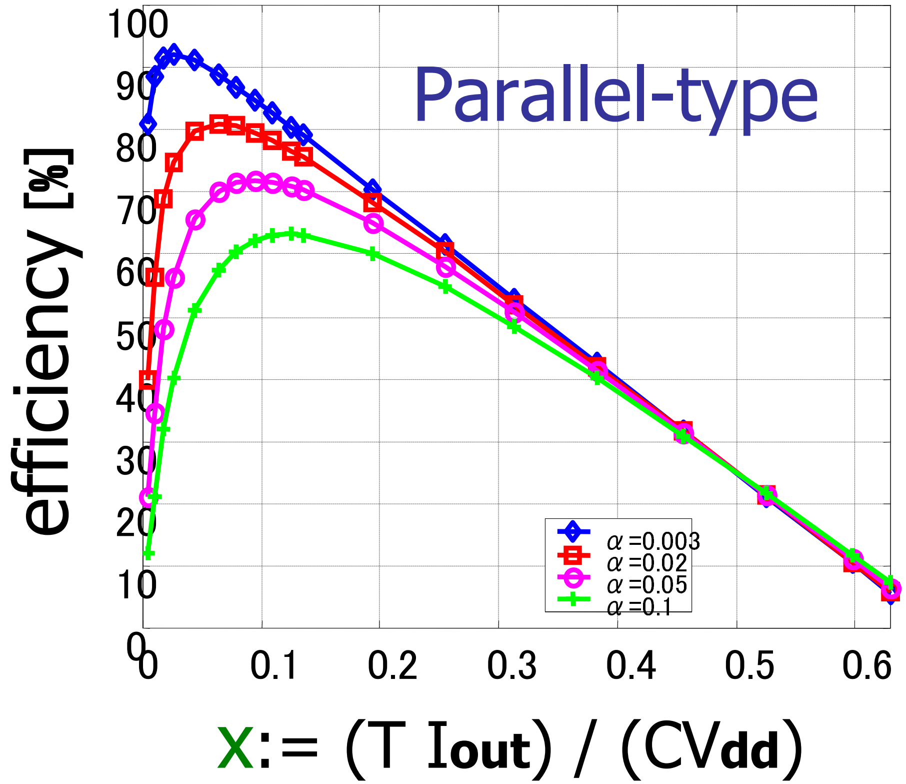
Vdd=5V

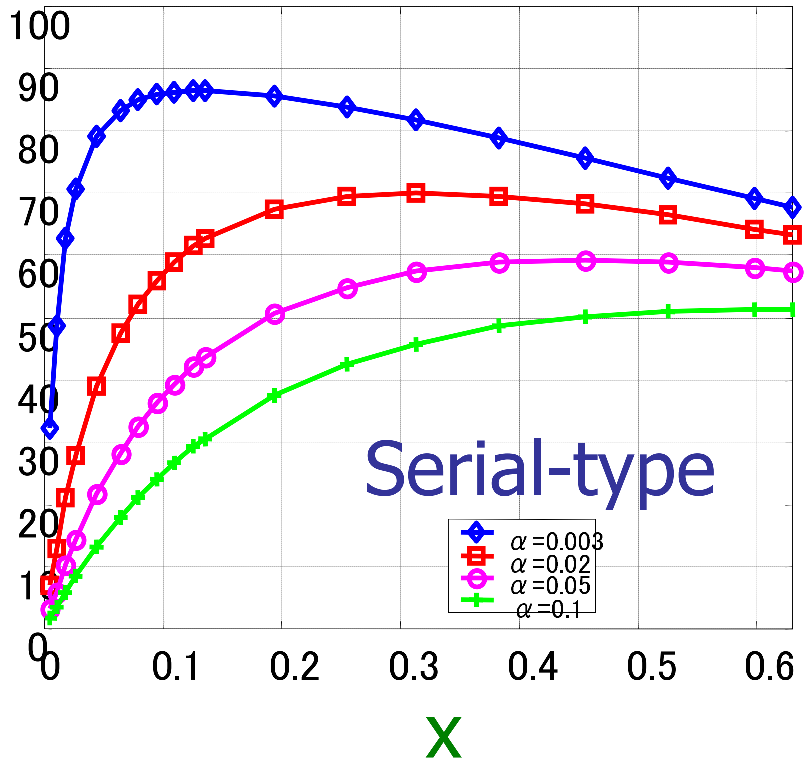


- For small x, the parallel-type is better.

Efficiency Comparison of Parallel- and Serial-types

β =Vd/Vdd=0





- For small x, the parallel-type is better.

4. Summary

The followings are clarified:

- Parallel-type Charge Pump
  - In transient state,

    Node voltage, Energy flow
  - In steady state

    Output node voltage, Efficiency
- Serial-type Charge Pump
  - In steady state

    Output node voltage, Efficiency