Modeling Technologies from Analog/Mixed-Signal Circuit Designer Viewpoint

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Renesas Electronics
Self Introduction

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Mixed-Signal IC Design & Testing

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Device Modeling

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Device Physics

Yushiro Okabe: Adjunct Associate Professor, Gunma Univ., Formerly Sanyo Electric  
Device Modeling

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Mixed-Signal IC Design

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Computer Fluid Dynamics
Contents

- Target of this talk
- CMOS and Bipolar
- Device Physics and Model
- Modeling Technologies
- Collaboration of Circuit Design and Modeling
- Layout Dependent Effect Modeling
- Electrical and Thermal Effect Modeling
- Device Model Technologies Supported by AI
- Modeling Education at Gunma Univ.
- Modeling Research at Gunma Univ.
- Conclusion
- Appendix: Research for Monte Carlo Simulation
Contents

- **Target of this talk**
  - CMOS and Bipolar
  - Device Physics and Model
  - Modeling Technologies
  - Collaboration of Circuit Design and Modeling
  - Layout Dependent Effect Modeling
  - Electrical and Thermal Effect Modeling
  - Device Model Technologies Supported by AI
  - Modeling Education at Gunma Univ.
  - Modeling Research at Gunma Univ.
  - Conclusion
  - Appendix: Research for Monte Carlo Simulation
Address what the circuit designer expects to device modeling technologies as a model user
Contents

- Target of this talk
- **CMOS and Bipolar**
  - Device Physics and Model
  - Modeling Technologies
  - Collaboration of Circuit Design and Modeling
  - Layout Dependent Effect Modeling
  - Electrical and Thermal Effect Modeling
  - Device Model Technologies Supported by AI
  - Modeling Education at Gunma Univ.
  - Modeling Research at Gunma Univ.
- Conclusion
- Appendix: Research for Monte Carlo Simulation
• Why so many CMOS models?

• How about Bipolar?
  – Bipolar ICs are still used in analog companies
CMOS
CMOS device structure is simple. However, its accurate modeling is difficult.
- That is why so many CMOS models.

Bipolar
Bipolar transistor device structure is complicated. However, its accurate modeling is relatively easy.
- That is why only a few bipolar transistor models.
Contents

- Target of this talk
- CMOS and Bipolar
- **Device Physics and Model**
- Modeling Technologies
- Collaboration of Circuit Design and Modeling
- Layout Dependent Effect Modeling
- Electrical and Thermal Effect Modeling
- Device Model Technologies Supported by AI
- Modeling Education at Gunma Univ.
- Modeling Research at Gunma Univ.
- Conclusion
- Appendix: Research for Monte Carlo Simulation
Device physics is difficult for the circuit designer to learn.

Modeling is good to learn device physics.
Interface Between Circuit and Device

- Circuit designer
- Fabless company
- Device, process researcher
- Foundry company

 Interface
  - Mask data
  - Device model
  - Model parameters

Mead-Conway method
• Physical model with limited fitting parameters is desirable.

• Pure mathematical model is often difficult to use.
BSIM2
Mathematical model

BSIM3
- Physical model
- Based on CMOS device physics (+ fitting parameters)
  Device, process parameter values in model
  \[ \Rightarrow \text{Prediction of MOS characteristics} \]
  change
Prof. Syukuro Manabe
Nobel Prize Winner in Physics, 2021

“For the physical modeling of Earth's climate, quantifying variability and reliably predicting global warming"

His model can predict:
CO₂ increase $\Rightarrow$ global warming

Prediction is essential in modeling technology
Contents

● Target of this talk
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● Device Physics and Model
● **Modeling Technologies**
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  ● Layout Dependent Effect Modeling
  ● Electrical and Thermal Effect Modeling
  ● Device Model Technologies Supported by AI
● Modeling Education at Gunma Univ.
● Modeling Research at Gunma Univ.
● Conclusion
● Appendix: Research for Monte Carlo Simulation
“All models are wrong, but some are useful”.
George E. P. Box
British statistician, 1919-2013

MOS model needs to be accurate only in the region where the designed circuit operates.
Circuit Designer: Application Oriented Mind

For amplifier design
For DC-DC converter

High frequency CMOS circuit design
RF-CMOS model

Modeling should be accurate in the focused region
The other regions do NOT matter
Myth
Fine CMOS: Characteristics deteriorate for analog circuit performance

Truth
FinFET: Characteristics improve for analog circuit performance
- Large $r_{out}$, $g_m$
- Small Drain-Induced Barrier Lowering (DIBL) effect
- No body effect
Research for FinFET Analog Circuit

Strong research motivation for analog circuit design with FinFET
- New frontier
- Challenging

• Perfect FinFET model for analog circuit with layout dependency information is desired.

• Access to FinFET process is difficult; high cost

• Chip implementation and measurement verification are not easy.

“All models are wrong, but some are useful”.

Model should be correct in all operating regions.
Contents

- Target of this talk
- CMOS and Bipolar
- Device Physics and Model
- Modeling Technologies
  - **Collaboration of Circuit Design and Modeling**
  - Layout Dependent Effect Modeling
  - Electrical and Thermal Effect Modeling
  - Device Model Technologies Supported by AI
  - Modeling Education at Gunma Univ.
  - Modeling Research at Gunma Univ.
- Conclusion
- Appendix: Research for Monte Carlo Simulation
Many circuit designers use CMOS model and SPICE parameters from foundry as black box.

For analog circuit design with a small number of MOSFETs, collaboration between circuit designer and modeling researcher is effective.
Reference Current Source
Insensitive to Supply Voltage and Temperature

Drain Current Temperature Characteristics

- For $V_{GS} = V_{CP}$, $I_{DS}$ is insensitive to temperature.

- At high temperature,
  - For $V_{GS} < V_{CP}$, $I_{DS}$ becomes larger
  - For $V_{GS} > V_{CP}$, $I_{DS}$ becomes smaller.

MOS device, modeling researcher interpretation is useful.
**VCP and Small Channel Length** $L$

SPICE simulation result with BSIM3v3 model parameters

$L \rightarrow \text{small} \rightarrow VCP \rightarrow \text{increase}

Explained by short channel effect using BSIM3v3 model equations

NMOS drain current temperature characteristics

- $V_{GS}$
- $V_{DS}$
- $I_{DS}$
- $W/L$
- $5\mu m$
- $0.5V$
- $\sqrt{I_{DS}}$

$V_{CP}$
$V_T$
Increasing temperature
Mobility decrease
Increasing temperature
$V_{GP}$
$V_{CP}$
increase
Decrease
**VCP and Drain-Source Voltage** $V_{DS}$

SPICE simulation result with BSIM3v3 model parameters

$V_{DS} \rightarrow$ small $\rightarrow$ $V_{CP} \rightarrow$ increase

Explained by drain induced barrier lowering (DIBL)

using BSIM3v3 model equations

NMOS drain current temperature characteristics
Contents

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- CMOS and Bipolar
- Device Physics and Model
- Modeling Technologies
- Collaboration of Circuit Design and Modeling
  - Layout Dependent Effect Modeling
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- Modeling Education at Gunma Univ.
- Modeling Research at Gunma Univ.
- Conclusion
- Appendix: Research for Monte Carlo Simulation
Layout Dependent Effect Modeling

Digital-to-Analog Converter (DAC)

Unary DAC
Configuration & Operation

Digital input = 2
Vout = 2IR

Digital input = 8
Vout = 8IR
Actual DAC Circuits on IC

Current source mismatch $\Delta I_k$

Systematic gradient $\Delta I_k$

DAC non-linearity
Digital-to-Analog Converter (DAC) Nonlinearity

Regular layout
- Current source mismatch $\Delta I_k$
- DAC nonlinearity

Random layout
- Layout dependent
- Cancelled

$\Delta I_k$
DAC nonlinearity due to mismatch

Important issue

Accurate mismatch modeling is desired.

Many layout algorithms

"Digital-to-Analog Converter Linearity Improvement Technique Based on Classical Number Theory for Modern ULSI"
30th International Workshop on Post-Binary ULSI Systems (May 2021)
Contents

- Target of this talk
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- Device Physics and Model
- Modeling Technologies
- Collaboration of Circuit Design and Modeling
- Layout Dependent Effect Modeling
- **Electrical and Thermal Effect Modeling**
- Device Model Technologies Supported by AI
- Modeling Education at Gunma Univ.
- Modeling Research at Gunma Univ.
- Conclusion
- Appendix: Research for Monte Carlo Simulation
Thermal effect modeling is expected:

- Power device and circuit
- High precision measurement circuit
- Audio amplifier

Self-heating, affect from nearby thermal sources
Thermal Effect for High Precision Measurement Circuit

Electric Motive Force (EMF):
Issue for high precision μV-order voltage measurement circuit

FFT-Based DC-AC Conversion

**DC-AC Conversion Circuit**

Vin = 1 μV

![DC-AC Conversion Circuit Diagram]

- Single-End Amplifier 100x
- AC Amplifier ~ 100x
- 16bit ADC
- Sampling Rate 100 kHz
- Clock = 1 kHz

**FFT Result**

- LTspice FFT Condition:
  - Fs = 409.6 kHz, Fres = 100 Hz, N = 4096, Rectangle Window

- Ignored system noises

- Measurement as low as 1 nV is possible, based on simulation
- Thanks to FFT, system noises can be ignored

Measurement without EMF care

Sampling Rate: 100 kHz, Sample: 10 k, Averaging: 100, Frequency Resolution: 10 Hz

It’s possible to measure as low as 2 μV

EMF countermeasure is essential for further performance

EMF Countermeasure

Upside down Switch IC (4053) contact Heatsink via Copper Tape (GND)

Switch IC (4053) is covered by Styrofoam

Styrofoam Box

EMF Countermear Effectiveness

Initial Condition (Exposed in atmosphere)

- Vin = OPEN
- CMOS SW 4053
- Peripheral Circuit
- Circuit Board
- Offset affected EMF is equivalent to Vin = 1 μV

Improved Condition (Constant Temperature)

- Vin = OPEN
- CMOS SW 4053
- Peripheral Circuit
- Monitor
- Heatsink
- Copper Tape (GND)
- Styrofoam Box
- It's possible to measure as low as Vin = 1 μV

It's possible to measure as low as Vin = 1 μV

Measurement with EMF Countermeasure

Low voltage measurement w/o EMF Countermeasure

![Graph showing Measurable Voltage: 2.0 μV](image)

Low voltage measurement w/ EMF Countermeasure

![Graph showing Measurable Voltage: 0.2 μV](image)

Linearity is improved

• **IBM Watson System** (Medical Area)
  – A lot of medical research papers.
  – Medical doctor cannot read all of them.
  – Watson system can identify the disease name and show its treatment immediately.

**Apply to Modeling Technologies**

A lot of modeling technologies
Papers, text books, patents,...

**Smart database**
Contents

- Target of this talk
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- Modeling Technologies
- Collaboration of Circuit Design and Modeling
- Layout Dependent Effect Modeling
- Electrical and Thermal Effect Modeling
- Device Model Technologies Supported by AI
- **Modeling Education at Gunma Univ.**
- Modeling Research at Gunma Univ.
- Conclusion
- Appendix: Research for Monte Carlo Simulation
Graduate Course Lecture

- By J. Matsuda (16.5 hours)
  MOS Device Physics
  Yannis Tsividis, Colin McAndrew
  Operation and Modeling of the MOS Transistor,

- By Y. Okabe (3 hours)
  Semiconductor Device Modeling

- By A. Motozawa (3 hours)
  PLL Design – From Basics to State-of-the-Art
  System level modeling
Open Seminar

● By S. Yoshitomi, KIOXIA (1.5 hours)
  Semiconductor Device Modeling for RF CMOS Circuit

● By H. Aoki, founder of MoDeCH Inc. (many times)
  Seminar Series of MOS Modeling
  from basics to state-of-the-art
  from fine CMOS to power, high voltage devices
Contents

- Target of this talk
- CMOS and Bipolar
- Device Physics and Model
- Modeling Technologies
- Collaboration of Circuit Design and Modeling
- Layout Dependent Effect Modeling
- Electrical and Thermal Effect Modeling
- Device Model Technologies Supported by AI
- Modeling Education at Gunma Univ.
- **Modeling Research at Gunma Univ.**
- Conclusion
- Appendix: Research for Monte Carlo Simulation
Led by Gunma U. Visiting Professor Hitoshi Aoki from 2014 to 2017

[1] "A Novel Approach for Velocity Saturation Calculations of 90nm N-channel MOSFET”,
   International Conference on Mechanical, Electrical and Medical Intelligent System (Nov. 2017)
[2] “Bias and 1/f Noise Degradation Modeling of 90 nm n-Channel MOSFETs Induced by Hot Carrier Stress”,
   Key Engineering Materials (2016)
[3] “A Study on HCI Induced Gate Leakage Current Model Used for Reliability Simulations in 90nm n-MOSFETs,”
   IEEE International Conference on ASIC (Nov. 2015)
   International Conference on Solid State Devices and Materials (Sept. 2016)
[9] “Study on Maximum Electric Field Modeling Used for HCI Induced Degradation Characteristic of LDMOS Transistors,”
   IEEE International Conference on ASIC (Nov. 2015).
Contents

- Target of this talk
- CMOS and Bipolar
- Device Physics and Model
- Modeling Technologies
- Collaboration of Circuit Design and Modeling
- Layout Dependent Effect Modeling
- Electrical and Thermal Effect Modeling
- Device Model Technologies Supported by AI
- Modeling Education at Gunma Univ.
- Modeling Research at Gunma Univ.

**Conclusion**

- Appendix: Research for Monte Carlo Simulation
Conclusion

● There is a gap between circuit designers and modeling researchers.

● Circuit designers do not fully exploit benefits of modeling research results.

● Their demands may not be conveyed to modeling researchers.

● Hope that this talk can be a bridge between them.
Contents

- Target of this talk
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- Device Physics and Model
- Modeling Technologies
- Collaboration of Circuit Design and Modeling
- Layout Dependent Effect Modeling
- Electrical and Thermal Effect Modeling
- Device Model Technologies Supported by AI
- Modeling Education at Gunma Univ.
- Modeling Research at Gunma Univ.
- Conclusion
- Appendix: Research for Monte Carlo Simulation
Research for Monte Carlo Simulation

Pseudo-Random Signal Generation Algorithm for SPICE Monte Carlo Simulation

Random dots (Monte Carlo Method)
Equivalent-Time Sampling

- Technique for sampling repetitive waveform
- Used in sampling oscilloscope

Waveform under test

Sampling CLK

$T_{CLK}$
Waveform Missing Phenomena

\[ f_{\text{CLK}} \gg f_{\text{sin}} \quad f_{\text{CLK}} \approx \frac{1}{\alpha} f_{\text{sin}} \left( \alpha = \frac{1}{2}, \frac{1}{3}, \frac{2}{3}, \ldots, \frac{1}{6}, \ldots \right) \quad f_{\text{CLK}} \approx f_{\text{sin}} \]

Sampling points move little  → Requires long time
Golden Ratio Sampling

\[ f_{CLK} = \varphi \times f_{sig} \]

\( \varphi \) : Golden ratio ( = 1.6180339887… )

Sampling points disperse uniformly through measurement

[4] Y. Sasaki, Y. Zhao, A. Kuwana, H. Kobayashi,
"Highly Efficient Waveform Acquisition Condition in Equivalent-Time Sampling System"
27th IEEE Asian Test Symposium, Hefei, Anhui, China (Oct. 2018)
Pseudo Random Signal Generation

\[ f_{CLK} = \varphi \times f_{sig} \]

\( \varphi \) : Golden ratio ( = 1.6180339887… )

Our proposal:
Pseudo Random Signal With Uniform Distribution

Sampling points disperse uniformly