2D-MO1-2 Invited **Room C**
16:15-16:40 March 7, 2021 (Mon)

Modeling Technologies from Analog/Mixed-Signal Circuit Designer Viewpoint

Haruo Kobayashi, Hitoshi Aoki, Jun-ichi Matsuda
Yushiro Okabe, Atsushi Motozawa, Anna Kuwana

Gunma University
Teikyo Heisei University
Renesas Electronics

群馬大学
GUNMA UNIVERSITY

Self Introduction

Haruo Kobayashi: Professor, Gunma Univ.
Mixed-Signal IC Design & Testing

Hitoshi Aoki: Professor, Teikyo Heisei Univ. , Founder of MoDeCH Inc.
Device Modeling

Jun-ichi Matsuda: Visiting Professor, Gunma Univ., Formerly Sanyo Electric
Device Physics

Yushiro Okabe: Adjunct Associate Professor, Gunma Univ., Formerly Sanyo Electric
Device Modeling

Atsushi Motozawa: Renesas Electronics, Adjunct Lecturer, Gunma Univ.
Mixed-Signal IC Design

Anna Kuwana: Assistant Professor, Gunma Univ.
Computer Fluid Dynamics

Contents

- Target of this talk
- CMOS and Bipolar
- Device Physics and Model
- Modeling Technologies
- Collaboration of Circuit Design and Modeling
- Layout Dependent Effect Modeling
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- Modeling Research at Gunma Univ.
- Conclusion
- Appendix: Research for Monte Carlo Simulation

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Target of This Talk

Address
what the circuit designer expects
to device modeling technologies
as a model user

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CMOS and Bipolar

- Why so many CMOS models ?
- How about Bipolar ?
  - Bipolar ICs are still used in analog companies

First Encounter to Modeling Technology

Educated by Prof. Asad Abidi, at UCLA, in 1990

CMOS

CMOS device structure is simple.

However, its accurate modeling is difficult.

- That is why so many CMOS models.

Bipolar

Bipolar transistor device structure is complicated.

However, its accurate modeling is relatively easy.

- That is why only a few bipolar transistor models.

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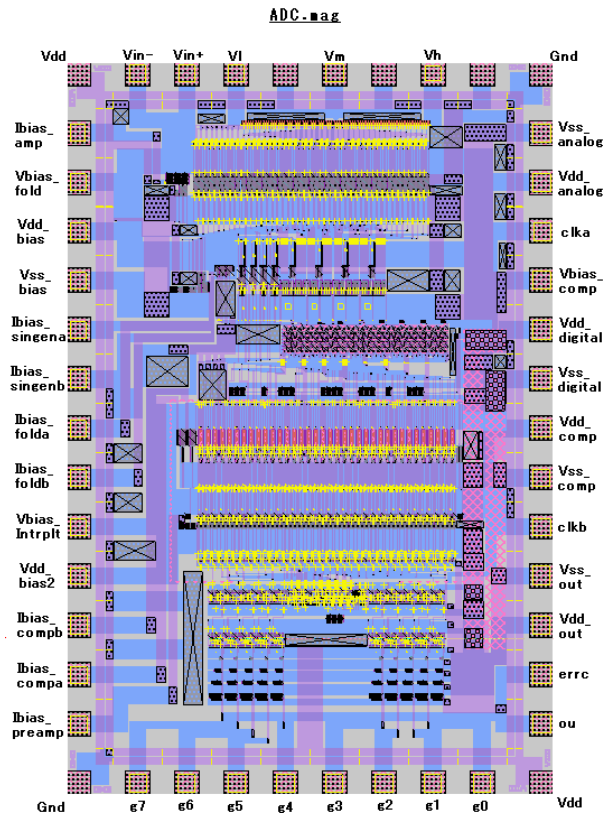
Device Physics and Model

Device physics is difficult
for the circuit designer to learn.

Modeling is good
to learn device physics.

Interface Between Circuit and Device

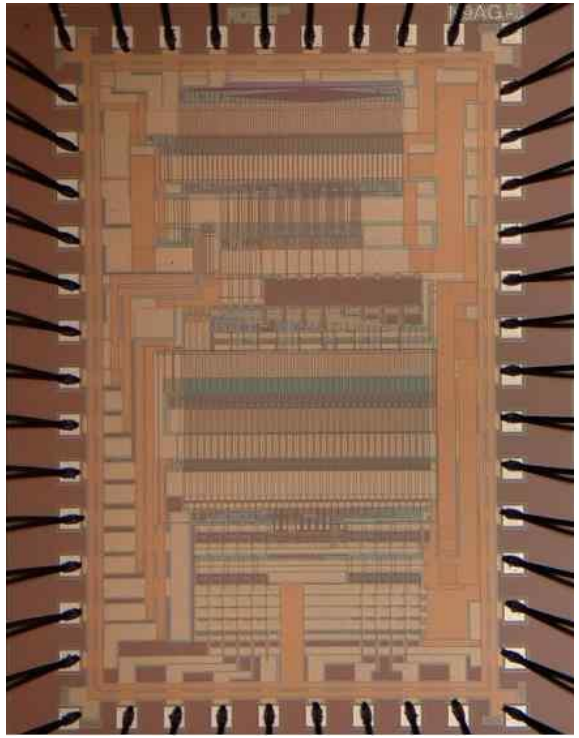
- Circuit designer
- Fabless company



- Device, process researcher
- Foundry company

Interface

- Mask data
- Device model
- Model parameters



Mead-Conway method

C. Mead and L. Conway, Introduction to VLSI Systems, Addison-Wesley, 1980.

Physical and Mathematical Models

- Physical model
  with limited fitting parameters
  is desirable.

- Pure mathematical model is
  often difficult to use.

CMOS Modeling: Mathematical and Physical

BSIM2

Mathematical model

Lectured by Sanyo Electric Corp in 2000

BSIM3

- Physical model
- Based on CMOS device physics (+ fitting parameters)

Device, process parameter values in model

⇨ Prediction of MOS characteristics

change

Modeling and Prediction

Prof. Syukuro Manabe
Nobel Prize Winner in Physics, 2021

"For the physical modeling of Earth's climate,
quantifying variability and
reliably predicting global warming"

His model can predict:

CO_2 increase ⇨ global warming

Prediction is essential in modeling technology

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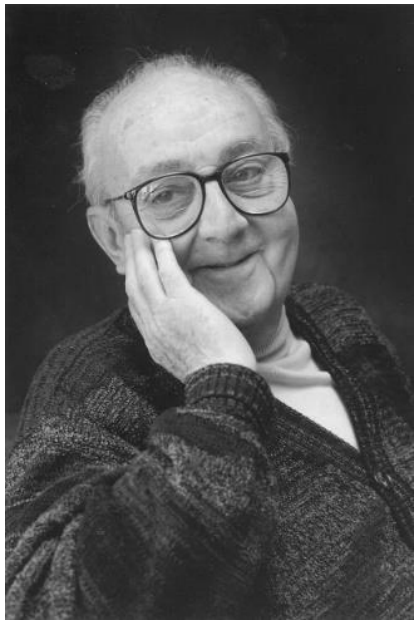
Modeling Technologies

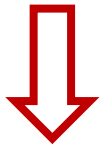
Statistics



"All models are wrong, but some are useful".

George E. P. Box

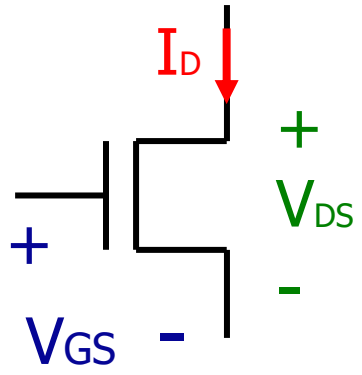
British statistician, 1919-2013



Device model

MOS model needs to be accurate
only in the region where the designed circuit operates.

Circuit Designer: Application Oriented Mind



High frequency CMOS circuit design

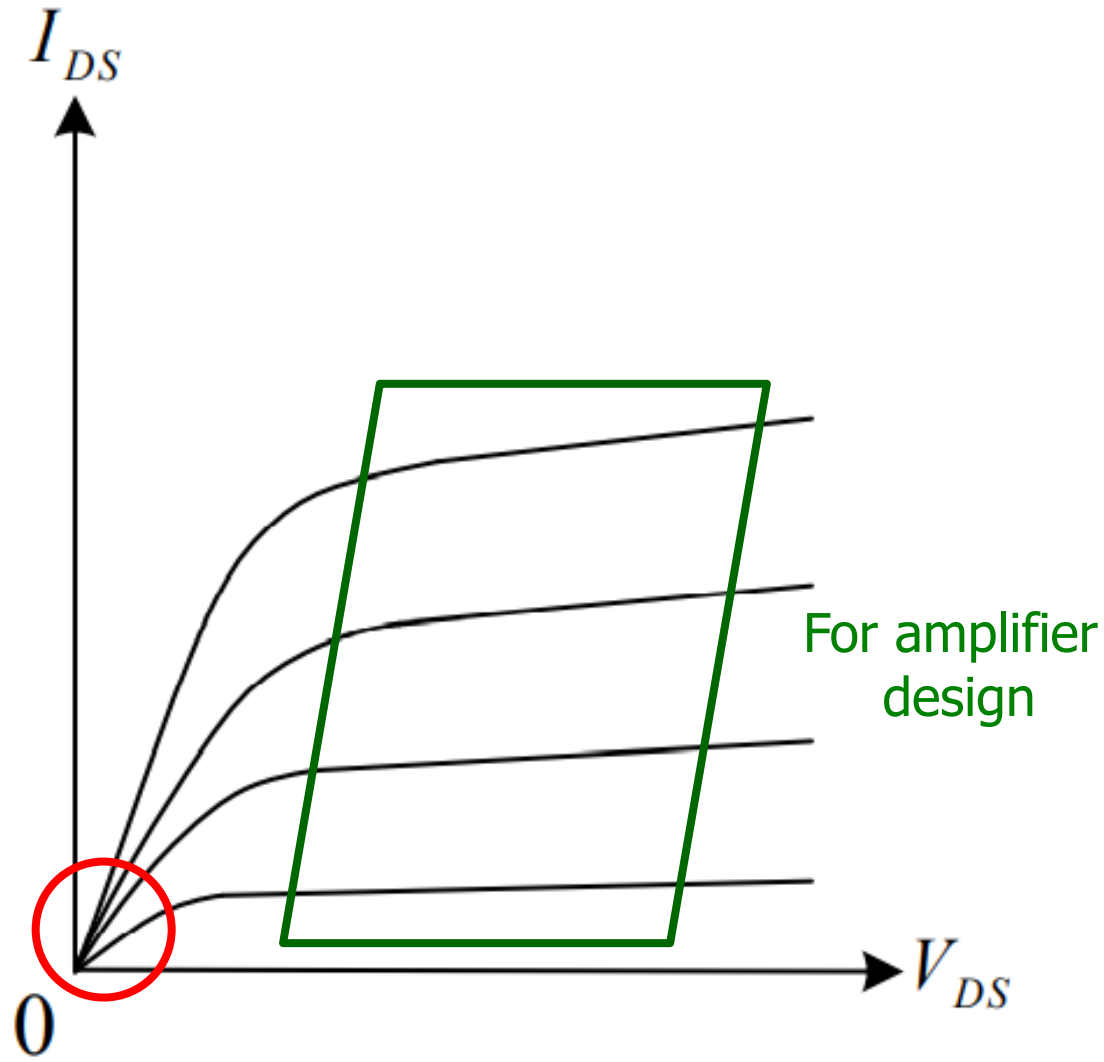
⇩

RF-CMOS model

Modeling should be accurate
in the focused region

⇩

The other regions do NOT matter



Modeling for FinFET Analog Circuit

Myth

Fine CMOS: Characteristics deteriorate for analog circuit performance

Truth

FinFET: Characteristics improve for analog circuit performance

- Large r_{out}, g_m
- Small Drain-Induced Barrier Lowering (DIBL) effect
- No body effect

Research for FinFET Analog Circuit

Strong research motivation
for analog circuit design with FinFET
- New frontier
- Challenging

~~"All models are wrong, but some are useful".~~

Model should be correct in all operating regions

- Perfect FinFET model for analog circuit with layout dependency information is desired.
- Access to FinFET process is difficult; high cost
- Chip implementation and measurement verification are not easy.

BSIM-CMG FinFET Model

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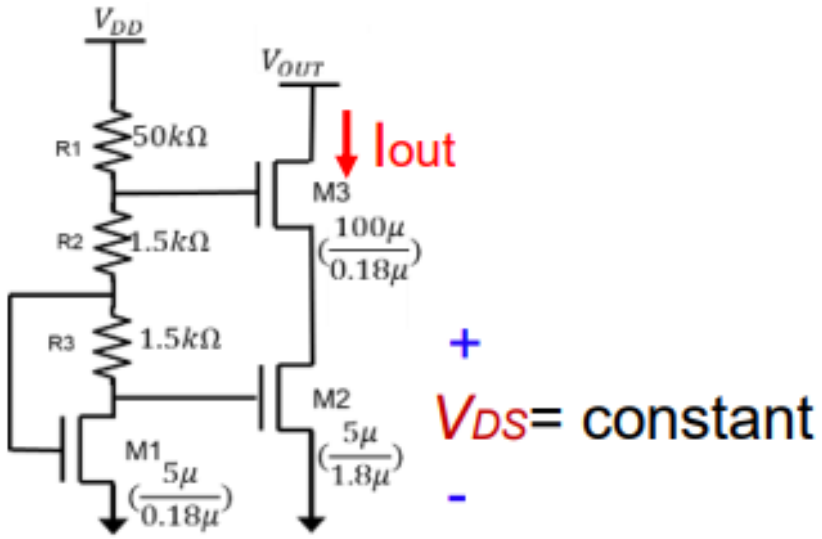
Topic Collaboration of Circuit Design and Modeling

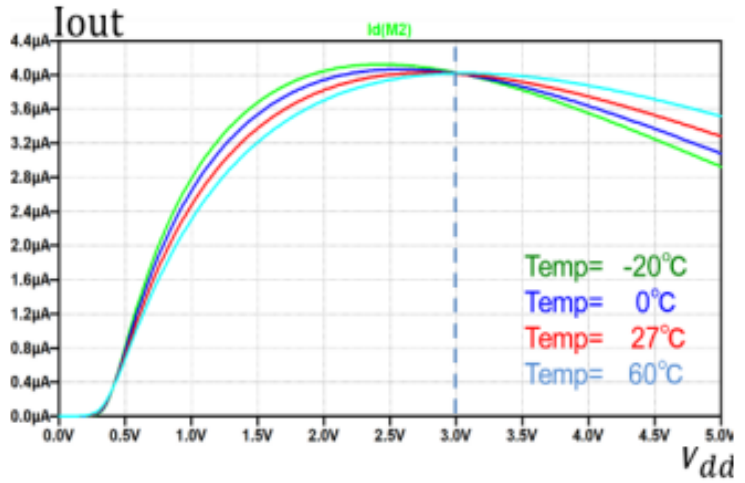
Many circuit designers use CMOS model and SPICE parameters from foundry as black box.

For analog circuit design with a small number of MOSFETs, collaboration between circuit designer and modeling researcher is effective.

Reference Current Source

Insensitive to Supply Voltage and Temperature

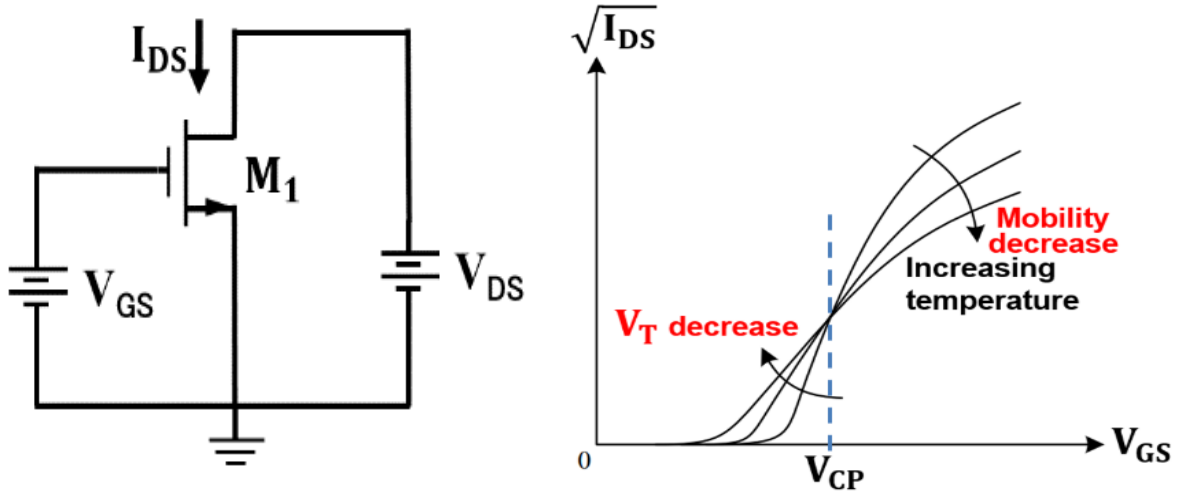




Current source insensitive to temperature and supply voltage

[1] T. Kamio, T. Hosono, S. Yamamoto, J. Matsuda, S. Katayama, A. Kuwana, A. Suzuki, S. Yamada, T. Kato, N. Ono, K. Miura H. Kobayashi, "Design Consideration on MOS Peaking Current Sources Insensitive to Supply Voltage and Temperature", International Conference on Analog VLSI Circuits, Bordeaux, France (Oct. 2021)

Drain Current Temperature Characteristics



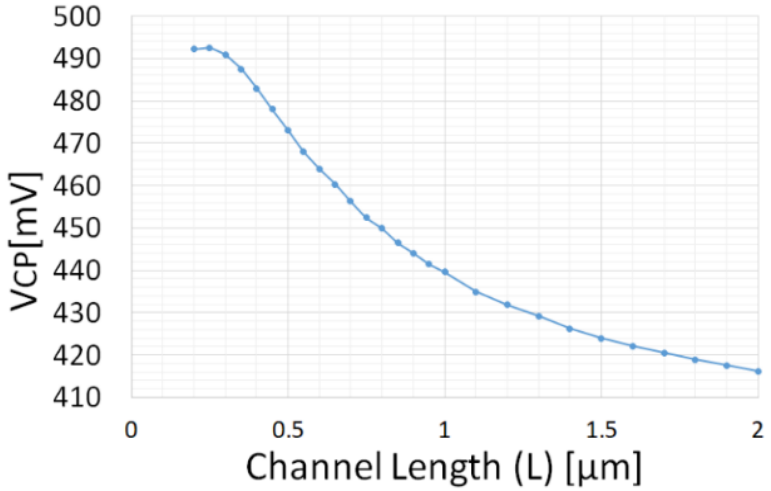
NMOS drain current temperature characteristics

- For $V_{GS} = V_{CP}$, I_{DS} is insensitive to temperature.
- At high temperature,
  For $V_{GS} < V_{CP}$, I_{DS} becomes larger

  For $V_{GS} > V_{CP}$, I_{DS} becomes smaller.

MOS device, modeling researcher interpretation is useful.

VCP and Small Channel Length *L*

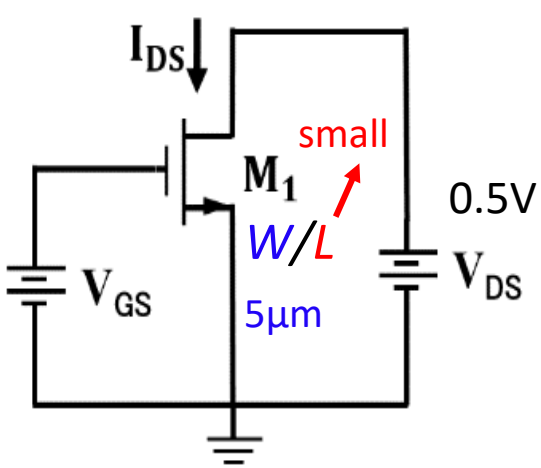


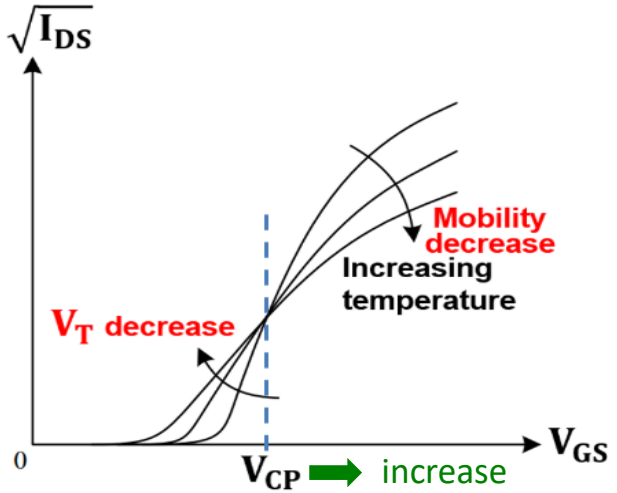
SPICE simulation result
with BSIM3v3 model parameters

L → small ➡ VCP → increase

Explained by short channel effect

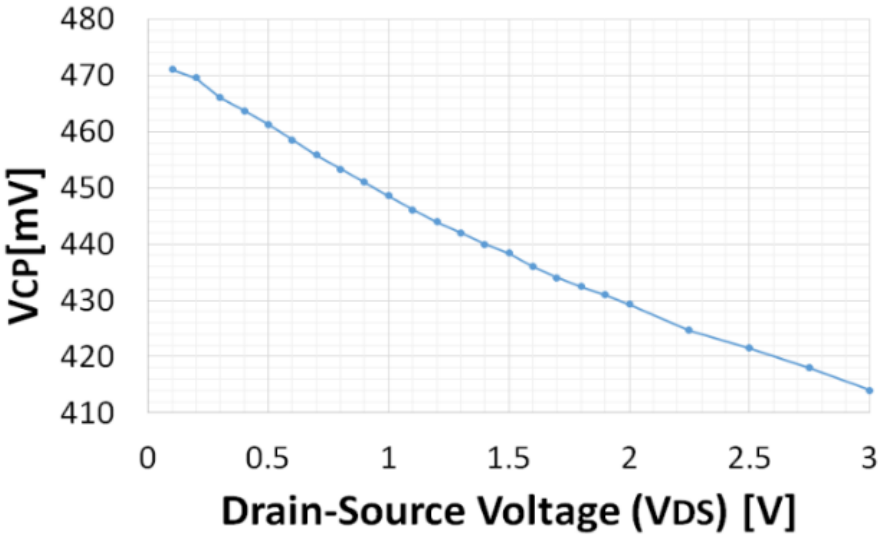
using BSIM3v3 model equations





NMOS drain current temperature characteristics

V_{CP} and Drain-Source Voltage V_{DS}

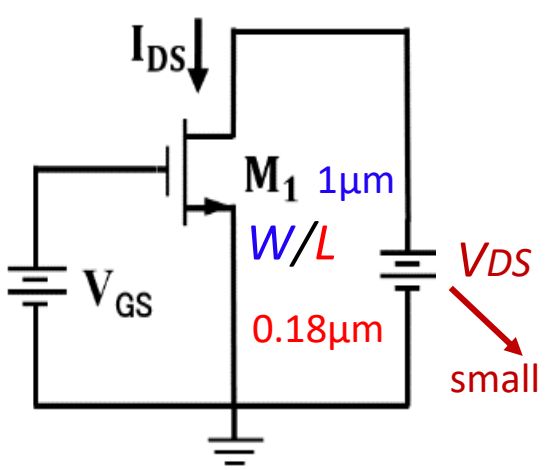


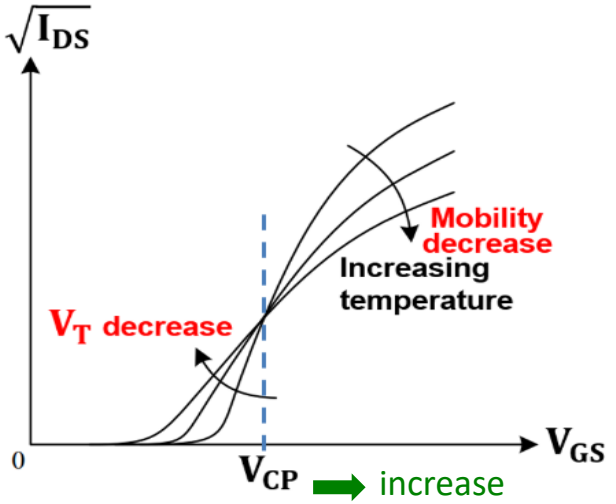
SPICE simulation result
with BSIM3v3 model parameters

V_{DS} → small ➡ V_{CP} → increase

Explained by
drain induced barrier lowering *(DIBL)*

using BSIM3v3 model equations





NMOS drain current temperature characteristics

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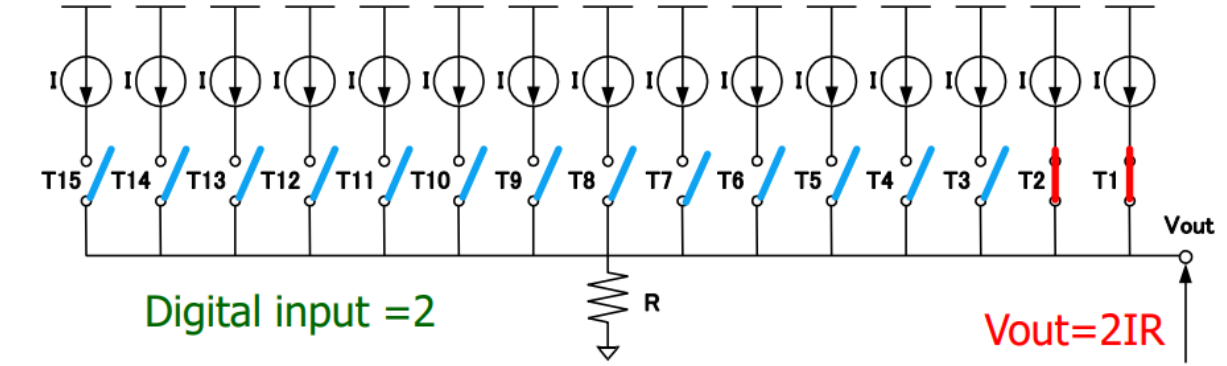
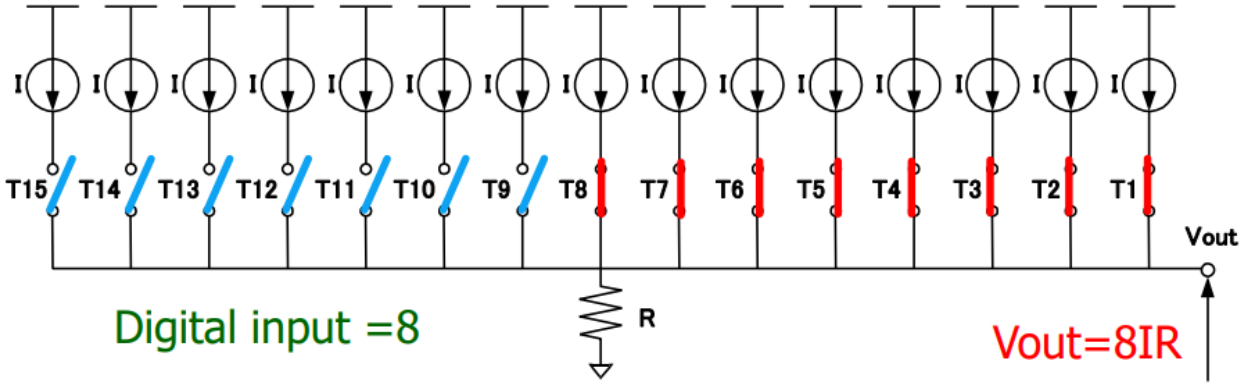
Digital-to-Analog Converter (DAC)

Unary DAC

Configuration
&
Operation



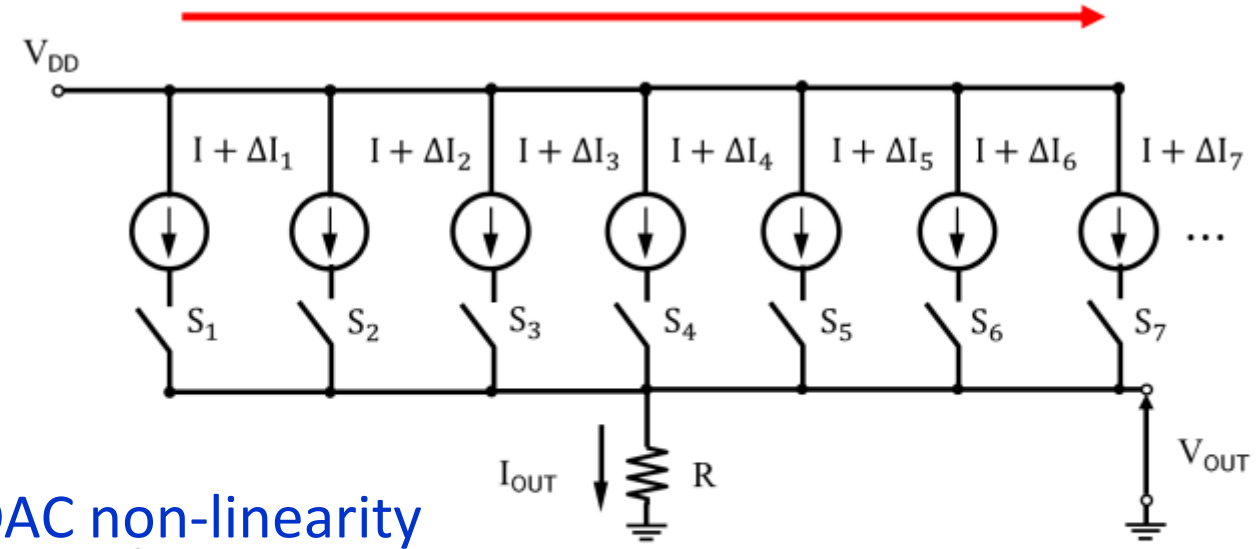


Actual DAC Circuits on IC

Current source mismatch ΔI_k

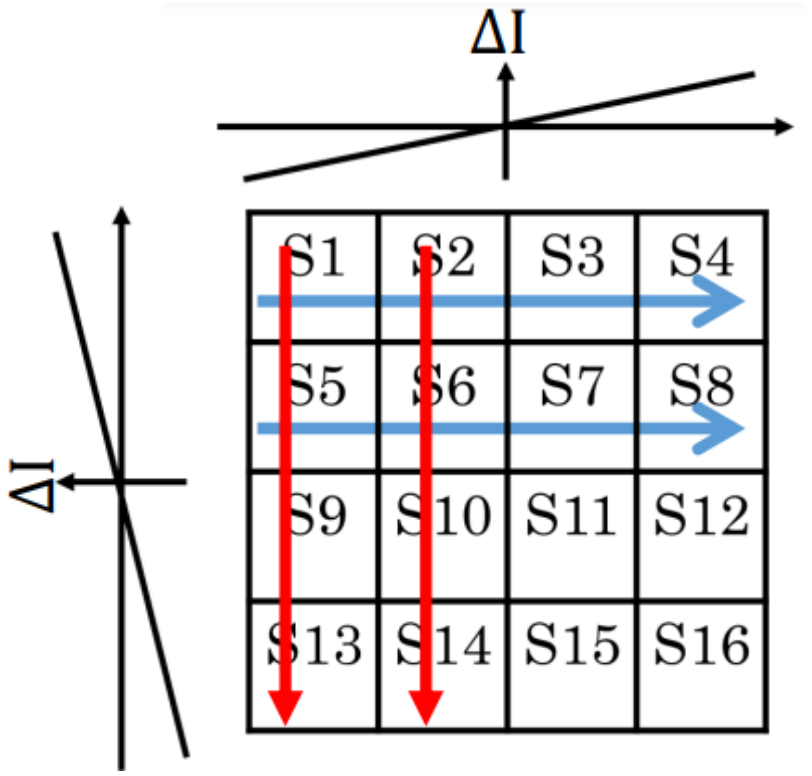
⇩

Systematic gradient ΔI_k

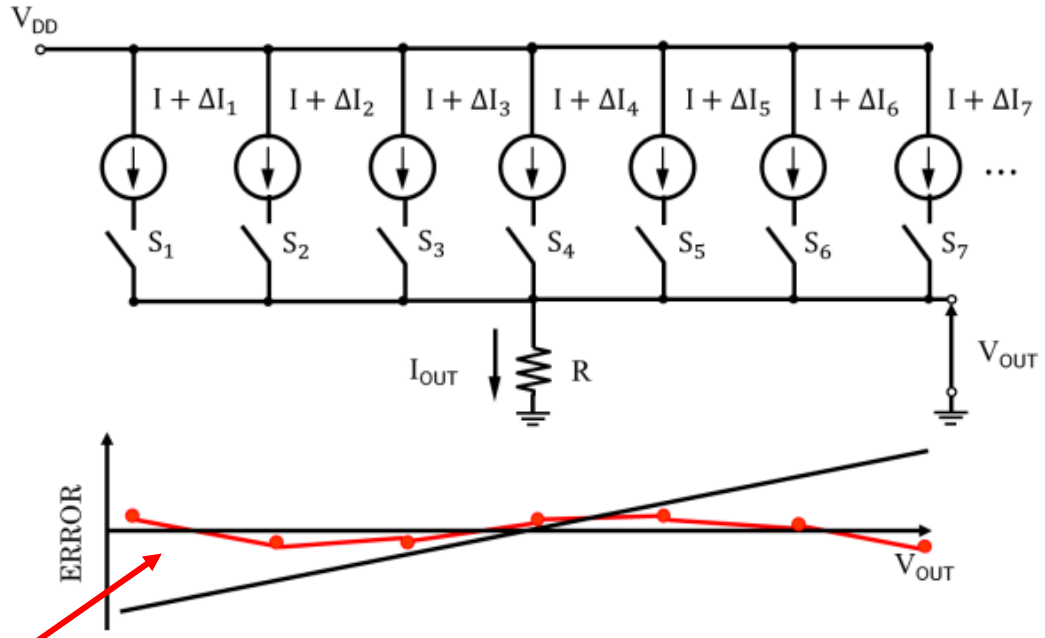


DAC non-linearity

Digital-to-Analog Converter (DAC) Nonlinearity



S4	S8	S12	S5
S14	S10	S6	S1
S9	S13	S2	S15
S3	S7	S16	S11



Regular layout

Random layout

Current source mismatch ΔI_k

Layout dependent

DAC nonlinearity

Cancelled

Layout Dependent Effect Modeling

DAC nonlinearity due to mismatch

⇩

Important issue

⇩

Accurate mismatch modeling is desired.

Many layout algorithms

Chess

Knight

1	48	31	50	33	16	63	18
30	51	46	3	62	19	14	35
47	2	49	32	15	34	17	64
52	29	4	45	20	61	36	13
5	44	25	56	9	40	21	60
28	53	8	41	24	57	12	37
43	6	55	26	39	10	59	22
54	27	42	7	58	23	38	11

260 260

8x8 Euler's Knight Tour

[2] D. Yao, A. Kuwana, H. Kobayashi, K. Kawauchi
"Digital-to-Analog Converter Linearity Improvement Technique Based on Classical Number Theory for Modern ULSI"
30th International Workshop on Post-Binary ULSI Systems (May 2021)

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Topic Electrical and Thermal Effect Modeling

Thermal effect modeling is expected:

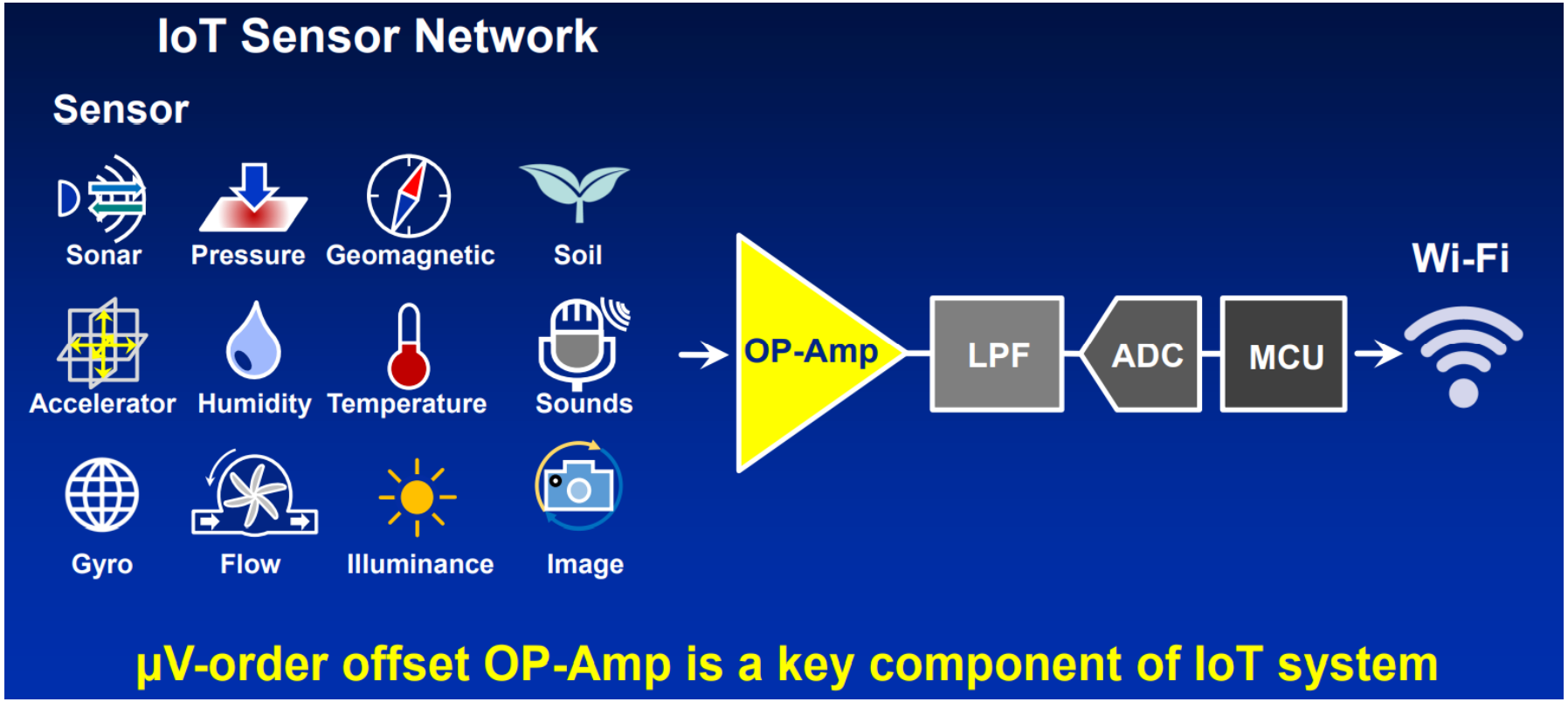
- Power device and circuit
- High precision measurement circuit
- Audio amplifier
  - ⇨ Thermal tail problem

Self-heating, affect from nearby thermal sources

Thermal Effect for High Precision Measurement Circuit

Electric Motive Force (EMF):

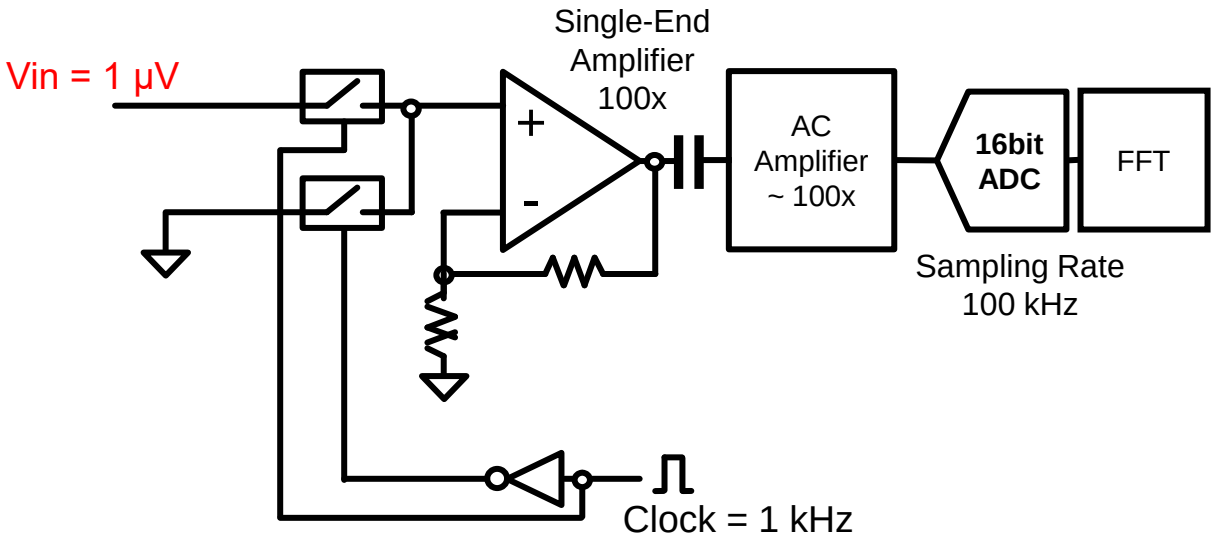
Issue for high precision μV-order voltage measurement circuit



[3] Y. Sasaki, K. Machida, R. Aoki, S. Katayama, T. Nakatani, J. Wang, K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, A. Kuwana, K. Hatayama, H. Kobayashi,
"Accurate and Fast Testing Technique of Operational Amplifier DC Offset Voltage in μV-order by DC-AC Conversion"
3rd IEEE International Test Conference in Asia, Tokyo (Sept. 2019).

FFT-Based DC-AC Conversion

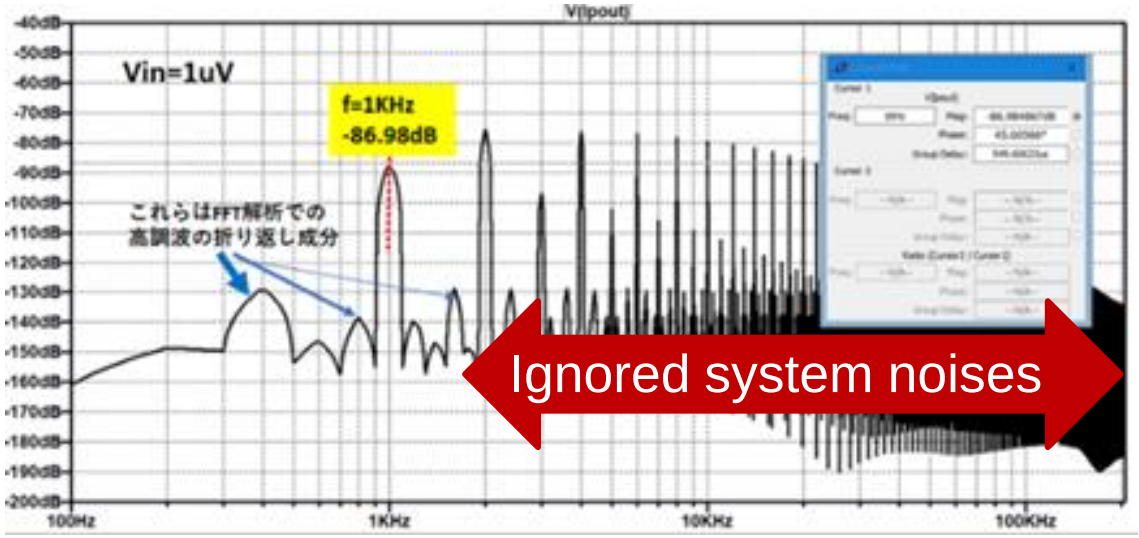
DC-AC Conversion Circuit



DC−AC Conversion Clock: 1 kHz (duty 50 %)

CMOS Switch: Nch FET (2N4393)

FFT Result



LTspice FFT Condition:

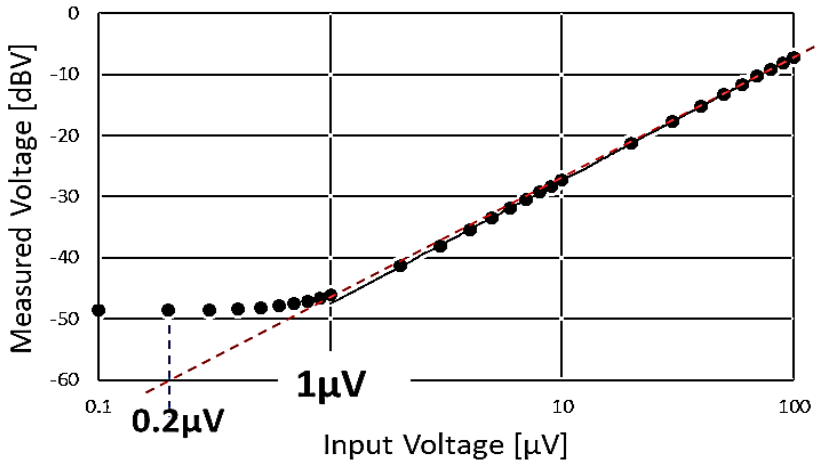
Fs = 409.6 kHz, Fres = 100 Hz, N = 4096, Rectangle Window

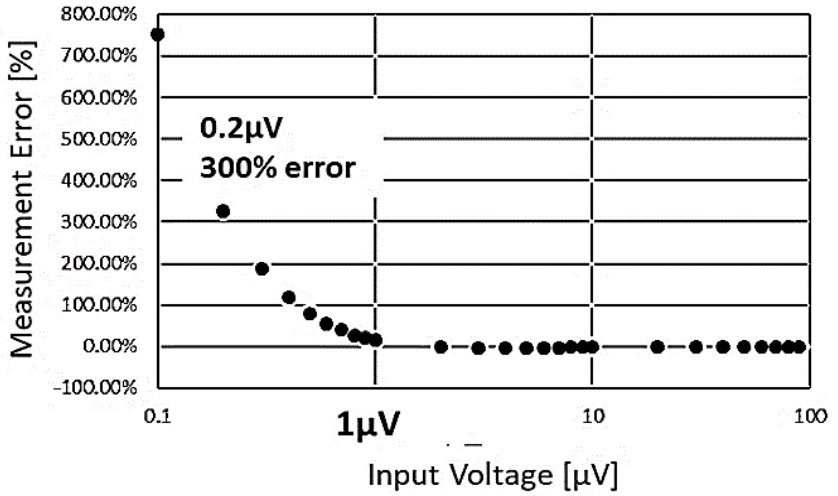
- ✓ Measurement as low as 1 nV is possible, based on simulation
- ✓ Thanks to FFT, system noises can be ignored

[3] Y. Sasaki, T. Nakatani, et. al.,
"Accurate and Fast Testing Technique of Operational Amplifier DC Offset Voltage in μV-order by DC-AC Conversion",
3rd IEEE International Test Conference in Asia, Tokyo (Sept. 2019).

Measurement without EMF care

Sampling Rate: 100 kHz, Sample: 10 k, Averaging: 100, Frequency Resolution: 10 Hz





It’s possible to measure as low as 2 μV

EMF countermeasure is essential for further performance

EMF: Electromotive

[3] Y. Sasaki, T. Nakatani, et. al.,
"Accurate and Fast Testing Technique of Operational Amplifier DC Offset Voltage in μV-order by DC-AC Conversion",
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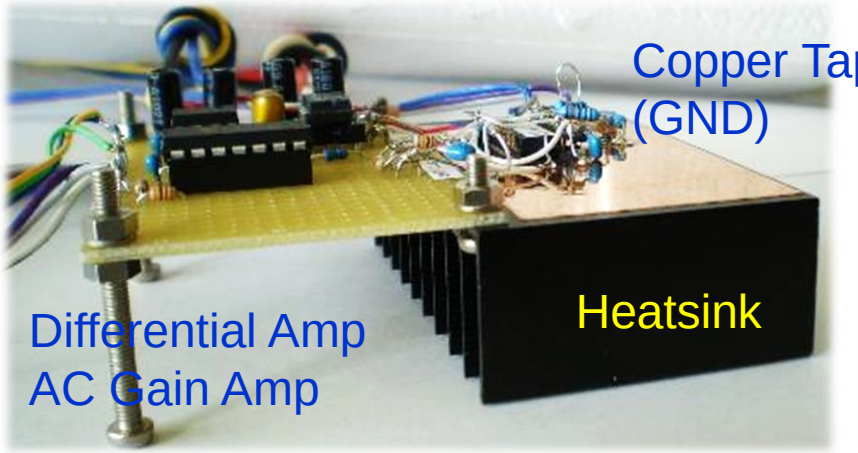
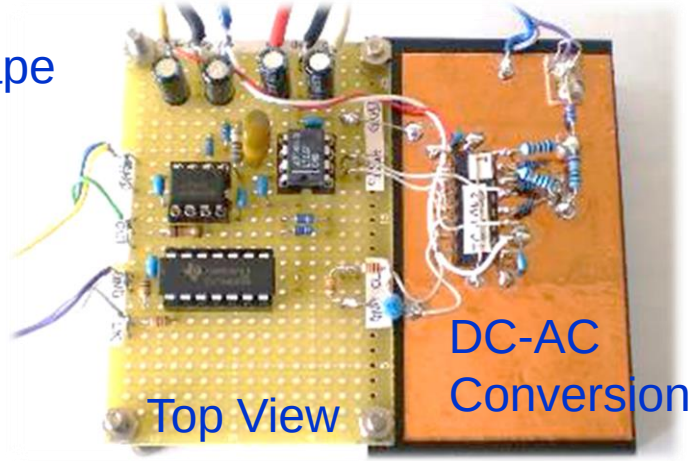
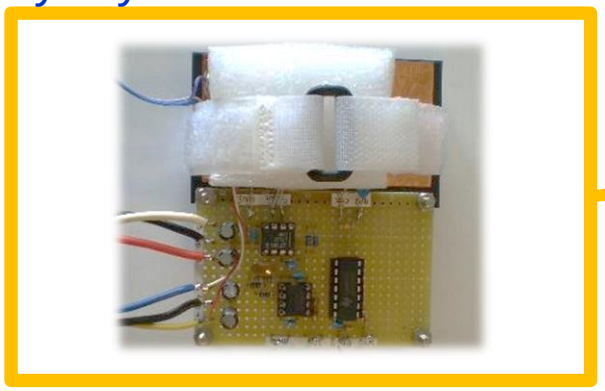
EMF Countermeasure

Upside down Switch IC (4053) contact Heatsink via Copper Tape (GND)

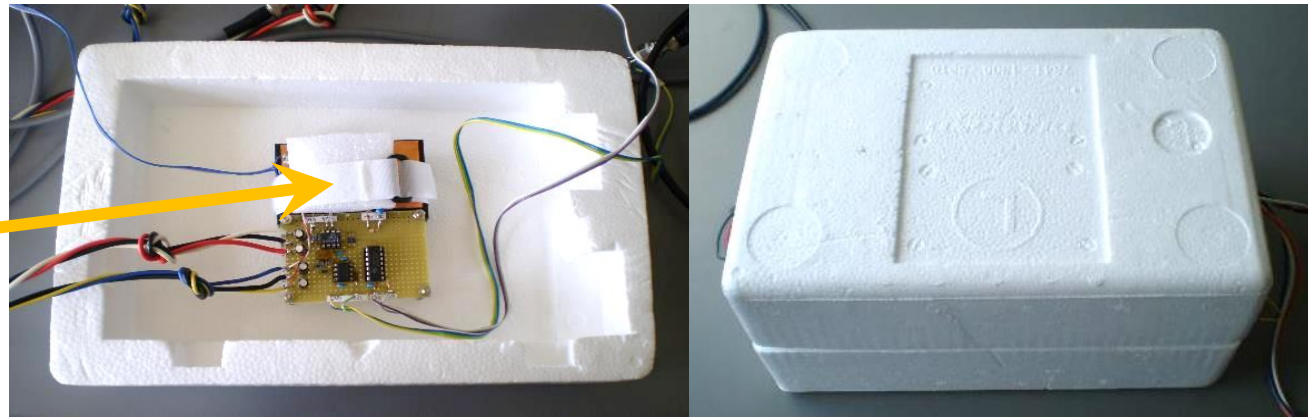




Switch IC (4053) is covered by Styrofoam



Styrofoam Box



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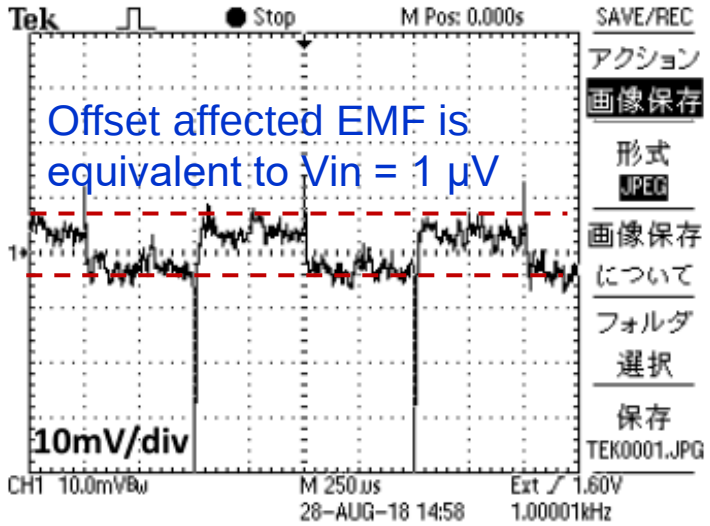
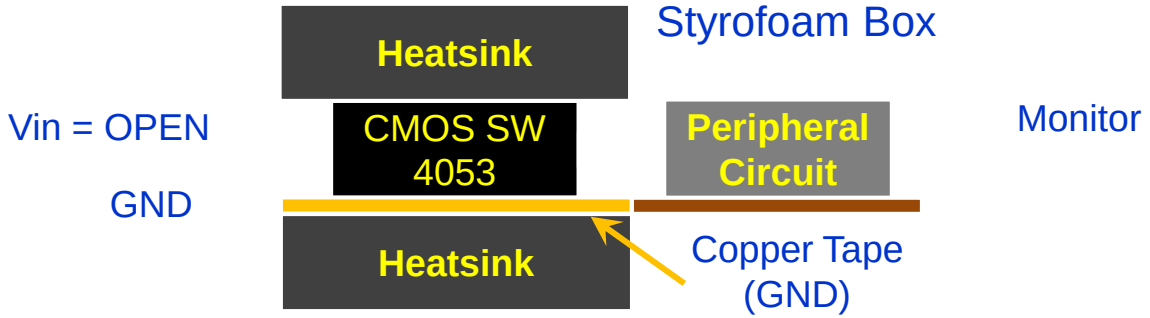
EMF Countermeasure Effectiveness

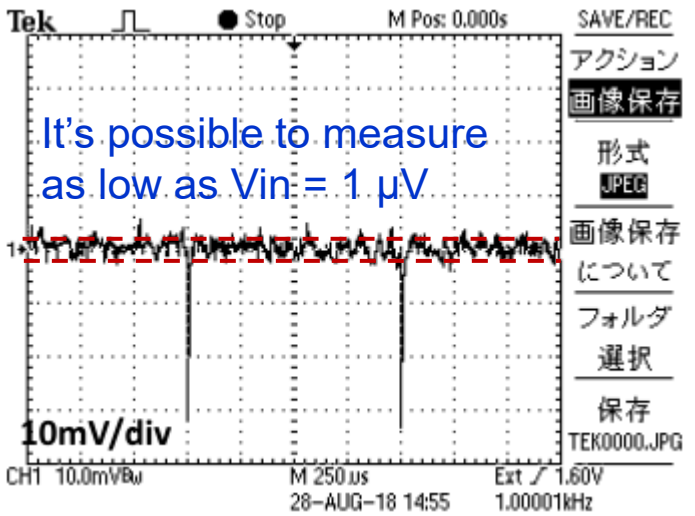
Initial Condition (Exposed in atmosphere)



EMF affects output

Improved Condition (Constant Temperature)



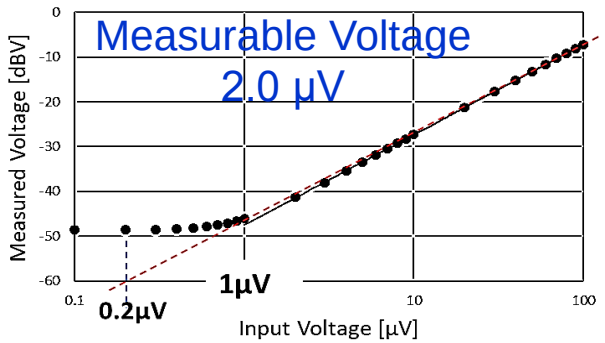


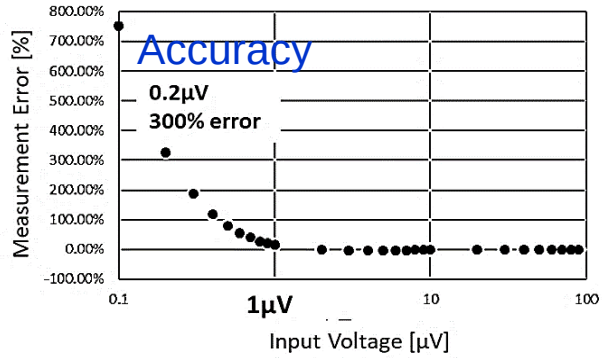
Significant Improvement

[3] Y. Sasaki, T. Nakatani, et. al.,
"Accurate and Fast Testing Technique of Operational Amplifier DC Offset Voltage in μV-order by DC-AC Conversion",
3rd IEEE International Test Conference in Asia, Tokyo (Sept. 2019).

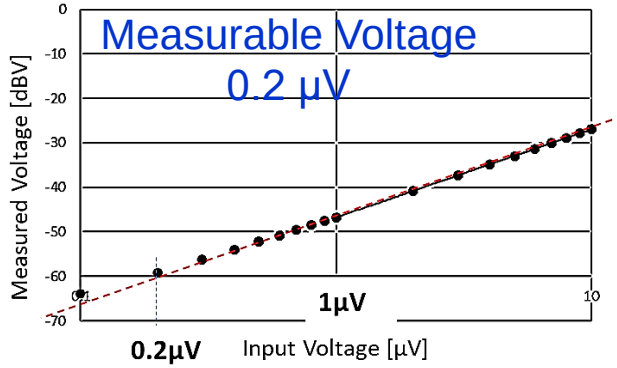
Measurement with EMF Countermeasure

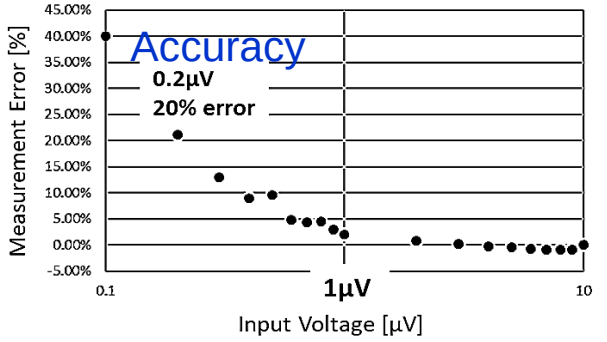
Low voltage measurement
w/o EMF Countermeasure





Low voltage measurement
w/ EMF Countermeasure





Linearity is improved

[3] Y. Sasaki, T. Nakatani, et. al.,
"Accurate and Fast Testing Technique of Operational Amplifier DC Offset Voltage in μV-order by DC-AC Conversion",
3rd IEEE International Test Conference in Asia, Tokyo (Sept. 2019).

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- Modeling Education at Gunma Univ.
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Topic Device Model Technologies Supported by AI

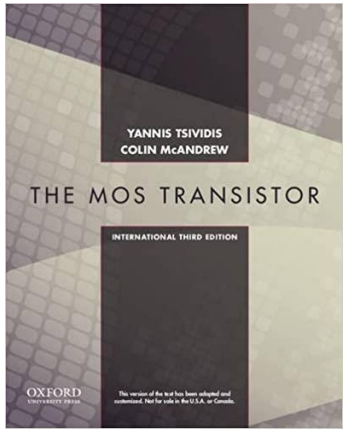
- IBM Watson System (Medical Area)
  - A lot of medical research papers.
  - Medical doctor cannot read all of them.
  - Watson system can identify the disease name and show its treatment immediately.

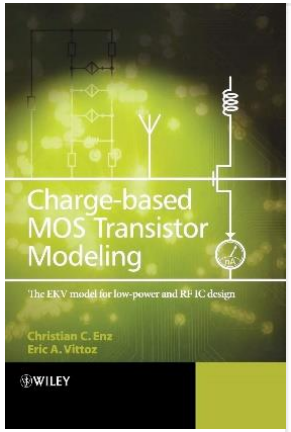
⇩

Apply to Modeling Technologies

A lot of modeling technologies
Papers, text books, patents,…

Smart database





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Topic Modeling Education at Gunma Univ. (1)

Graduate Course Lecture

- By J. Matsuda (16.5 hours)
  MOS Device Physics
  Yannis Tsividis, Colin McAndrew
  Operation and Modeling of the MOS Transistor,
  3rd edition, Oxford U. Press (2011)
- By Y. Okabe (3 hours)
  Semiconductor Device Modeling
- By A. Motozawa (3 hours)
  PLL Design – From Basics to State-of-the-Art
  System level modeling

Modeling Education at Gunma Univ. (2)

Gunma University Analog Integrated Circuit Society (GAIN)

Open Seminar

- By S. Yoshitomi, KIOXIA (1.5 hours)
  Semiconductor Device Modeling for RF CMOS Circuit

- By H. Aoki, founder of MoDeCH Inc. (many times)
  Seminar Series of MOS Modeling
  from basics to state-of-the-art
  from fine CMOS to power, high voltage devices

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Topic Modeling Research at Gunma University

Led by Gunma U. Visiting Professor Hitoshi Aoki from 2014 to 2017

[1] "A Novel Approach for Velocity Saturation Calculations of 90nm N-channel MOSFET”, International Conference on Mechanical, Electrical and Medical Intelligent System (Nov. 2017)

[2] “Bias and 1/f Noise Degradation Modeling of 90 nm n-Channel MOSFETs Induced by Hot Carrier Stress”, Key Engineering Materials (2016)

[3] “A Study on HCI Induced Gate Leakage Current Model Used for Reliability Simulations in 90nm n-MOSFETs,” IEEE International Conference on ASIC (Nov. 2015)

[4] “Gate Voltage Dependent 1/f Noise Variance Model Based on Physical Noise Generation Mechanisms in n-Channel Metal-Oxide-Semiconductor Field-Effect Transistors”, Japanese Journal of Applied (Feb. 2015).

[5] “A Typical MOSFET Modeling Procedure for RF Analog Circuit Design”, Key Engineering Materials (2016)

[6] “Self-Heat Characterizations and Modeling of Multi-finger n-MOSFETs for RF-CMOS Applications”, IEEE Tran. Electron Devices (Sept. 2015).

[7] “A New Self-heat Modeling Approach for LDMOS Devices”, Key Engineering Materials (2015).

[8] "Study on ON-Resistance Degradation Modeling Used for HCI Induced Degradation Characteristic of LDMOS Transistors", International Conference on Solid State Devices and Materials (Sept. 2016)

[9] “Study on Maximum Electric Field Modeling Used for HCI Induced Degradation Characteristic of LDMOS Transistors,” IEEE International Conference on ASIC (Nov. 2015).

[10] "Electron Mobility and Self-Heat Modeling of AlN/GaN MIS-HEMTs with Embedded Source Field-Plate Structures ", IEEE Compound Semiconductor Integrated Circuit Symposium (Oct. 2016)

[11] “A High Precision IGBT Macro-Model for Switching Simulations,” Key Engineering Materials (2016).

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Conclusion

- There is a gap
  between circuit designers and modeling researchers.
- Circuit designers do not fully exploit
  benefits of modeling research results.
- Their demands may not be conveyed to modeling researchers.
- Hope that this talk can be a bridge between them.

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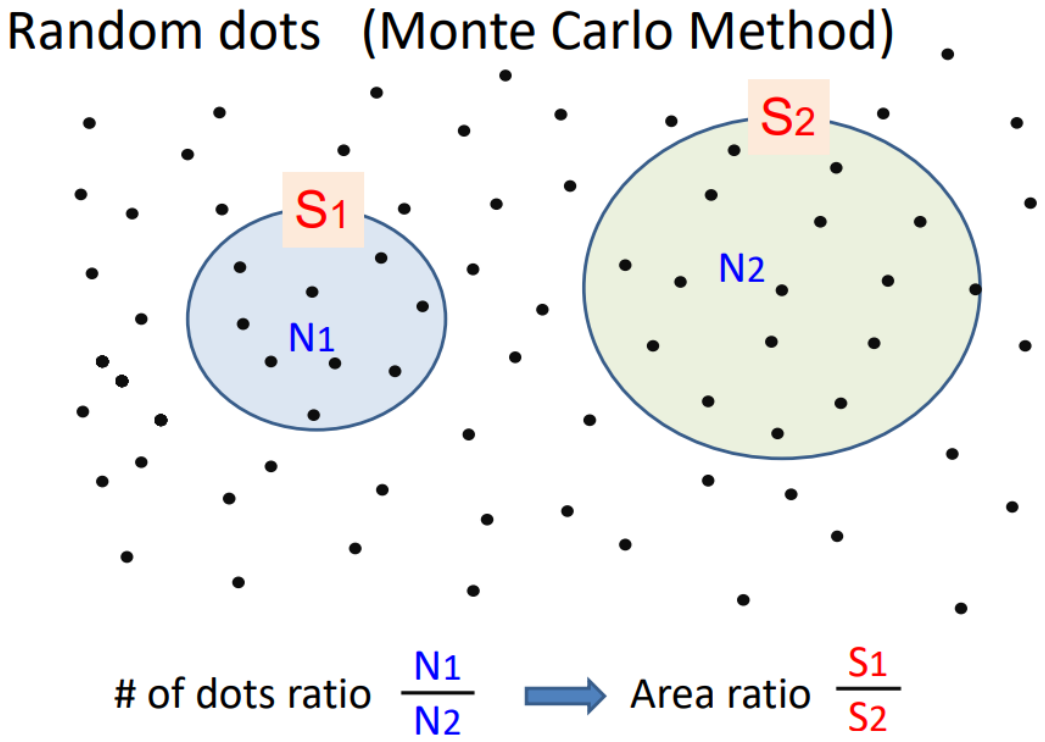
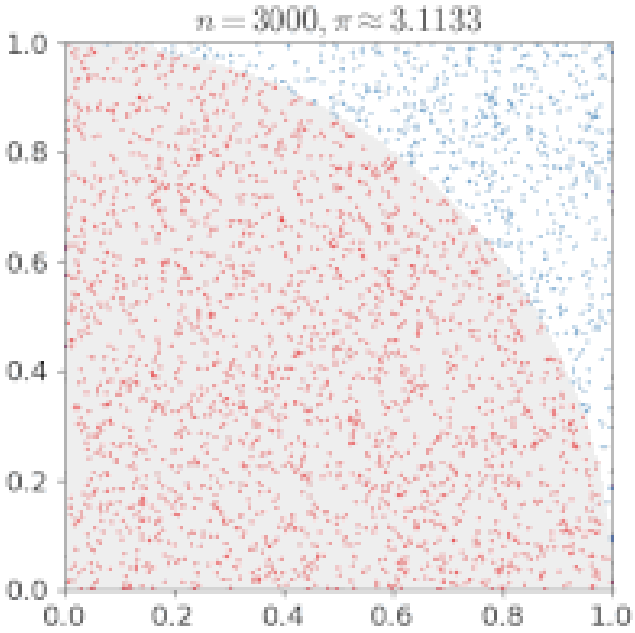
Research for Monte Carlo Simulation

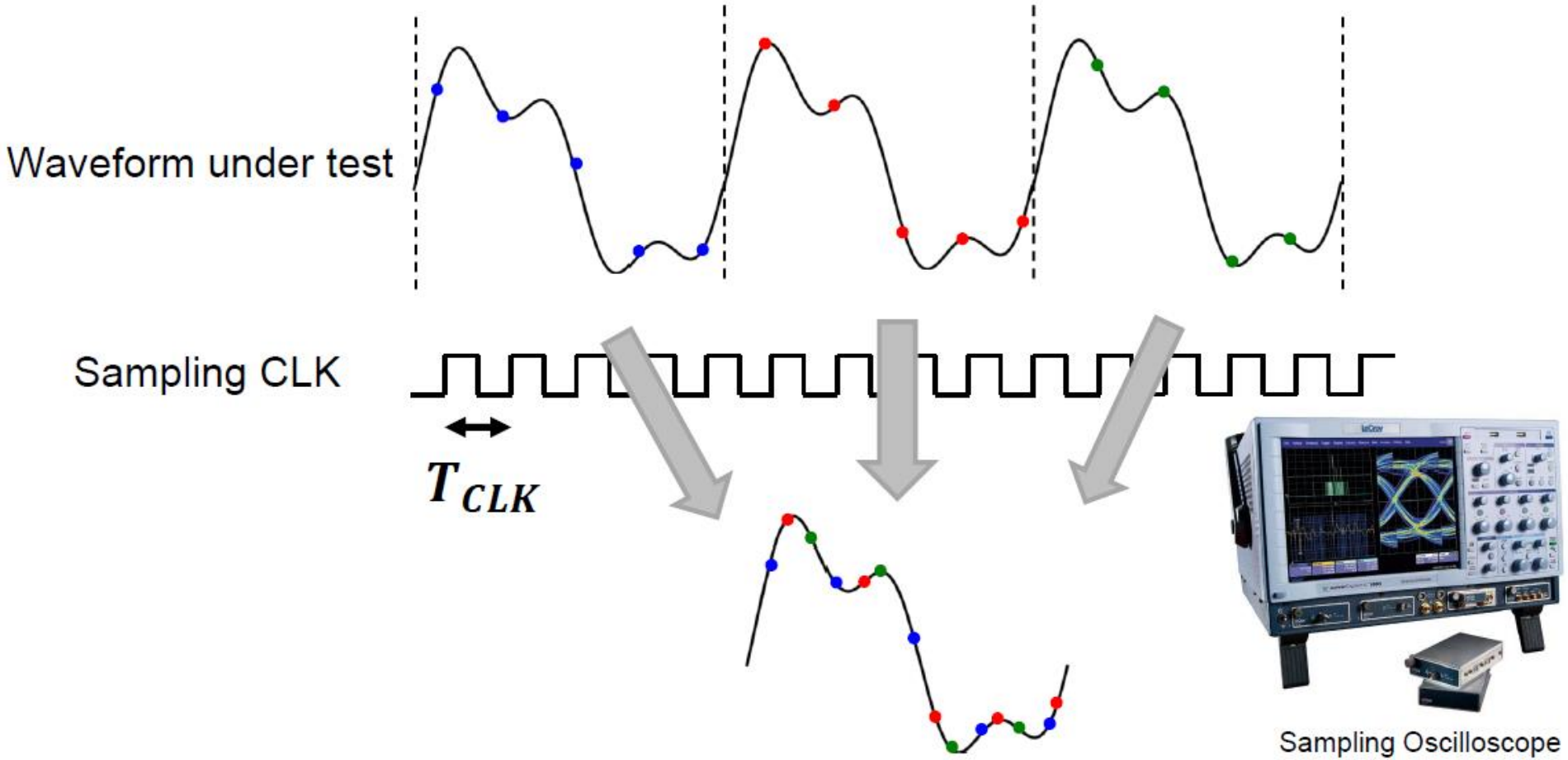
Pseudo-Random Signal Generation Algorithm for SPICE Monte Carlo Simulation





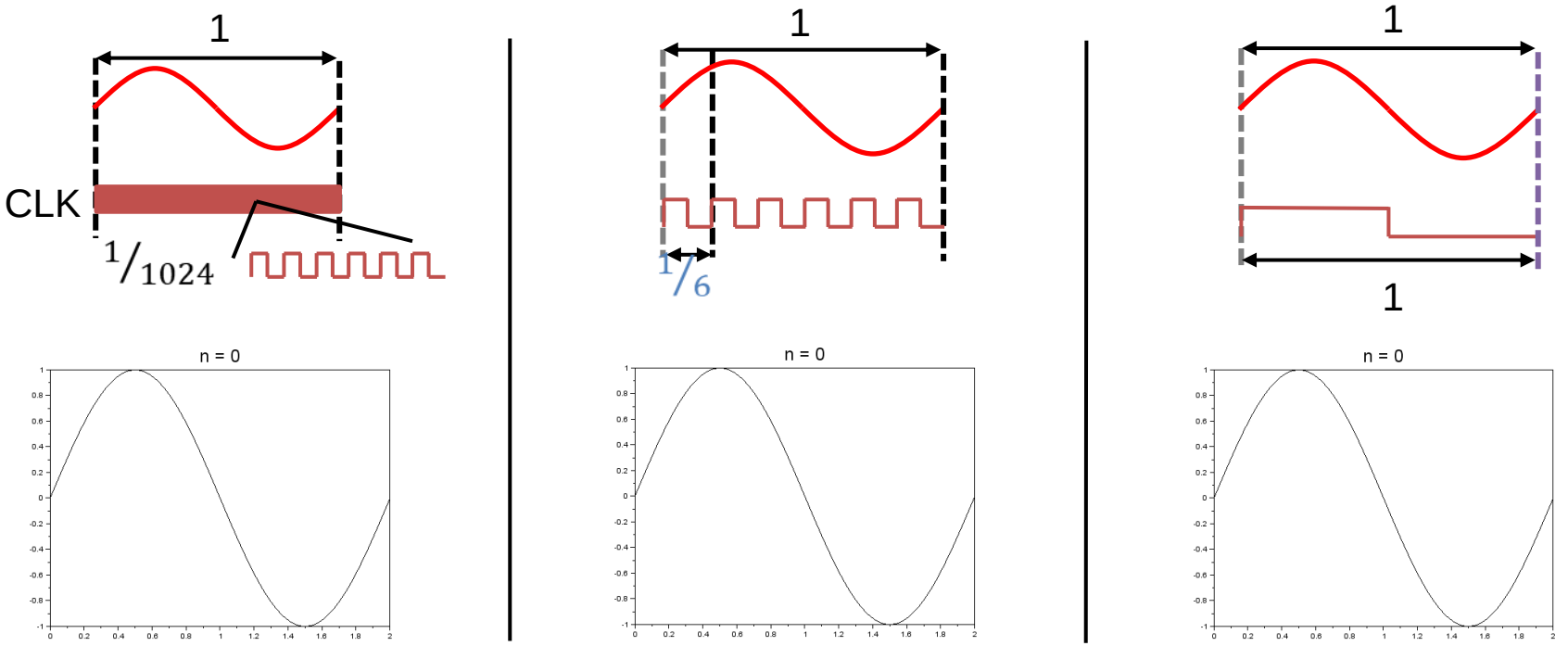
Equivalent-Time Sampling

- Technique for sampling repetitive waveform
- Used in sampling oscilloscope



Waveform Missing Phenomena

$f_{CLK} \gg f_{sin}$ $f_{CLK} \approx \frac{1}{\alpha} f_{sin} \left(\alpha = 1, \frac{1}{2}, \frac{1}{3}, \frac{2}{3}, \cdots, \frac{1}{6}, \cdots\right)$ $f_{CLK} \approx f_{sin}$

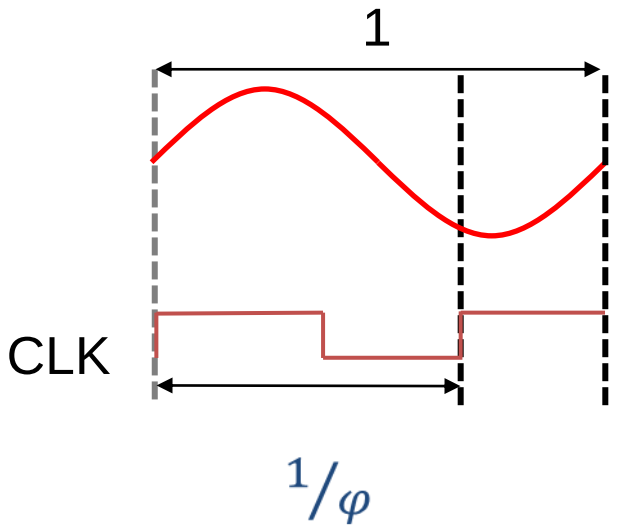


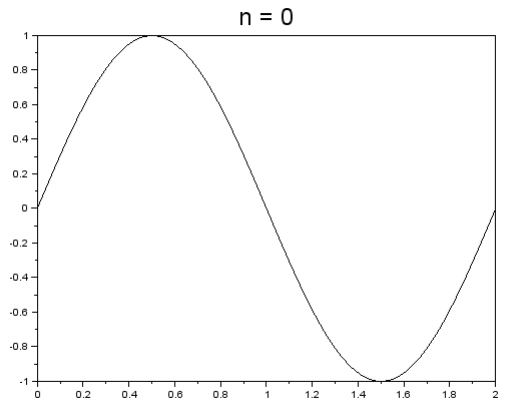
Sampling points move little ➡ Requires long time

Golden Ratio Sampling

$$f_{CLK} = \varphi \times f_{sig}$$

φ : Golden ratio (= 1.6180339887…)





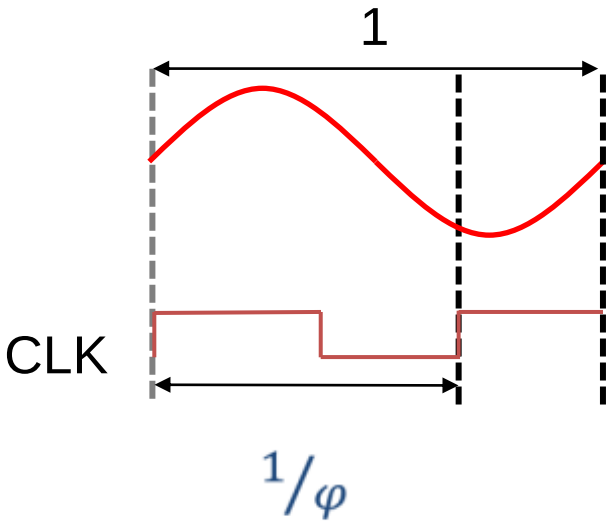
Sampling points disperse uniformly through measurement

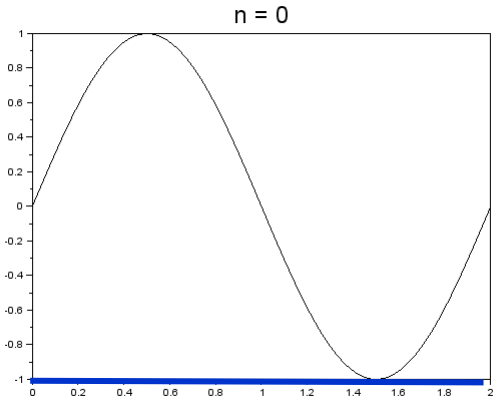
[4] Y. Sasaki, Y. Zhao, A. Kuwana, H. Kobayashi,
"Highly Efficient Waveform Acquisition Condition in Equivalent-Time Sampling System“
27th IEEE Asian Test Symposium, Hefei, Anhui, China (Oct. 2018)

Pseudo Random Signal Generation

$$f_{CLK} = \varphi \times f_{sig}$$

φ : Golden ratio (= 1.6180339887…)





Sampling points disperse uniformly

⇨

Our proposal:

Pseudo Random Signal
With Uniform Distribution