Panel:
Trends in mixed-signal test cost in current and future ICs

Haruo Kobayashi
Gunma University
Cost is the most important for LSI testing

- Analog portion continues to be difficult part of SOC test.
- Concept of “cost” makes “issues and challenges of analog circuit testing in mixed-signal SOC” clear and logical.
- Everything converges to “cost” in LSI testing technologies.
To Test, or Not to Test

Don’t test low cost
Consumer electronics ICs
  Design assurance
  Use on-chip measurement for design validation

To test if characteristics/reliability/yield critical
Automotive, medical application ICs

If accidents happen, huge cost.
Mixed-signal BIST or BOST

BIST, DFT

- Chip design time maybe longer
- Chip may be larger
- Difficult to assure its reliability

Use existing on-chip resources (CPU, Memory)

- Loopback test

BOST

- Design/implementation after tape out

Attractive
Phase Noise Test with $\Delta \Sigma$ TDC

Phase noise in oscillator

\begin{align*}
\text{Necessary signal} \\
\text{Power} & \quad \text{Phase Noise} \\
\text{frequency}
\end{align*}

Malfunction of electronic systems

- RF circuit & system
- ADC

Important

Phase noise test at low cost, in short time

Conventional

- Expensive: Spectrum analyzer
- Long: test time (~10 seconds)

Proposed

Simple circuit

$\Delta \Sigma$ Time-to-Digital Converter

Low cost, high quality Phase noise test

TDC BOSTs for Timing Signal Testing

- Single-bit ΔΣ TDC with analog FPGA
- Multi-bit ΔΣ TDC with analog FPGA
- Flash-type TDC with analog FPGA
- Flash-type TDC with digital FPGA

Experiments show that 1.67 ps RMS timing jitter can be measured.

Process: 65 nm CMOS
Supply Voltage: 1.2 V

Low IMD3 2-Tone Signal Generation with AWG for Communication Application ADC Testing

Conventional
\[ X(n) = \cos(2\pi f_1 n T_s) + \cos(2\pi f_2 n T_s) \]

Proposed phase switching
\[ X_0(n) = \cos(2\pi f_1 n T_s + \pi/6) + \cos(2\pi f_2 n T_s - \pi/6) \]
\[ X_1(n) = \cos(2\pi f_1 n T_s - \pi/6) + \cos(2\pi f_2 n T_s + \pi/6) \]

Measurement Results (AWG 2-tone output)

Complex Multi-Bandpass ΔΣ Modulator for I-Q Signal Generation

- Generation of high quality analog I-Q signals
- Testing of communication application ICs
- Digital rich

(Suitable to the realization by microscopic CMOS → Low cost)

DFT for SAR ADC Linearity

Shorten SAR ADC linearity test time.

Multi-tone Curve Fitting Algorithm for Communication Application ADC Testing

Power spectrum

2-tone

\[ \omega_1 \quad \omega_2 \quad \omega_2 - \omega_1 \quad \omega_1 + \omega_2 \]

Frequency

Multi-tone

\[ \text{IMD3} \]

Noise Power Ratio: NPR


No need for expensive instruments

ADSL application ADC testing
Time Interleaved ADC in ATE System

Channel ADC mismatch compensation

Cost effective high-speed ADC


Conclusion

There are a lot of research possibilities, challenges for mixed-signal IC test.

“Cost” concept makes our test research clear.

There is no science without measurement.

There is no production without test.