Panel:
Trends in mixed-signal test cost in current and future ICs

Haruo Kobayashi

Gunma University

群馬大学
GUNMA UNIVERSITY

Cost is the most important for LSI testing

- Analog portion continues to be difficult part of SOC test.
- Concept of “cost” makes “issues and challenges of analog circuit testing in mixed-signal SOC” clear and logical.
- Everything converges to “cost” in LSI testing technologies.

To Test, or Not to Test

Don't test low cost

Consumer electronics ICs

Design assurance

Use on-chip measurement for design validation

To test if characteristics/reliability/yield critical

Automotive, medical application ICs

If accidents happen, huge cost.

Mixed-signal BIST or BOST

BIST, DFT

Chip design time maybe longer — Long time-to-market

Chip may be larger — Costly

Difficult to assure its reliability — Should be simple

Use existing on-chip resources (CPU, Memory)

Loopback test — Cost-effective

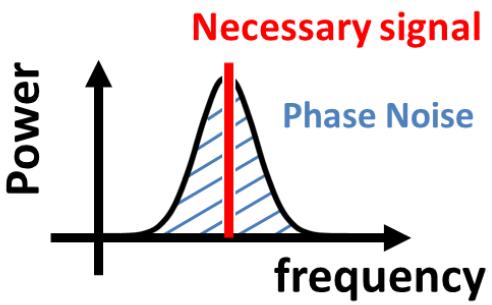
BOST

Design/implementation after tape out

Attractive

Phase Noise Test with ΔΣ TDC

Phase noise in oscillator



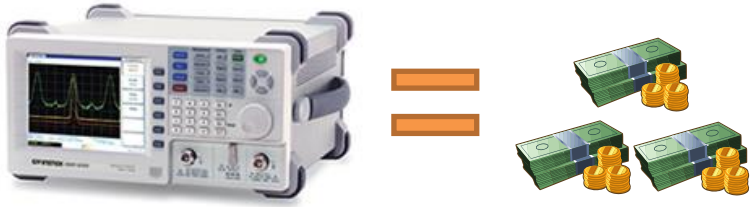
Malfunction of electronic systems

- RF circuit & system
- ADC

Important

Phase noise test at low cost, in short time

Conventional



- **Expensive** : Spectrum analyzer
- **Long** : test time (~10seconds)

cost high

Proposed

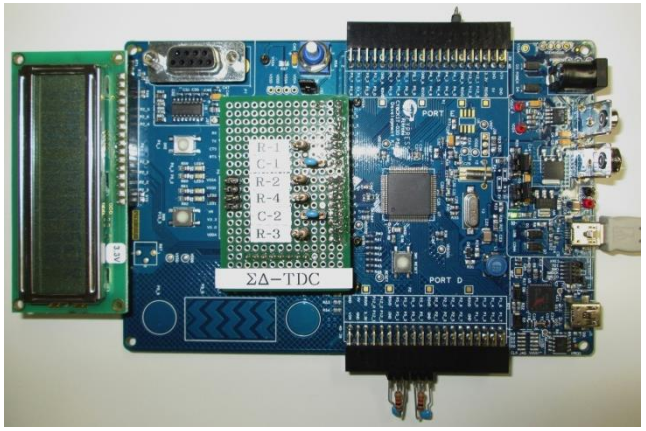
Simple circuit

ΔΣ Time-to-Digital Converter

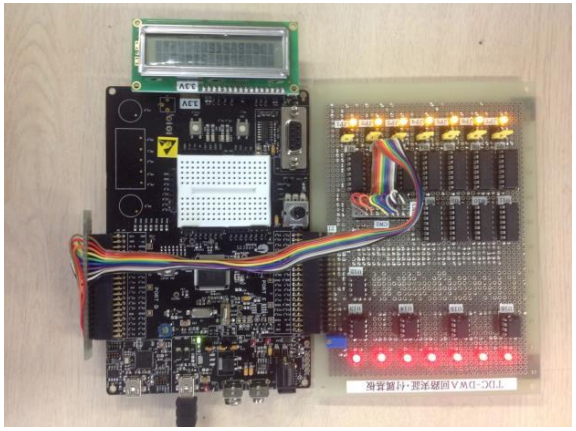
Low cost, high quality Phase noise test

[1] Y. Osawa, H. Kobayashi, "Phase Noise Measurement Techniques Using Delta-Sigma TDC", IEEE International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW'14), Porto Alegre, Brazil (Sept. 17-19, 2014).

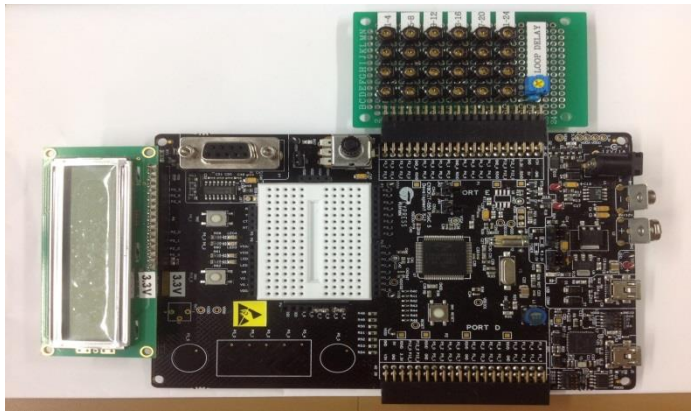
TDC BOSTs for Timing Signal Testing



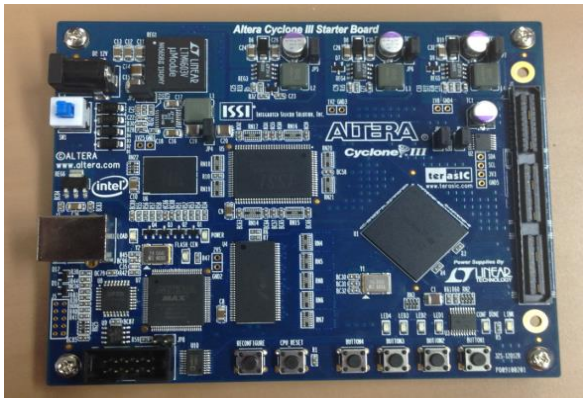
Single-bit ΔΣ TDC with analog FPGA



Multi-bit ΔΣ TDC with analog FPGA



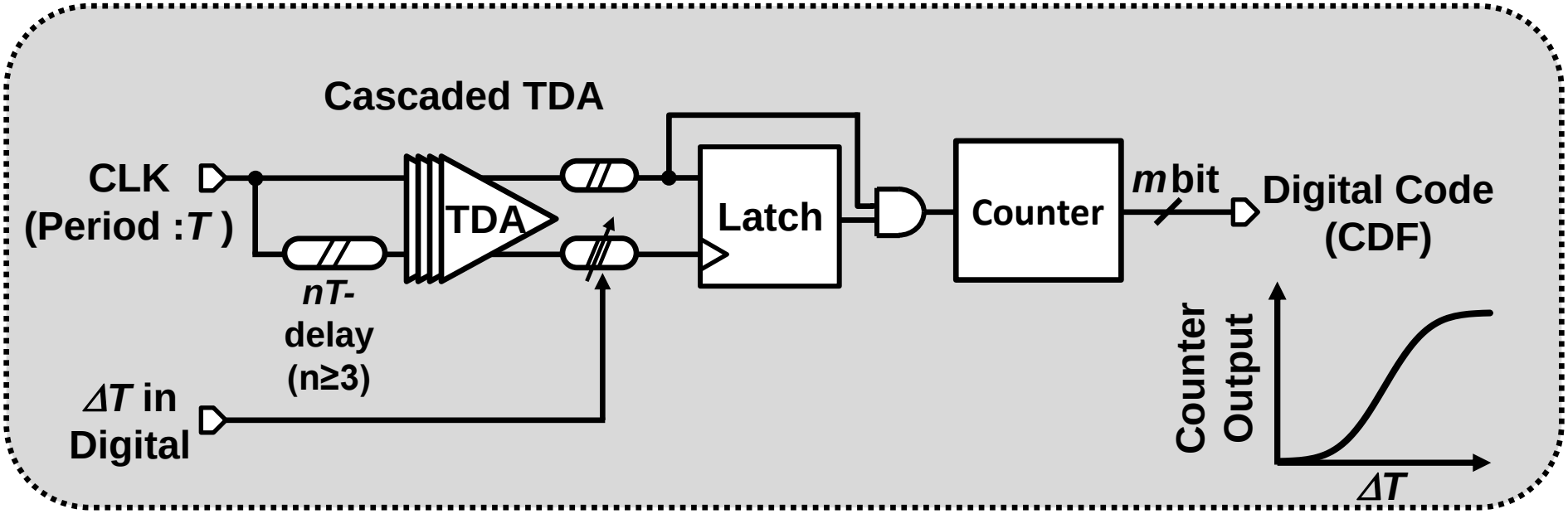
Flash-type TDC with analog FPGA



Flash-type TDC with digital FPGA

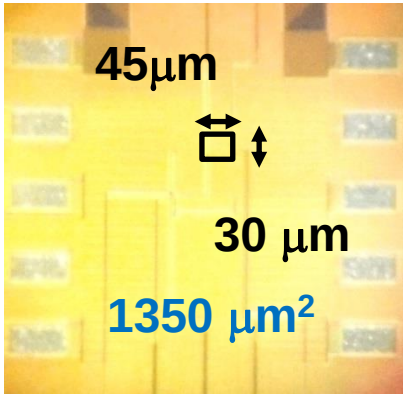
[2] T. Chujo, H. Kobayashi, “Experimental Verification of Timing Measurement Circuit With Self-Calibration”, IEEE International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW'14), Porto Alegre, Brazil (Sept. 17-19, 2014).

On-chip Jitter Measurement Circuit



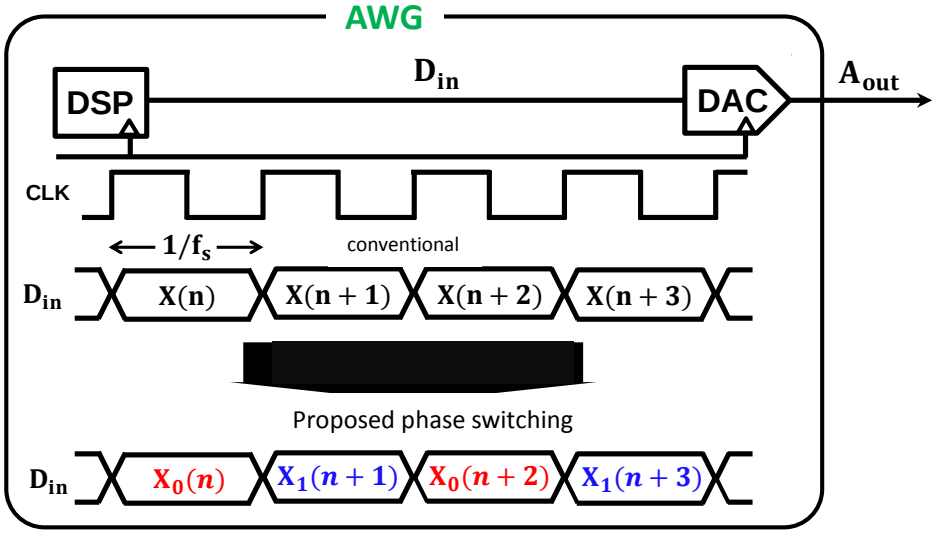
Experiments show that 1.67 ps RMS timing jitter can be measured

Process : 65 nm CMOS
Supply Voltage : 1.2 V



[3] K. Niitsu, H. Kobayashi , "CMOS Circuits to Measure Timing Jitter Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier with Duty-Cycle Compensation," IEEE Journal of Solid-State Circuits, Nov. 2012.

Low IMD3 2-Tone Signal Generation with AWG for Communication Application ADC Testing



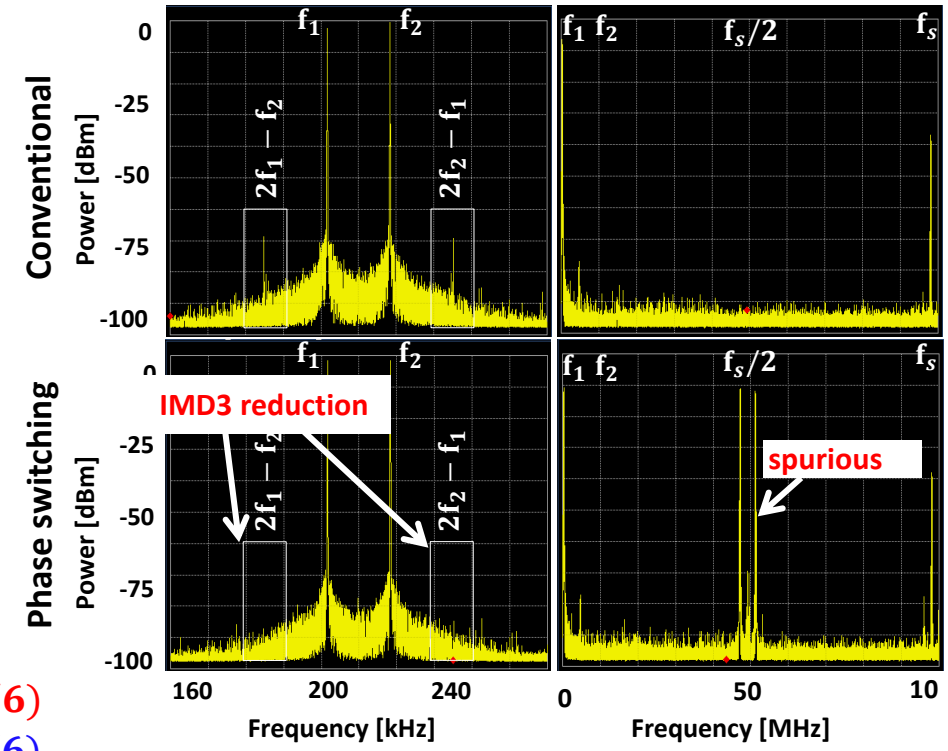
Conventional

$$X(n) = A\cos(2\pi f_1 n T_s) + A\cos(2\pi f_2 n T_s)$$

Proposed phase switching

$$X_0(n) = B\cos(2\pi f_1 n T_s + \pi/6) + B\cos(2\pi f_2 n T_s - \pi/6)$$
$$X_1(n) = B\cos(2\pi f_1 n T_s - \pi/6) + B\cos(2\pi f_2 n T_s + \pi/6)$$

Measurement Results（AWG 2-tone output）



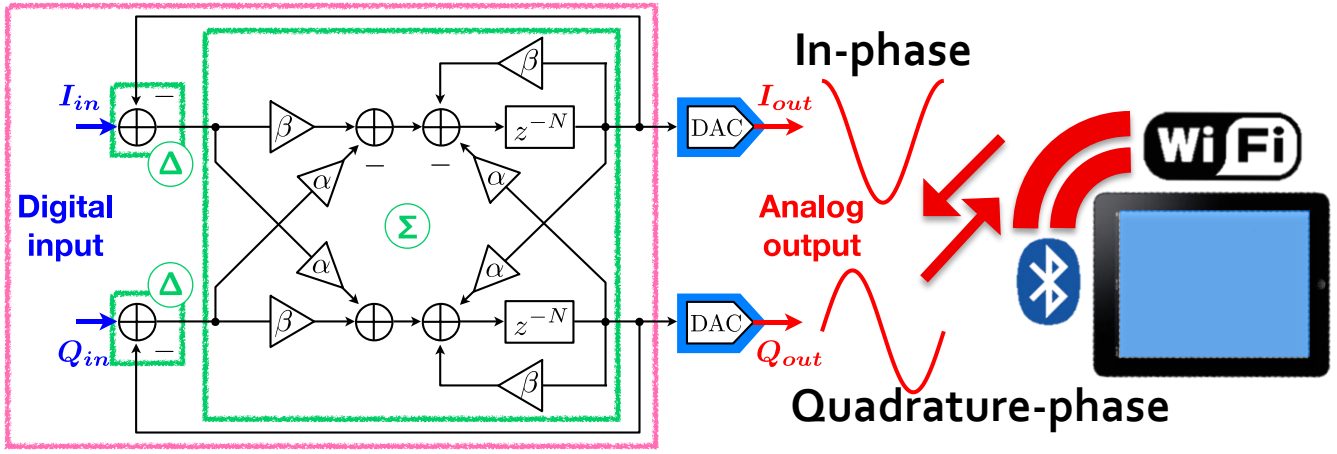
[4] K. Kato, H. Kobayashi,
"Two-Tone Signal Generation for Communication Application ADC Testing",
The 21st IEEE Asian Test Symposium, Niigata, Japan (Nov. 2012).

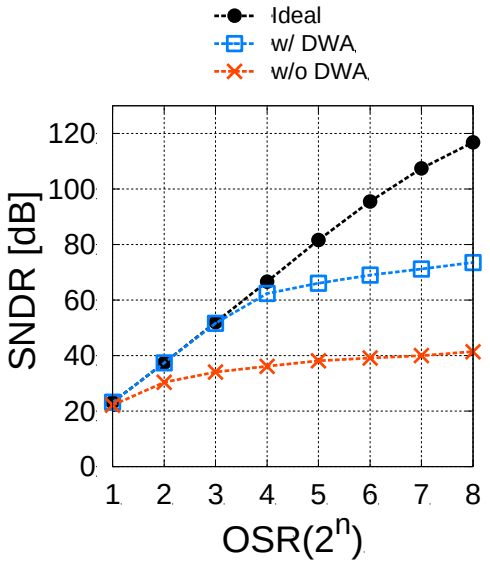
Complex Multi-Bandpass ΔΣ Modulator for I-Q Signal Generation

- Generation of high quality analog I-Q signals
- Testing of communication application ICs
- Digital rich

(Suitable to the realization by microscopic CMOS → Low cost)

ΔΣ modulation | Complex signal processing | Non-linear correction algorithm for Multi-bit DAC

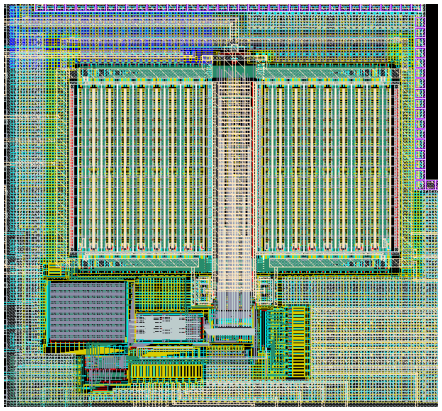




[5] M. Murakami, H. Kobayashi, "Study of Complex Multi-Bandpass ΔΣ Modulator for I-Q Signal Generation", IEICE International Conference on Integrated Circuits Design and Verification, (Nov. 2013).

DFT for SAR ADC Linearity

10bit SAR ADC
TSMC 180nm
$1.2 \times 1.2 mm^2$



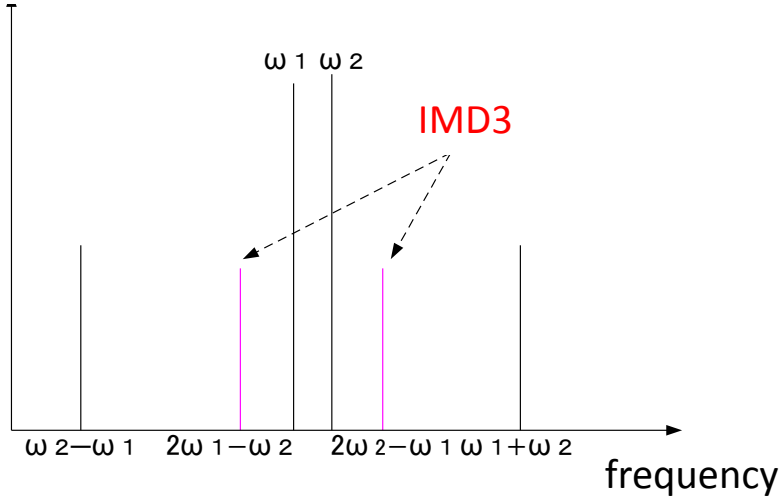
Shorten SAR ADC linearity test time.

[6] T. Ogawa, H. Kobayashi,
"Design for Testability That Reduces Linearity Testing Time of SAR ADCs”,
IEICE Trans. on Electronics (June 2011).

Multi-tone Curve Fitting Algorithm for Communication Application ADC Testing

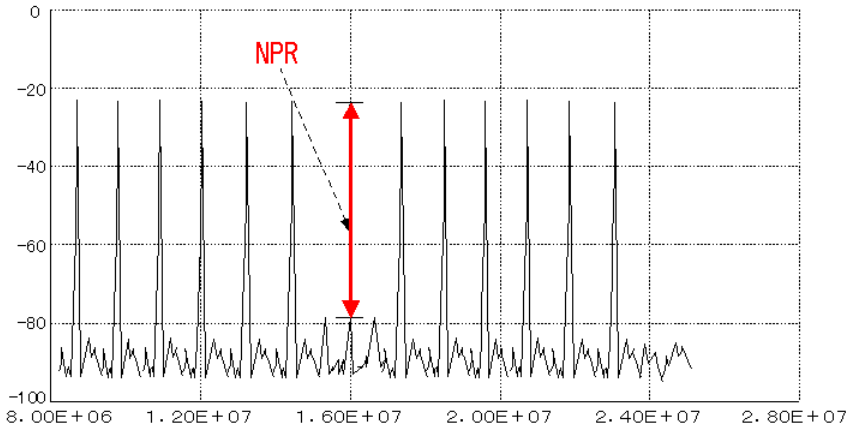
2-tone

Power spectrum



Multi-tone

Power spectrum



No need for expensive instruments

Noise Power Ratio: NPR

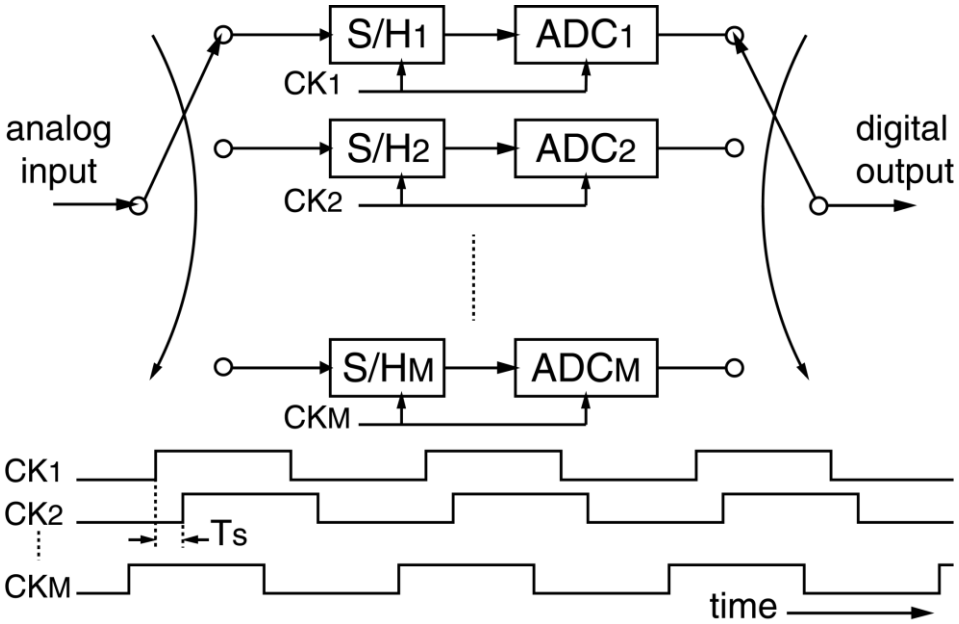
ADSL application ADC testing

[7] Y. Motoki, H. Kobayashi,
``Multi-Tone Curve Fitting Algorithms for Communication Application ADC Testing'',
Electronics and Communication in Japan: Part 2, Wiley Periodicals Inc. (2003).

Time Interleaved ADC in ATE System

Channel ADC mismatch compensation

Cost effective high-speed ADC



[9] N. Kurosawa, H. Kobayashi,
``Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems'',
IEEE Trans. on Circuits and Systems I (March 2001).

[10] R. Yi H. Kobayashi,
Digital Compensation for Timing Mismatches in Interleaved ADCs",
IEEE 22nd Asian Test Symposium, Yilan, Taiwan, (Nov. 2013)

[11] K. Asami, H. Kobayashi, "Timing Skew Compensation Technique using Digital Filter with Novel Linear Phase Condition,"
IEEE International Test Conference, Austin (Nov. 2010).

Conclusion

There are a lot of
research possibilities, challenges
for mixed-signal IC test.

"Cost" concept makes our test research clear.

There is no science without measurement.

There is no production without test.