Timing Measurement BOST Architecture with Full Digital Circuit and Self-Calibration Using Characteristics Variation Positively for Fine Time Resolution

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Outline

• Introduction
• Time to Digital Converter (TDC)
• Encoder Circuit
• Self-Calibration
• Stochastic TDC Structure
• RTL Simulation
• Conclusions
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Introduction

“Fine time resolution” and “high linearity”
TDC is essential for jitter, timing BOST

- High linearity TDC
  → Self-calibration circuit

- Fine time resolution TDC
  → Stochastic architecture

TDC: Time-to-Digital Converter
BOST: Built-Out Self-Test
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Time to Digital Converter (TDC)

- time interval → Measurement → Digital value

- Key component of time-domain analog circuit

- Higher resolution can be obtained with scaled CMOS

![Diagram of TDC](image)

Higher resolution with CMOS scaling

![Graph showing trend](image)
Time to Digital Converter (TDC)

Timing chart

- Start
- D0=1
- D1=1
- D2=1
- D3=0
- D4=0
- Stop

Encoder

Thermometer code

Binary code

Dout
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Encoder Circuit

DFF outputs Dout
0 0 0 0 0 0 0 0 0 0
1 0 0 0 0 0 0 0 0 1
1 1 0 0 0 0 0 0 0 2
1 1 1 0 0 0 0 0 0 3
1 1 1 1 0 0 0 0 0 4
1 1 1 1 1 0 0 0 0 5
1 1 1 1 1 1 0 0 0 6
1 1 1 1 1 1 1 0 0 7
1 1 1 1 1 1 1 1 1 8

Buffer delay
DFF offset mismatch

Bubble error
Encoder Circuit

Count the number of “1” outputs from DFFs

To ensure monotonicity of the TDC
Encoder Circuit

Bubble error effects are suppressed.
Encoder Circuit

Designed the encoder using an array of full adders
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TDC Architecture with Self-Calibration

START

Test mode

STOP

MUX

MUX

MUX

MUX

# of 1's counter

Histogram Engine & Digital Error Correction

Dout
Self-Calibration Mode

Test mode

START

STOP

# of 1's counter

Histogram Engine & Digital Error Correction

Dout

NOT Synchronized
Normal Operation Mode

Normal mode

START

Test mode

STOP

# of 1’s counter

Digital Error Correction

Dout
Measurement with Histogram

Random dots

# of dots ratio \( \frac{N_1}{N_2} \) \quad \text{Area ratio} \quad \frac{S_1}{S_2}
Test mode

The two oscillators are different from each other and not synchronized

The histograms in all bins will be equal, after collection of a sufficiently large number of data, if the TDC has perfect linearity.
Delay Variation Measurement

TDC is non-linear

buffer delay

$\tau + \Delta \tau_1$  $\tau + \Delta \tau_2$  $\tau + \Delta \tau_3$  $\tau + \Delta \tau_4$

$\Delta \tau_2$  $\Delta \tau_3$  $\Delta \tau_4$  $\Delta \tau_5$

$\tau$

TDC digital output

Histogram
Histogram Data is Proportional to Delay Value

Histogram bin of digital code with **large** delay is high.
Histogram bin of digital code with **small** delay is low.
Principle of Self-Calibration

1. Histogram
   - Nonlinear TDC

2. Nonlinear TDC
   - INL calculation

3. Linearized by inverse function
   - \( D_{out} = f(T) \)

4. Histogram
   - Linear TDC

Histogram of ideally Linear TDC
Simulation Result of Self-Calibration

before calibration

after calibration

Sampling points  28,848,432

\[ \tau_1 = 60 \sim 69 \text{ ps} \]

\[ \tau_2 = 10 \text{ ns} \]

Histogram for each bin is the same when the TDC is linear.
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Stochastic TDC Structure

Use the random offset proactively
Stochastic TDC for Fine Time Resolution

DFF random offsets

# of “1”s Counter, Histogram Engine & Digital Correction
Circuit performance characteristics like voltage, delay, slew and power are stochastic processes.

Example:
Statistical process variation on gate leakage, subthreshold leakage, dynamic power and propagation delay in a 2-input NAND gate

(source: http://www.cse.unt.edu/~smohan/Projects/CCF_0702361/CCF_0702361.html)
Setup/hold times of each DFF are different due to stochastic variation.

Setup/hold times = 19.31ps
19.36ps
19.40ps
19.60ps
19.82ps
Ex.
DFF number = 400

Setup/hold times of 400 DFFs are normally distributed
Mean = 20ps, standard deviation = 6ps

But nonlinear !!

Time resolution = 0.08ps
How to Convert a Nonlinear TDC into a Linear TDC?

Self-calibration is applied to improve linearity!!
Input-output Characteristics Before and After Calibration

TDC linearity is improved after calibration !!
INL Reduction After Calibration

Stage of buffers

INL value

before calibration

after calibration

# of DFFs = 100

# of DFFs = 200

# of DFFs = 400
Measurement Time Resolution

Time resolution after calibration can reach sub-picosecond level!!

<table>
<thead>
<tr>
<th>DFF Number</th>
<th>Time Resolution</th>
</tr>
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<tbody>
<tr>
<td>100</td>
<td>0.3258ps</td>
</tr>
<tr>
<td>200</td>
<td>0.1613ps</td>
</tr>
<tr>
<td>400</td>
<td>0.0876ps</td>
</tr>
</tbody>
</table>

Comparison with other TDC architectures

<table>
<thead>
<tr>
<th>TDC architecture</th>
<th>Time resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>0.0876ps</td>
</tr>
<tr>
<td>Vernier gated ring oscillator [12]</td>
<td>3.2ps</td>
</tr>
<tr>
<td>Delay line [13]</td>
<td>6.25ps</td>
</tr>
<tr>
<td>2D Vernier [14]</td>
<td>4.8ps</td>
</tr>
<tr>
<td>Local passive interpolation [15]</td>
<td>4.7ps</td>
</tr>
<tr>
<td>Inverter-chain [16]</td>
<td>80.0ps</td>
</tr>
<tr>
<td>Two-step [17]</td>
<td>3.75ps</td>
</tr>
</tbody>
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Conclusions

- High linearity TDC → Self-Calibration circuit
- Fine time resolution TDC → Stochastic architecture

Note: Stochastic ADC linearity calibration is NOT easy.

- Fine digital CMOS implementation
  - Verification
  - Self-calibration
  - Consists of digital cells
    (FPGA implementation is possible)
Final Statement

Stochastic process theory advances precise timing measurement technology.

Prof. Kiyoshi Ito  (1915-2008)
Japanese Mathematician

Great contribution to
- Stochastic calculus
- Stochastic differential equation