21<sup>st</sup> IEEE International Mixed-Signal Testing Workshop Catalunya, Spain

July 5, 2016 9:00-9:30am

Conference Room: Goya



#### Timing Measurement BOST Architecture with Full Digital Circuit and Self-Calibration Using Characteristics Variation Positively for Fine Time Resolution

Congbing Li, Junshan Wang, <u>Haruo Kobayashi</u> Ryoji Shiota

Gunma University, Socionext Inc.



- Introduction
- Time to Digital Converter (TDC)
- Encoder Circuit
- Self-Calibration
- Stochastic TDC Structure
- RTL Simulation
- Conclusions

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#### Introduction

#### "Fine time resolution" and "high linearity" TDC is essential for jitter, timing BOST



High linearity TDC

→Self-calibration circuit

Fine time resolution TDC

→ Stochastic architecture

TDC: Time-to-Digital Converter BOST: Built-Out Self-Test

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### Time to Digital Converter (TDC)

• time interval  $\rightarrow$  Measurement  $\rightarrow$  Digital value



#### **Higher resolution with CMOS scaling**



- Key component of time-domain analog circuit
- Higher resolution can be obtained with scaled CMOS

#### Time to Digital Converter (TDC)



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### **Encoder Circuit**



### **Encoder Circuit**



Count the number of "1" outputs from DFFs



To ensure monotonicity of the TDC

### **Encoder Circuit**



Bubble error effects are suppressed.



Designed the encoder using an array of full adders

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# TDC Architecture with Self-Calibration



#### Self-Calibration Mode



### **Normal Operation Mode**



#### **Measurement with Histogram**



### Histogram in Ideal Case

Test mode

The two oscillators are different from each other and not synchronized



The histograms in all bins will be equal, after collection of a sufficiently large number of data, if the TDC has perfect linearity

### **Delay Variation Measurement**



#### Histogram Data is Proportional to Delay Value

Histogram bin of digital code with large delay is high. Histogram bin of digital code with small delay is low.



### **Principle of Self-Calibration**



#### Simulation Result of Self-Calibration



Sampling points 28,848,432

 $\tau_1 = 60 \sim 69 ps$  $\tau_2 = 10 ns$ 

Histogram for each bin is the same when the TDC is linear.

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### Stochastic TDC Structure



Use the random offset proactively

#### Stochastic TDC for Fine Time Resolution



#### Stochastic Variation of Delay at Sub-Picosecond Level

#### Circuit performance characteristics like voltage, delay, slew and power are stochastic processes.



Example:

Statistical process variation on gate leakage, subthreshold leakage, dynamic power and propagation delay in a 2-input NAND gate

(source: http://www.cse.unt.edu/~smohanty/Projects/CCF\_0702361/CCF\_0702361.html)

#### Delay Variation in Stochastic TDC

Setup /hold times of each DFF are different due to stochastic variation



#### Input-Output Characteristics of Stochastic TDC



#### How to Convert a Nonlinear TDC into a Linear TDC?



#### Self-calibration is applied to improve linearity !!

#### Input-output Characteristics Before and After Calibration



#### **INL Reduction After Calibration**



#### **Measurement Time Resolution**

DFF Number	Time Resolution
100	0.3258ps
200	0.1613ps
400	0.0876ps

Time resolution after calibration can reach sub-picosecond level !!

#### Comparison with other TDC architectures

TDC architecture	Time resolution
This work	0.0876ps
Freeze Vernier [11]	4.88ps
Vernier gated ring oscillator [12]	3.2ps
Delay line [13]	6.25ps
2D Vernier [14]	4.8ps
Local passive interpolation [15]	4.7ps
Inverter-chain [16]	80.0ps
Two-step [17]	3.75ps

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### Conclusions

High linearity TDC

→Self-Calibration circuit

• Fine time resolution TDC  $\rightarrow$  Stochastic architecture

Note: Stochastic ADC linearity calibration is NOT easy.

#### Fine digital CMOS implementation

- Verification
- Self-calibration
- Consists of digital cells (FPGA implementation is possible)

#### **Final Statement**

## Stochastic process theory advances precise timing measurement technology.

Prof. Kiyoshi Ito (1915-2008) Japanese Mathematician



Great contribution to

- Stochastic calculus
- Stochastic differential equation

