Experimental Verification of a Timing Measurement Circuit With Self-Calibration

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群馬大学 GUNMA UNIVERSITY

Outline

- Research Background
- TDC Circuit and Problems
- Histogram Method Self-Calibration
- Analog FPGA Implementation
- Measurement Results
- Conclusions

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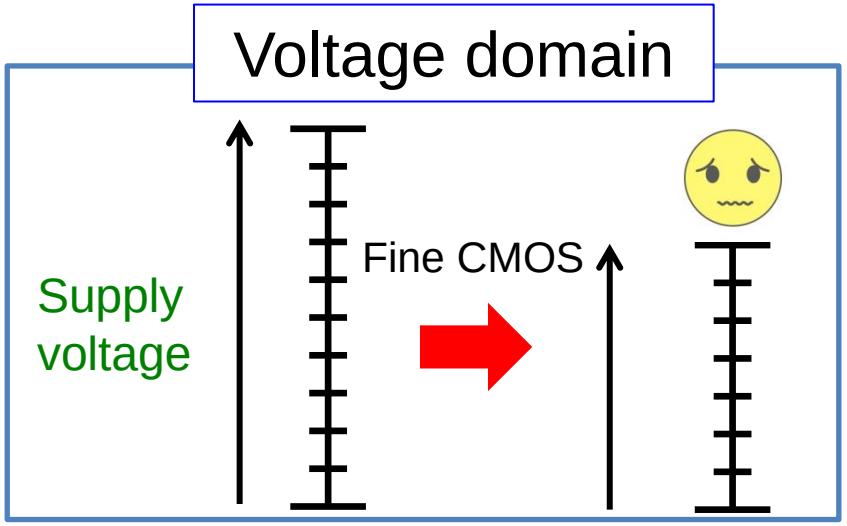
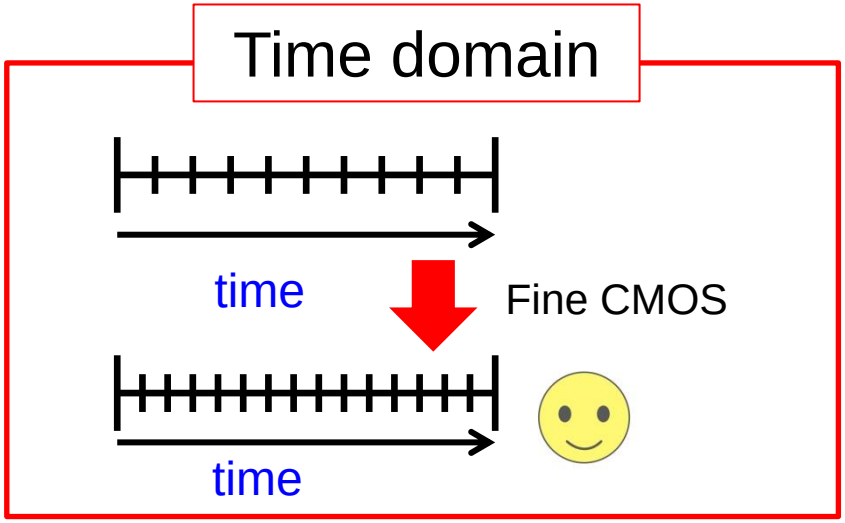
Research Background

Advanced CMOS VLSI

- Low power-supply voltages
- Fast switching speeds





A Time-to-Digital Converter (TDC) provides a digital output proportional to the time between two clock transitions.

The TDC is a key component in time-domain analog circuits,

（**e.g. Sensor Interfaces, All-Digital PLLs, ADCs, ..** ）

Research Objective

Validate TDC linearity self-calibration with histogram method

All-digital implementation

Suitable for fine CMOS

Experimentally validate design with FPGA

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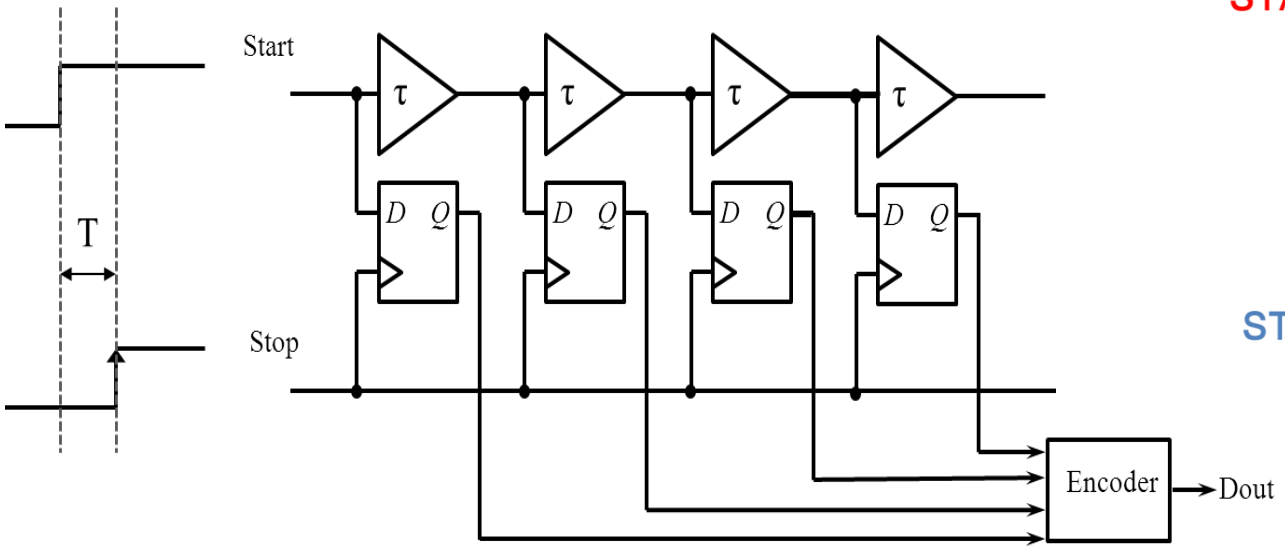
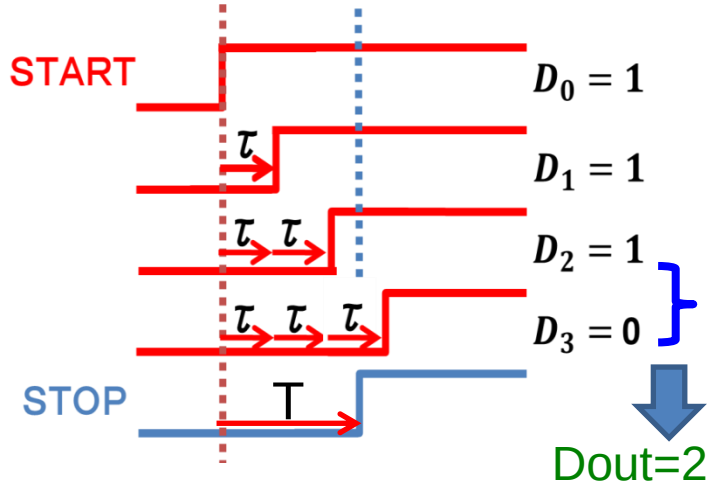
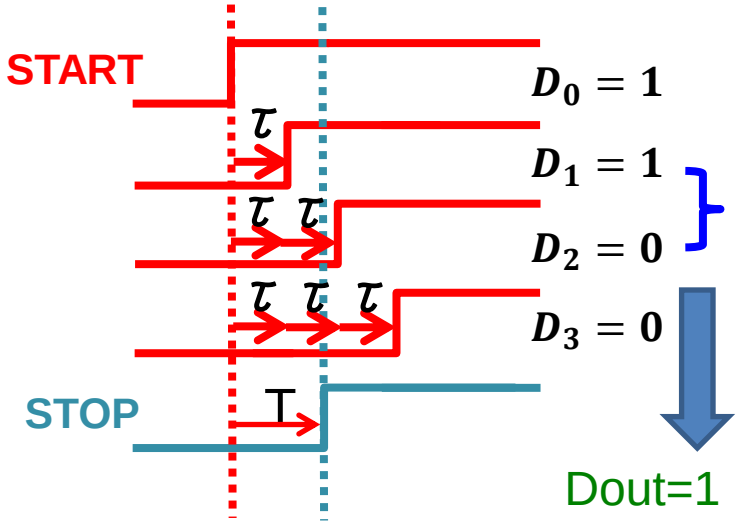
Flash-type TDC

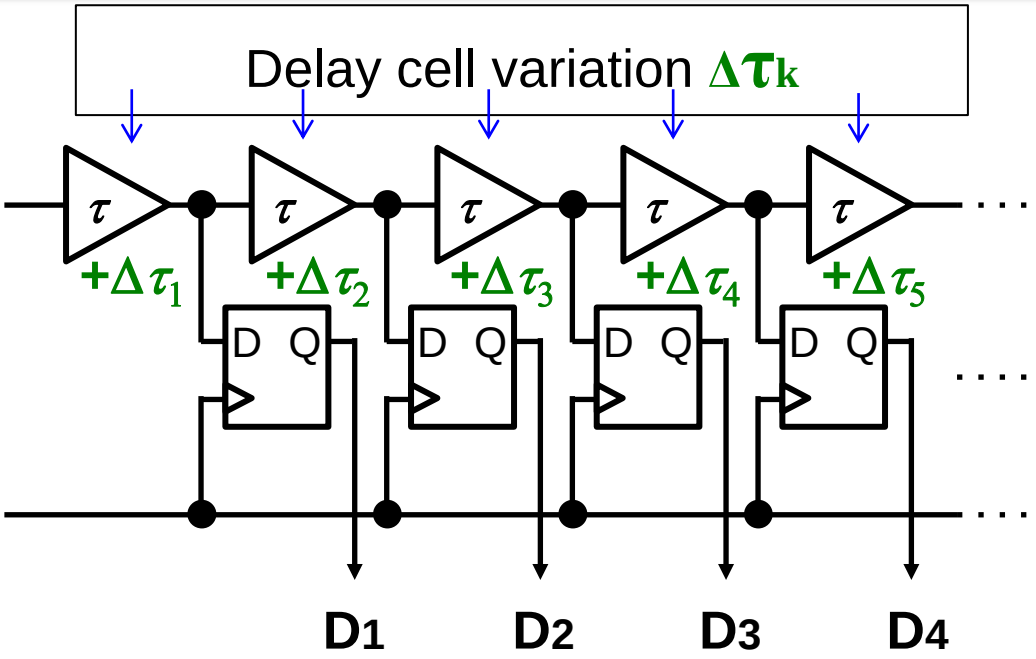




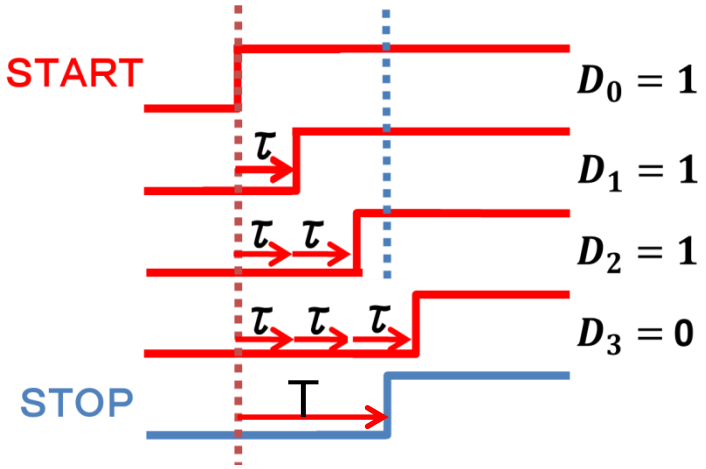


- Digital output (Dout) proportional to time difference between rising edges (T)
- Time resolution τ

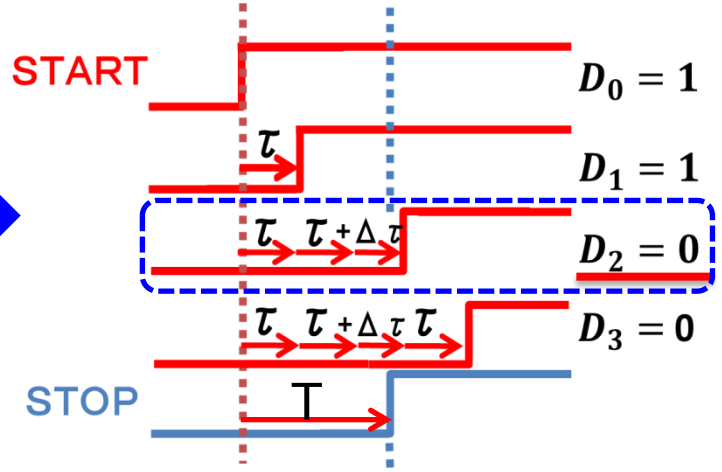
Delay Cell Variation Inside TDC Circuit



TDC nonlinearity



(a) Without delay variation



(b) With delay variation

Random Variation among Delay Cells

- Delay τ variation

  Relative variation

  ➡ TDC nonlinearity

  Absolute（average value) variation

  ➡ TDC input range & time resolution

- Focus on Relative variation here.

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Research Objective (revisited)

- TDC linearity self-calibration with histogram

Dout(0)=1
Dout(1)=3
Dout(2)=5
Dout(3)=8
.
.

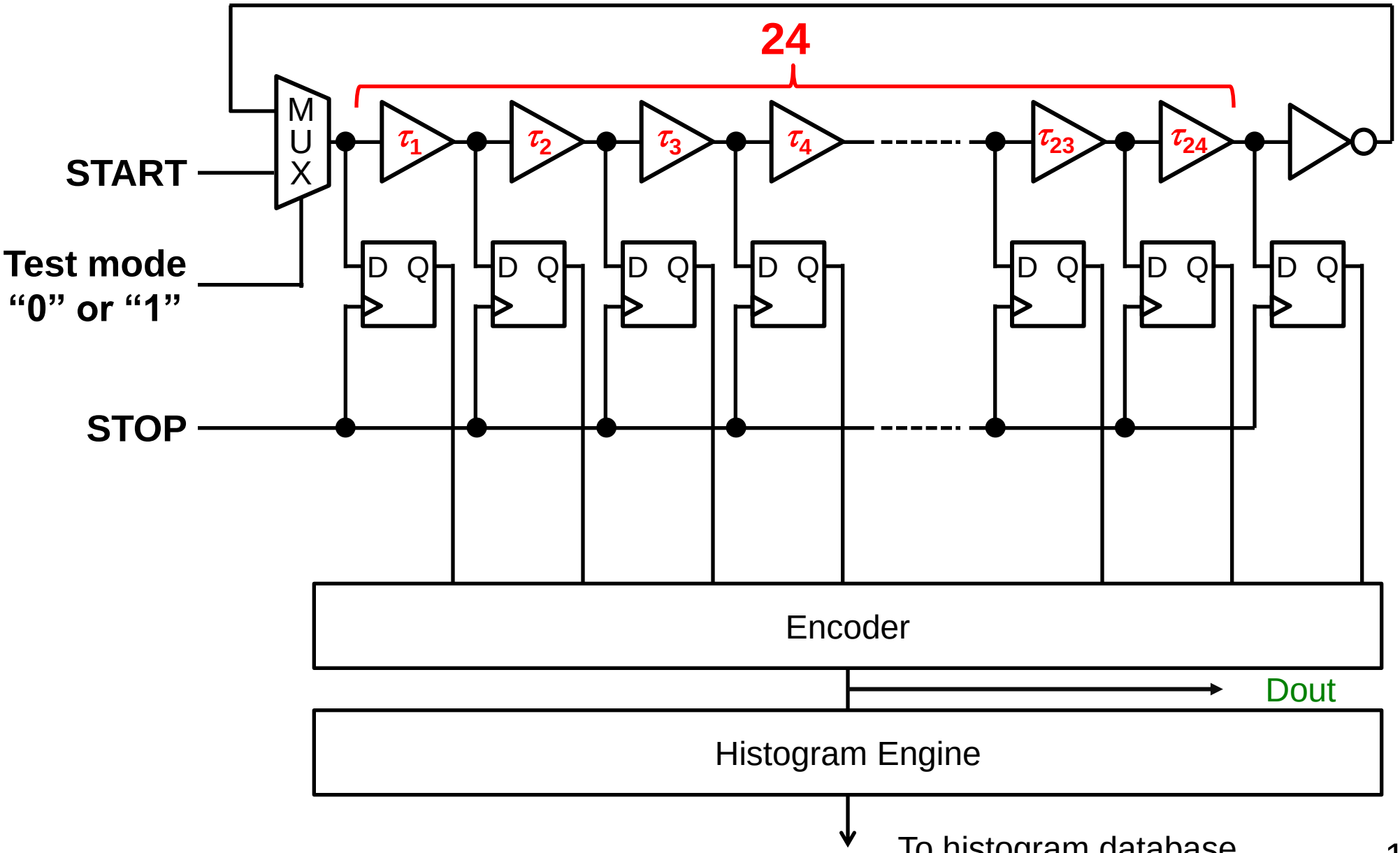
Calibration

Dout(0)=0.3
Dout(1)=2.8
Dout(2)=4.5
Dout(3)=7.3
.
.

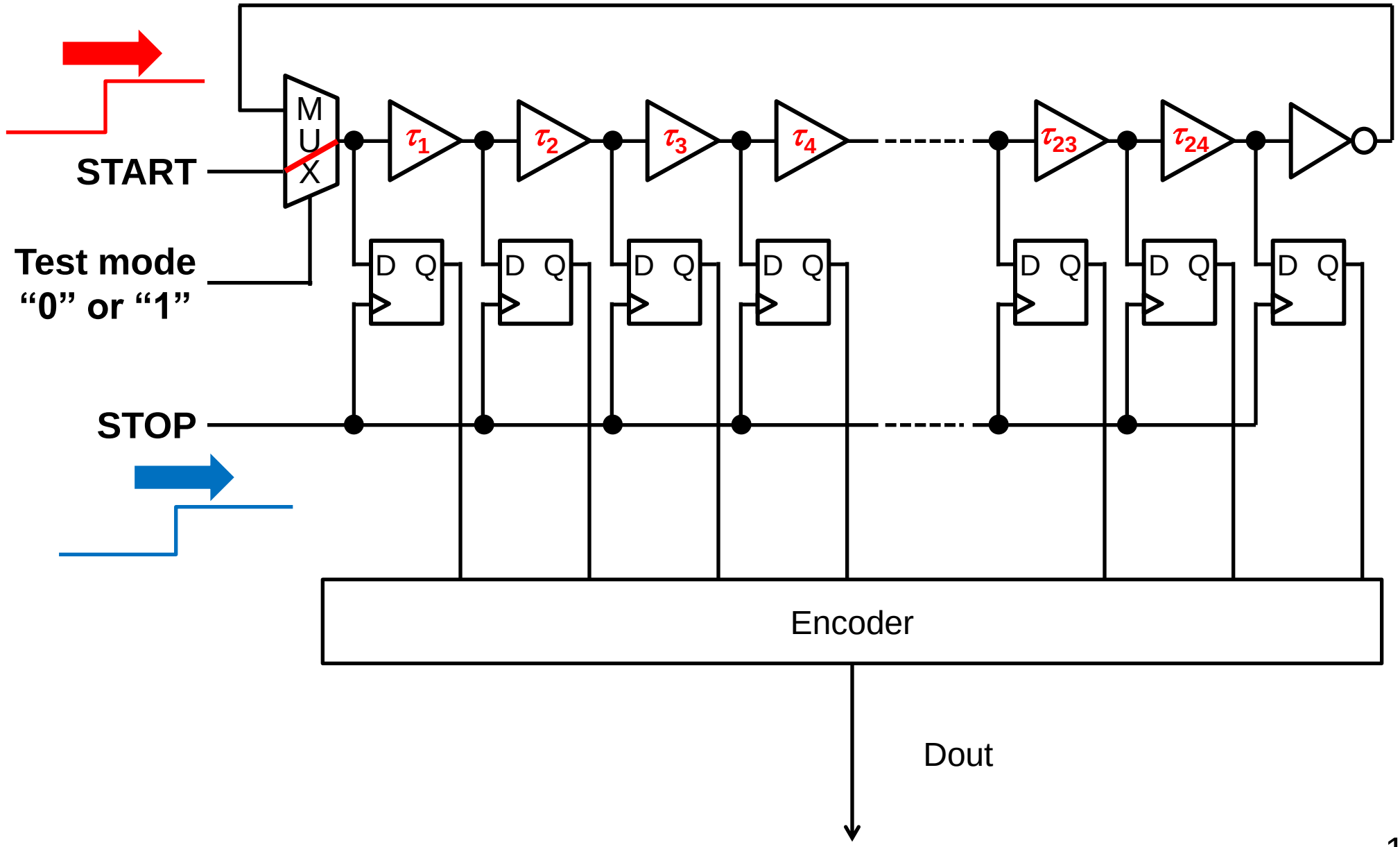
Corrected based on delay variation evaluation

- Analog FPGA（PSoC） implementation, evaluation

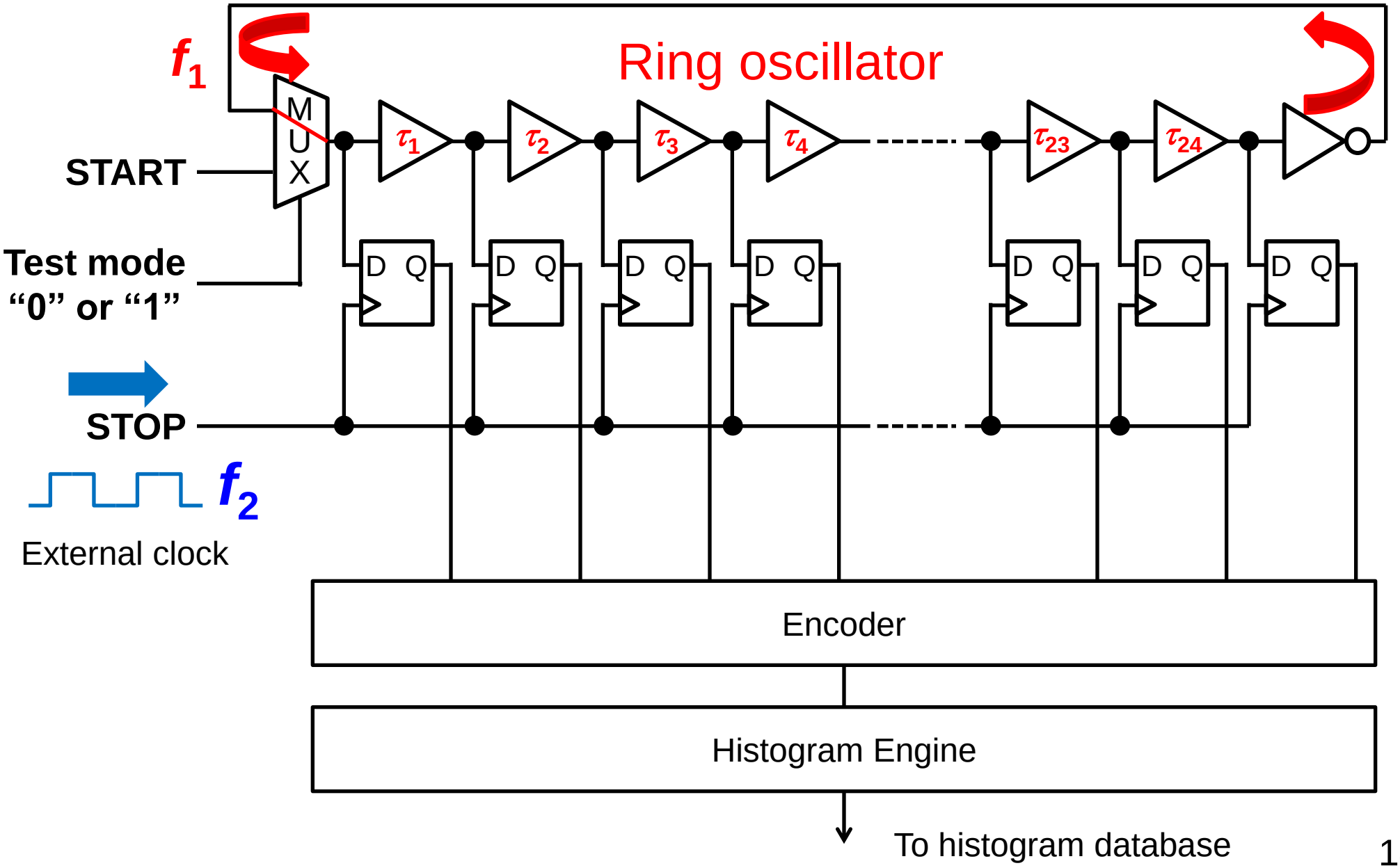
TDC with Self-Calibration



Normal Operation Mode



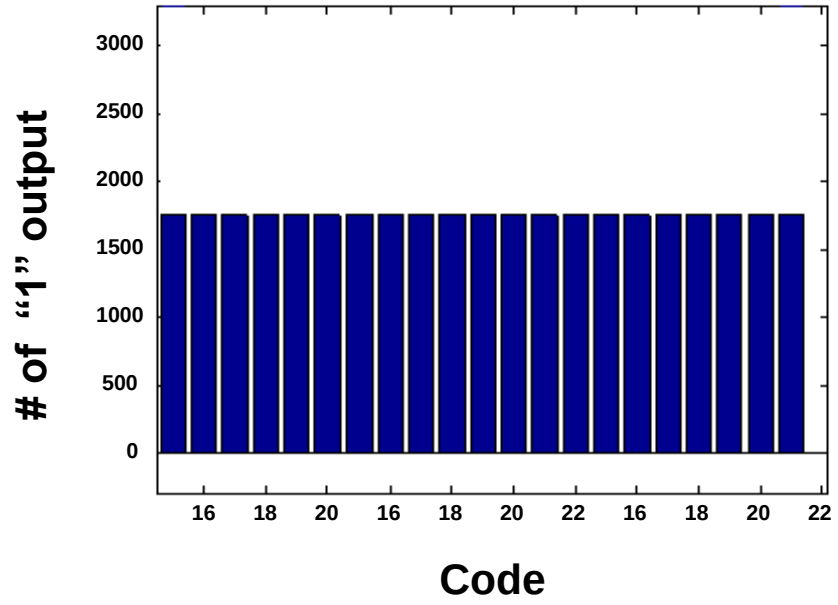
Self-Calibration Mode



Self-Calibration

Self-calibration mode

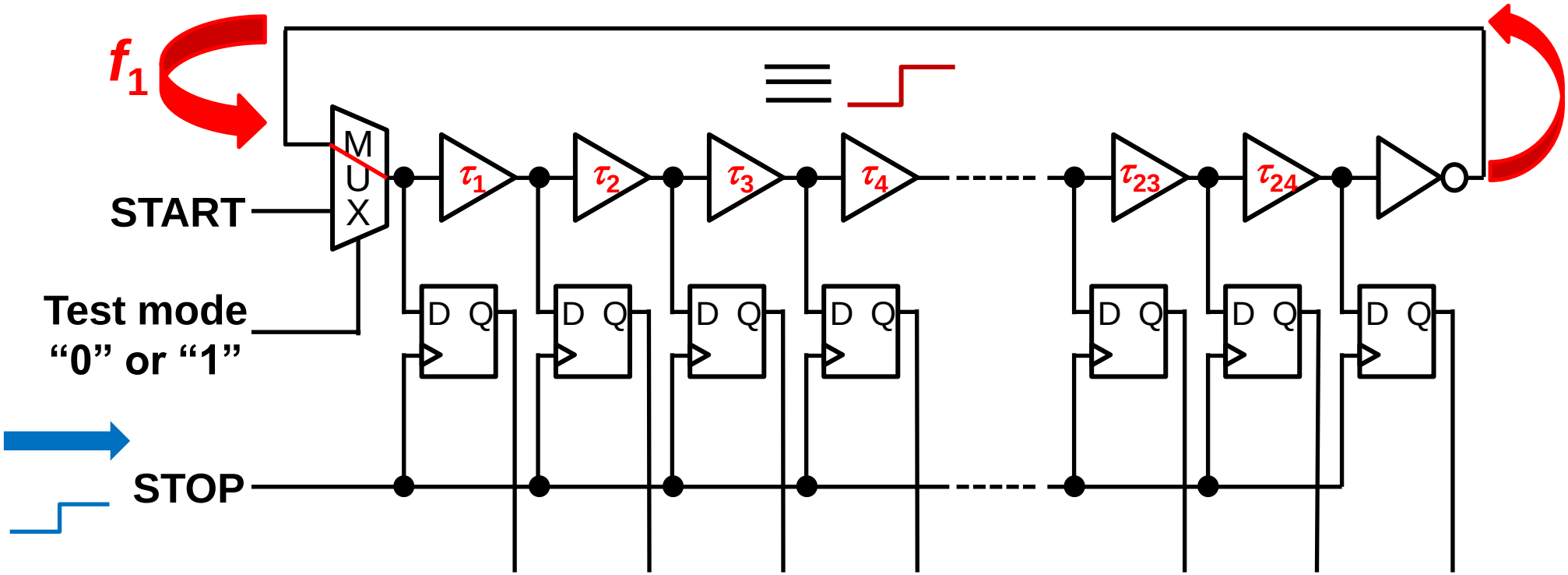
START, STOP signals
are NOT synchronized



Histogram data in all bins will be equal,
after collection of a sufficiently large number of data,
if the TDC has perfect linearity

Principle of TDC Linearity Calibration

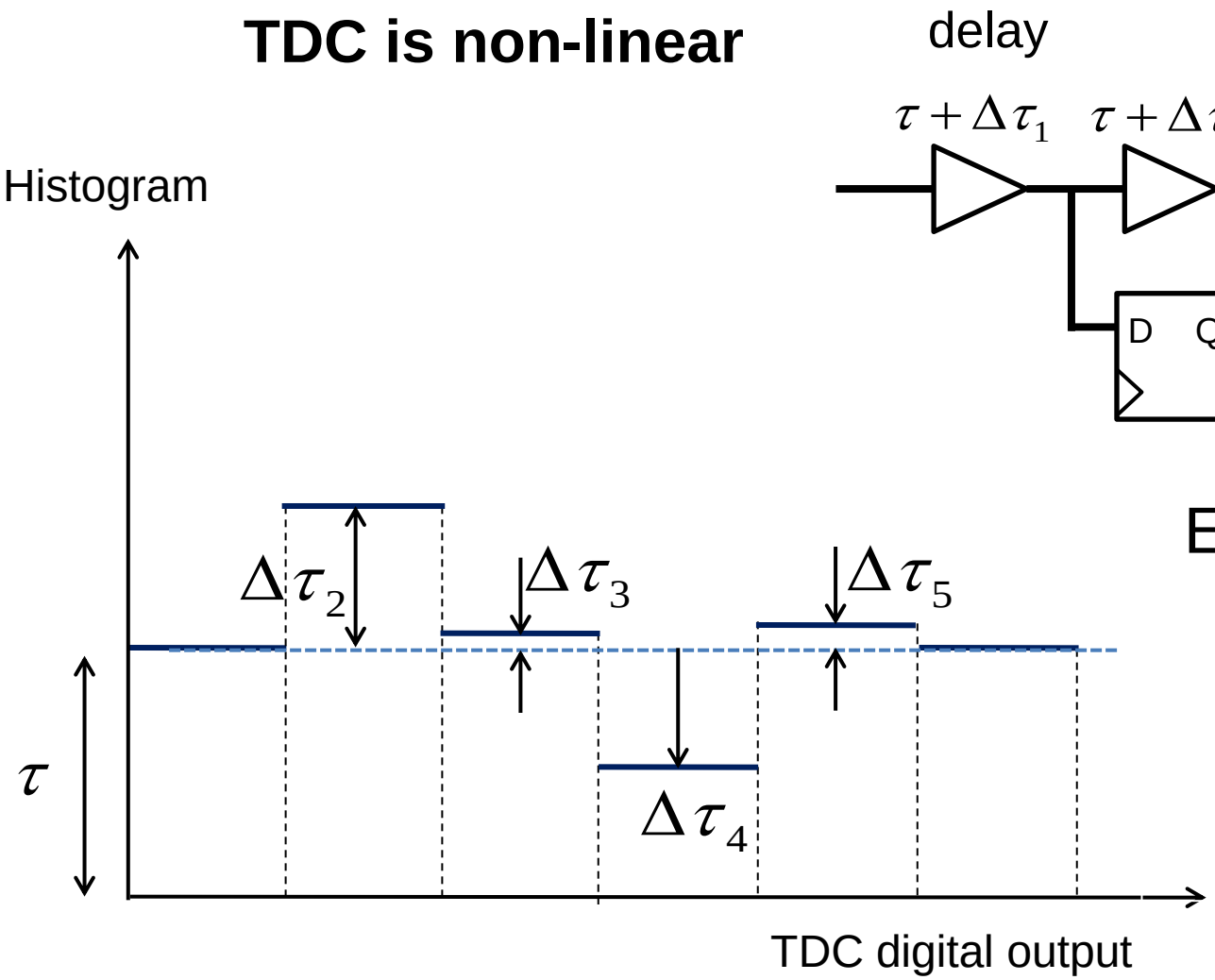
- START (ring oscillator) and STOP signals are asynchronous.



- Probability of digital code for large delay is high.
- Probability of digital code for small delay is low.

Self-Calibration

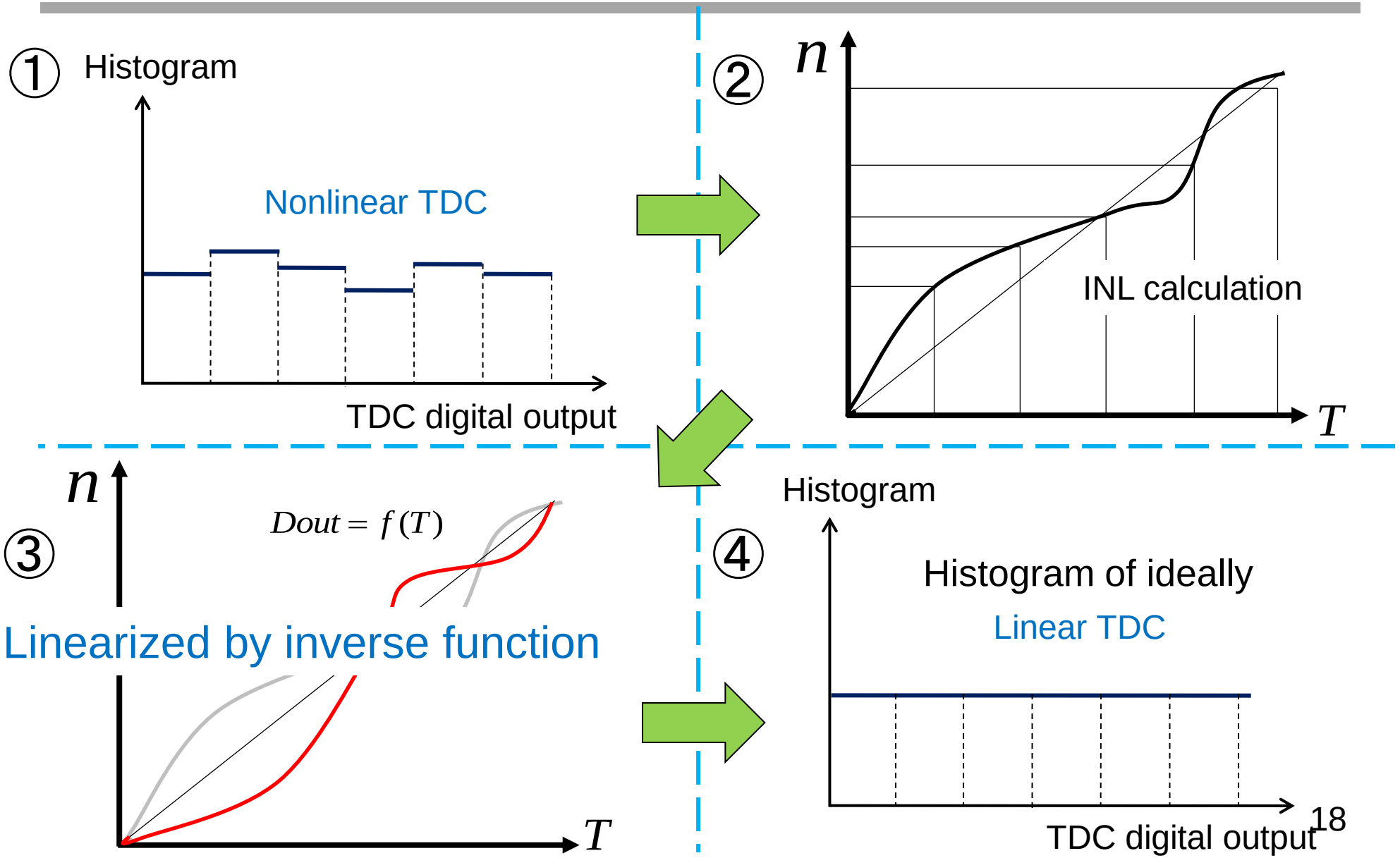
TDC is non-linear



Each bin of histogram

Varies with corresponding delay value

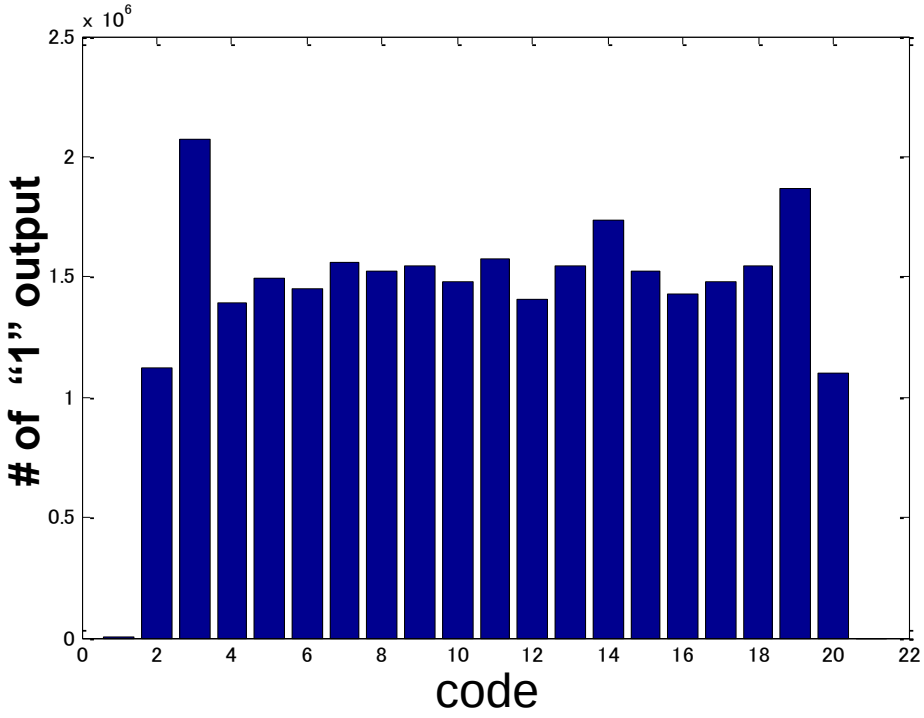
Principle of Self-Calibration



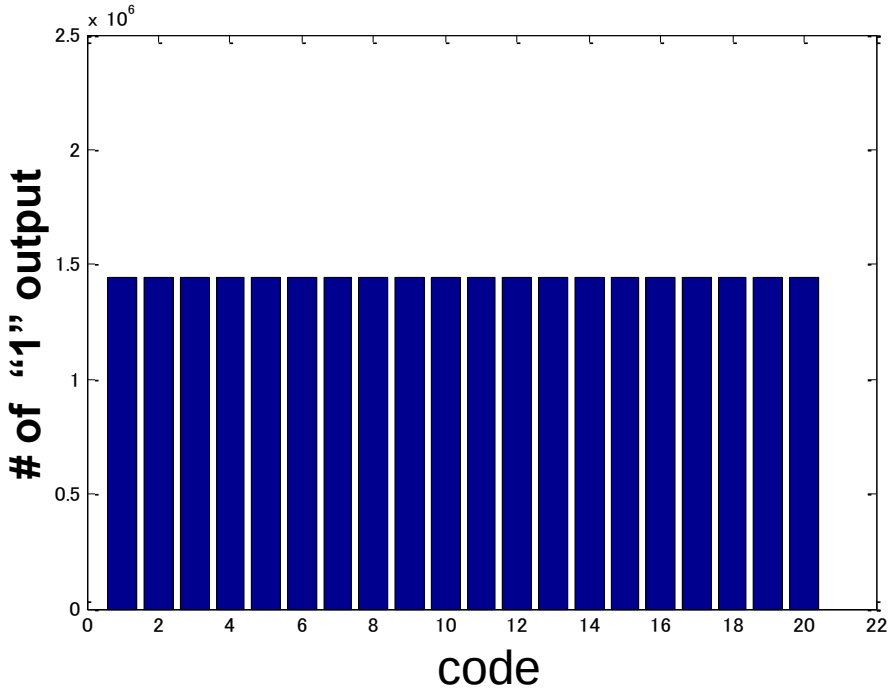
Simulation Result of Self-Calibration

MATLAB

before calibration



after calibration



Sampling points 28,848,432

$\tau_1 = 60 \sim 69\,ps$

$\tau_2 = 10\,ns$

Histogram for each bin is the same when the TDC is linear.

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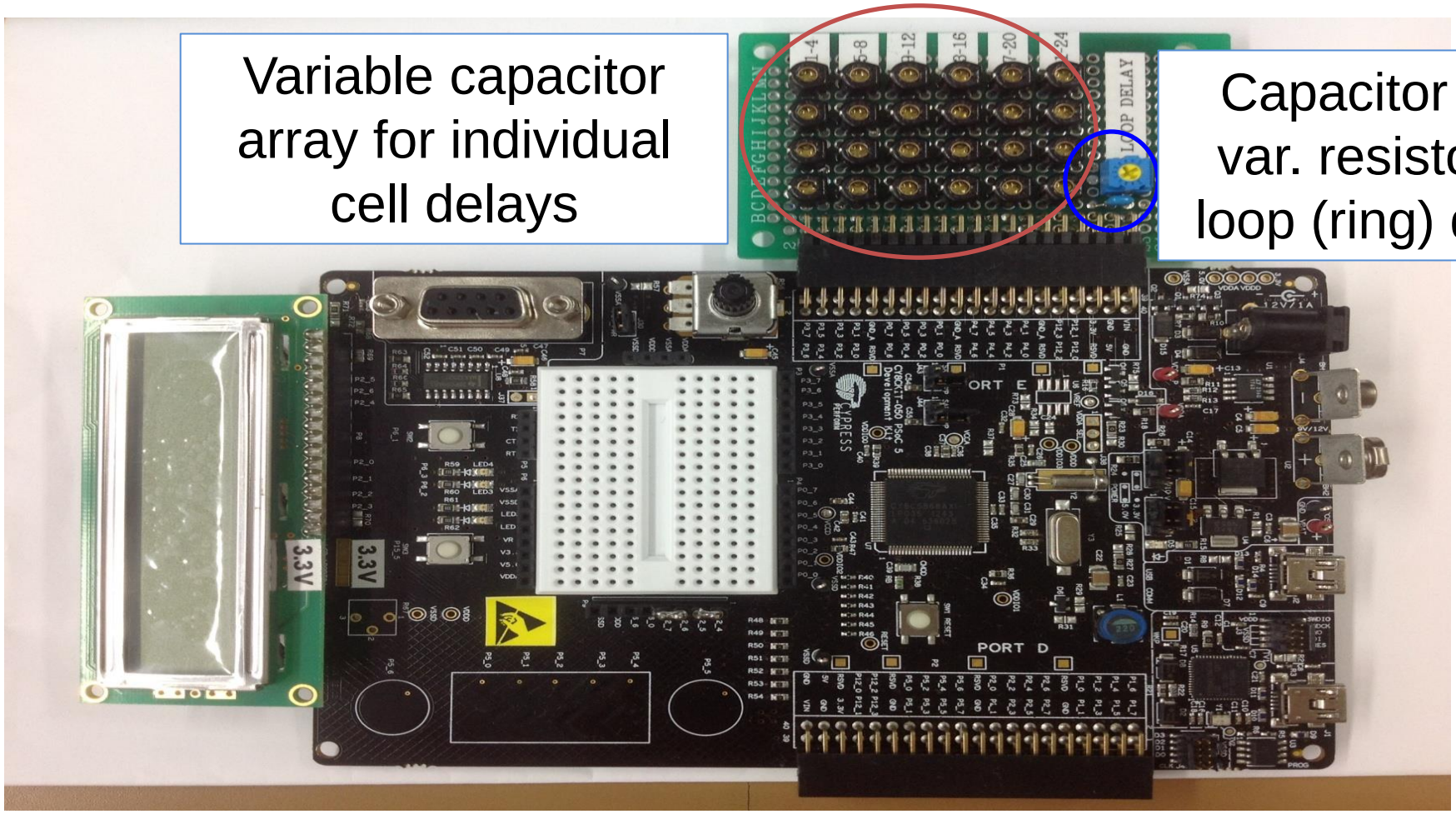
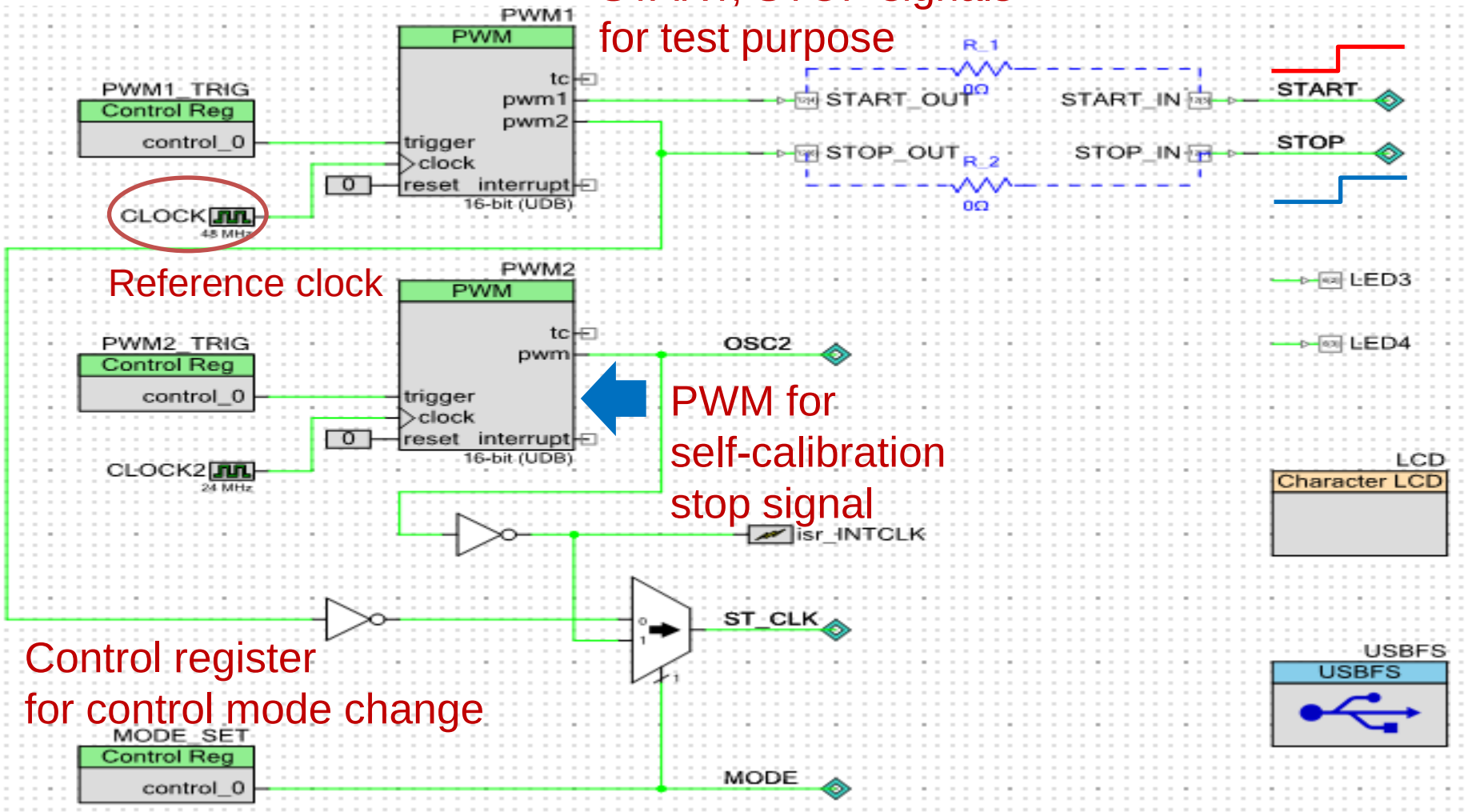
Implementation of TDC with Self-Calibration

Programmable System-on-Chip (PSoC) 5LP and external components



TDC Control Circuit in PSoC



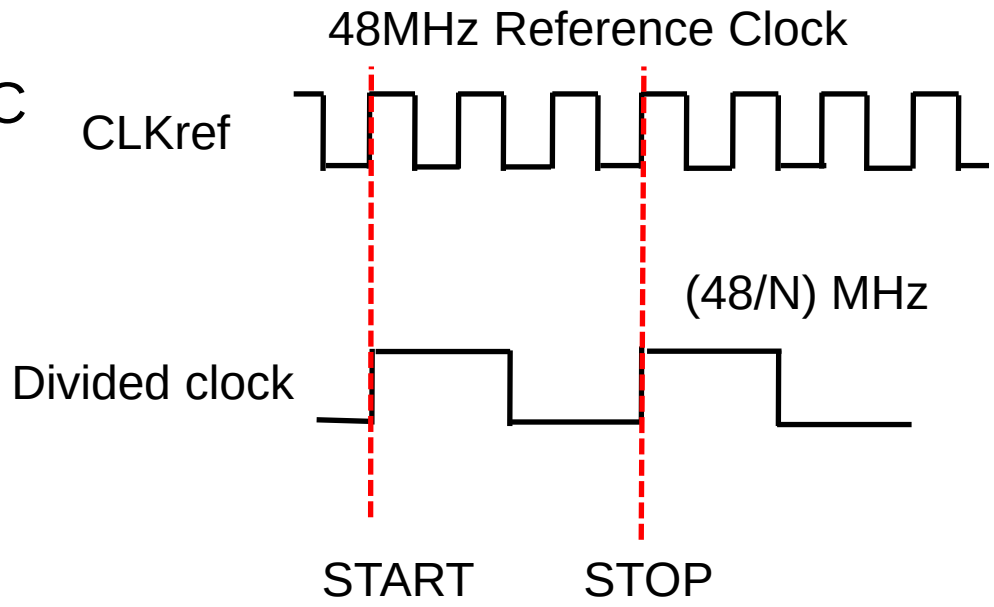
START, STOP Generation for TDC Evaluation

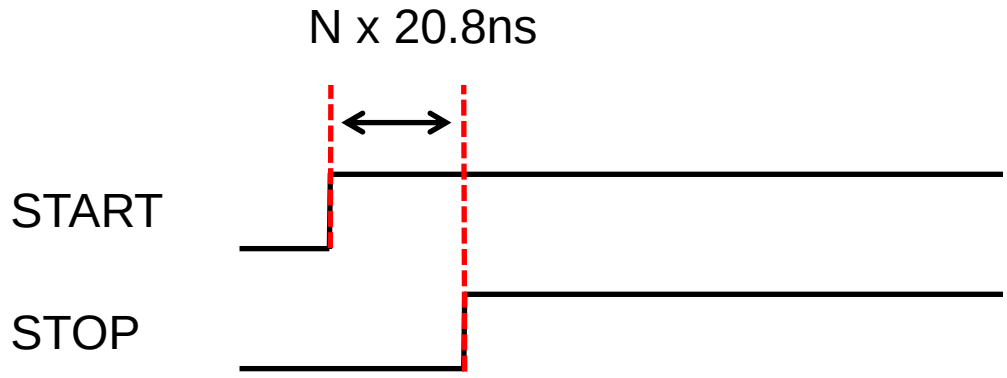
48MHz reference clock inside PSoC

Program control

- Divide reference clock
- Timing difference of N x 20.8ns

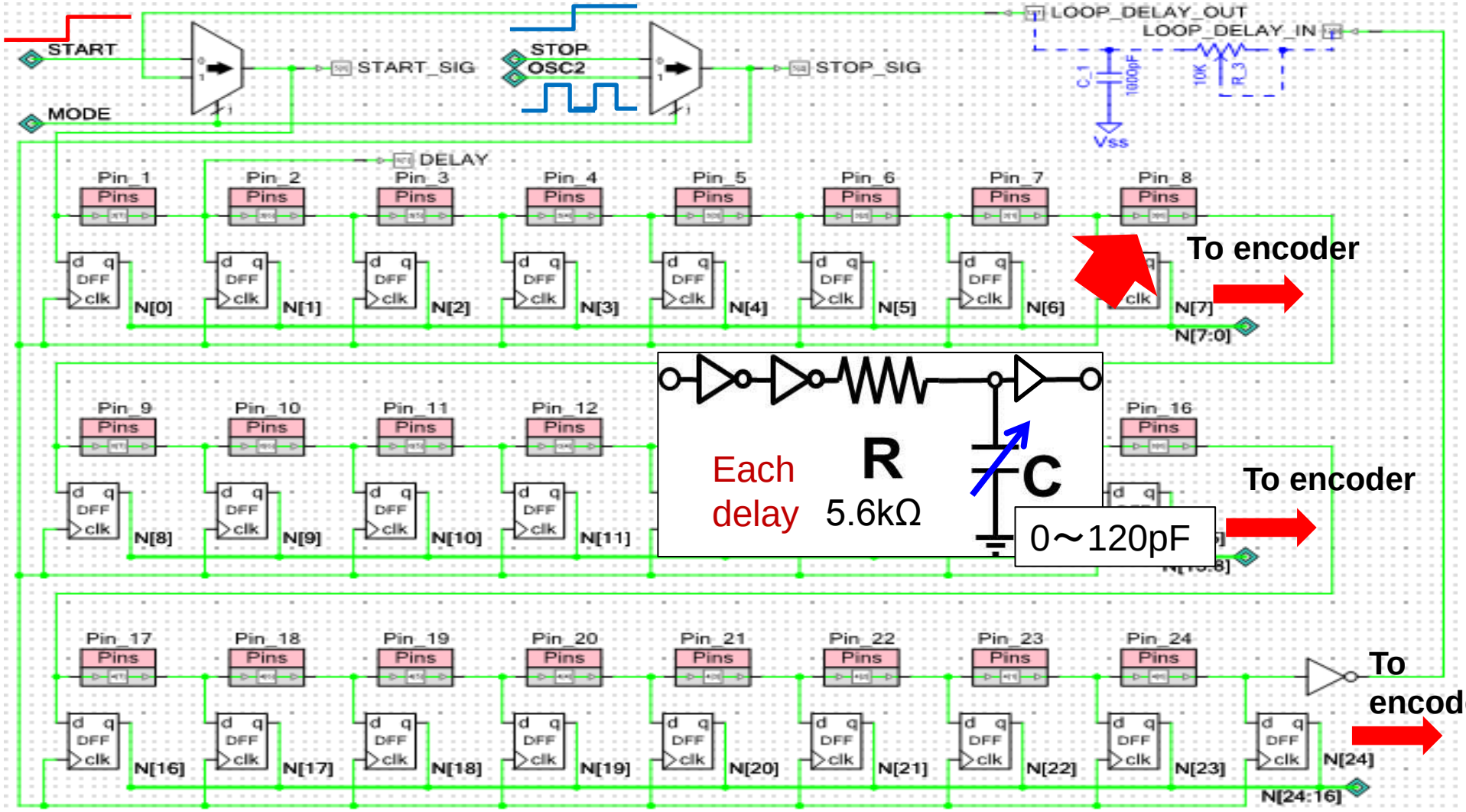
Precise timing signal generation





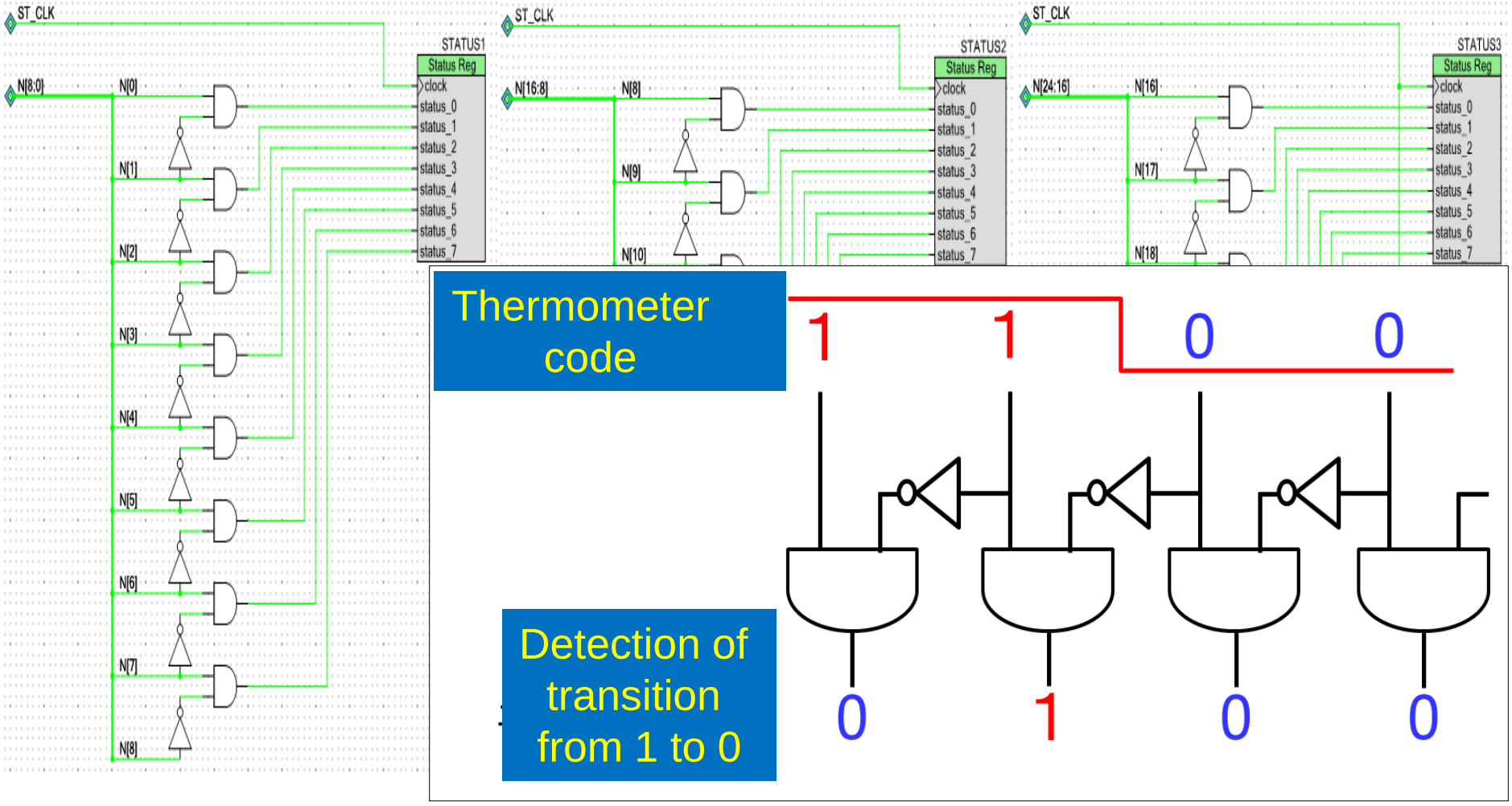
Use for TDC linearity evaluation

TDC and Ring Oscillator Circuit



Encoder Circuit

Thermometer code to binary code



Encode to binary code

Data Processing Software

- C＃ program
- Data were transferred via USB to a PC and processed there.

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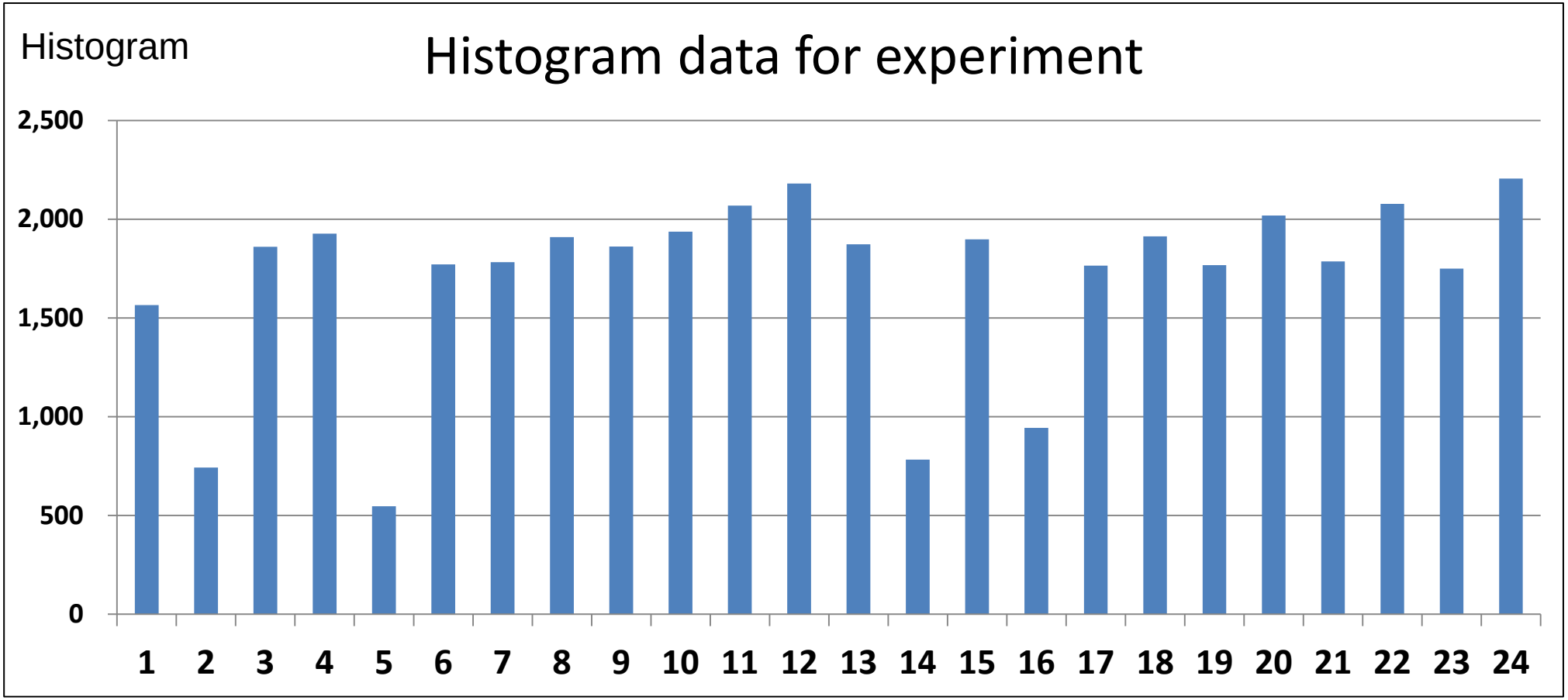
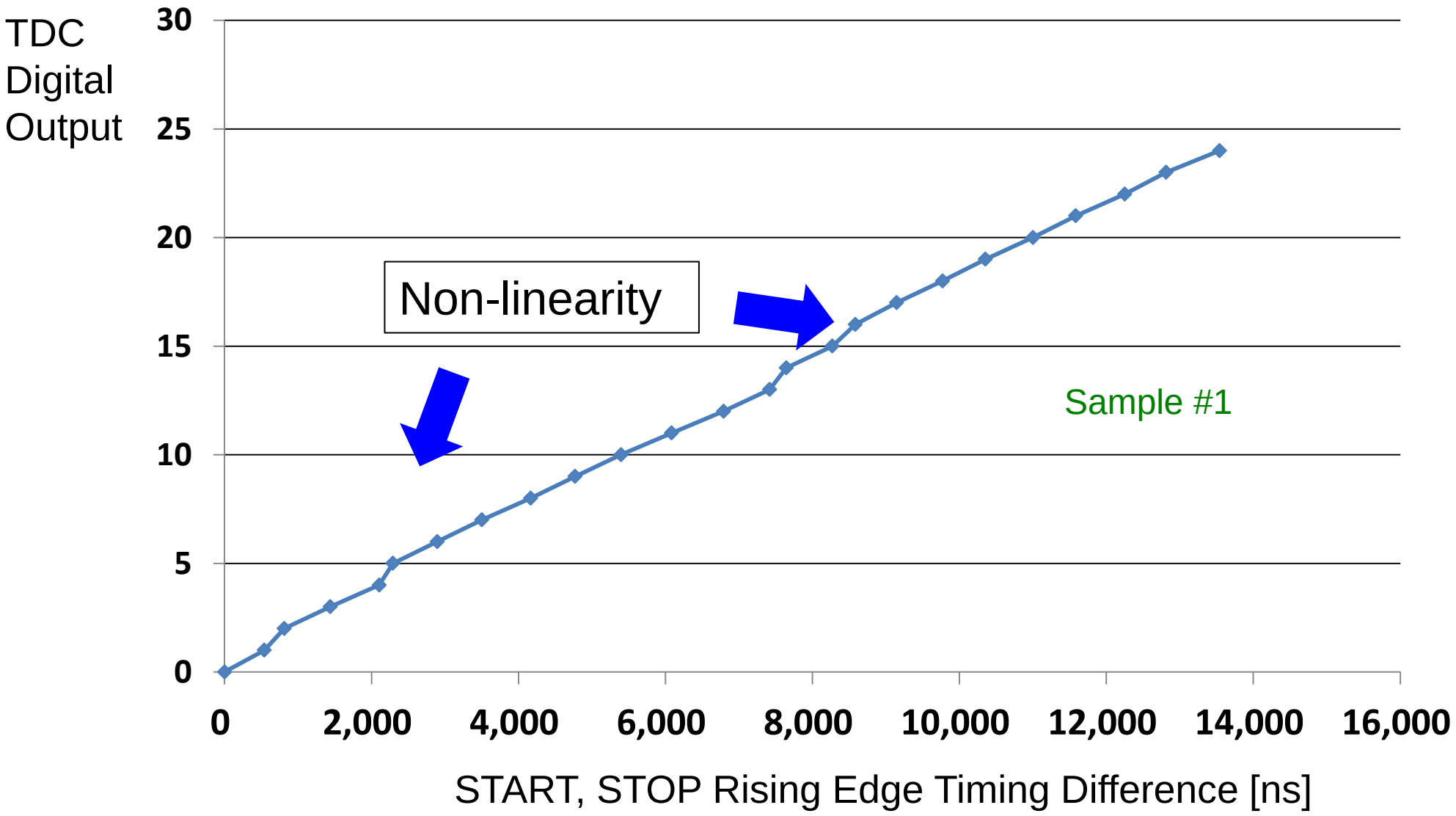
Histogram in Calibration Mode



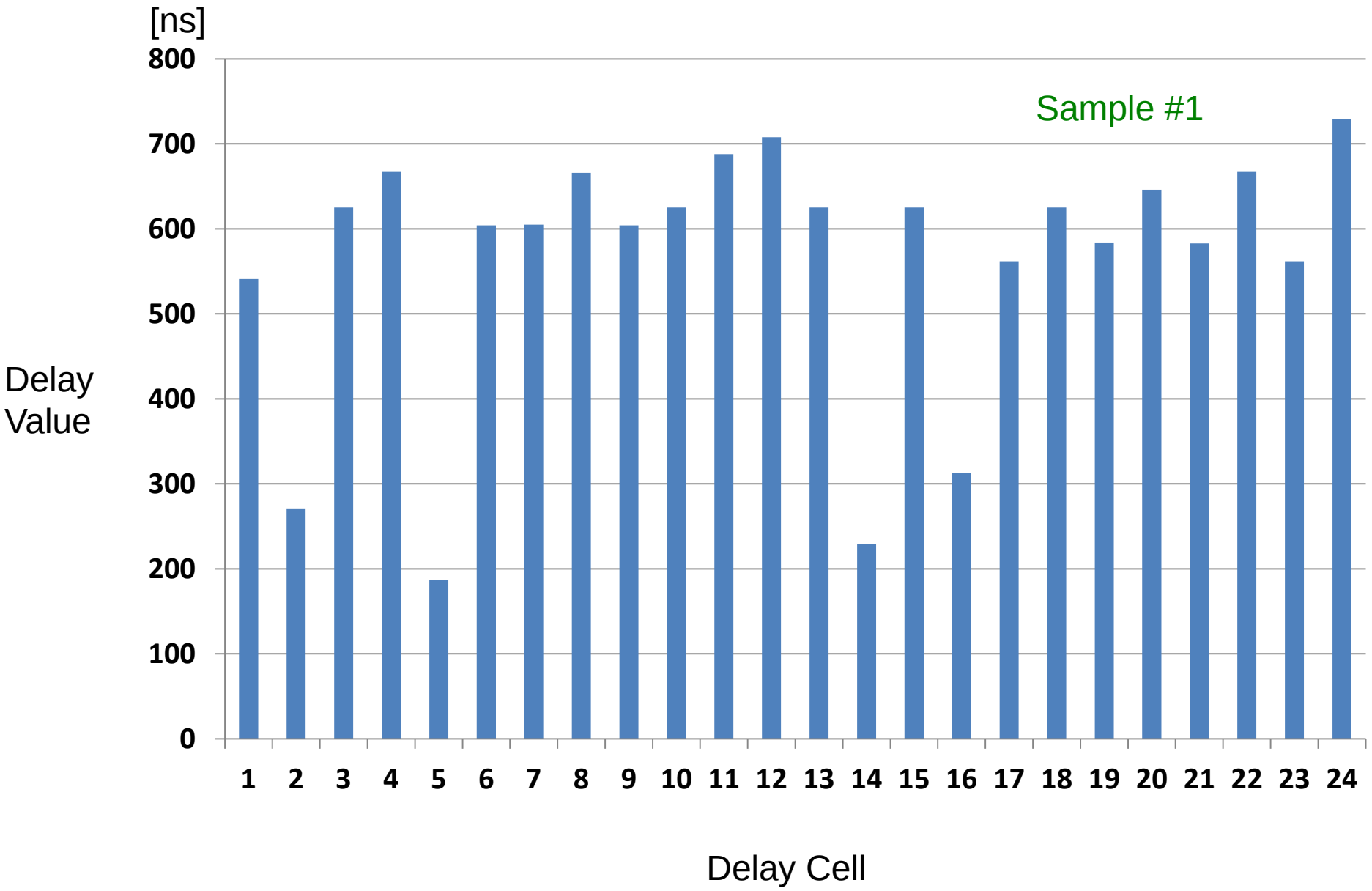
Sample #1

- Total number of data: 40934
- Average number of data for each bin: 1700

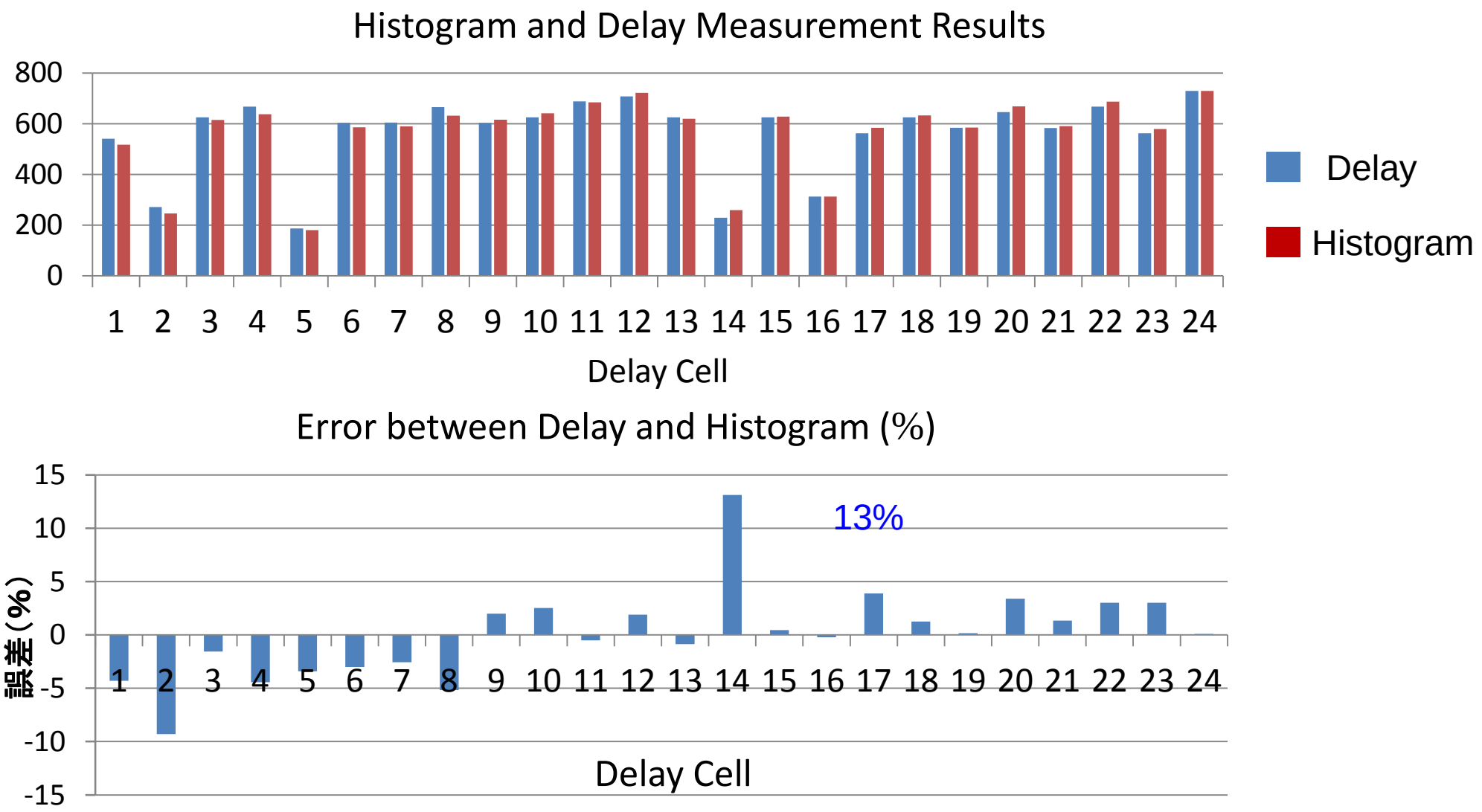
TDC Measurement Without Calibration



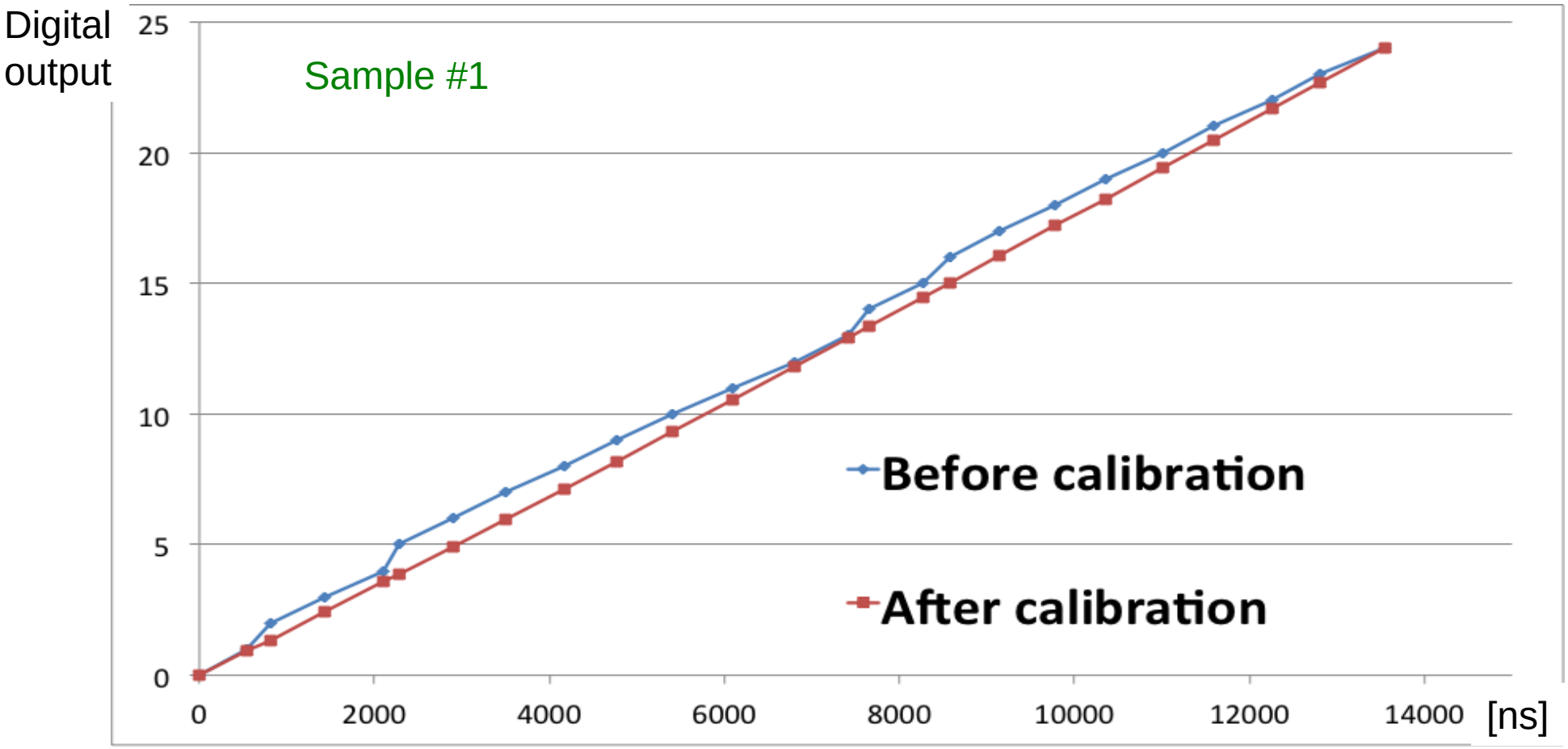
Actual Delay Data by Direct Measurement



Correlation Between Histogram and Delay

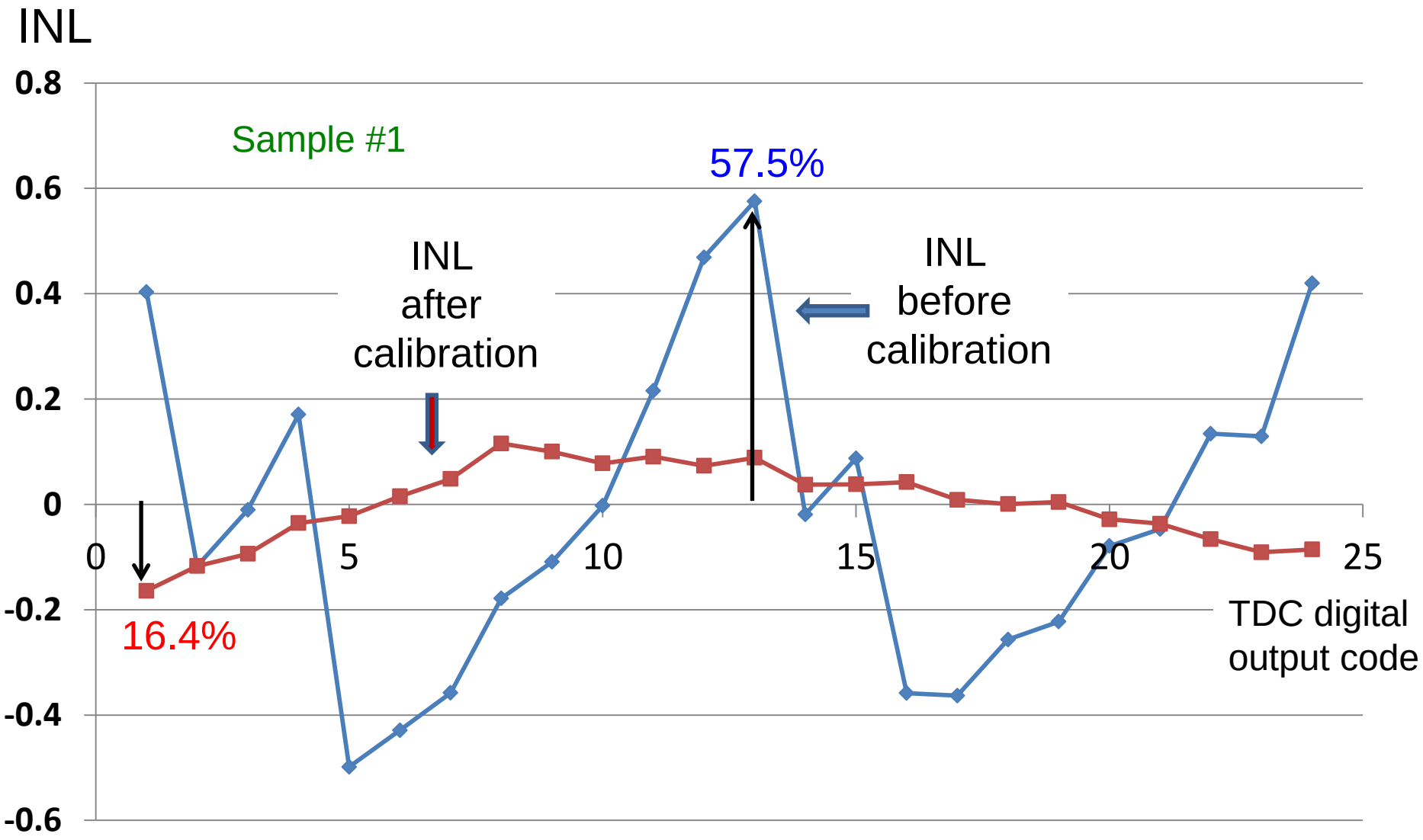


TDC Characteristics Before and After Calibration

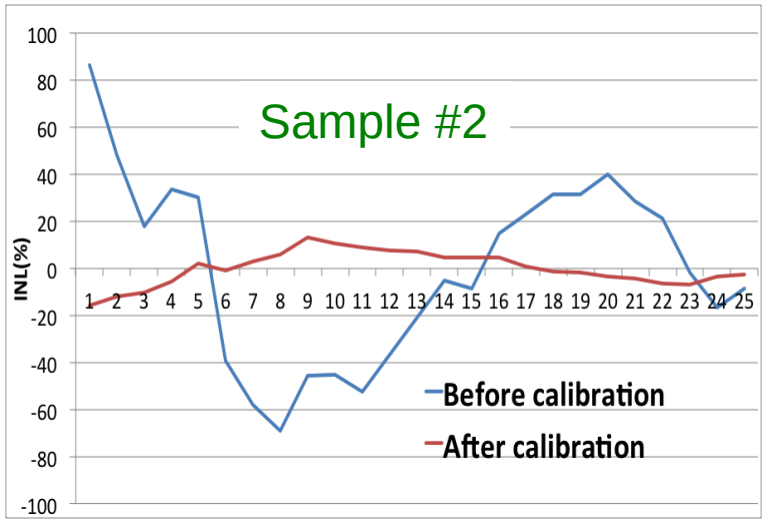


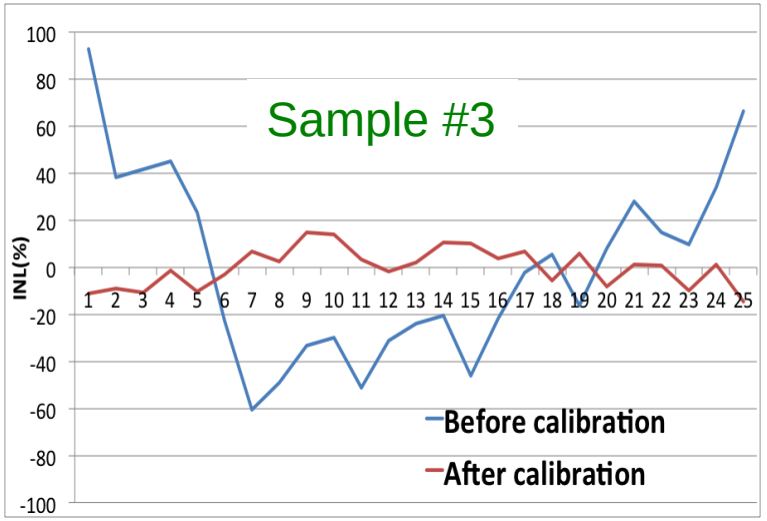
Time difference between two clock rising edges

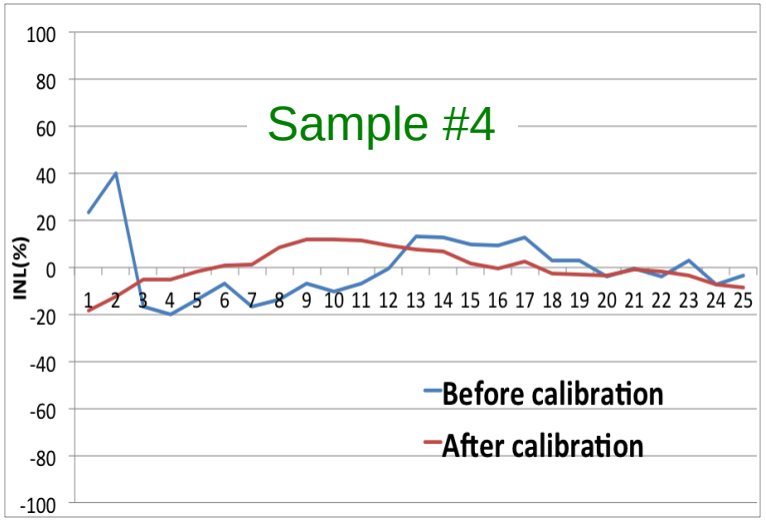
INL Before and After Calibration (1)

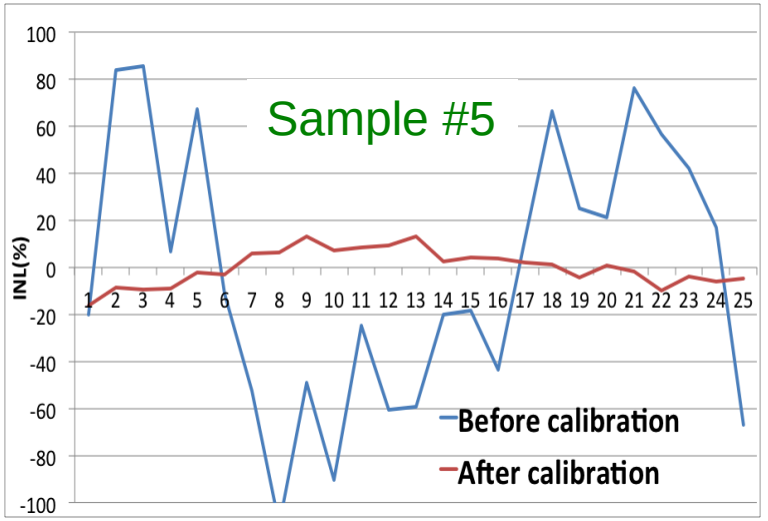


INL Before and After Calibration (2)









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Conclusion

- A TDC with self-calibration was implemented using an analog FPGA.
- Measurement results showed

  ➡ Linearity improved by self-calibration.
- All-digital implementation is possible.

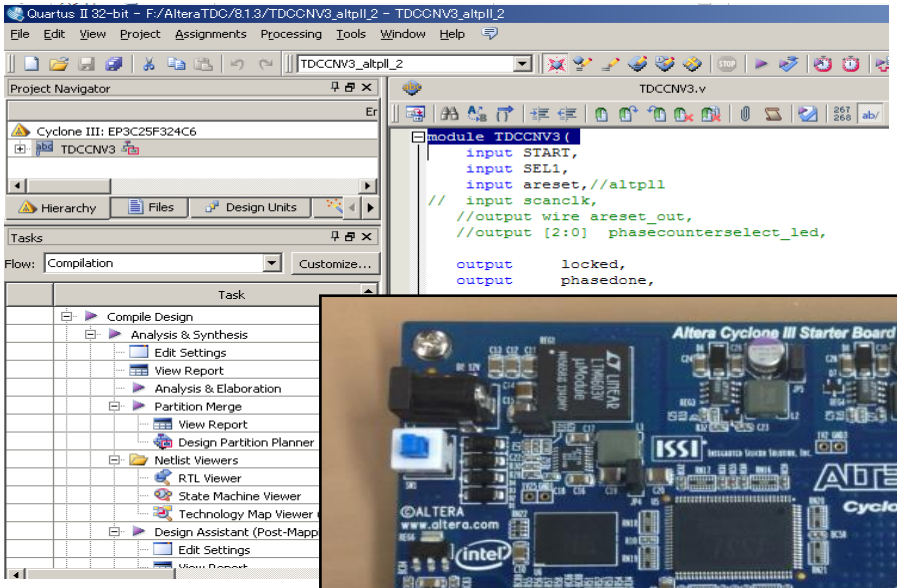
  ➡ Suitable for fine CMOS

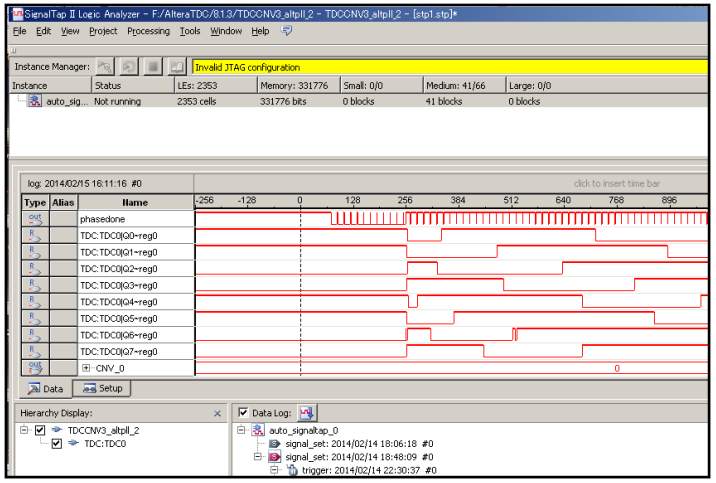
  ➡ BOST for timing signal test

Altera FPGA (Full digital Implementation)

TDC with histogram method self-calibration

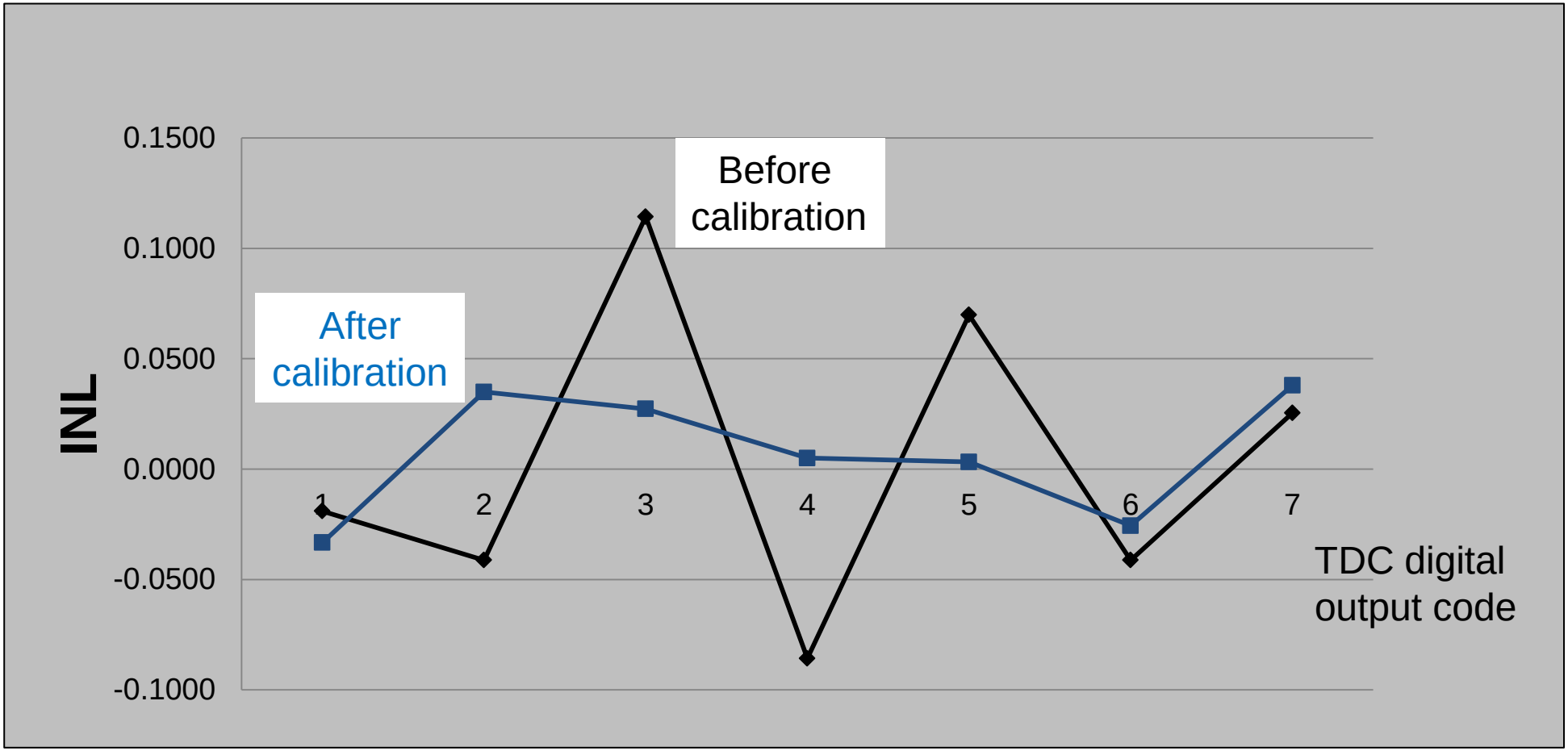
Delay cell array was implemented with a CMOS inverter chain.





INL Before and After Self-Calibration

Measurement results



Thank you for kind attention

Time continues indefinitely.

Kobayashi Laboratory

We are analog design & test researchers, but we appreciate digital technology.

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