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Performance Improvement of Analog / Mixed-Signal IC Using Signal Processing Techniques

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群馬大学
GUNMA UNIVERSITY

Contents

- Motivation
- Digitally Assisted Analog Technology
  - Region1： Continuous Amplitude, Continuous Time
  - Region2： Continuous Amplitude, Discrete Time
  - Region3： Discrete Amplitude, Continuous Time
  - Region4： Discrete Amplitude, Discrete Time
- Discussion
- Conclusion

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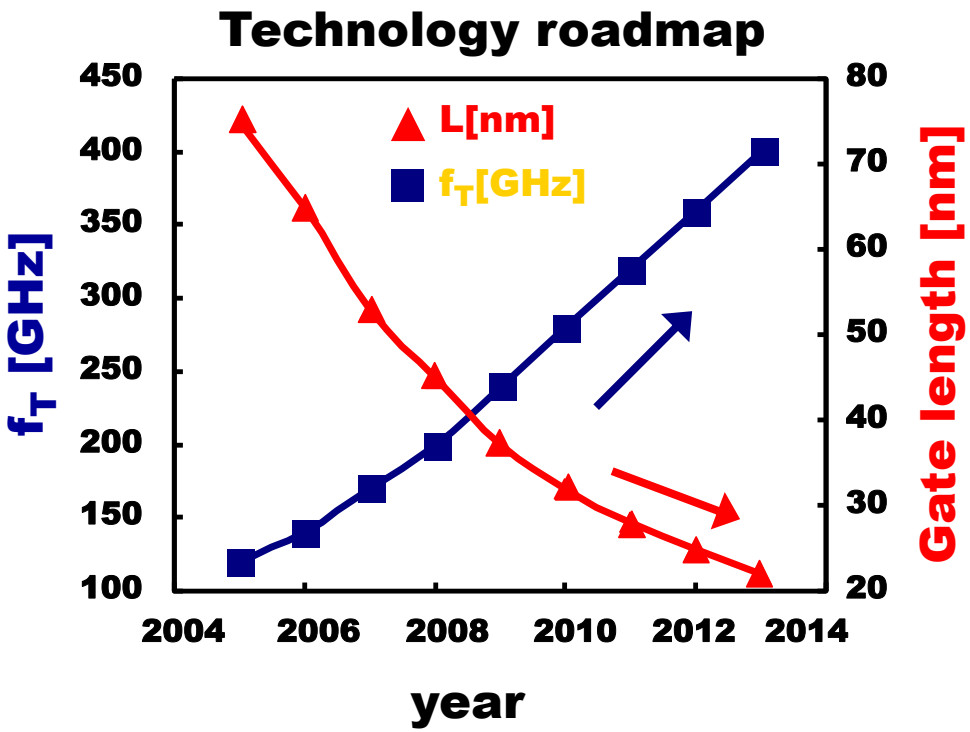
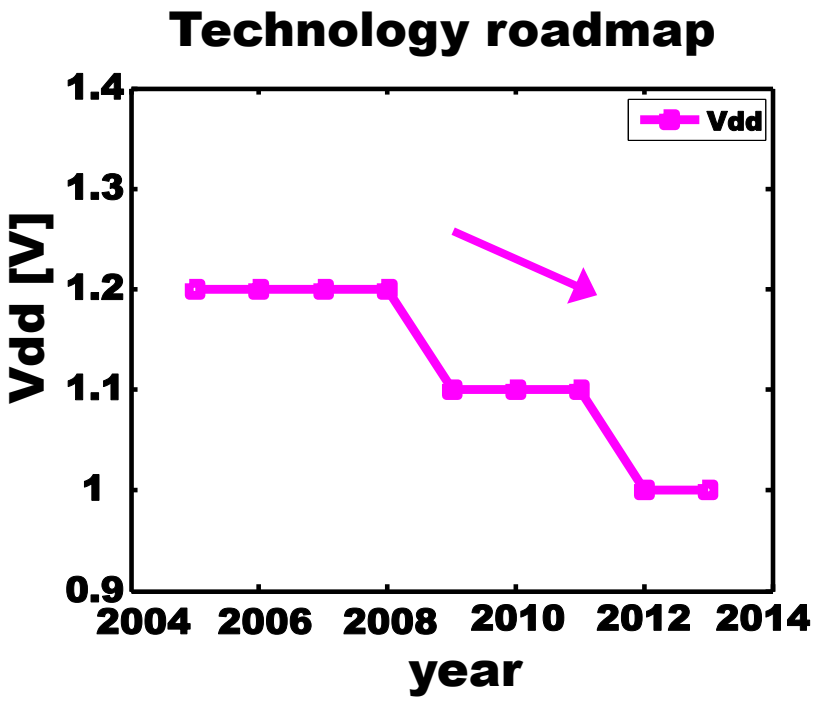
Nano CMOS Era Has Come





- Fine CMOS ⇒ High Speed （Time domain resolution)

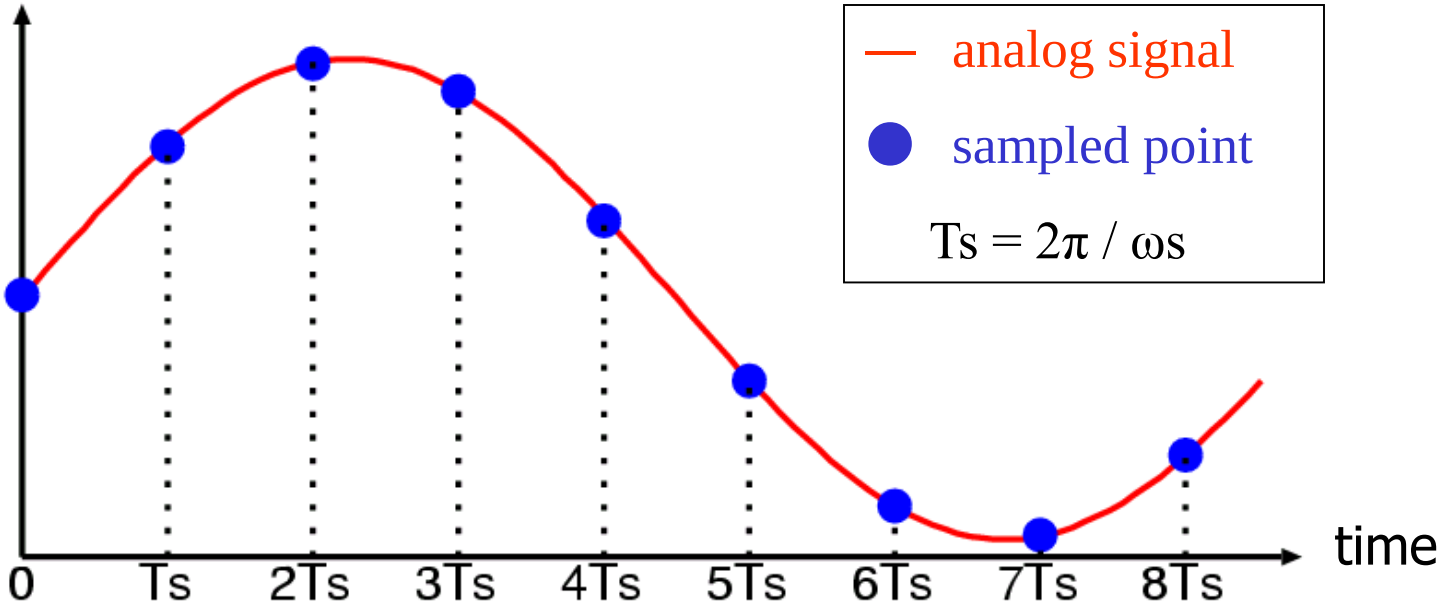
Low breakdown (Vdd→ low) , Drain resistance → small

Position of Analog Technology in Modern Electronics

- Digital technology is great !
- Today,
  analog technology is
  for digital technology.

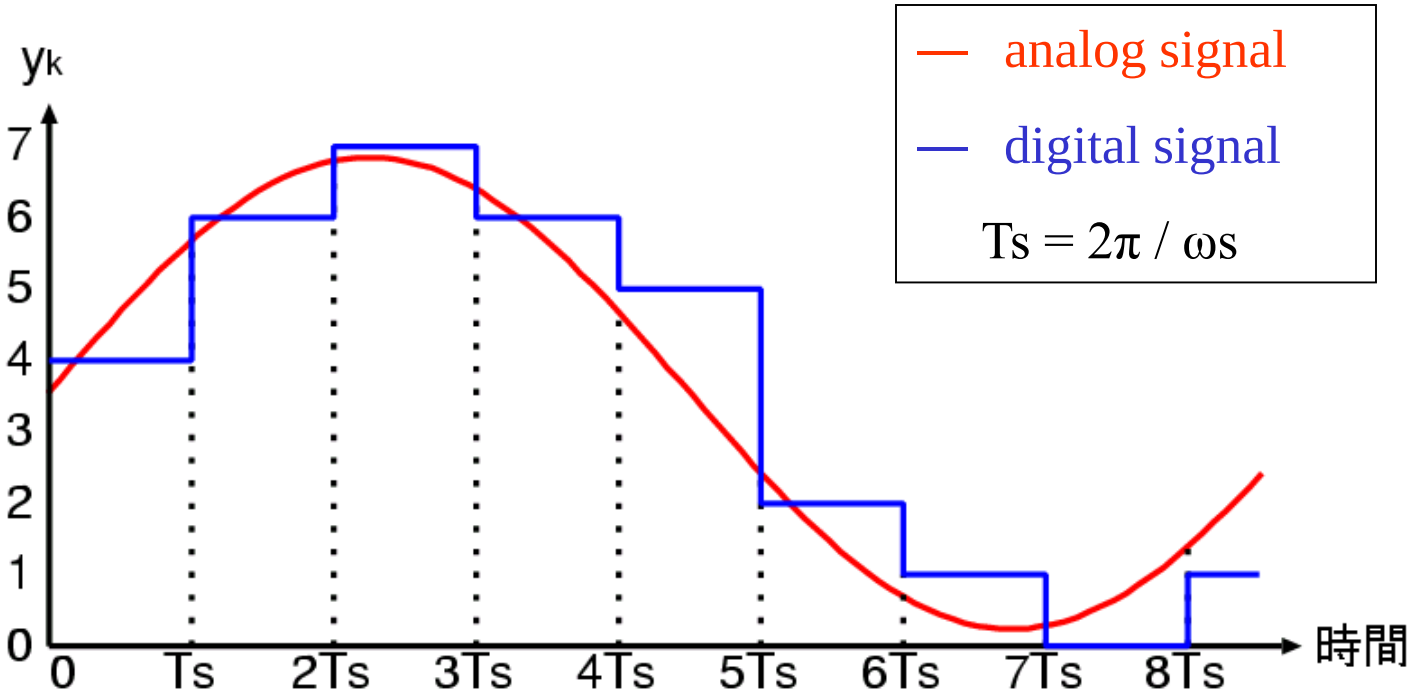
Cooperation between analog and digital is important !

Digital Signal Feature（1）
Discrete Time（Sampling）



Take sampled points and discard the others.

Digital Signal Feature(2)
Amplitude Quantization



Amplitude rounding

4 Regions for Circuit Design

	Continuous Time	Discrete Time
Continuous Amplitude	Region 1 Analog	Region 2 Switched Cap. Sampler
Discrete Amplitude	Region 3 TDC, PWM	Region 4 Digital

Region 1 : Good for bipolar

Region 2, 3, 4 : Good for CMOS

Statement of this paper

Analog in nano CMOS era ⇒ Use all 4 regions

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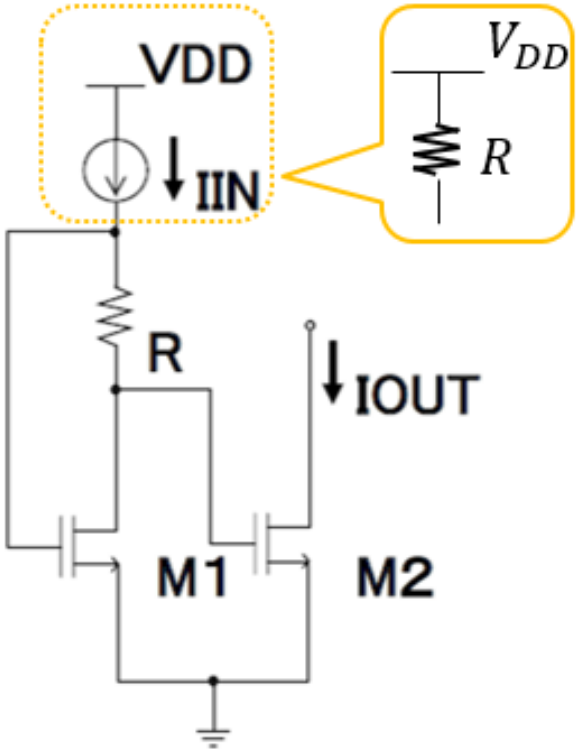
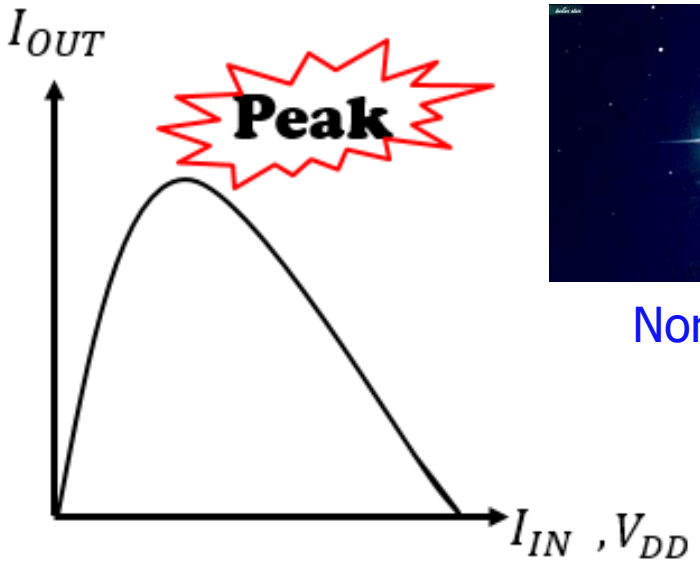
[1] M. Hirano, N. Kushita, Y. Moroshima, H. Harakawa, T. Oikawa, N. Tsukiji, T. Ida, Y. Shibasaki, H. Kobayashi, “Silicon Verification of Improved Nagata Current Mirrors”, IEEE International Conference on Solid-State and Integrated Circuit Technology (Nov. 2018)

[2] M. Hirano, N. Tsukiji, Haruo Kobayashi, "Simple Reference Current Source Insensitive to Power Supply Voltage Variation - Improved Minoru Nagata Current Source", IEEE International Conference on Solid-State and Integrated Circuit Technology (Oct., 2016)

Original Nagata Current Mirror



MOS Nagata
Current Mirror Circuit



Peaking current characteristics

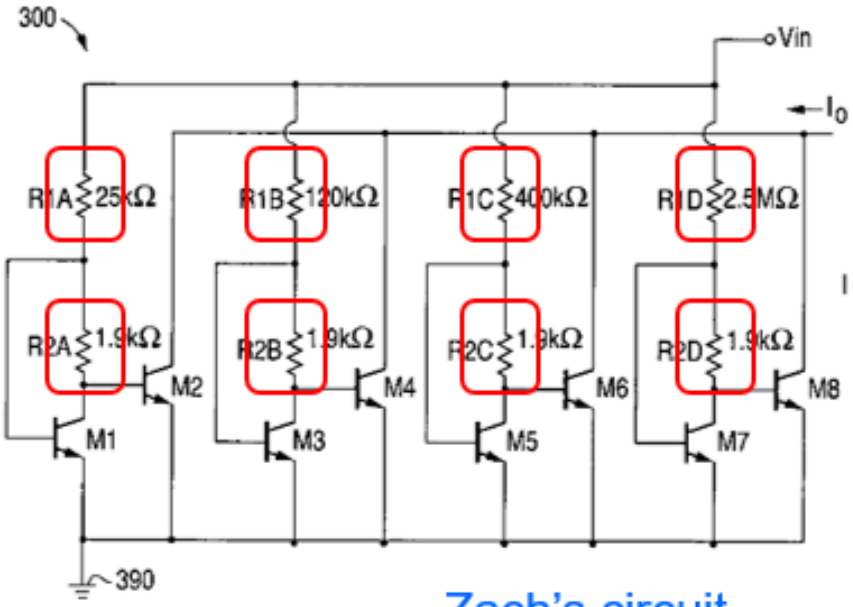
North Star

At peak vicinity

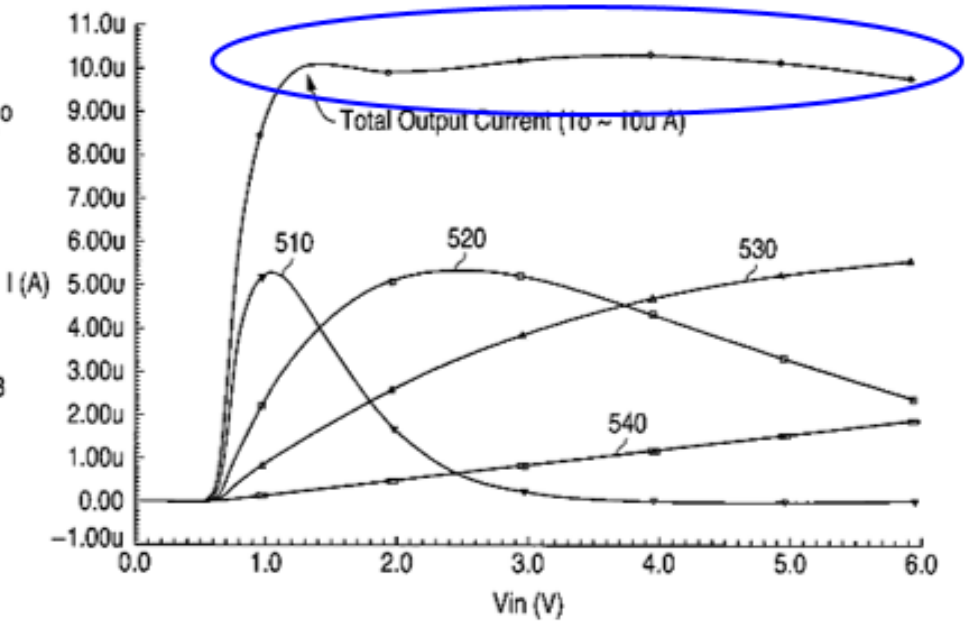
Small output current change
against input current change

Simple ➡ Widely used. Ex: in DC-DC converter ICs

Previous Improved Circuit



Zach's circuit

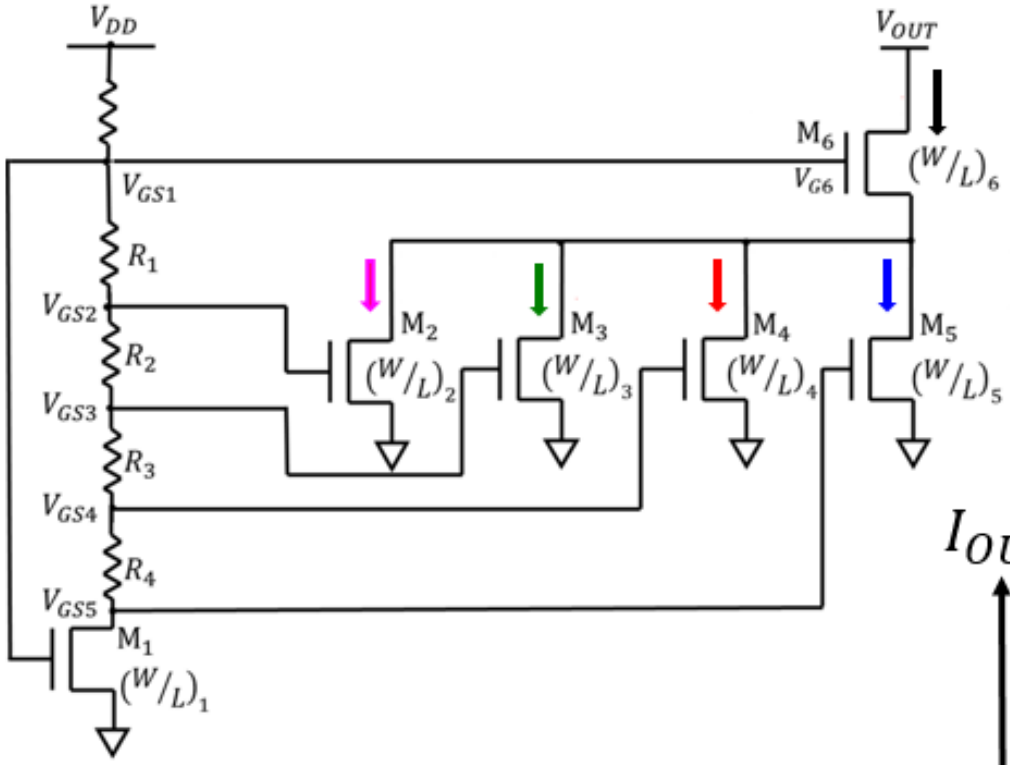


Inventor
Zachary Zehner Nosker
Obtained Ph.D.
from Gunma Univ.
Kobayashi Lab.

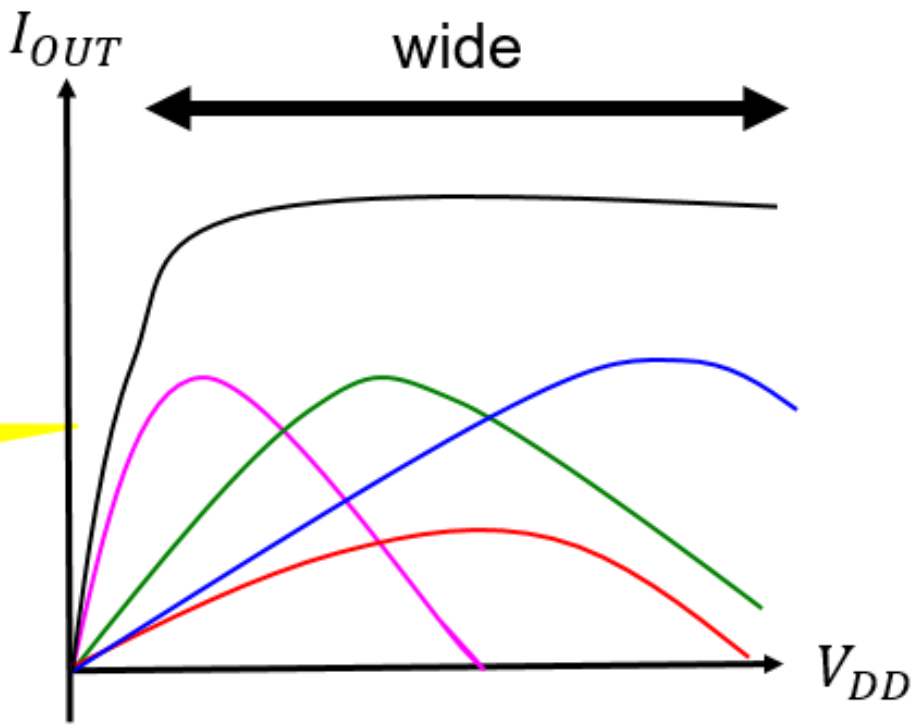
Problem

Parallel Resistors → Large chip area

MOS Reference Current Source Operation

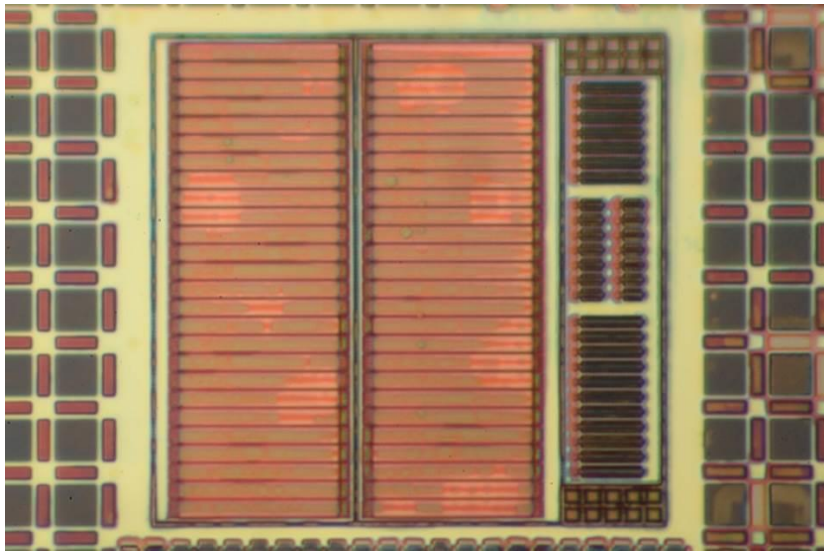


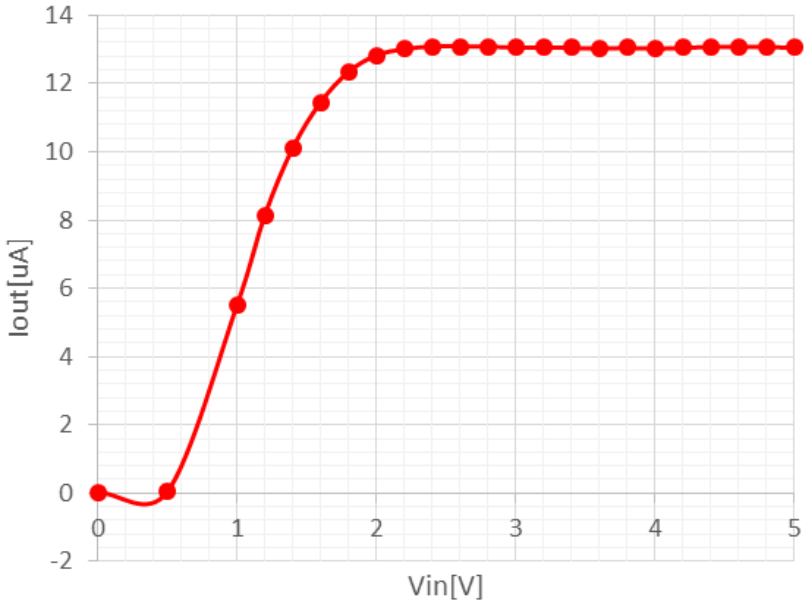
Almost constant total current



Simple Reference Current Source

Chip Fabrication / Measurement





Supported by ASO Inc.

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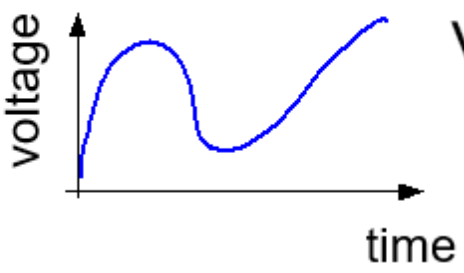
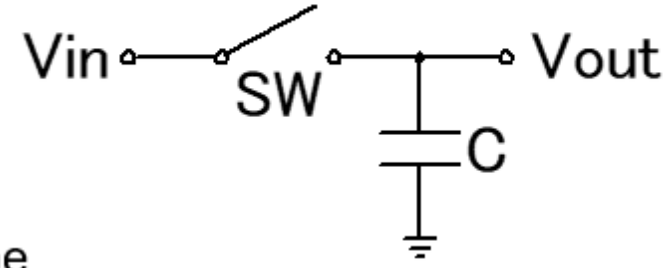
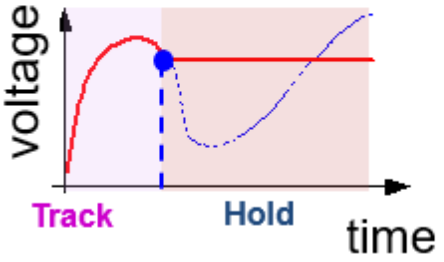
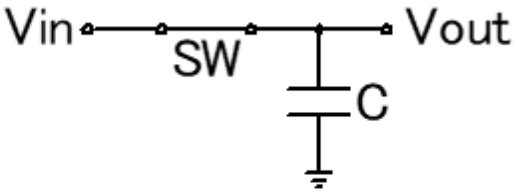
Sampling Circuit





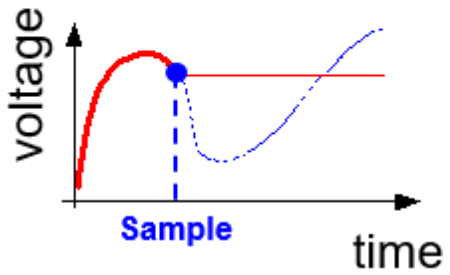


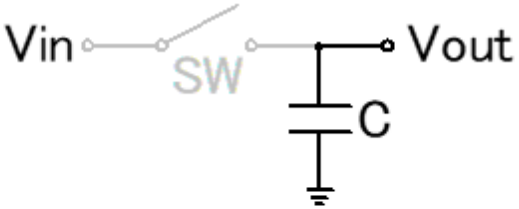


SW ON

- Vout(t) = Vin(t)

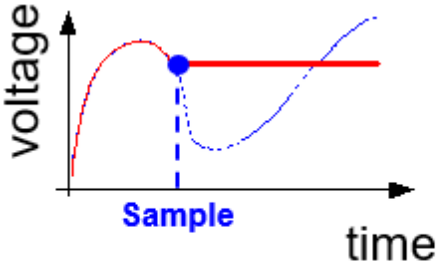
Track mode





- SW OFF
- Vout(t) = Vin(t_{OFF})

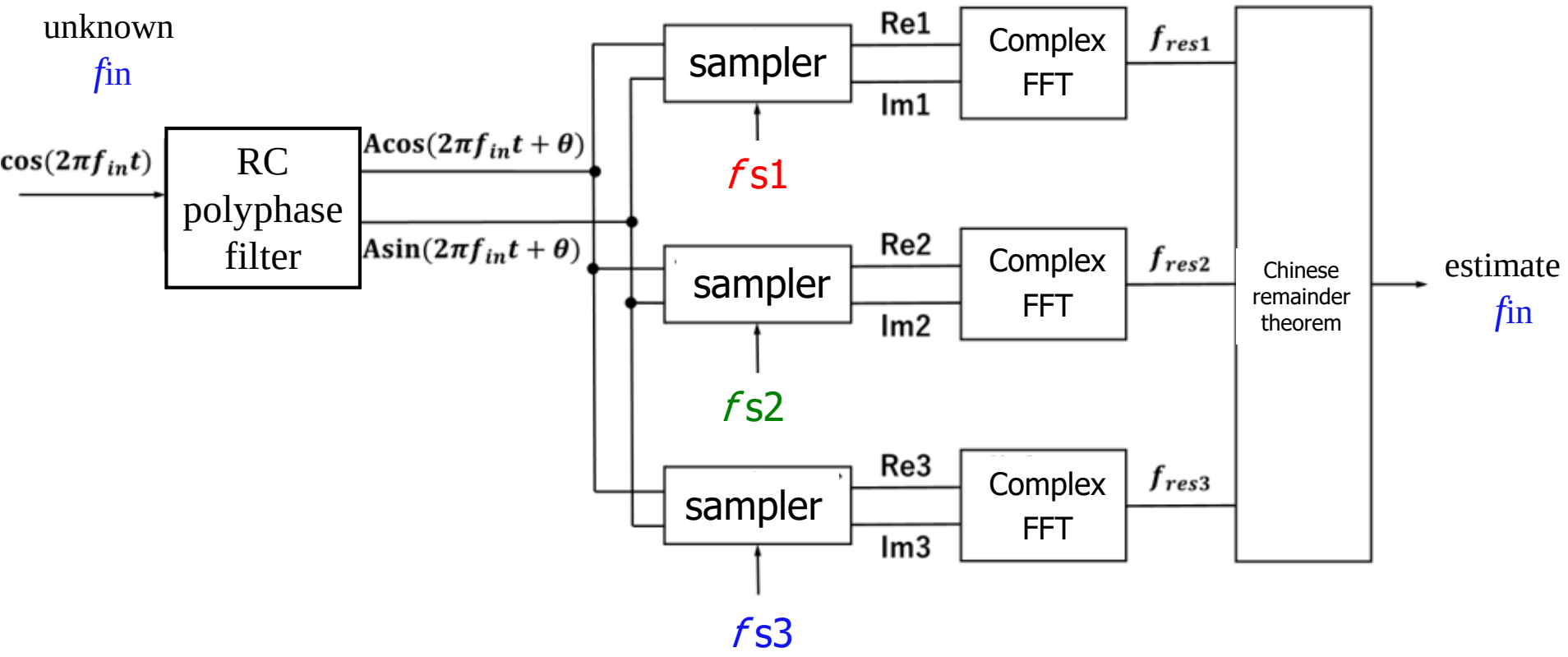
Hold mode



Frequency Estimation Sampler System

Giga Hertz order

Based on residue number system



kHz order sampling frequencies

f_{s1}, f_{s2}, f_{s3} are prime numbers.

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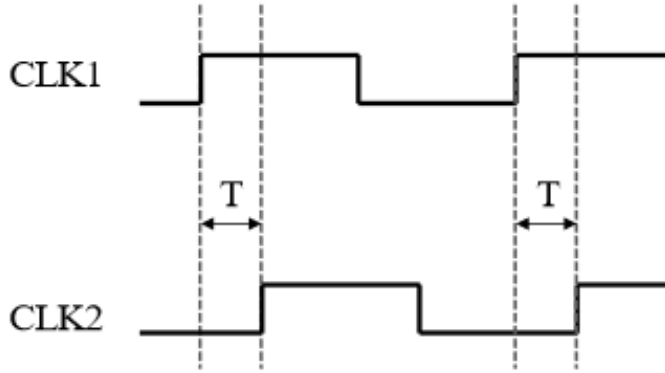
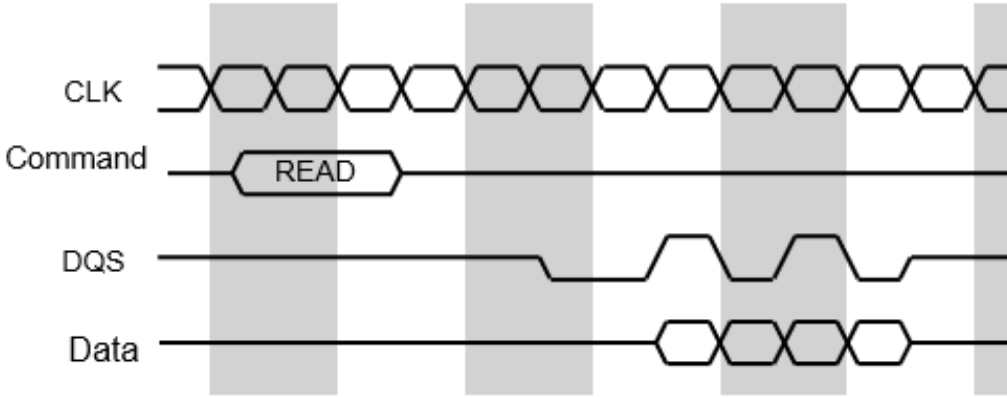
Time-to-Digital Converter (TDC)

- Testing the timing between two repetitive digital signals
  - Ex. Data and clock in Double Data Rate memory





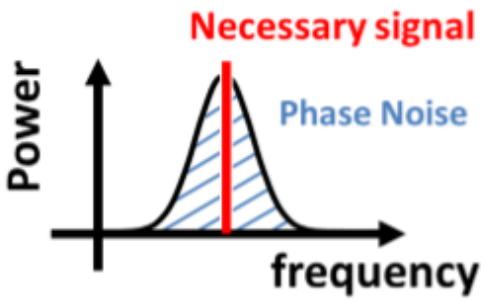
- Short testing time
- Good accuracy

Implement BOST with small circuitry

BOST: Built-Out Self-Test

Phase Noise Test with ΔΣ TDC

Phase noise in oscillator



Malfunction of electronic systems

- RF circuit & system
- ADC

Important

Phase noise test at low cost, in short time

Conventional

- **Expensive** : Spectrum analyzer
- **Long** : test time (~10seconds)

cost high

Proposed

Simple circuit

ΔΣ Time-to-Digital Converter

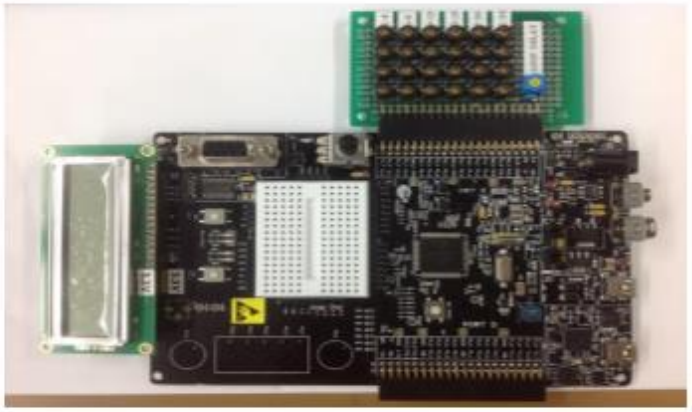
Low cost, high quality Phase noise test

[1] Y. Osawa, H. Kobayashi, "Phase Noise Measurement Techniques Using Delta-Sigma TDC", IEEE International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW'14), Porto Alegre, Brazil (Sept. 17-19, 2014).

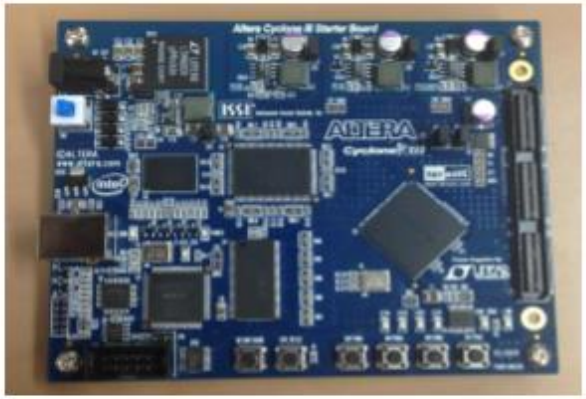
TDC BOSTs for Timing Signal Testing

Single-bit ΔΣ TDC with analog FPGA

Multi-bit ΔΣ TDC with analog FPGA



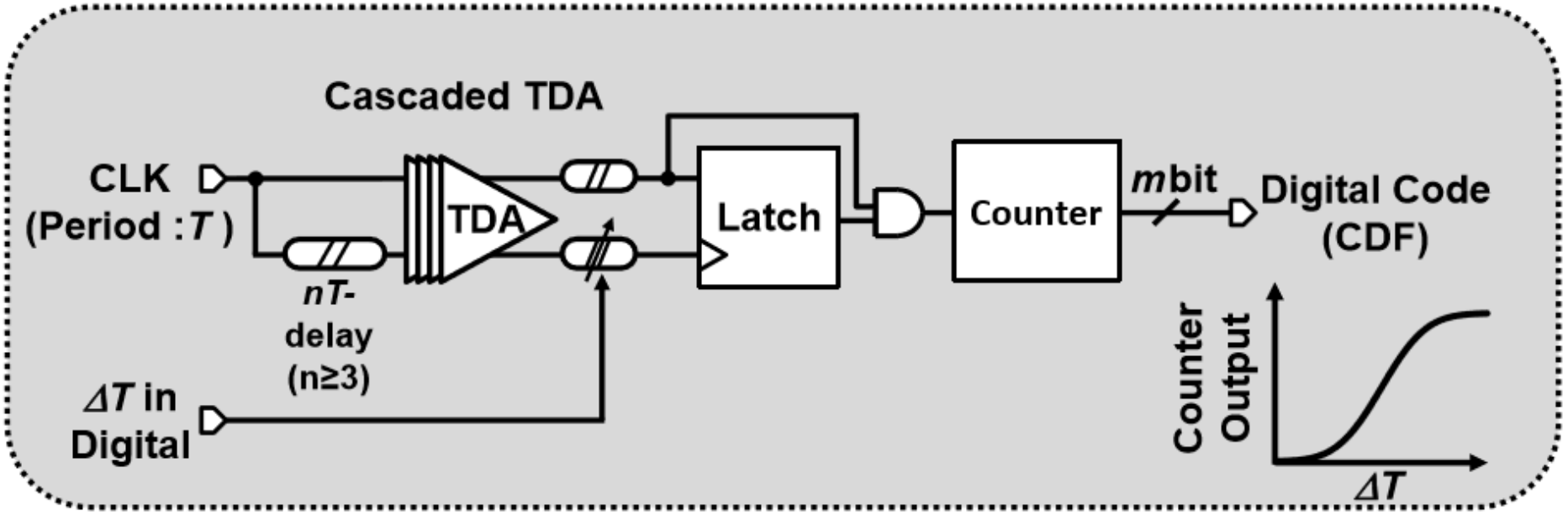
Flash-type TDC with analog FPGA



Flash-type TDC with digital FPGA

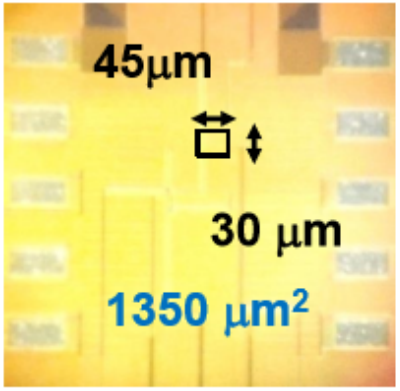
[2] T. Chujo, H. Kobayashi, "Experimental Verification of Timing Measurement Circuit With Self-Calibration", IEEE International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW'14), Porto Alegre, Brazil (Sept. 17-19, 2014).

On-chip Jitter Measurement Circuit



Experiments show that 1.67 ps RMS timing jitter can be measured

Process : 65 nm CMOS
Supply Voltage : 1.2 V



[3] K. Niitsu, H. Kobayashi , "CMOS Circuits to Measure Timing Jitter Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier with Duty-Cycle Compensation," IEEE Journal of Solid-State Circuits, Nov. 2012.

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[1] Ru YI, Minghui WU, Koji ASAMI, Haruo KOBAYASHI, Ramin KHATAMI, Atsuhiro KATAYAMA, Isao SHIMIZU, Kentaroh KATOH
"Digital Compensation for Timing Mismatches in Interleaved ADCs",
IEEE 22nd Asian Test Symposium, Yilan, Taiwan, (Nov. 2013).

Research Background & Objective

ATE System

■ Background

High-speed sampling time-interleaved ADC for ATE system

Timing skew ➡ Big issue

Error compensation of timing skew effects

Conventional

Analog method + Digital method

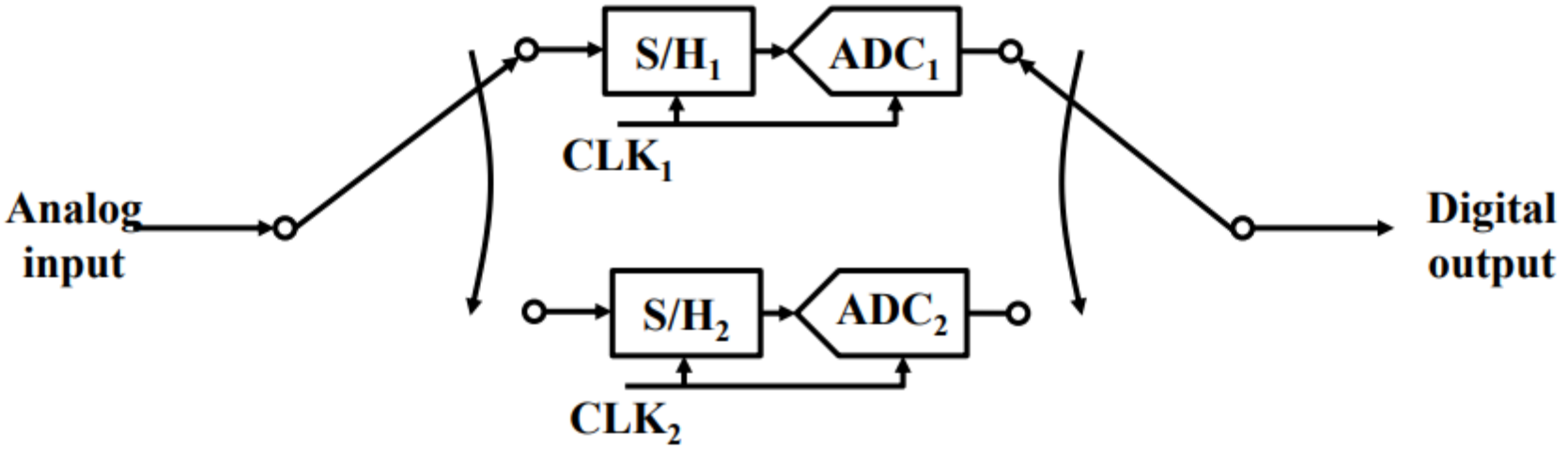
■ Objective

Proposal

Full digital method

High accuracy, Stable, Reliable

2-channel Interleaved ADC

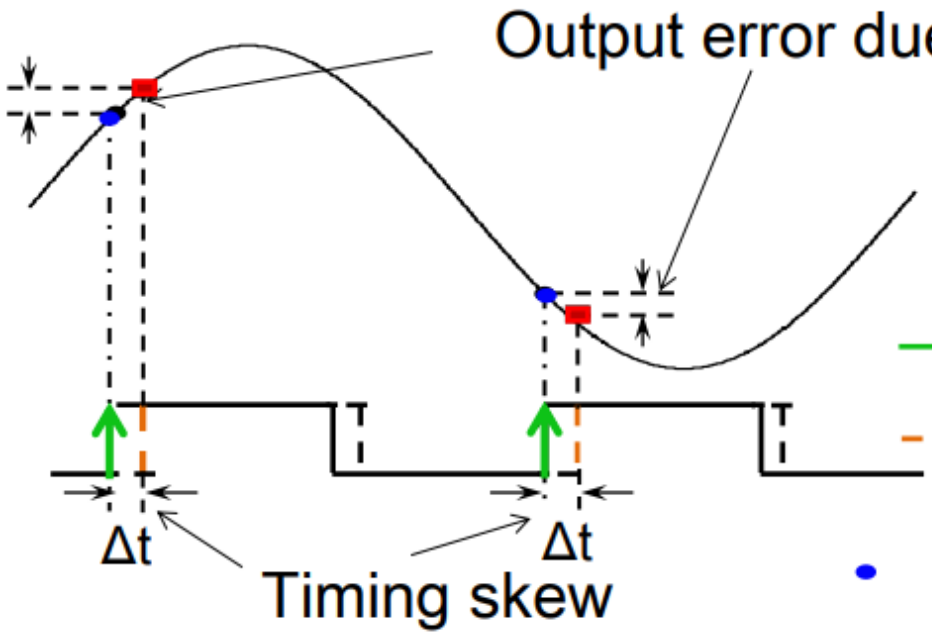


CLK1 reference

CLK2 delayed by half period

2 times sampling rate

Timing Error in Sampling



Ideal clock

Actual clock

Ideal sampling points

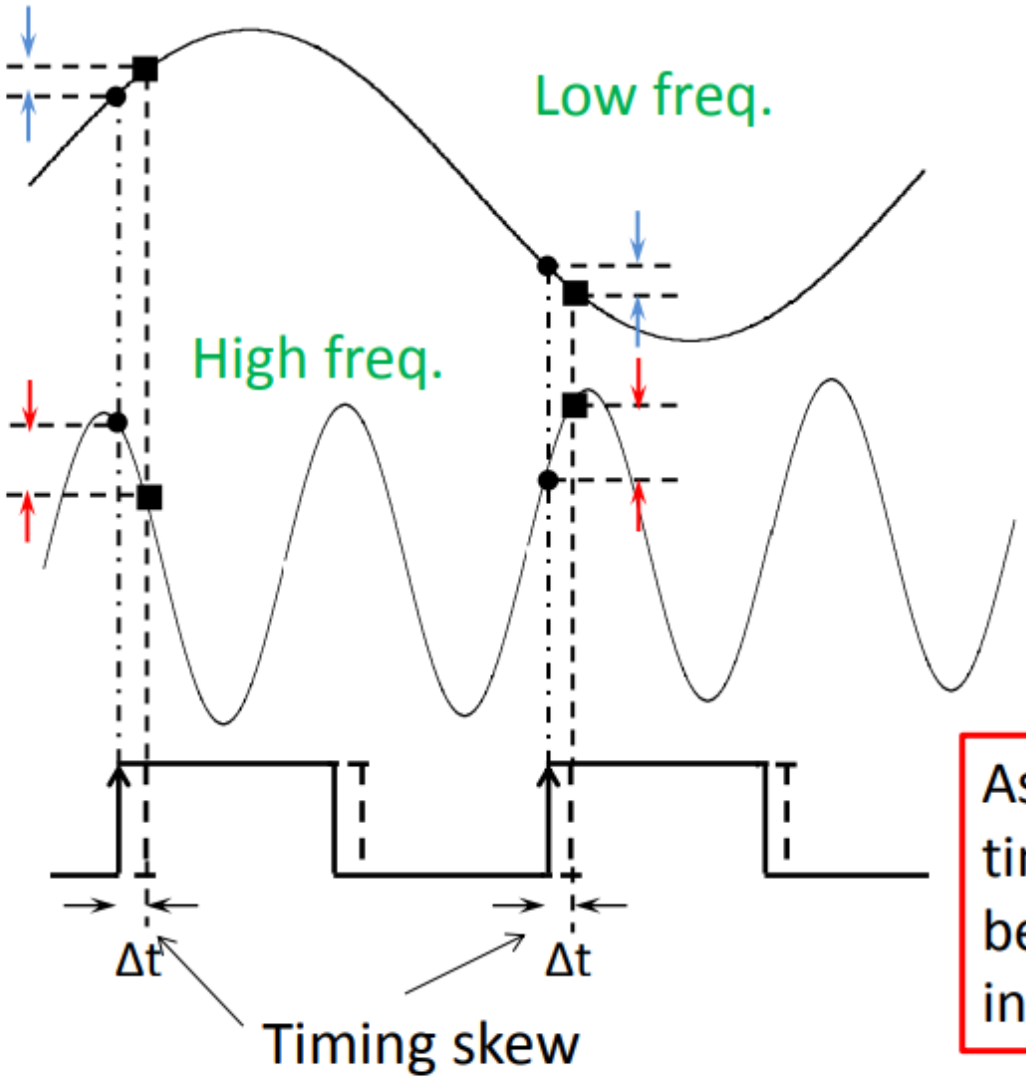
Actual sampling points

Timing error (horizontal error)

↓

Sampled voltage error (vertical error)

Input Frequency & Output



Input freq. ⬆

⬇

Output error⬆

As input frequency increases,
timing skew problem
becomes serious
in interleaved ADC.

Proposed Calibration System

- Full digital
- Timing Skew Detection
  - Cross-correlation of two channel ADC outputs
- Timing Skew Effect Compensation
  - Delay linear digital filter
- Calibration Control
  - Successive approximation algorithm
  - Foreground calibration

Correlation of R(0)and R(1)

CH1 ADC output: $f[n]$

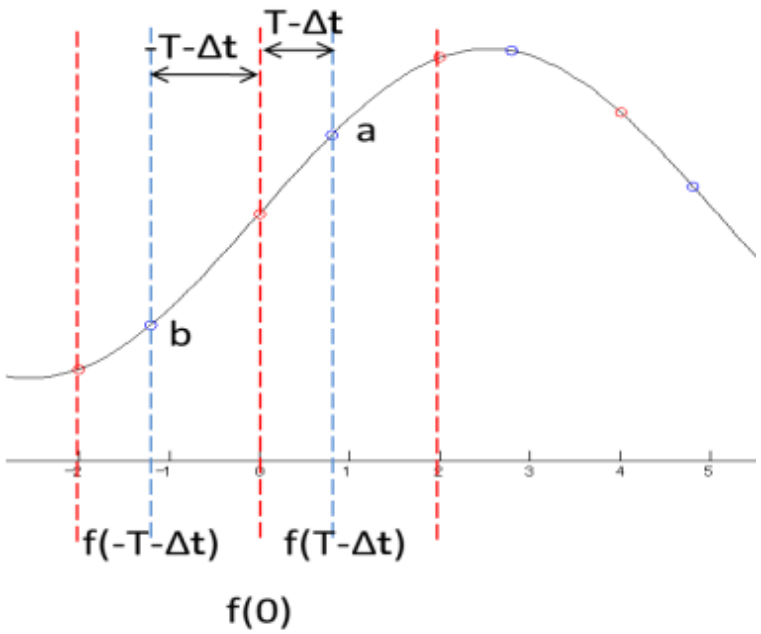
CH2 ADC output: $g[n] = f[n+T-\Delta t]$

lag 0,

$$R(0) = R_{ff}[0] = \lim_{n\to\infty} \frac{1}{n} \sum_{-n}^{n} f[n] f[n+T-\Delta t]$$

lag 1,

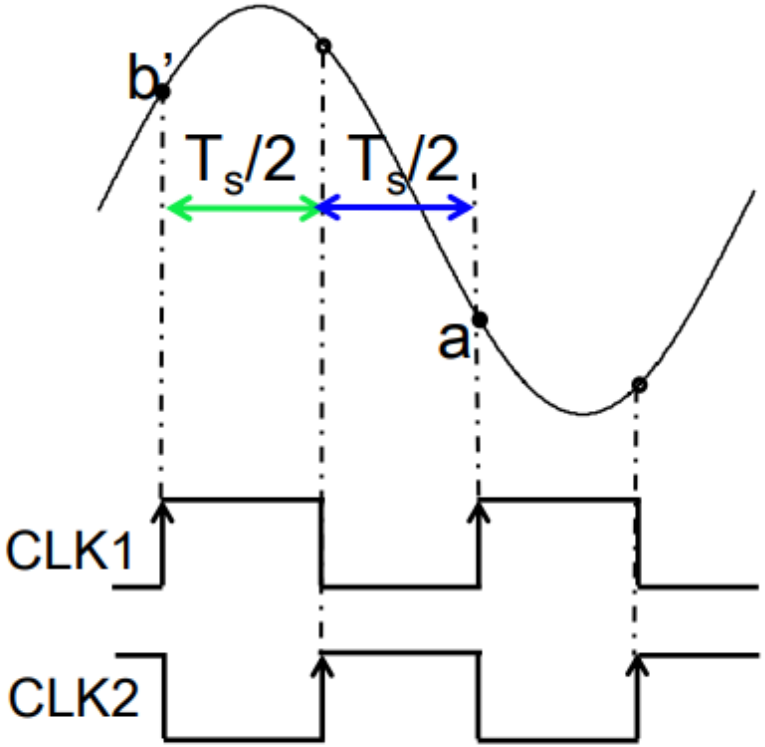
$$R(1) = R_{ff}[-2T] = \lim_{n\to\infty} \frac{1}{n} \sum_{-n}^{n} f[n] f[n-T-\Delta t]$$

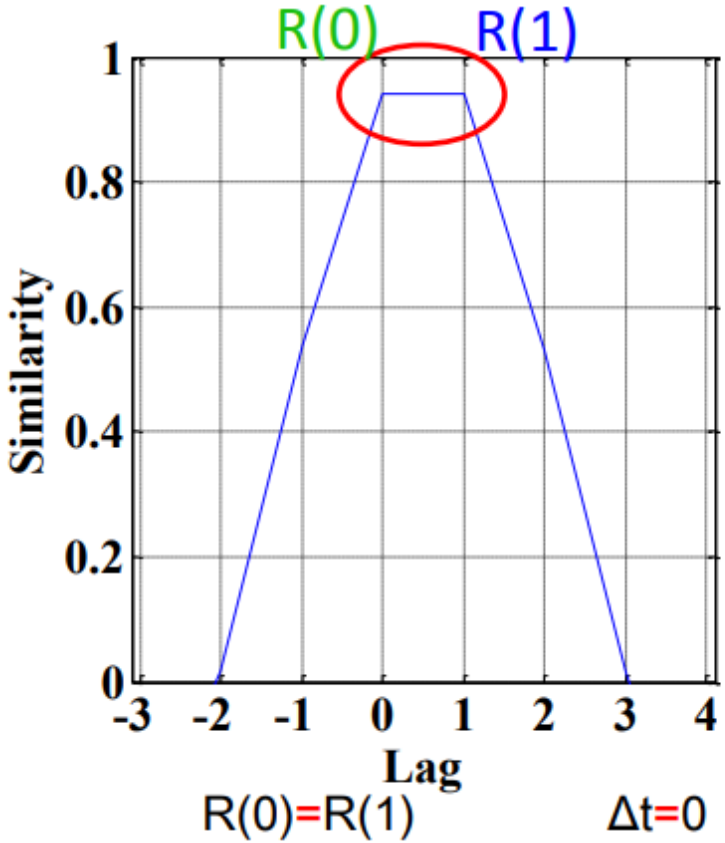


Timing skew Δt

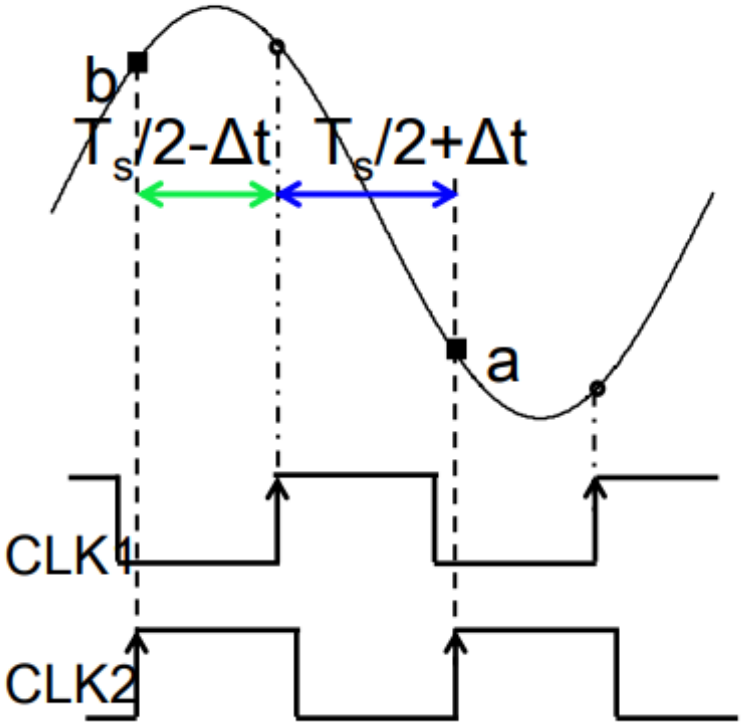
Timing Skew Detection

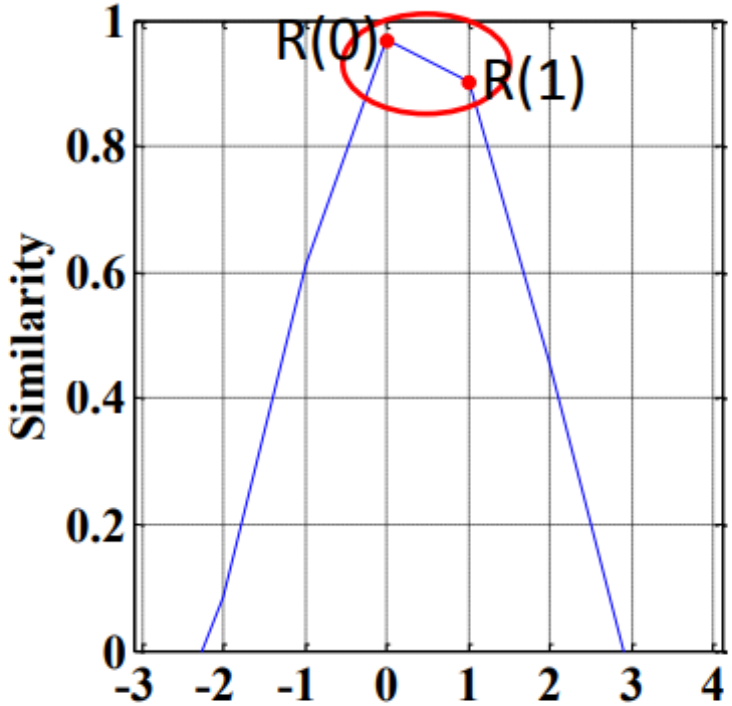
Cross-Correlation without Timing Skew





Cross-Correlation with Timing Skew





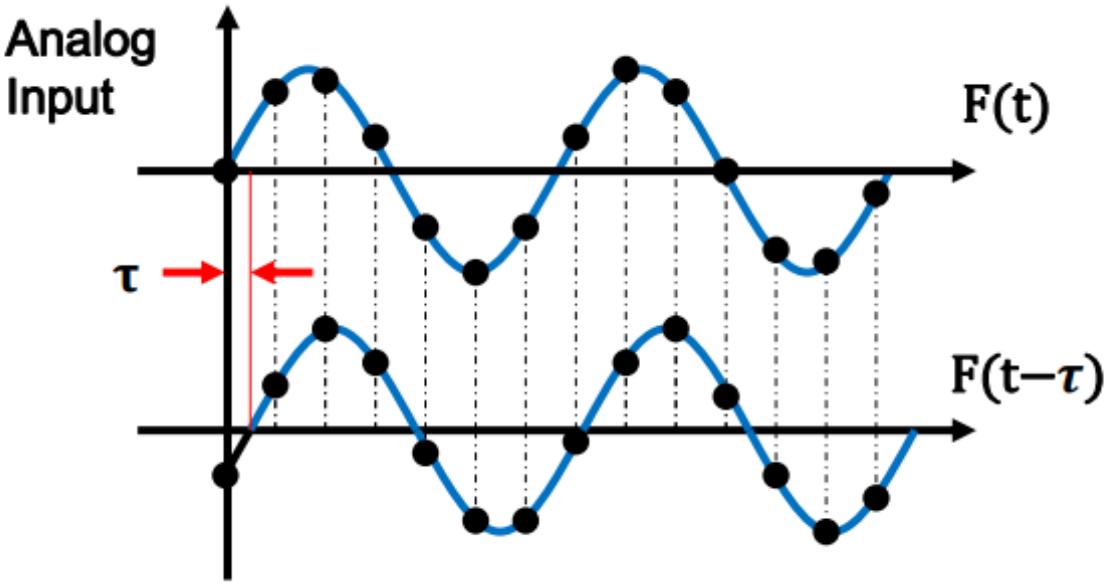
R(0)>R(1) Δt<0

R(0)<R(1) Δt>0

cross-correlation value ⇒ Sign of Δt (Δt >0 or Δt <0)

Magnitude of |Δt|

Linear Phase Delay Digital Filter



Linear phase ⇒ maintain time-domain waveform

Conventional Linear-Phase Digital Filter :

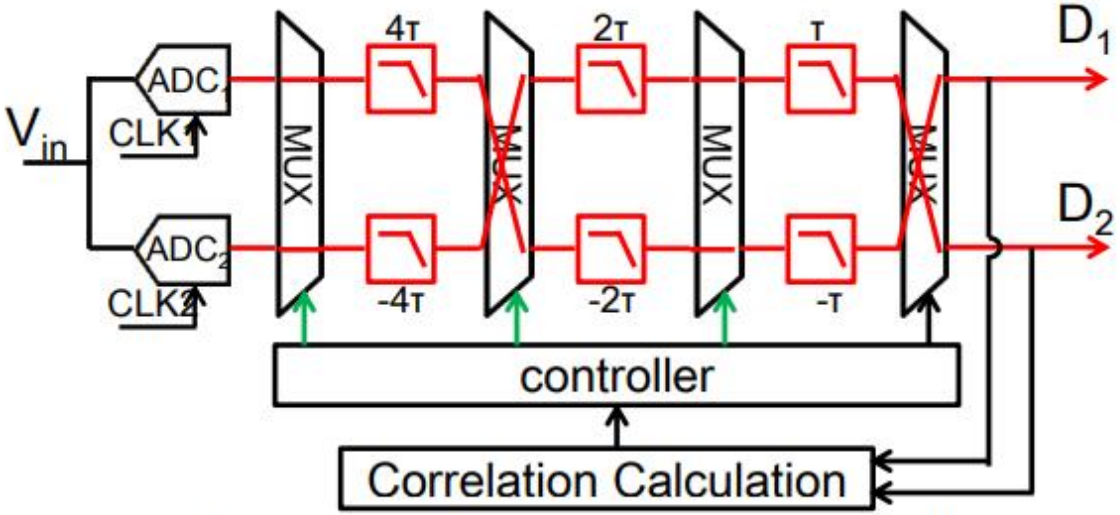
Group delay time resolution $T_s/2$

Proposed Linear-Phase Delay Digital Filter [1] :

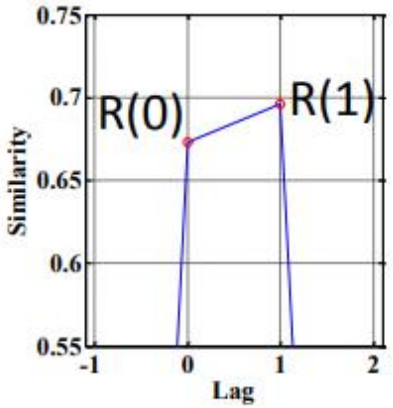
Arbitrary small time resolution τ

[1] K. Asami, et. al., "Timing Skew Compensation Technique using Digital Filter with Novel Linear Phase Condition," IEEE International Test Conference (Nov. 2010).

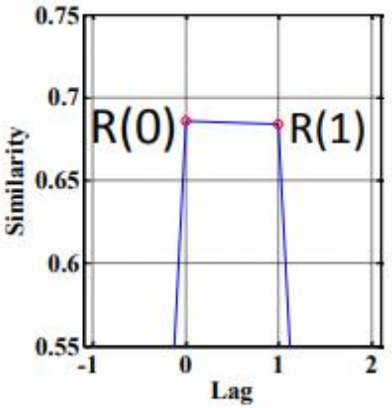
Calibration Done



before calibration



after calibration



Binary-search, successive approximation

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Conclusion

In nano CMOS era,
analog/mixed signal IC design should use
all of 4 circuit design regions.
Analog & digital signal processing

Good performance, low power,
low cost, fast turn around time
can be achieved.