Analog / Mixed-Signal Circuit Design Based on Mathematics

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Contents

● Statement of This Paper
● Analog Circuit Design based on Mathematics
● ADC/DAC Design based on Mathematics
● TDC Design based on Mathematics
● Conclusion
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Beautiful mathematics

\[ \Rightarrow \] good analog/mixed-signal circuit

Besides transistor level design

- Control theory
- Number theory
- Statistics
- Coding theory
- Modulation
- Signal processing algorithm

Enhance analog/mixed-signal circuit performance
Contents

- Statement of This Paper
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  - Complex Signal Processing and Analog Filter
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- TDC Design based on Mathematics
- Conclusion
Contents

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Our proposal

For
Analysis and design of operational amplifier stability

Use
Routh-Hurwitz stability criterion
    - Popular in control theory
    - Not in circuit design

We can obtain
Explicit stability condition for circuit parameters
(which can NOT be obtained only with Bode plot).

Routh-Hurwitz Stability Criteria

- **Transfer function of closed-loop system**

\[
G(s) = \frac{A(s)}{1 + fA(s)} = \frac{N(s)}{D(s)}
\]

- **Suppose**

\[
N(s) = b_m s^m + b_{m-1} s^{m-1} + \cdots + b_1 s + b_0
\]

\[
D(s) = a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + a_0
\]

- **System is stable if and only if**

Maxwell and Stodola found out!!

real parts of all the roots \( s_p \) of the following are **negative**:

\[
D(s) = a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + a_0 = 0
\]

- **To satisfy this, what are the conditions for** \( a_n, a_{n-1}, \ldots, a_1, a_0 \)?

Routh and Hurwitz solved this problem independently!!
Open-loop transfer function from small signal model

\[ A(s) = \frac{v_{out}(s)}{v_{in}(s)} = A_0 \frac{1 + b_1 s}{1 + a_1 s + a_2 s^2} \]

\[ b_1 = -\frac{C_r}{G_{m2}} \]

\[ A_0 = G_{m1}G_{m2}R_1R_2 \]

\[ a_2 = R_1R_2C_2 \left[ C_1 + \left(1 + \frac{C_1}{C_2}\right)C_r \right] \]

\[ a_1 = R_1C_1 + R_2C_2 + (R_1 + R_2 + R_1G_{m2}R_2)C_r \]
Explicit Condition for Feedback Stability

Closed-loop transfer function:

\[
\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{A(s)}{1 + fA(s)} = \frac{A_0(1 + b_1 s)}{1 + fA_0 + (a_1 + fA_0 b_1)s + a_2 s^2}
\]

Necessary and sufficient stability condition based on R-H criterion

\[a_1 + fA_0 b_1 > 0\]

\[R_1 C_1 + R_2 C_2 + (R_1 + R_2)C_r + (G_{m2} - fG_{m1})R_1 R_2 C_r > 0\]

Explicit stability condition for parameters
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RC Polyphase Filter

- Its input and output are complex signals.
- Passive RC analog filter
- One of key components in wireless transceiver analog front-end
  - I, Q signal generation
  - Image rejection

Differential Complex Input: \( V_{in} = I_{in} + j Q_{in} \)
Differential Complex Output: \( V_{out} = I_{out} + j Q_{out} \)

Roles of RC Polyphase Filter

● Sine, cosine signal generation

\[ I_{in} = \cos(\omega_{LO} t) \]
\[ Q_{in} = 0 \]

Polyphase Filter

\[ I_{out} = A \cos(\omega_{LO} t + \theta) \]
\[ Q_{out} = A \sin(\omega_{LO} t + \theta) \]

● Image rejection

\[ I_{in} = (A + B) \cos(\omega t) \]
\[ Q_{in} = (A - B) \sin(\omega t) \]

Polyphase Filter

\[ I_{out} = A \cos(\omega t) \]
\[ Q_{out} = A \sin(\omega t) \]

\[ Ae^{j\omega t} + Be^{-j\omega t} \]
Nyquist Chart of Complex Transfer Function $G_2$

Gain characteristics $|G_2(j\omega)|$

But in general

$|G_2(j\omega_1)| = |G_2(j\omega_2)|$

But in general

$|G_2(j\sqrt{\omega_1\omega_2})| = |G_2(j\omega_1)| = |G_2(j\omega_2)|$
Our Idea for Flat Passband Gain Algorithm

Gain characteristics $|G_2(j\omega)|$

Nyquist chart of $G_2(j\omega) = X(\omega) + j Y(\omega)$

If we make $|G_2(j\omega_1)| = |G_2(j\omega_2)| = |G_2(j\sqrt{\omega_1\omega_2})|$, gain would be flat from $\omega_1$ to $\omega_2$. 
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  - Adaptive Signal Processing and ADC Calibration
  - Magic Square and DAC Design
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**ADC:** Analog-to-Digital Converter
**DAC:** Digital-to-Analog Converter
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ADC: Analog-to-Digital Converter
DAC: Digital-to-Analog Converter
SAR ADC Configuration

Based on Principle of Balance

Generally use binary weights

(1, 2, 4, 8, 16, 32, 64, ...)

Object

Balance Scale

Sample Hold

Comparator

Digital Output

SAR Logic

DAC

CLK

Clock

Analog Input

Weight

Based on Principle of Balance
**Binary Search SAR ADC Operation**

**5bit-5step SAR ADC**
- Binary weight
  \[ p(k) = 16, 8, 4, 2, 1 \]
- Analog input 7.3

One-to-one mapping between decimal and binary codes

**\[ D_{out} = (00111)_2 \]**

7 = 16 - 8 - 4 + 2 + 1 + 0.5 - 0.5
5bit-6step SAR ADC

- Redundant weight $p(k) = 16, 10, 6, 3, 2, 1$
- Analog input 6.3

Increase number of comparison steps

$6 \Rightarrow 010001 \Rightarrow 6$

$16 - 10 + 6 - 3 - 2 - 1 + 0.5 - 0.5 = 6$
**Fibonacci Sequence**

**Definition** \((n=0,1,2,3...)**

\[
F_0 = 0 \\
F_1 = 1 \\
F_{n+2} = F_n + F_{n+1}
\]

Example of numbers (Fibonacci number)

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89...

**Property**

The closest terms ratio converges to **“Golden Ratio”**!

\[
\lim_{{n \to \infty}} \frac{F_n}{F_{n-1}} = 1.618033988749895 = \varphi
\]
We select $N$ bit and $M$ step SAR ADC $k$-th step reference voltage $p(k)$. Here $p(1) = 2^{N-1}$

**Proposed solution**

Using Fibonacci sequence for $p(k)$: $p(k) = F_{M-k+1}$

<table>
<thead>
<tr>
<th>Binary Weight</th>
<th>64</th>
<th>32</th>
<th>16</th>
<th>8</th>
<th>4</th>
<th>2</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radix 1.8 Weight</td>
<td>34.0</td>
<td>18.9</td>
<td>10.5</td>
<td>5.8</td>
<td>3.2</td>
<td>1.8</td>
<td>1</td>
</tr>
<tr>
<td>Fibonacci Weight (Radix 1.62 Weight)</td>
<td>13</td>
<td>8</td>
<td>5</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Property converging to Golden Ratio**

Realize **Radix 1.62 Weight** by using **only integer**!
Internal DAC Settling Time

DAC Settling model by a simple first-order RC circuit

$$V_{DAC}(t) = V_{ref}(k) + \{V_{ref}(k-1) - V_{ref}(k)\}e^{-\frac{t}{\tau}}$$

Settling time (binary)

Settling time (redundancy)

Error range to get correct output

Correctable difference

$$\tau = RC$$
SAR ADC Speed and DAC Settling

Redundancy → Incomplete settling

5bit SAR ADC

Binary search (complete settling)

<table>
<thead>
<tr>
<th>Step1</th>
<th>Step2</th>
<th>Step3</th>
<th>Step4</th>
<th>Step5</th>
</tr>
</thead>
</table>

Redundant search (incomplete settling)

<table>
<thead>
<tr>
<th>Step1</th>
<th>Step2</th>
<th>Step3</th>
<th>Step4</th>
<th>Step5</th>
<th>Step6</th>
<th>Step7</th>
</tr>
</thead>
</table>

Error correction

Fibonacci search (incomplete settling)

<table>
<thead>
<tr>
<th>Step1</th>
<th>Step2</th>
<th>Step3</th>
<th>Step4</th>
<th>Step5</th>
<th>Step6</th>
<th>Step7</th>
</tr>
</thead>
</table>

Error correction

The shortest AD conversion time!!
We have found the following:

- **Reliable**
  Comparator decision errors can be recovered with redundancy.

- **Fastest SAR AD Conversion**
  In case the internal DAC incomplete settling is considered.


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**ADC**: Analog-to-Digital Converter
**DAC**: Digital-to-Analog Converter
Power Consumption of Pipelined ADC

- First stage amplifier : Consumes considerable power

- First stage amplifier : Open-loop
- Low power consumption
- Nonlinearity of open-loop amplifier : background self-calibration
Split ADC Structure

- Each channel ADC: half gm, half capacitor different residue logic converge quickly
- Power consumption: small overhead
- Chip area: small overhead

Complicated Adaptive Signal Processing for Calibration

\[ g_{al}(V_{a1}) = \alpha_1 \cdot V_{a1} + \alpha_3 \cdot V_{a1}^3 \]

- Adding pseudo randomly
  → Generate two residue waveforms
- RNG(A & B) : Set default value to different

\[ \text{RNG} = 1 \Rightarrow \frac{V_{ref}}{16} \]
\[ \text{RNG} = 0 \Rightarrow 0 \]

\[ \text{RNG}_A \]
\[ \text{RNG}_B \]
\[ \text{ADC}_A \]
\[ \text{ADC}_B \]
\[ \text{MSB}_A \]
\[ \text{MSB}_B \]
\[ \text{LSB}_A \]
\[ \text{LSB}_B \]

V_i → V_{rA} → Backend → ADC_A → MSB_A → LSB_A → ...

V_i → V_{rB} → Backend → ADC_B → MSB_B → LSB_B → ...

RNG : Random Number Generator

\[ \text{RNG} = 1 \Rightarrow \frac{V_{ref}}{16} \]
\[ \text{RNG} = 0 \Rightarrow 0 \]
Validate the Effectiveness with MATLAB

**ADC_A (Stage1_A)**
- C mismatch: 2% (σ)
- Nonlinearity of amplifier:
  \[ g_{al}(V_{al}) = 7.5 \cdot V_{al} + (-15) \cdot V_{al}^3 \]

**ADC_B (Stage1_B)**
- C mismatch: 2% (σ)
- Nonlinearity of amplifier:
  \[ g_{bl}(V_{bl}) = 7.6 \cdot V_{bl} + (-15.2) \cdot V_{bl}^3 \]

- Nonlinearity correction
  - LMS loop:
    \[ \mu_A = 1/8192 \]
  - IIR filter gain:
    \[ \mu_{3a} = 1/512 \]

- Gain error, C mismatch correction
  - IIR filter gain:
    \[ \mu_{1a} = 1/1024 \]
DNL and INL of the ADC output

No calibration

- Maximum DNL = +0.18/−0.96 LSB
- Maximum INL = +7.2/−4.5 LSB

Gain error and capacitor mismatch calibration

- Maximum DNL = +0.5/−0.93 LSB
- Maximum INL = +1.8/−0.94 LSB

Nonlinearity, Gain error and capacitor mismatch calibration

- Maximum DNL = +0.21/−0.27 LSB
- Maximum INL = +0.16/−0.12 LSB

• Calibrate all error: DNL, INL are within ±0.5 LSB
Output Power Spectrum

- Calibrate all error: SNDR = 73.9 dB
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**ADC:** Analog-to-Digital Converter
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What is Magic Square (魔方陣)?

- Classical mathematics
- Origin from Chinese academia
- “Constant sum” characteristics
- Varieties of magic squares

<table>
<thead>
<tr>
<th>59</th>
<th>5</th>
<th>4</th>
<th>62</th>
<th>63</th>
<th>1</th>
<th>8</th>
<th>58</th>
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<tr>
<td>7</td>
<td>60</td>
<td>61</td>
<td>3</td>
<td>2</td>
<td>64</td>
<td>57</td>
<td>6</td>
</tr>
</tbody>
</table>

3x3 魔方陣

![Magic Square Diagram](image-url)
Unary DAC and Mismatch Problem

In practice, current sources have mismatches. DAC becomes non-linear.
Possibility of Using Magic Square (魔方陣)

- Semiconductor devices have random and systematic mismatches
- Changing the switching order with magic square → Cancellation of mismatch effects

Error vs. Din graph showing normal algorithm vs. magic square algorithm.

![Magic Square](image)

Inspired New Algorithm

Unit current source selection-order change algorithm

1. Measure the order of unit current cells
2. Align them virtually in magic square
3. Select current cells
MATLAB Simulation Result

Integral Non-Linearity (INL)

- 5.7 LSB improvement by the magic square algorithm

\[ \text{INL}_{\text{magic square}} = 1.95 \text{ LSB} \]
\[ \text{INL}_{\text{conventional}} = 7.63 \text{ LSB} \]
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  - Gray Code and TDC Design
  - ΔΣ Modulation and TDC
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**TDC:** Time-to-Digital Converter
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**TDC**: Time-to-Digital Converter
Time to Digital Converter (TDC)

- time interval → Measurement → Digital value

Start → T → Stop

- Key component of time-domain analog circuit
- Higher resolution can be obtained with scaled CMOS

Higher resolution with CMOS scaling

LSB [ps]

Year

Flash-type TDC

Timing chart:
- Start
- D0 = 1
- D1 = 1
- D2 = 1
- D3 = 0
- D4 = 0
- Stop

Thermometer code

Binary code

Encoder

Dout
Delay Cell Variation Inside TDC Circuit

Delay cell variation $\Delta \tau_k$

Without delay variation (a)

With delay variation (b)

TDC nonlinearity

(a) Without delay variation

(b) With delay variation
Measurement with Histogram

# of dots ratio $\frac{N_1}{N_2} \quad \rightarrow \quad$ Area ratio $\frac{S_1}{S_2}$
TDC is non-linear due to delay variation

\[ t + \Delta t_1 \quad t + \Delta t_2 \quad t + \Delta t_3 \quad t + \Delta t_4 \]


Principle of Self-Calibration

1. Histogram
2. \( n \)
   \[ TDC \text{ digital output} \]
   \[ \text{Histogram of ideally} \]
   \[ \text{Linear TDC} \]
   \[ \text{INL calculation} \]

3. Linearized by inverse function
   \[ Dout = f(T) \]
   \[ T \]
   \[ \text{Histogram} \]

4. \( TDC \text{ digital output} \)
Measurement Results (INL)

Sample #1

Sample #2

Sample #3

Sample #4
Contents

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**TDC**: Time-to-Digital Converter
Concept of Gray code

Gray code is a binary numeral system where two successive values differ in only one bit.

### 4-bit Gray code vs. 4-bit Natural Binary Code

<table>
<thead>
<tr>
<th>Decimal numbers</th>
<th>Natural Binary Code</th>
<th>4-bit Gray Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>1</td>
<td>0001</td>
<td>0001</td>
</tr>
<tr>
<td>2</td>
<td>0010</td>
<td>0011</td>
</tr>
<tr>
<td>3</td>
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<td>1110</td>
<td>1001</td>
</tr>
<tr>
<td>15</td>
<td>1111</td>
<td>1000</td>
</tr>
</tbody>
</table>

Gray code was invented by Frank Gray at Bell Lab in 1947.
How to utilize Gray code in TDC

In a ring oscillator, between any two adjacent states, only one output changes at a time.

For any given Gray code, each bit can be generated by a certain ring oscillator.

<table>
<thead>
<tr>
<th>8-stage Ring Oscillator Output</th>
<th>4-bit Gray Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>R1</td>
</tr>
<tr>
<td>----</td>
<td>----</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>1</td>
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</tbody>
</table>
Proposed 4-bit Gray code TDC

A large Flash TDC

A set of smaller Flash TDCs performed in parallel

Proposed Gray code TDC architecture in 4-bit case
FPGA measurement results of 8-bit Gray code TDC

Gray code TDC works with good linearity as expected

## Flash TDC vs. Gray code TDC

<table>
<thead>
<tr>
<th></th>
<th>Number of delay cells</th>
<th>Number of DFFs</th>
<th>Maximum stage of RO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gray code TDC</td>
<td>$2^n - 2$</td>
<td>$n$</td>
<td>$2^{n-1}$</td>
</tr>
<tr>
<td>Flash-type TDC</td>
<td>$2^n$</td>
<td>$2^n$</td>
<td>$2^n$</td>
</tr>
</tbody>
</table>

For large measurement range, the number of flip-flops in Gray code TDC decreases rapidly ($n << 2^n$)

Reduction of circuit complexity!!
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**TDC:** Time-to-Digital Converter
ΔΣ TDC Features

Timing $T$ measurement between CLK1 and CLK2

ΔΣ Time-to-Digital Converter (TDC)

- Simple circuit
- High linearity
- Measurement time $\rightarrow$ longer $\Rightarrow$ time resolution $\rightarrow$ finer

$T \propto \#$ of 1’s at Dout
Principle of $\Delta \Sigma$TDC

CLK1 $\rightarrow$ $\Delta \Sigma$TDC delay: $\tau$ $\rightarrow$ Dout 0 or 1

CLK2 $\rightarrow$

Dout # of 1’s is proportional to $\Delta T$

$\Delta T$ # of 1’s

short few long many

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
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ΔΣTDC Configuration

Multi-bit ΔΣTDC

For short measurement time:

DWA: Data Weighted Averaging

DSP algorithm of compensation for mismatches among delays.
Measured Result

Analog FPGA Implementation

10,000 TDC output data are measured.
Contents

● Statement of This Paper
● Analog Circuit Design based on Mathematics
● ADC/DAC Design based on Mathematics
● TDC Design based on Mathematics
● Conclusion
Traditionally, people believe that analog / mixed-signal circuit design is art and craft.

Here we show that mathematics can contribute to the design as science.

Both art and science are used for good analog / mixed-signal circuit design.
思而不学則殆

Analog /mixed-signal IC designers should study mathematics for sophisticated design.
Abstract - This paper presents that techniques of mathematics, such as number theory, statistics, coding theory, modulation, control theory, and signal processing algorithms besides transistor-level circuit design are required to enhance the performance of analog/mixed-signal circuit performance. Several research examples in the authors’ laboratories are shown. Keywords: analog circuit, mixed-signal circuit, signal processing, number theory, coding theory, statistics

1. Introduction
Analog circuit design at the transistor level is art rather than technology, with which industry can differentiate their products. However, as the LSI technology advances, digital technology can be utilized and so called digitally-assisted analog/mixed-signal circuit technology becomes effective [1]. It uses mathematics such as signal processing and control theory extensively. This paper introduces such research results at the author’s laboratory and validates our argument that beautiful mathematics leads to very good circuit/system design.

2. Control Theory and Operational Amplifier Design
We propose to use Routh-Hurwitz stability criterion for analysis and design of the opamp feedback stability, after deriving its small equivalent circuit and transfer function; this can lead to explicit stability condition derivation for opamp circuit parameters, which would be effective when it is used together with Bode plots [2].

3. Fibonacci Sequence and SAR ADC Design
We have investigated a redundant successive approximation register (SAR) ADC design method for high-reliability and high-speed AD conversion using digital error correction [3, 4]. We apply Fibonacci sequence $F_n$ and its property of convergence to the Golden ratio $\varphi$ there.

$$F_{n+2} = F_n + F_{n+1}, \quad F_0 = 0, \quad F_1 = 1$$

$$F_n = 0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, \ldots$$

$$\lim_{n\to\infty} \frac{F_{n+1}}{F_n} = 1.6180339887 = \varphi$$

We have found that the SAR AD conversion time becomes the shortest when Fibonacci sequence weights are used and the internal DAC incomplete setting is considered. We have come up with simple golden-ratio weighted DAC topologies (R-R ladder, C-C ladder) for its internal usage.

4. Adaptive Signal Processing and ADC Calibration
We investigate a background calibration algorithm for a pipelined ADC with an open-loop amplifier using a split ADC structure and adaptive signal processing [5, 6]. The open-loop amplifier is employed as a residue amplifier in the first stage of the pipelined ADC for low power and high speed. However it suffers from nonlinearity, and hence needs calibration. We investigate the split ADC structure for fast background calibration of the residue amplifier nonlinearity and gain error as well as the DAC nonlinearity all together with fast convergence.

5. Correlation and ADC Timing Correction
We investigate a digital method of reducing timing
mismatch effects in time-interleaved ADCs (Fig.1(a)) used in ATE systems [7]: we use correlation (Fig.1(b)) among channel ADC outputs to detect channel timing skew, and make successive approximation (SA) adjustments to our linear-phase digital delay filter [8] to compensate for the timing skew. Simulation results validate the effectiveness of the proposed method. We found that using multi-tone input signals with correlation of outputs provided a more robust way of detecting timing skew than using a single-tone input.

Fig. 3 (a) Interleaved ADC. (b) Auto-correlation (right).

Fig.4 Successive approximation minimization of timing skew using our delay digital filter.

6. Magic Square and DAC Design

We propose a switching or current source sorting algorithm using magic square properties (Fig. 5 (a)) to improve the linearity of a unary digital-to-analog converter (DAC) (Fig. 5 (b)) by canceling random and systematic mismatch effects among unit current cells [8]. Simulation results show DAC linearity improvement with the proposed algorithm.

![Magic Square](image)

(a) Magic square and constant sum characteristics. (b) Unary current-steering DAC.

7. Residue Arithmetic, Gray Code and TDC Design

A time-to-digital converter (TDC) measures the rising edge timing difference between Start and Stop signals and provides digital output. Fig. 6 shows a basic flash-type TDC, however it requires large hardware and power. We investigate a TDC architecture with residue arithmetic or Chinese Remainder theorem [10], because its residues can be obtained easily with ring oscillators. It can reduce hardware and power significantly compared to a basic flash-type TDC while keeping comparable performance.

However, the residue arithmetic TDC can cause some glitches due to the delay mismatches. Then we came up with its improvement, a glitch-free TDC based on Gray code [11] (Table I, Fig. 7). Gray-code (reflected binary code) is a binary numeral system where two successive values differ in only one bit. So a Gray-code driven DAC is capable to reduce the glitch. The proof-of-concept prototype of Gray code based TDC was implemented on FPGA.

![TDC Architecture](image)

Fig. 6. Basic flash-type TDC

Table I Binary and Gray codes

<table>
<thead>
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<th>Binary Code</th>
<th>Gray Code</th>
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</table>

![Gray Code TDC Architecture](image)

Fig. 7 6-bit Gray code based TDC architecture

We have also designed Gray code input DAC topologies (current, voltage and charge modes) for glitch reduction.

8. Histogram and TDC Linearity Calibration

We have studied the flash-type TDC linearity self-calibration, with histogram obtained by uncorrelated ring oscillators (Fig. 8) [12]. FPGA measurement results show that TDC linearity is improved by the self-calibration [13] (Fig. 9). All TDC circuits, as well as the self-calibration circuits can be implemented as digital FPGA instead of full custom ICs,
which is suitable for fine CMOS implementation with short design time.

(a) Histogram data acquisition
(b) Delay variation and histogram data
(c) TDC linearity correction with digital calculation

Fig. 8 TDC linearity calibration principle.

Fig. 9 Measured results of TDC nonlinearity before and after the proposed calibration.

9. Statistics and Fine Time-Resolution TDC Design
We have investigated another TDC architecture to measure the timing difference between single-event two pulses with fine time resolution [12, 14]. Its features are as follows: (i) The architecture is based on stochastic process and statistics theory. (ii) It utilizes the stochastic variation in CMOS process positively for fine time resolution so that MOSFETs with minimum sizes are utilized. (iii) It needs a large number of D Flip-Flops (DFFs) for statistics but advanced fine CMOS technology can realize it. The larger the number of DFFs is, the finer the time resolution is. (iv) The self-calibration technique using the histogram method is applied to compensate the nonlinearity due to the circuit characteristics variation as well as timing skew by layout and routing. (v) The proposed TDC can be implemented with full digital circuit including the self-calibration circuit.

(b) Delay variation and histogram data

Fig. 10 Investigated stochastic TDC architecture

10. ΔΣ Modulation, DWA and TDC
We investigate design and implementation of a multi-bit ΔΣ TDC with Data Weighted Averaging (DWA) algorithm on analog FPGA [15] (Figs. 11, 12). We propose here simple test circuitry for measuring digital signal timing of I/O interfacing circuits. We focus on ΔΣ TDC for fine timing-resolution, digital output, and simple circuitry. The ΔΣ TDC can measure the repetitive signal timing; as the measurement time is longer, its time resolution becomes finer. We also use multi-bit architecture for short testing time. However, the multi-bit ΔΣ TDC suffers from delay mismatches among delay cells. Then we apply the DWA algorithm, which averages the mismatches in time and obtain good linearity.

Fig. 11 Multi-bit ΔΣ TDC with DWA logic

(a) DWA operation
11. Complex Signal Processing and Analog Filter

We derive a design algorithm of a 2nd-order RC polyphase filter (which has complex or quadrature analog inputs and outputs) to obtain its flat passband gain, using its Nyquist chart [16]. The condition for its solution as well as the image rejection ratio formula are also derived. We also clarify that the RC polyphase filter has characteristics as a complex analog Hilbert filter.

![2nd order RC polyphase filter](image)

(a) 2nd order RC polyphase filter

(b) Gain characteristics, before and after the algorithm. Fig. 12 2nd-order RC polyphaser filter and gain characteristics before and after the proposed algorithm

We have also developed complex or quadrature bandpass DWA algorithms [17]; concept of complex signal processing is useful especially communication circuits.

12. Concluding Remarks

This paper has presented that techniques of mathematics besides transistor-level circuit design are attractive to enhance the performance of analog/mixed-signal circuit performance in nano CMOS. It is the authors’ experience that beautiful structure / topology of circuits and systems based on mathematics leads to very good performance.

The authors thank their lab members for contributions.

REFERENCES