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Limit Cycle Suppression Technique Using Digital Dither in Delta Sigma DA Modulator

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Research Objective

Objective

- **Development of high linear & high resolution ΔΣ DAC**

Our Approach

- **Limit cycle suppression using digital dither**

Outline

- Research Background
- Proposed Circuit
- Simulation Configuration & Results
- FPGA Implementation
- Conclusion

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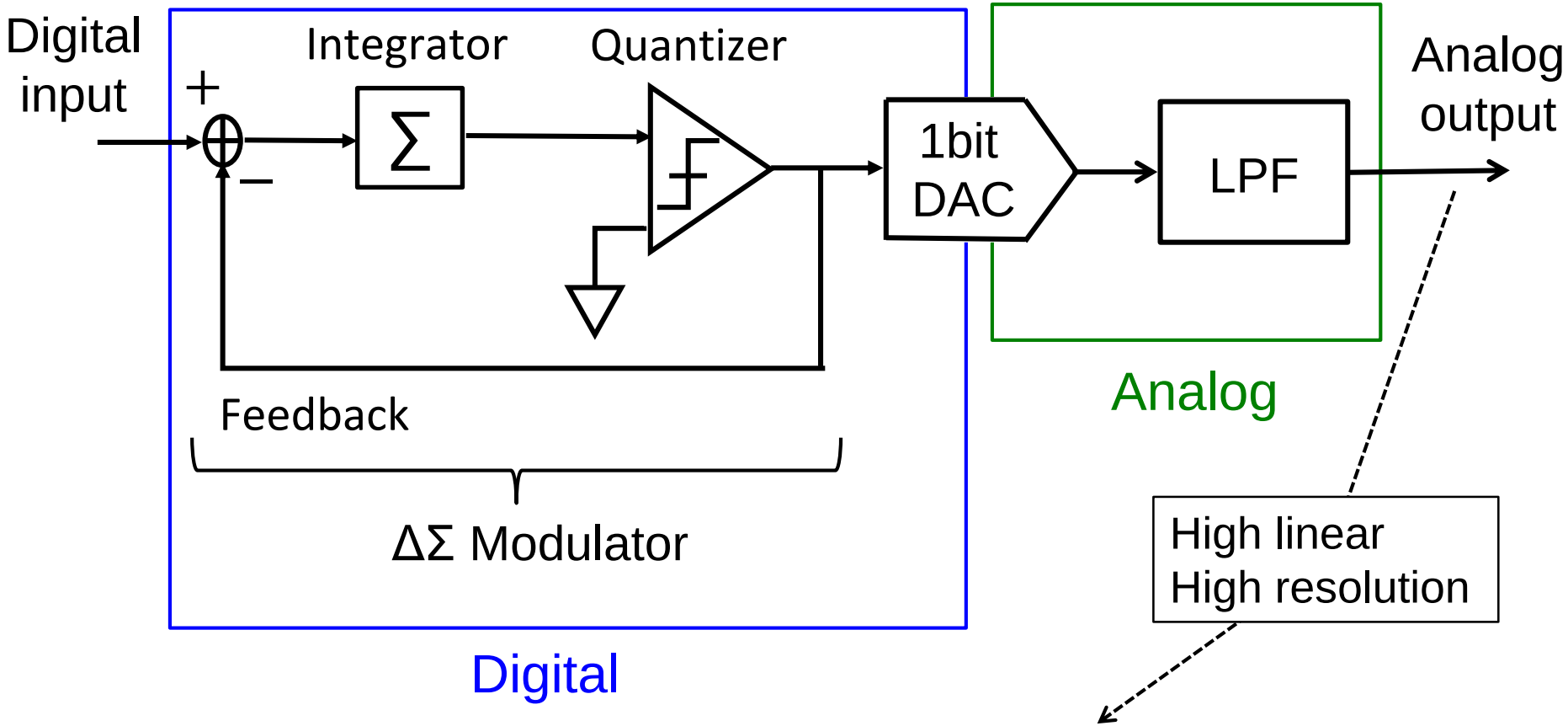
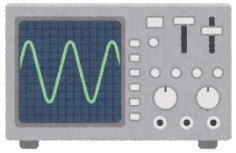
ΔΣ DA Converter



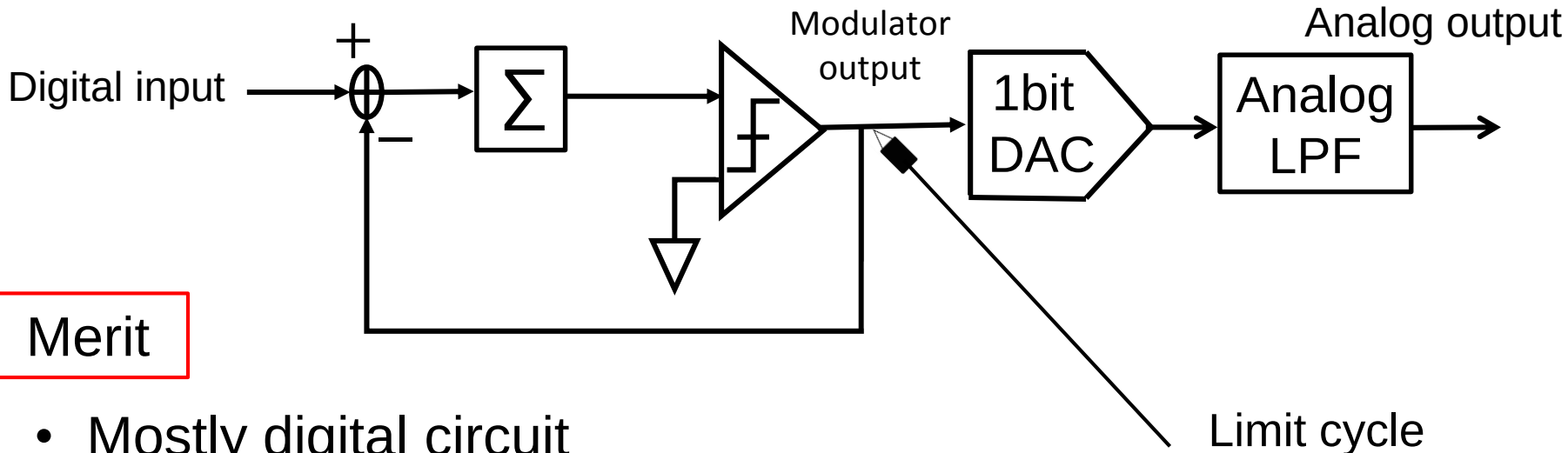
High linear
High resolution

＜Usage＞

- Measurement
- Audio



Merits & Demerits of ΔΣ DAC



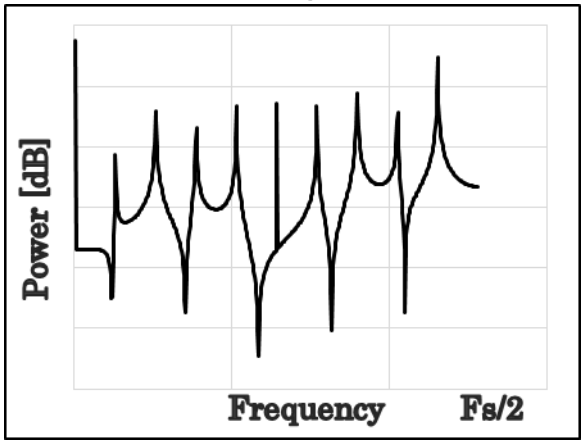
Merit

- Mostly digital circuit
- High linear & high resolution
  for low frequency signal generation

Demerit

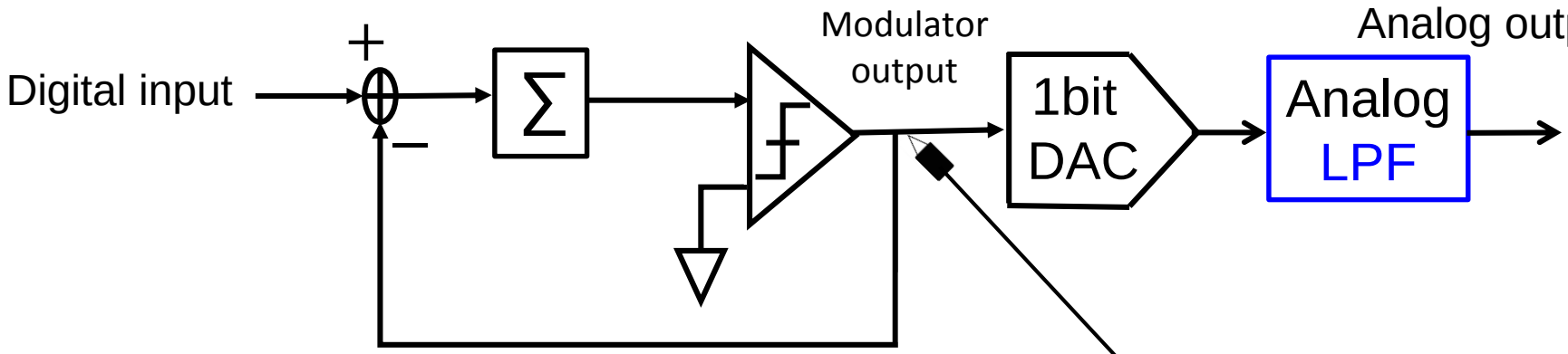
- Limit cycle problem for small input

Limit cycle



※ Due to modulator nonlinearity by quantizer

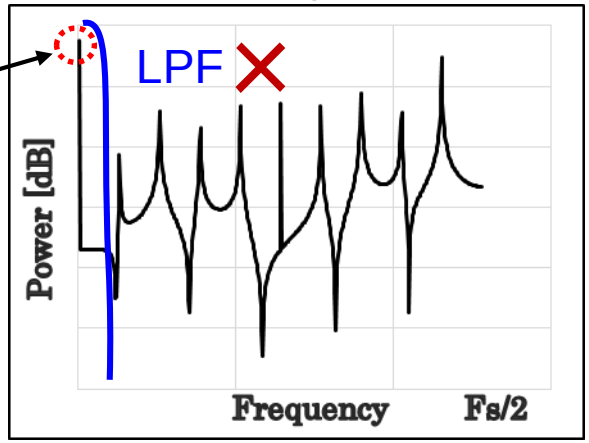
Limit Cycle Problem



Removal of analog signal by LPF sharply

⇒ difficult

Limit cycle

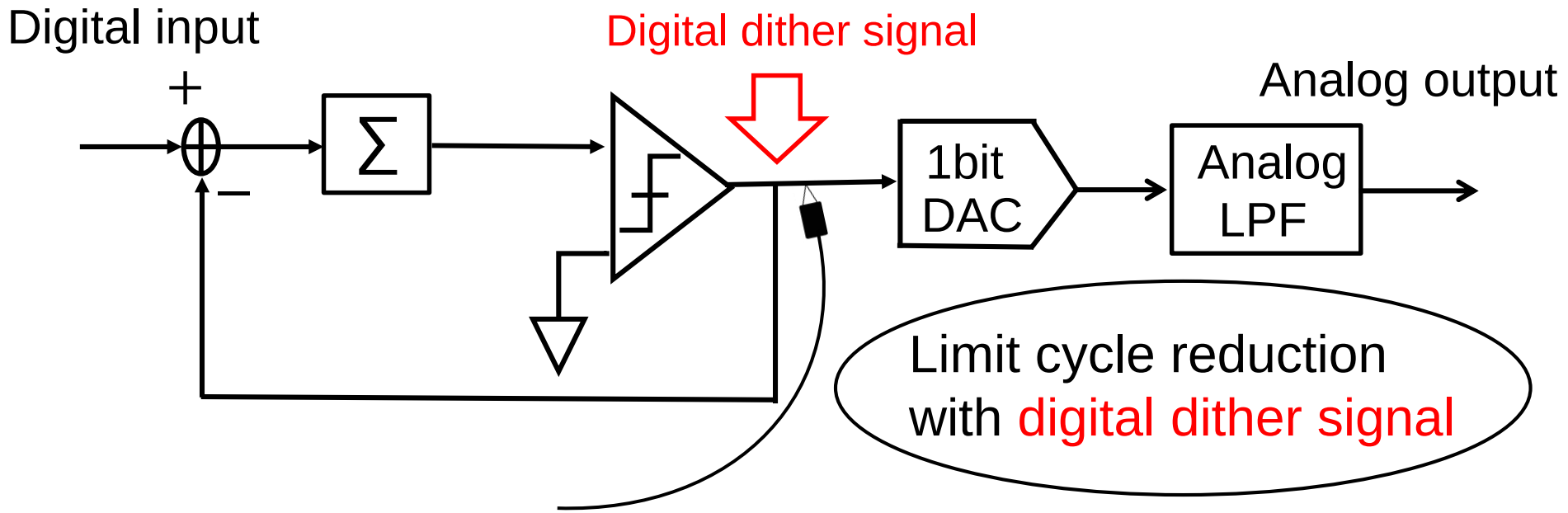


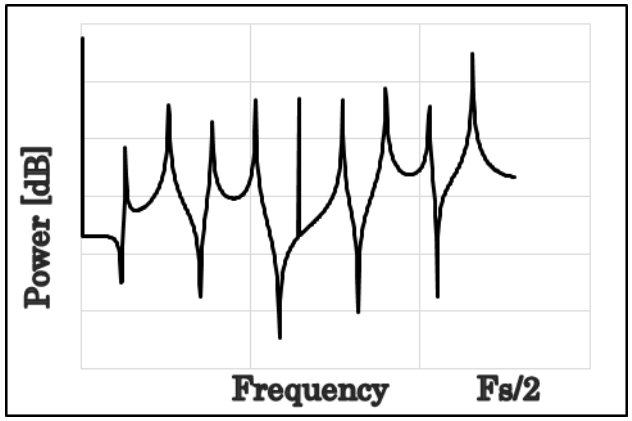
Analog output = Signal + Limit cycle

(Noise)

Objective
- Limit cycle suppression
- Relax LPF requirement

Our Approach





Limit cycle

Stair

Smoothness !

Outline

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- **Proposed Circuit**
- Simulation Configuration & Results
- FPGA Implementation
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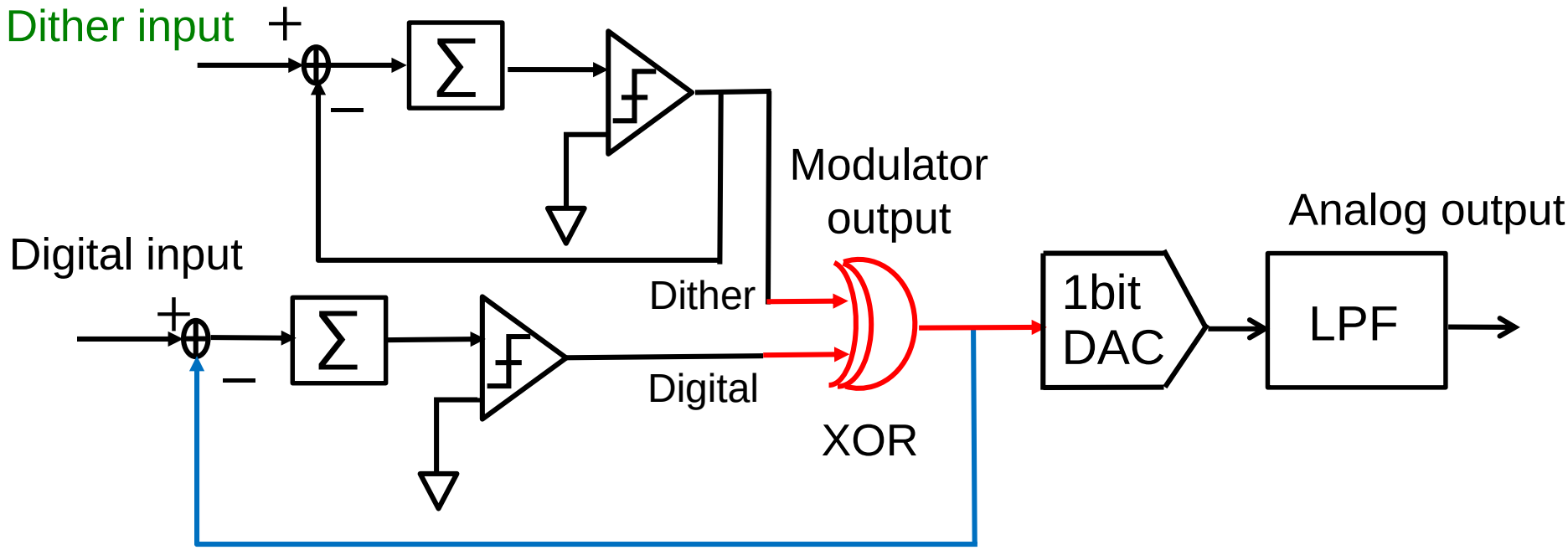
Proposed Circuit



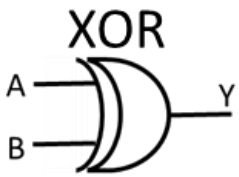
< Features >

① 1-bit output

② Digital dither

⇒ NOT affect output signal, thanks to feedback

③ Easily generated digital dither



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Digital signal “1” reverses comparator output with XOR

Outline

- Research Background
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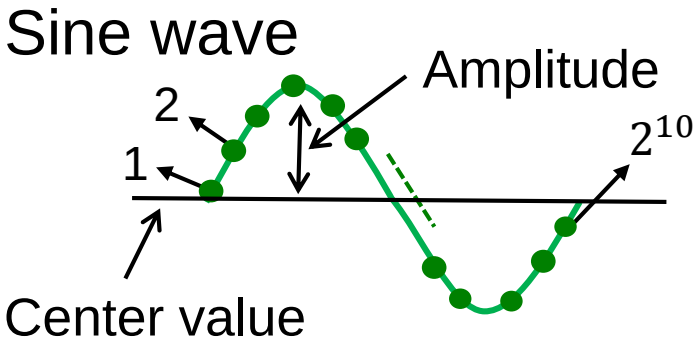
- **Simulation Configuration & Results**
- FPGA Implementation
- Conclusion

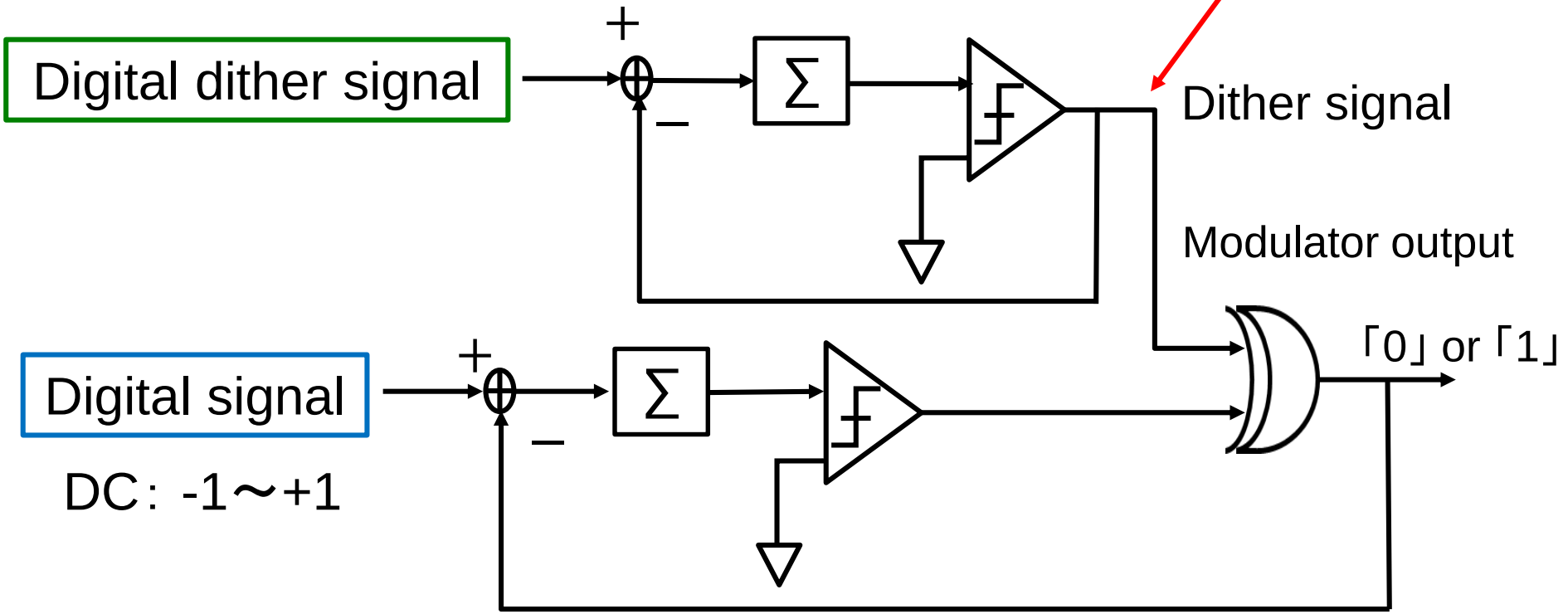
Simulation Configuration

◆ In 10-bit case



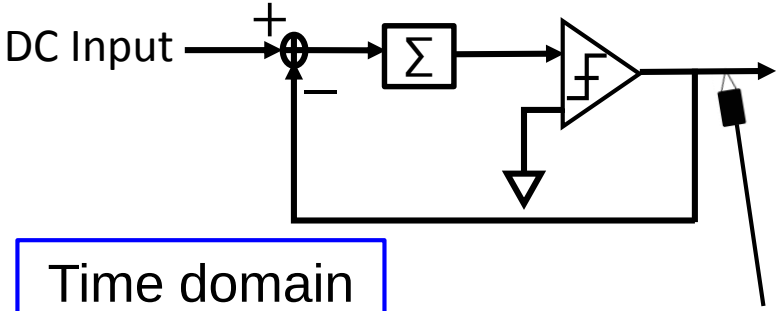
Amplitude and center value

➡ Controlled by number of 1's



Modulator Operation

- Without dither

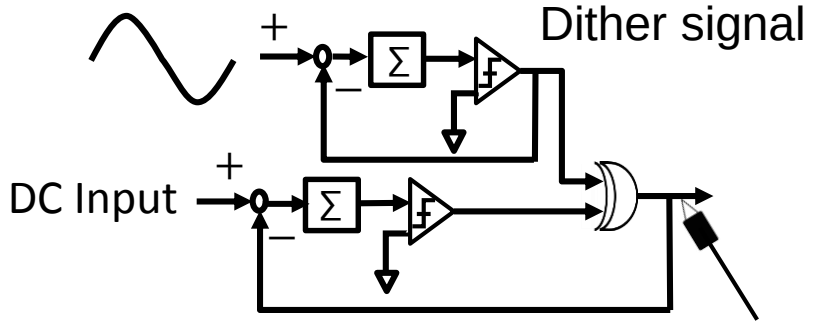


Time domain

1 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0

Period

- With dither



1 0 0 0 0 1 0 1 0 0 0 0 0 1 0 0

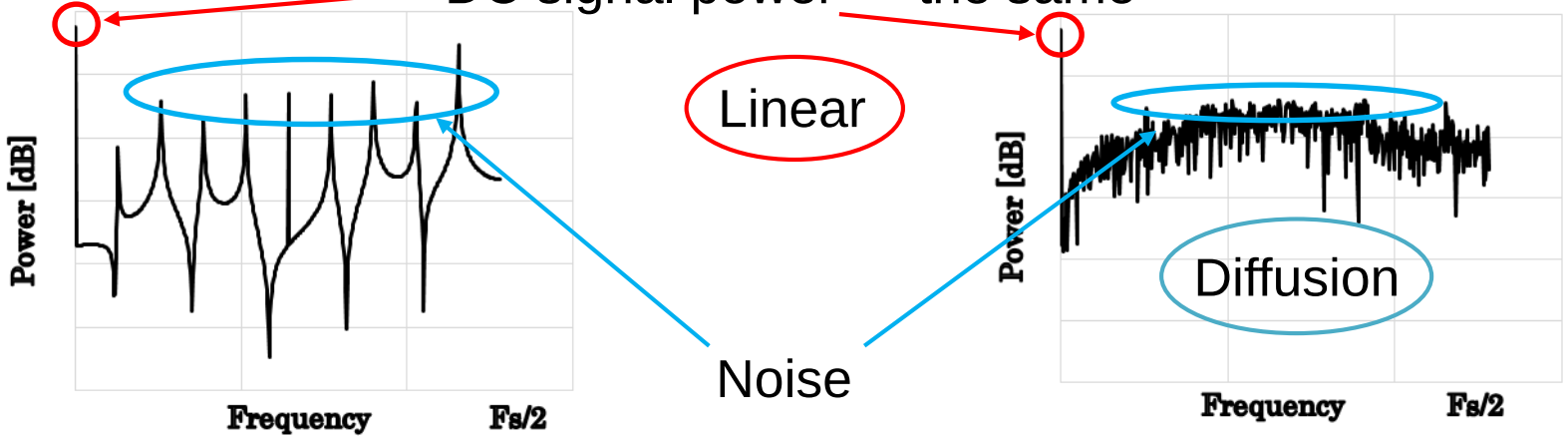
Not Periodic

✓ Orders of ‘0’ and ‘1’ ⇒ different

✓ Total numbers of 1’s ⇒ the same

Frequency domain

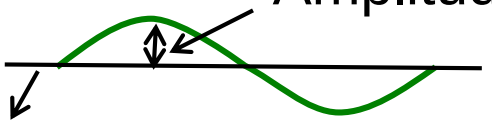
DC signal power ⇒ the same



10-bit case

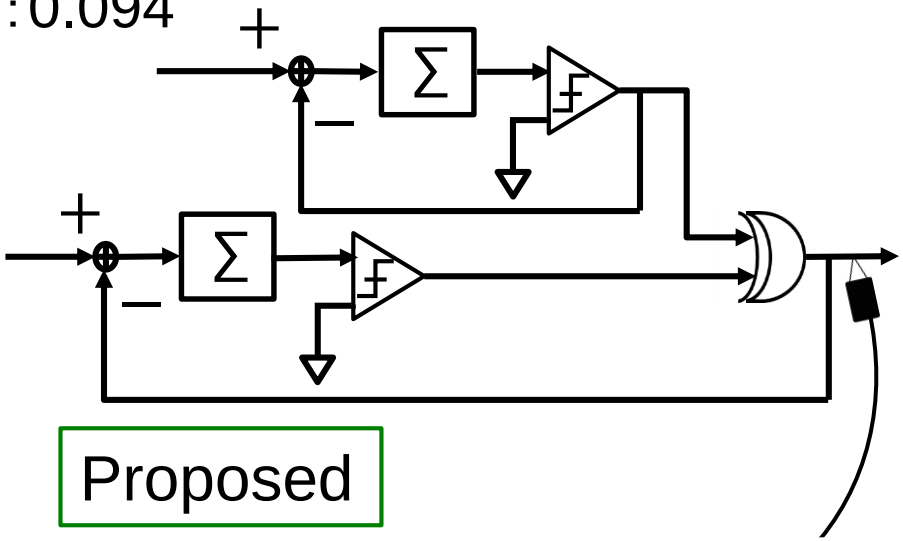
Simulation Results

Sine wave

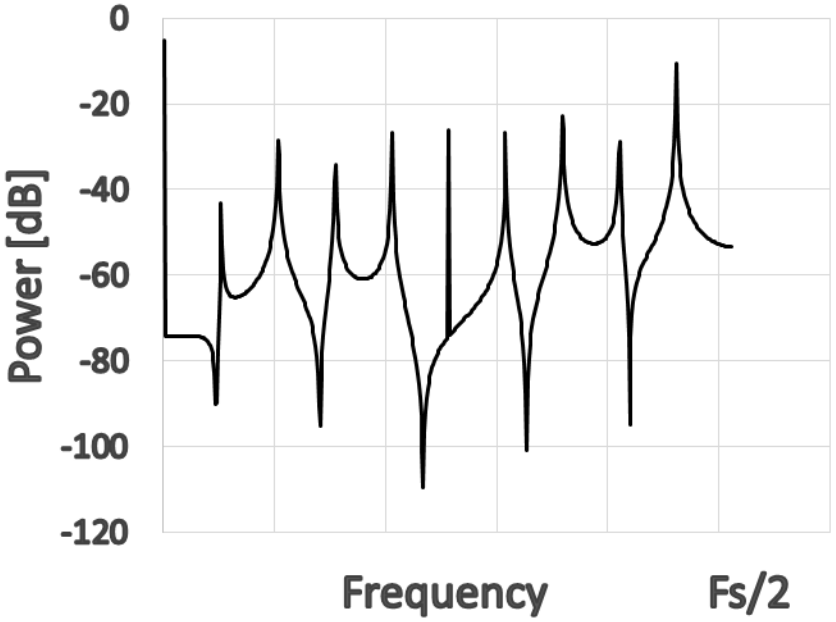


Center value : -0.520

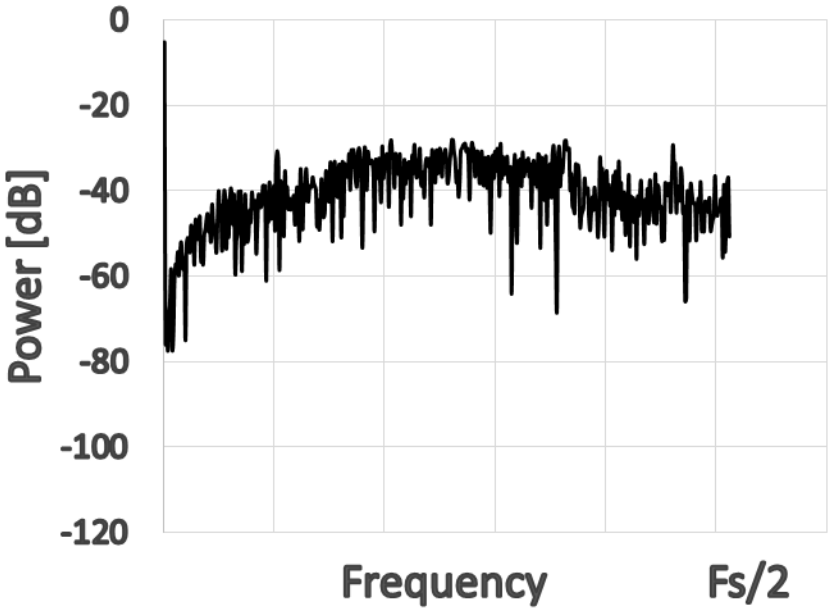
DC = 0.1



Conventional



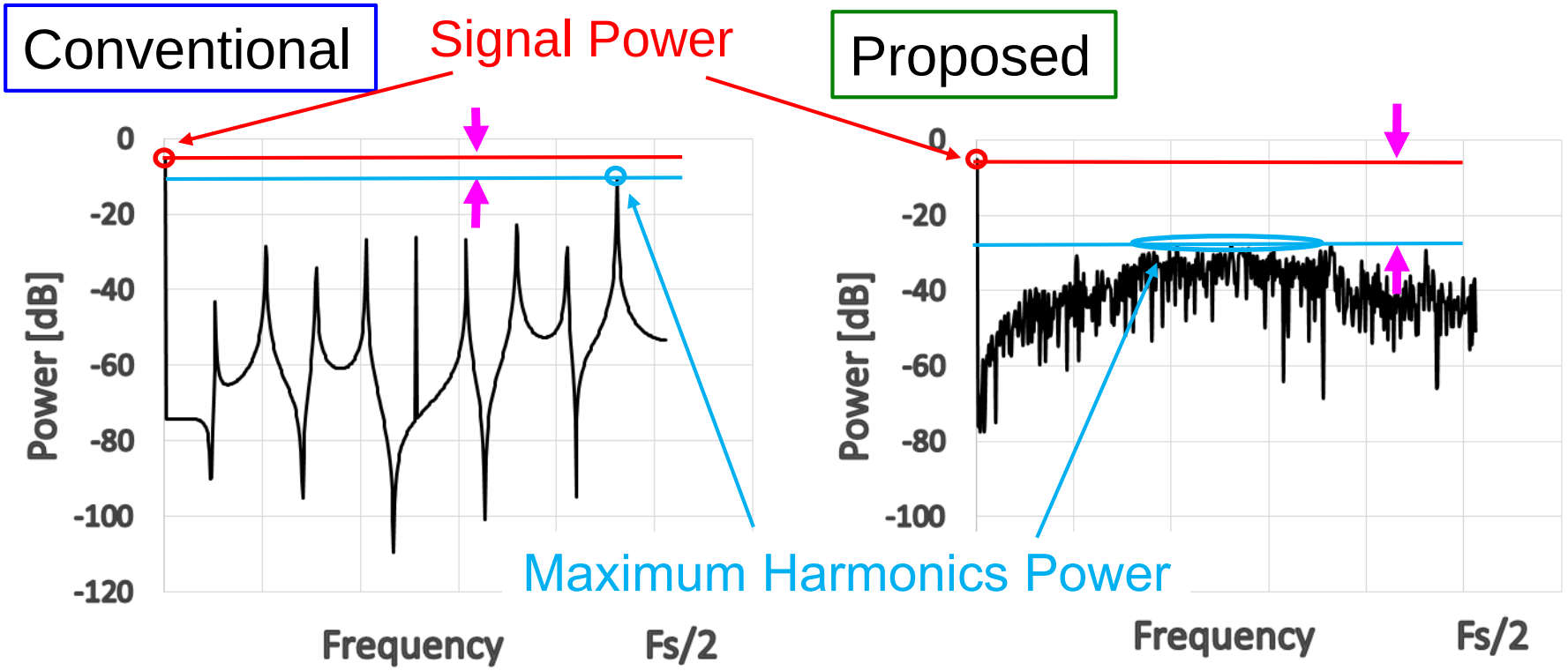
Proposed



SFDR (Spurious Free Dynamic Range)

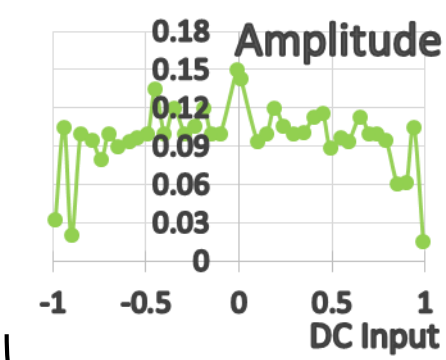
$$\mathrm{SFDR} = \frac{\text{Signal Power}}{\text{Maximum Harmonics Power}}$$

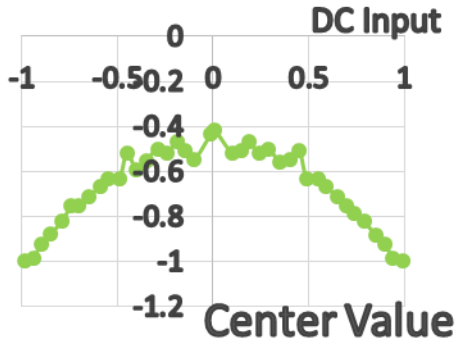
SFDR = 5.4 dB ＜ 22.9 dB

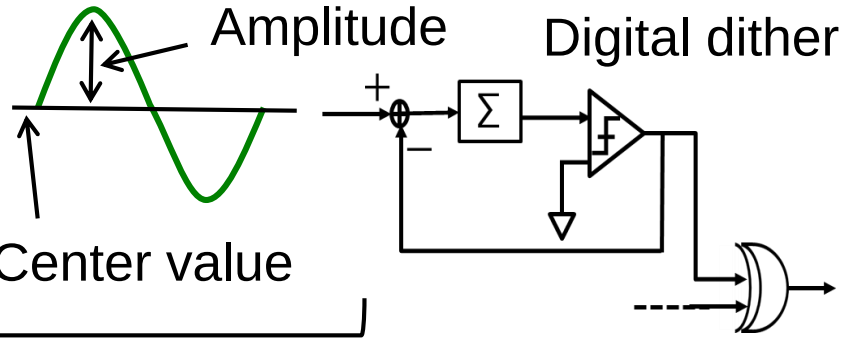


10-bit case

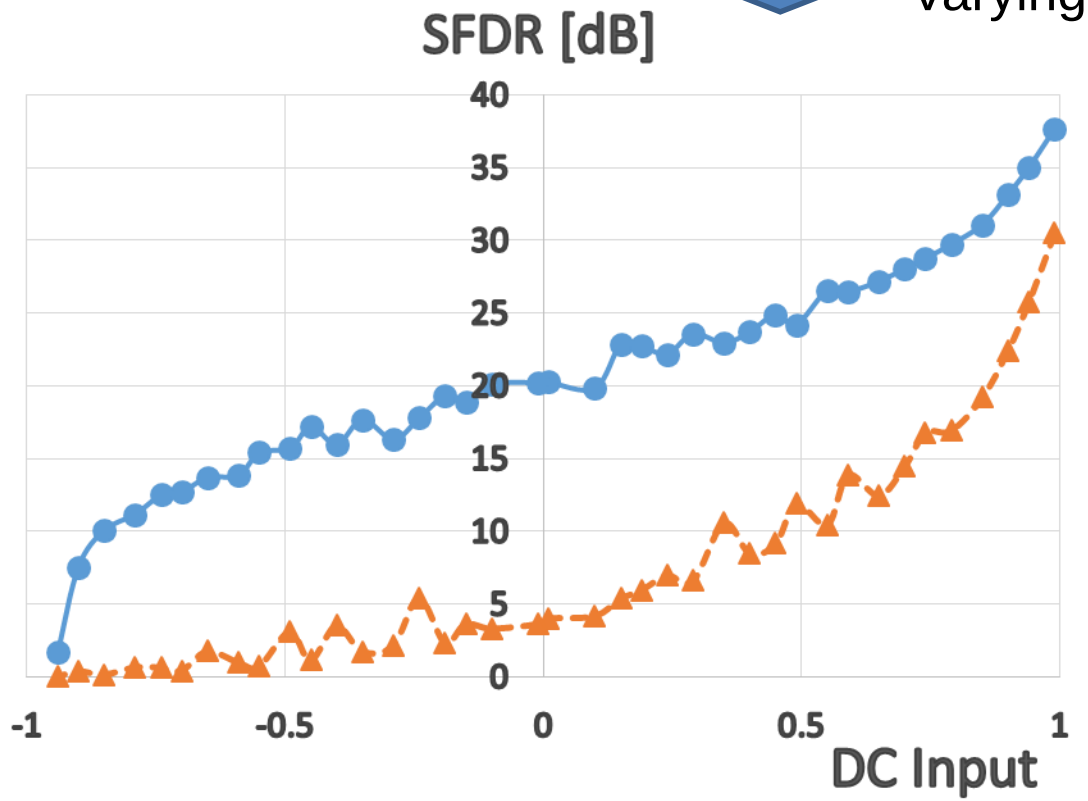
SFDR Comparison







Varying DC input



With dither
Without dither

SFDR improvement
by more than 10dB

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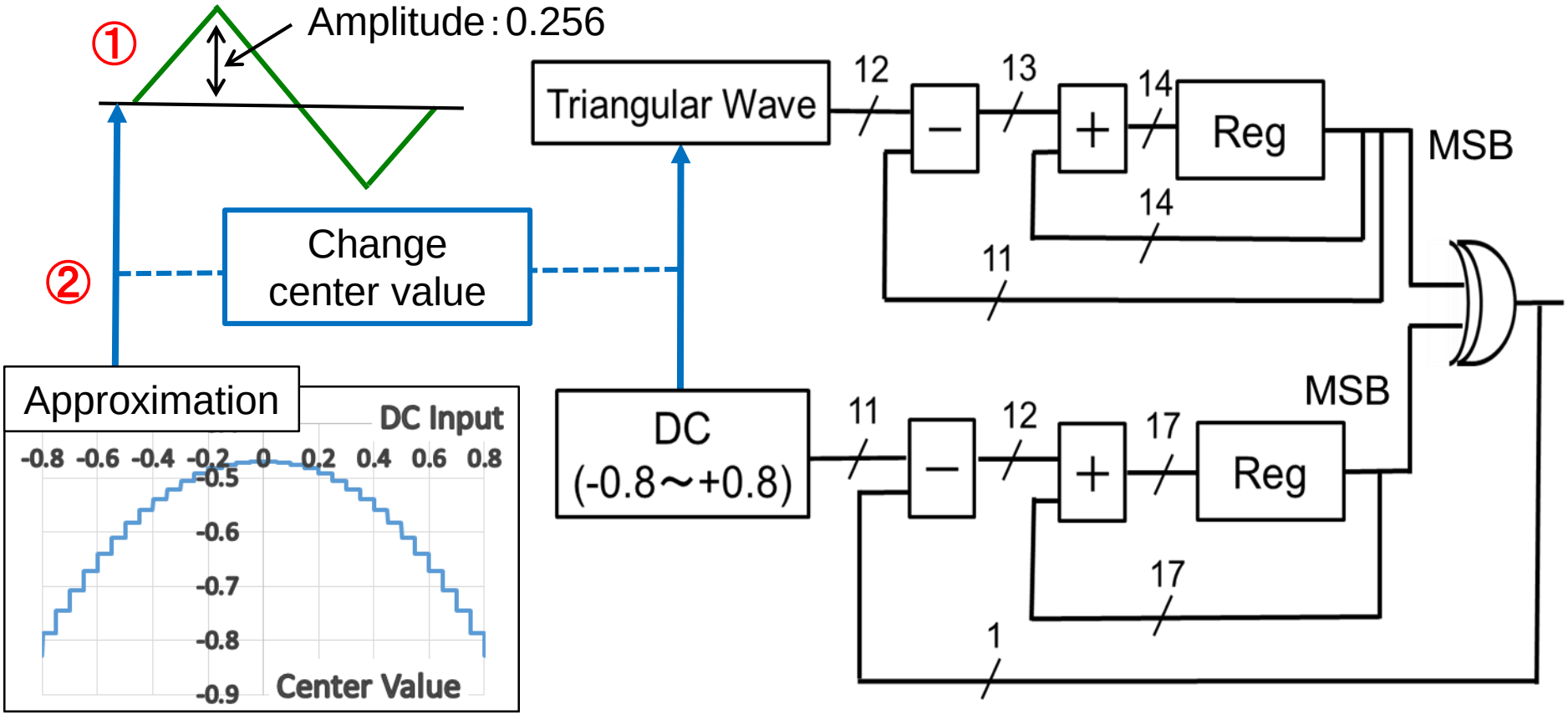
Design Modification for FPGA Implementation

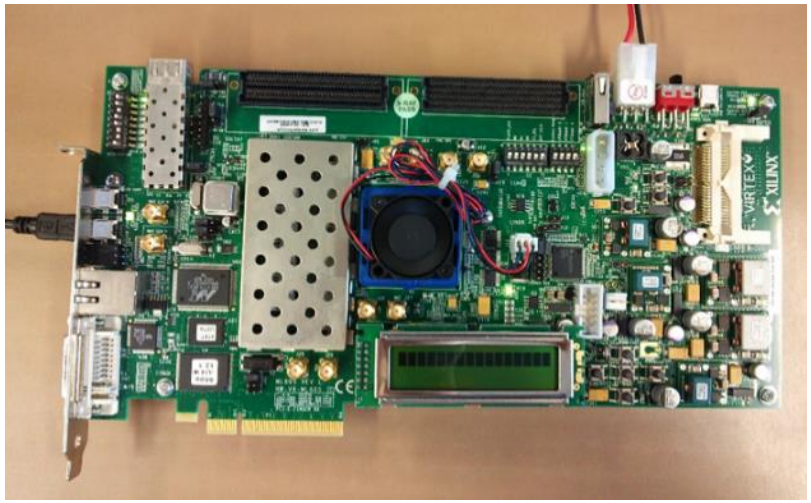
Complication

① Digital sine wave
⇒ Triangular wave

② Change amplitude and center value
⇒ Use approximation



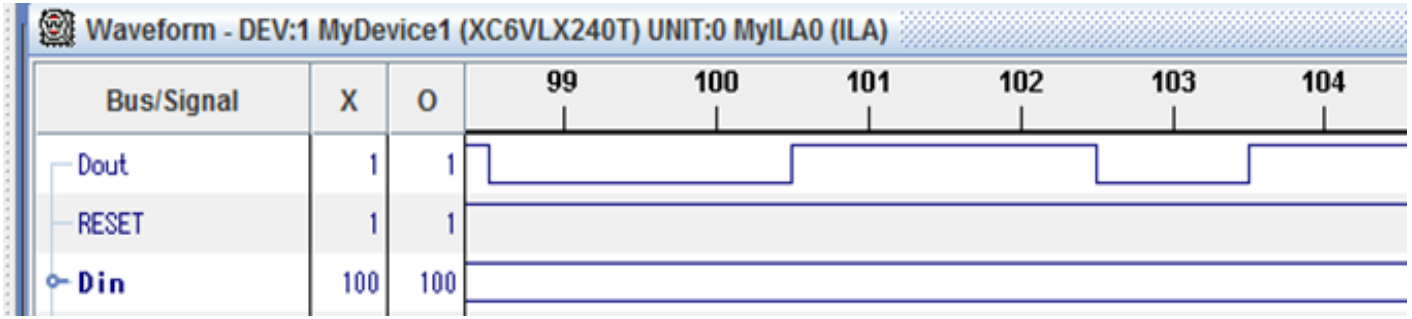
FPGA Board & Output Signal Waveforms



Xilinx
Virtex-6 ML605

FPGA Board

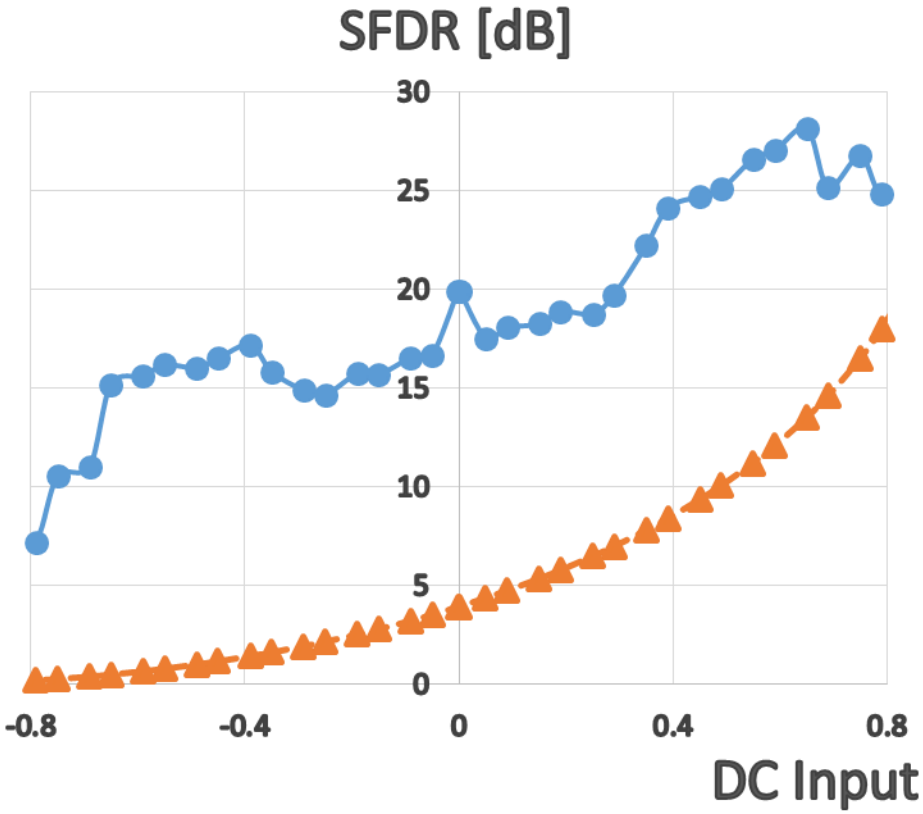
(Clock Freq. 50MHz)

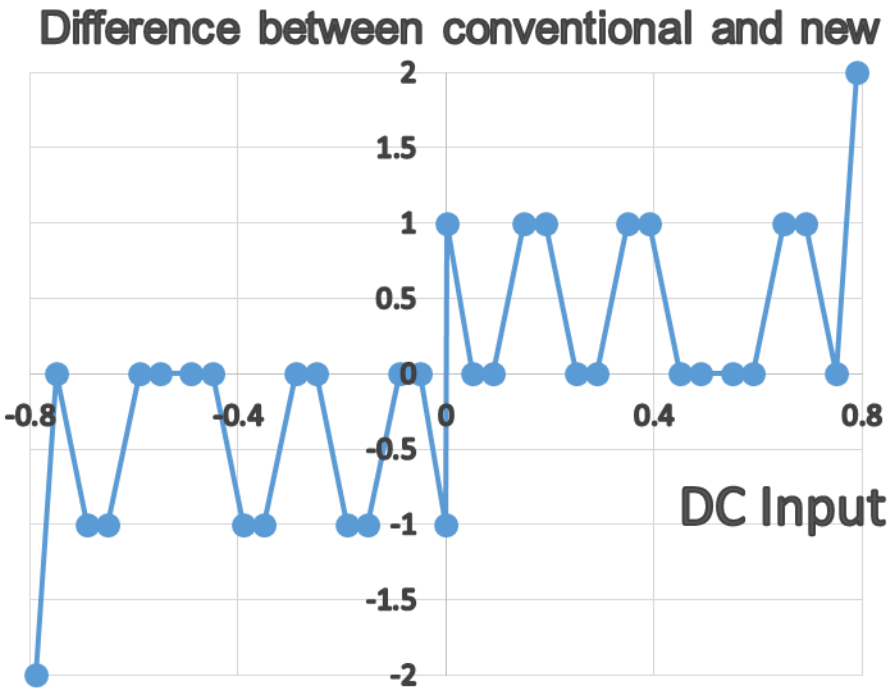


Part of output waveforms

FPGA Measurement Results

- 10-bit case





Difference between numbers of 1's
⇒ within ± 2
(※Total number is 1024)

SFDR improvement
⇒ more than 10dB

⇒ Linear DC

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Conclusion

＜ ΔΣ DA modulator ＞

Conventional：Limit cycle problem for small input

Proposed：Using digital dither

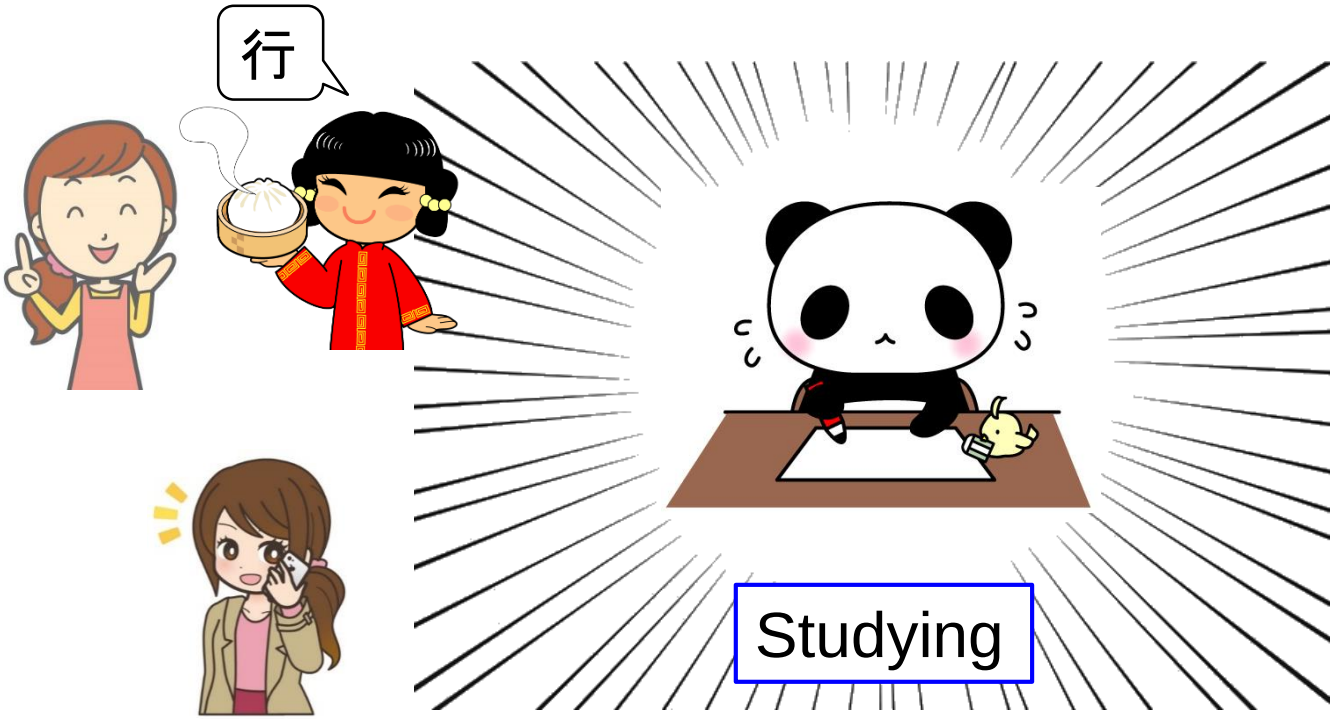
- Limit cycle reduction ⇒ Relax LPF requirement
- SFDR improvement by 10 dB
- Linear DC
- 1-bit DAC following a modulator thanks to XOR
- FPGA implementation

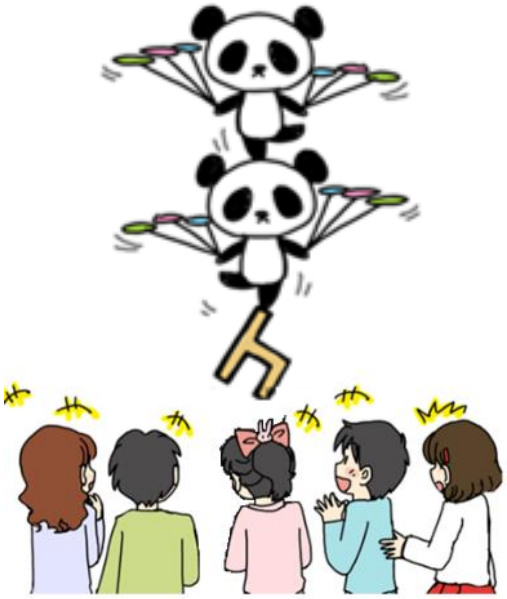
Human & Circuit are the Same

We can NOT concentrate
at completely quiet place

Philip E. Vernon
British Psychologist

Small ‘noise’ is good environment



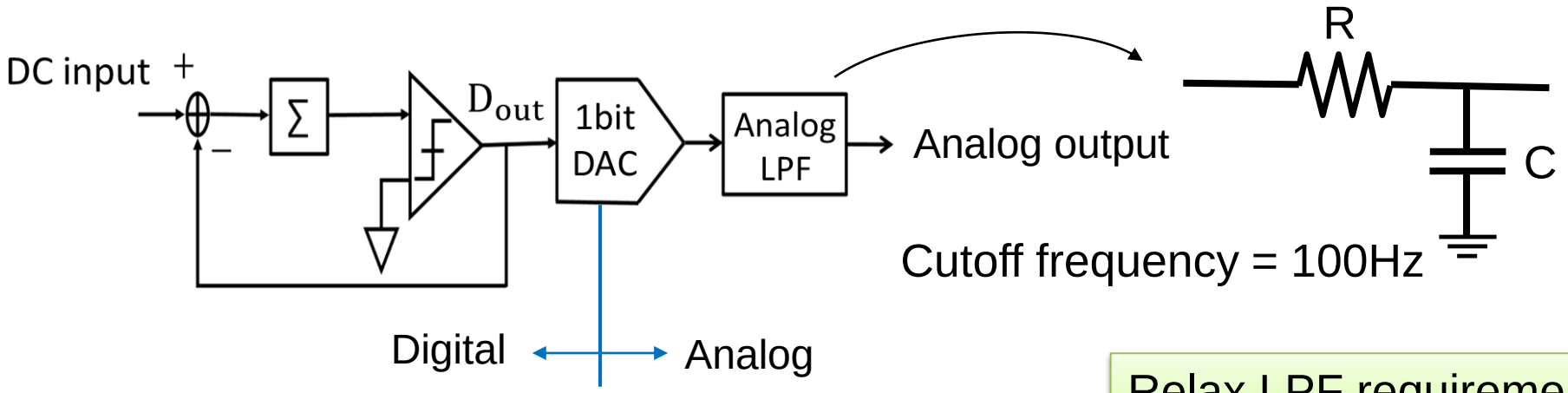


Appendix

App.

10-bit case
DC = 0.1

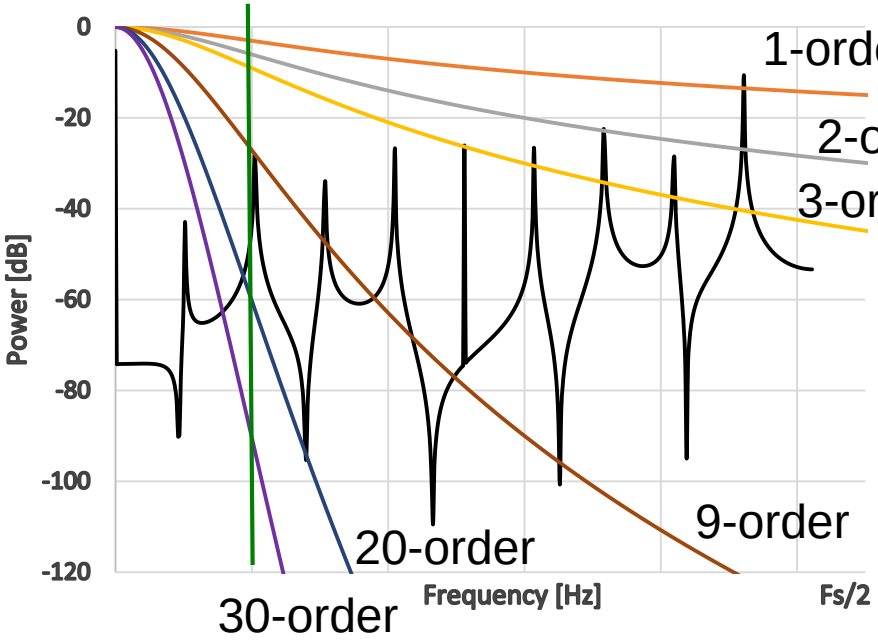
Latter LPF



Relax LPF requirement

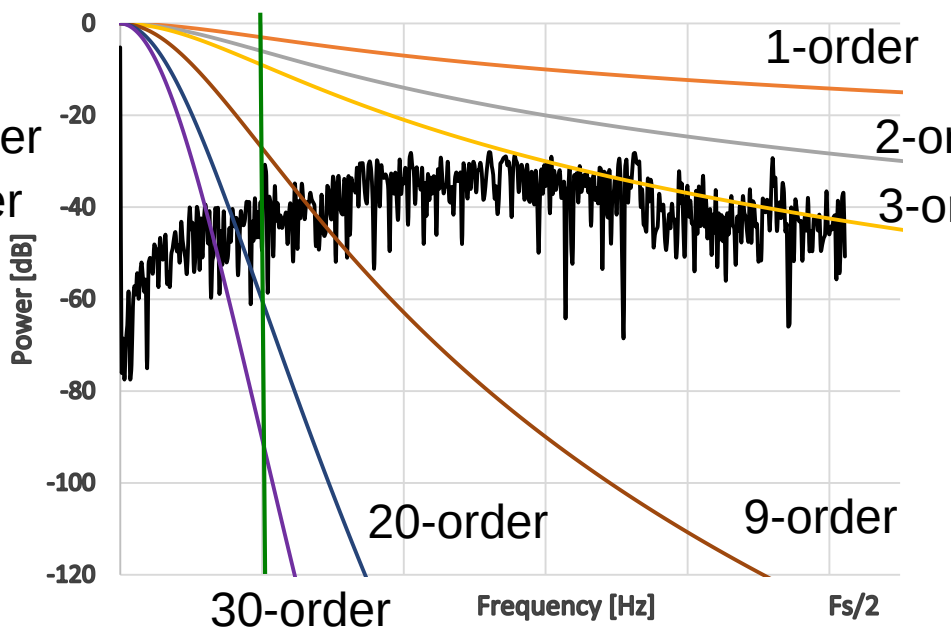
Conv.

f = 100Hz



Prop.

f = 100Hz

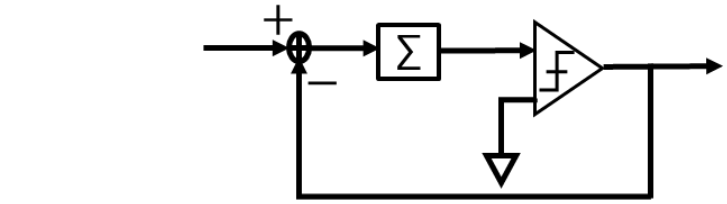


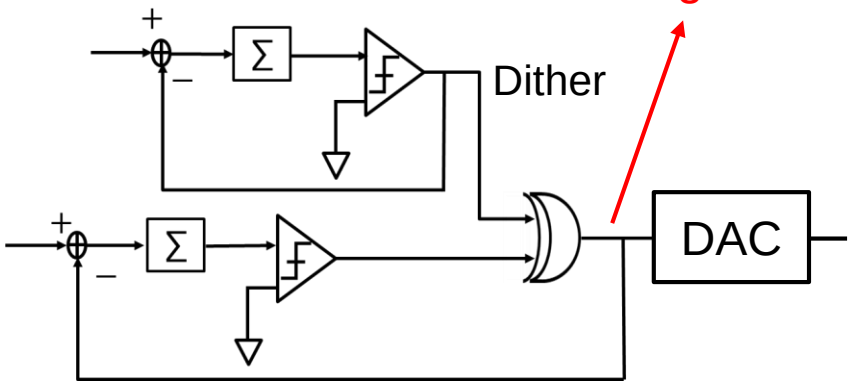
Using XOR gate

- Proposed circuit

Using XOR gate

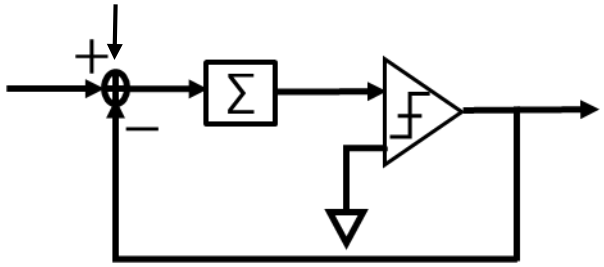
The conventional





- Input dither before ΔΣ modulator

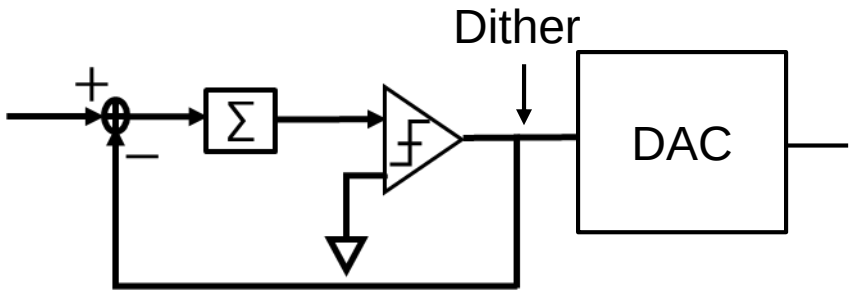
Dither



Increased noise

due to dither adds quantization error

- Input dither after ΔΣ modulator



Multi-bit DAC

Q1:なぜディザ入力信号に1Hzの正弦波を入力したが、
なぜ1Hzにしたのか？

A1: Because the sine wave of 1Hz is very simple. Also, I think I do not want to input the larger noise.

Q2:どのようにして最適な振幅、中心値を決めたのか？

A2:I determine the amplitude and the center value for maximum SFDR.

Q3:SFDRで評価しているが、後段にLPFがあるのでリミットサイクルは低周波側のみを評価するべきではないか。なぜ、高周波側で評価しているのか。

A3:Because relax the most of LPF requirement.
In addition, SFDR is simple indicator, and can apply the various signal bands, such as DC.

Q4:量子化器で出力された「0」または「1」をXORで反転させるのは、とても大きなディザ(ノイズ)を入れていると思うのだが大丈夫なのか。小さいディザの方が小さい誤差となるのではないのか。

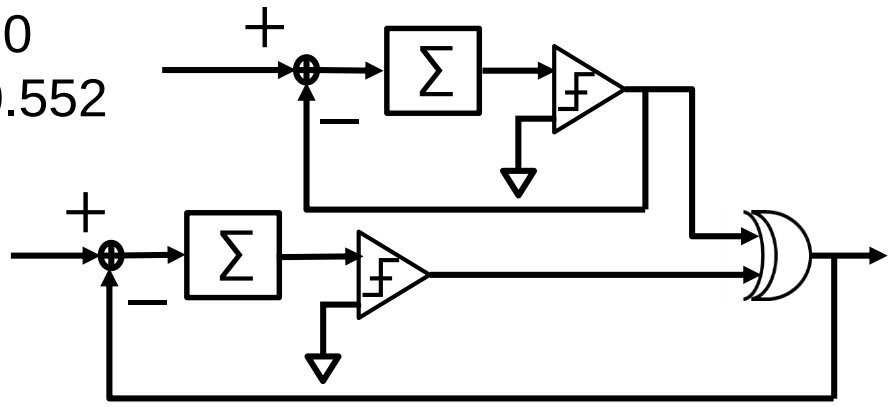
A4:The modulator output of the proposed is the same as that of the conventional.
So, the proposed circuit has no problem.

Some audio systems have the limit cycle in the signal band.
So, the limit cycle cannot be removed by LPF.
It is necessary to reduce the limit cycle in advance.

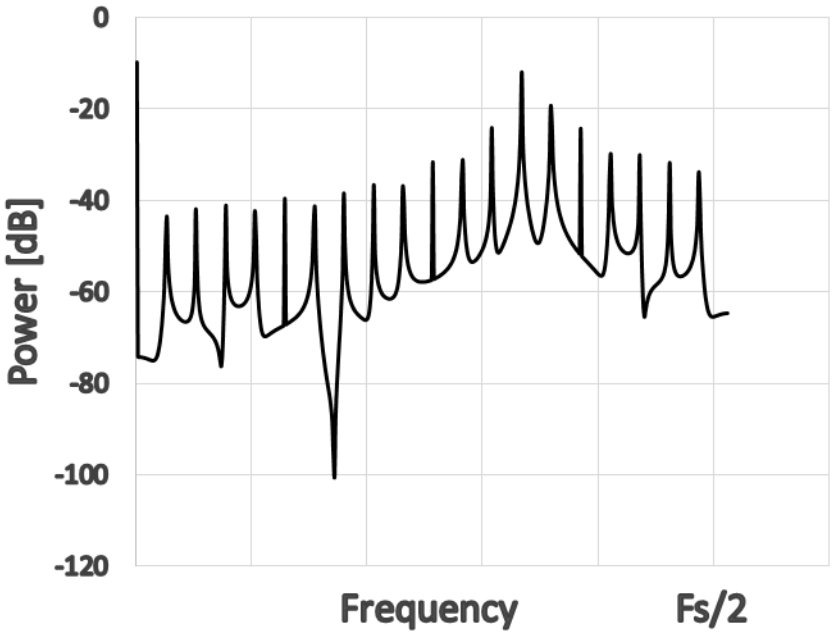
Simulation Results 10-bit case

Sine Wave Amplitude : 0.120
Center Value : -0.552

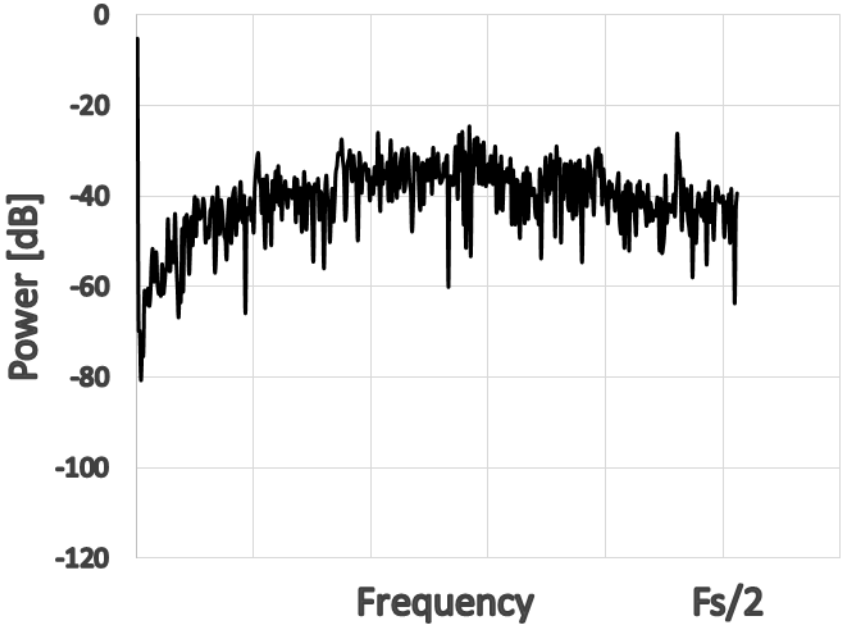
DC = -0.35 V



Conventional



Proposed



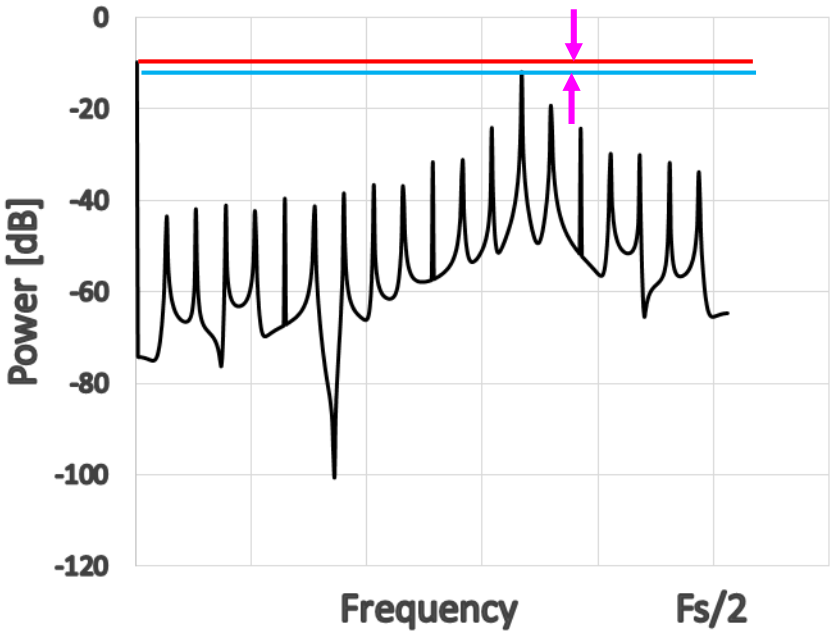
Simulation Results

10-bit case
DC = -0.35

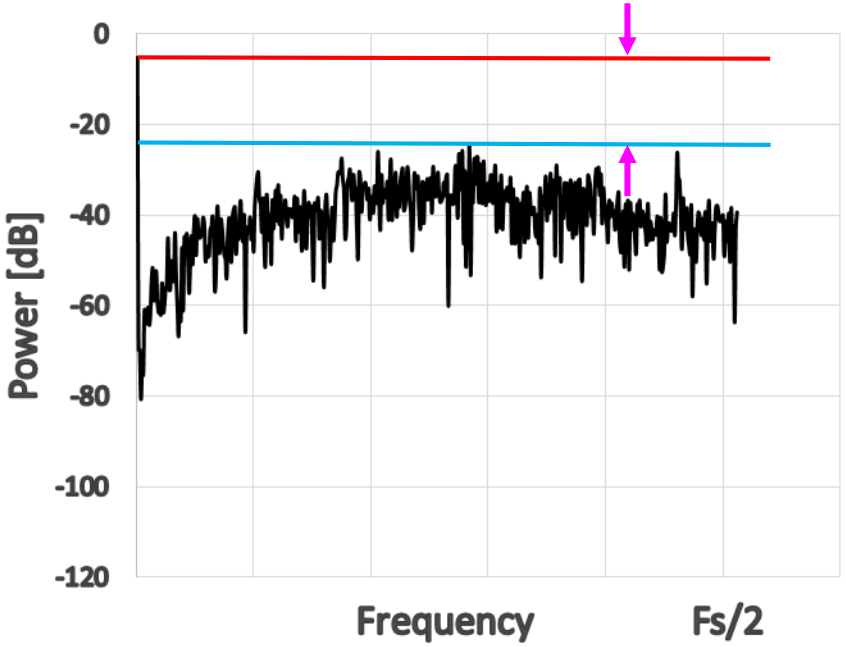
$$SFDR = \frac{\text{Signal Power}}{\text{Maximum Harmonics Power}}$$

SFDR = 2.16 dB < 16.33 dB

Conventional

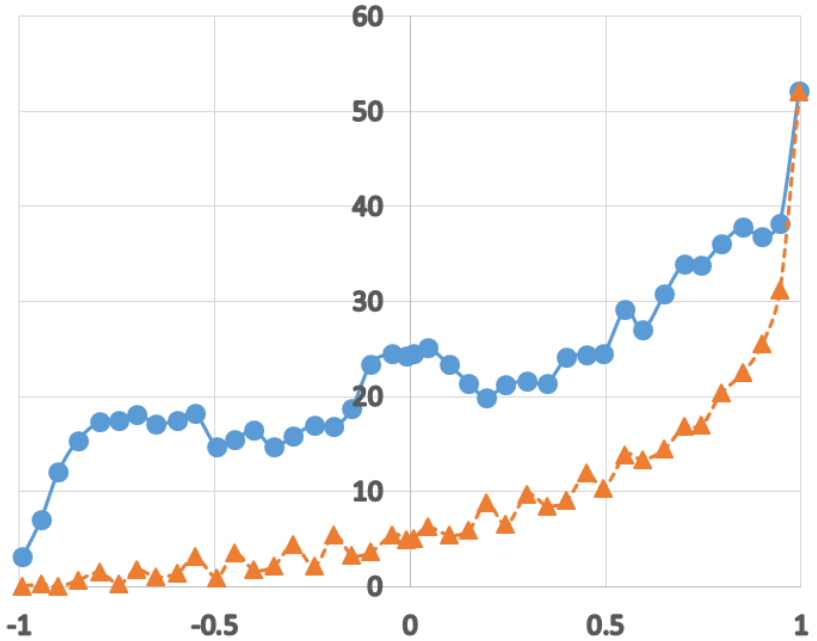


Proposed



Simulation Results 14-bit case

SFDR [dB]

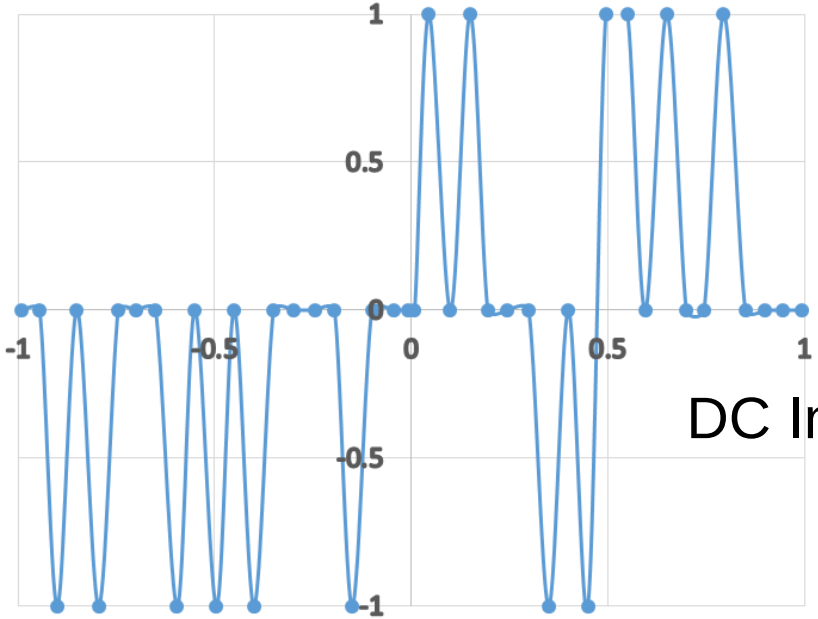


With dither
Without dither

DC Input

SFDR improvement
⇒ more than 10dB

Difference between conventional and new



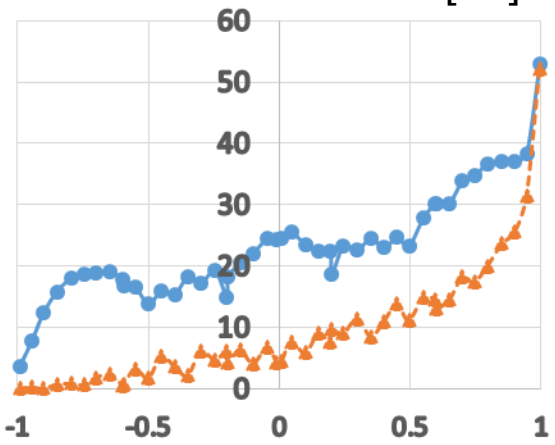
DC Input

Difference between numbers of 1's
⇒ within ± 1
(※Total number is 16384)

Linear DC

Simulation Results

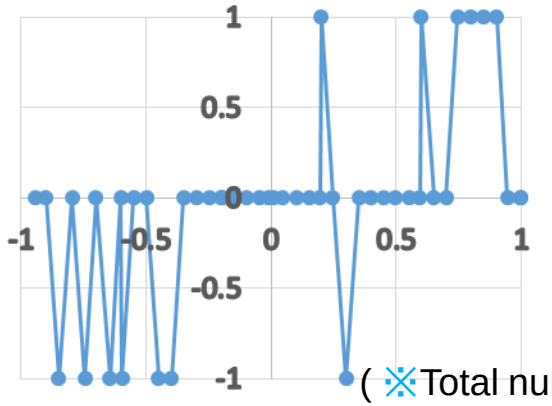
SFDR [dB]



DC Input

16-bit

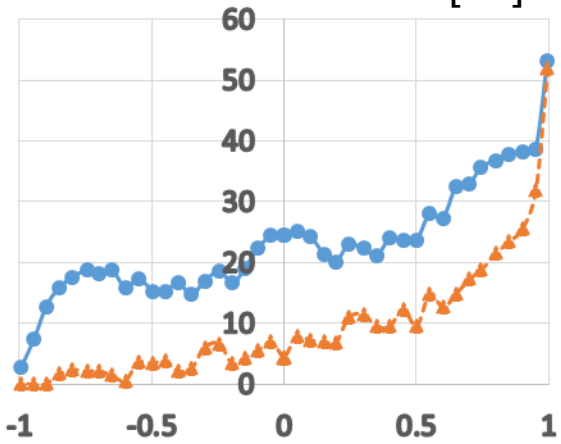
Difference between conventional and new



DC Input

(※Total number is 65536)

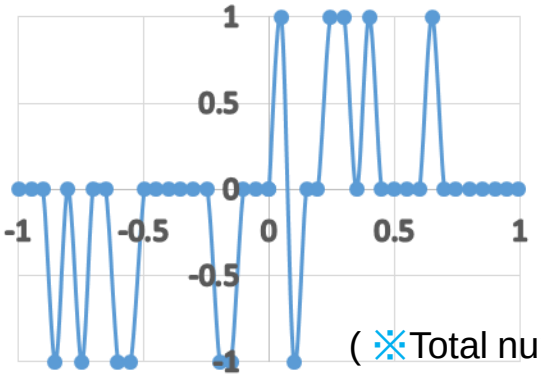
SFDR [dB]



DC Input

18-bit

Difference between conventional and new



DC Input

(※Total number is 262144)

With dither — Without dither - - -

Difference between numbers of 1's

⇒ within ± 2

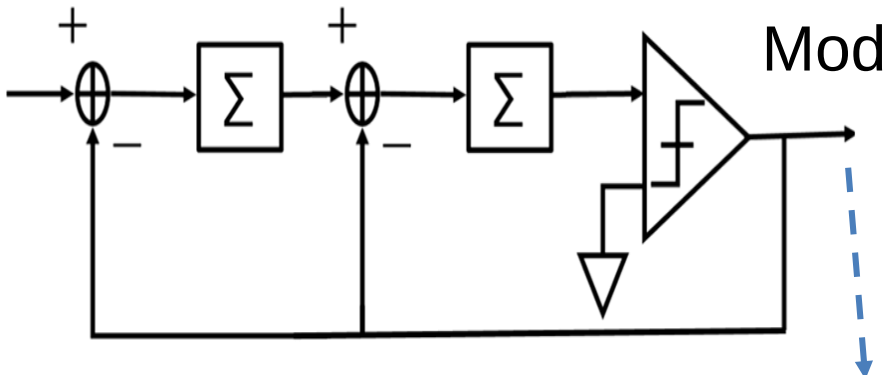
SFDR improvement ⇒ more than 10dB

⇒ Linear DC

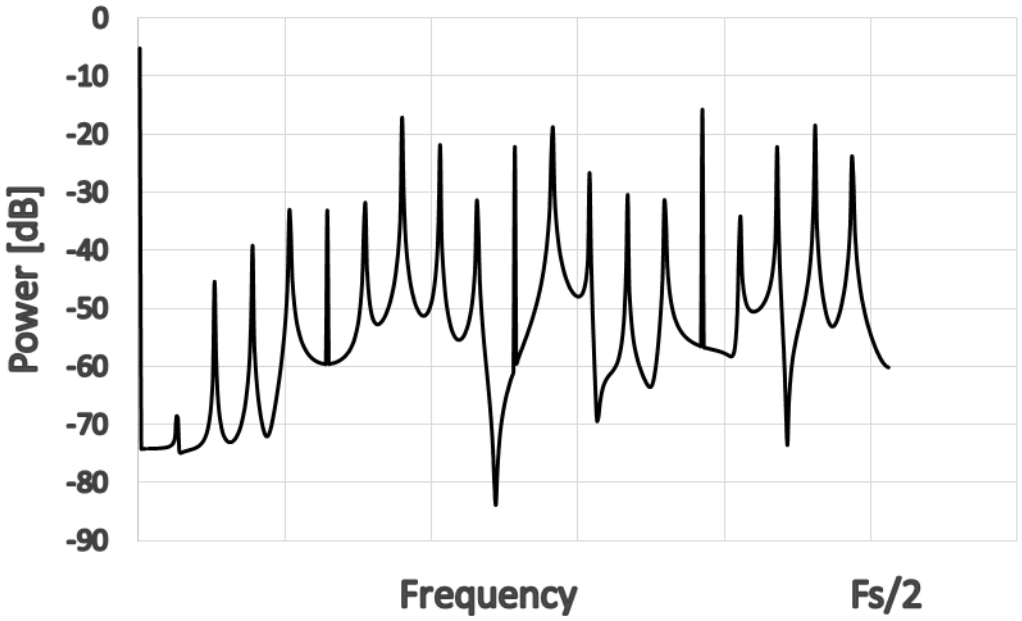
Second-Order ΔΣ modulator

10-bit case

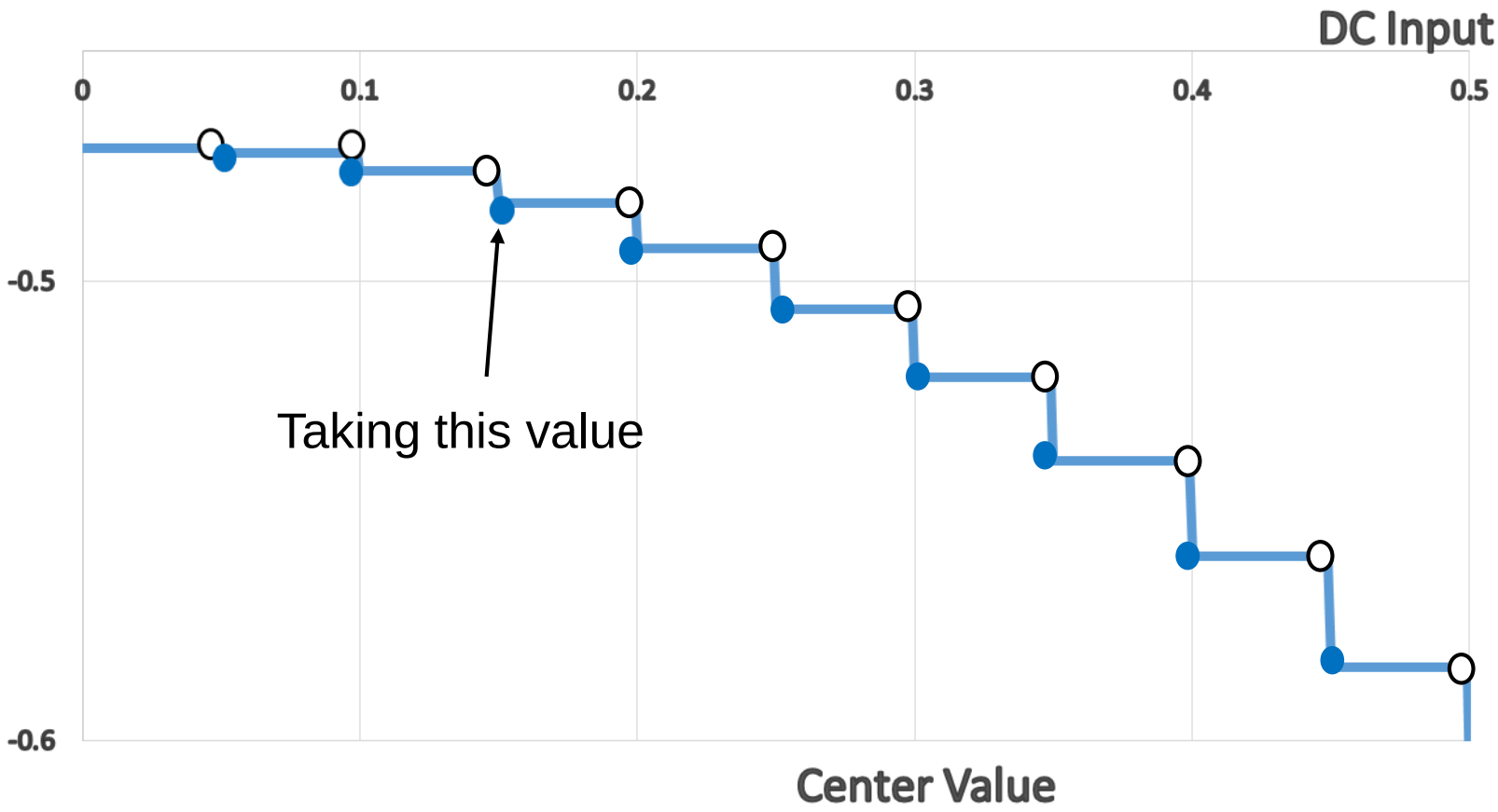
DC = 0.1



Modulator output

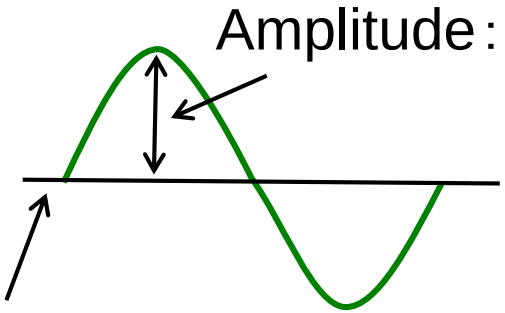


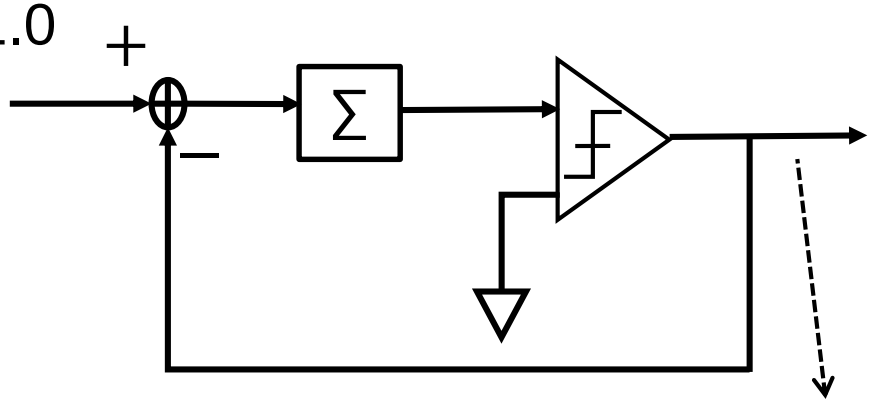
Approximation of Center Value

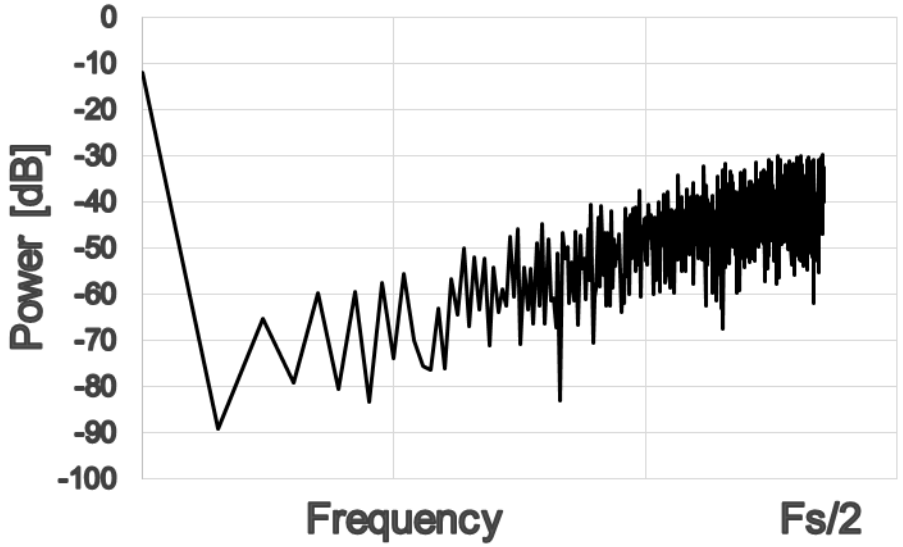


Noise Shaped 10-bit case

Sine Wave







Q & A 発表日:2016/10/28

Q1: FPGA実装で、三角波を正弦波にするとどうなるか。

A1: 正弦波の場合は行っていない。

Q2: FPGAの振幅0.256を、違う値に変えるとどうなるか。

A2: 値を変えた場合は行っていない。

Q3: FPGA実装で、なぜ振幅0.256としたのか。

A3:1周期の三角波に1024点を取っている。1024÷4=256を参考にし、0.001ずつ増加、または減少させ、1周期で三角波が生成できるように設定した。

Limit Cycle Suppression Technique Using Digital Dither in Delta Sigma DA Modulator

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Abstract - This paper proposes a digital dither technique to suppress limit cycles in a ΔΣ DA modulator. It uses an exclusive OR (XOR) gate at the modulator output and the digital dither is generated by another ΔΣD modulator. The resolution of the DAC following the modulator is 1-bit (instead of multi-bit) thanks to XOR gate usage, and the overall SNR does not degrade because the dither is added at the output and hence it is noise-shaped. Our MATLAB simulation and FPGA implementation results have verified the effectiveness of the proposed method.

1. Introduction

A ΔΣ DA converter consists of mostly digital circuit, and it is frequently used for electronic measurement and test equipment as well as audio systems because it can produce highly linear DC and low frequency signal with high resolution (Fig. 1). However the ΔΣ DA modulator suffers from a limit cycle problem when its input amplitude is small [1, 2, 3, 4].

We propose here a digital dither method to solve this problem. It uses an XOR gate at the modulator output and the digital dither. The proposed method has 3 important features: (i) A 1-bit DAC following the modulator can be used thanks to using an XOR gate. (ii) The digital dither is noise-shaped and does not affect the SNR because it is effectively added at the modulator output. (iii) A digital dither is also generated by another ΔΣ digital modulator.

Our MATLAB simulation results as well as FPGA implementation results confirm that the limit cycles are suppressed for all 10, 14, 16, 18-bit cases.

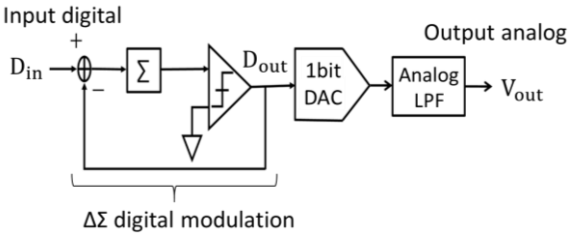

Fig. 1. Block diagram of the first-order ΔΣ DA converter

2. ΔΣDA modulator (Digital modulator)

< 2.1 > ΔΣ DA modulator configuration

A ΔΣ DA modulator consists of all digital circuits with feedback configuration using an integrator and a comparator (Fig. 1). The error signal is accumulated at the integrator, and its output compared by a comparator. The comparator output (0 or 1) is the ΔΣ modulator output. Also the comparator output is fed back to the input. It is known in [1, 2] that the output power spectrum is noise-shaped; quantization noise is reduced at low frequency while increased at high frequency.

< 2.2 > ΔΣ modulator with digital dither

The digital dither, 0 or 1, is defined as (pseudo-)random signal, and it is used to remove the limit cycles of the ΔΣ DA modulator when input amplitude is very small. If the digital dither is added at the input of the modulator, the noise component is increased so that the overall SNR may degrade. On the other hand, if it is directly added to the ΔΣ modulator output, a multi-bit DAC (instead of a 1-bit DAC) following the modulator is required, and the multi-bit DAC suffers from nonlinearity problem [1, 2]. The proposed technique solves these two problems.

< 2.3 > Proposed ΔΣ modulator with XOR

We propose here a new technique using XOR gate whose inputs are the comparator output and the digital dither generated by another modulator (Fig. 2). The modulator output is the XOR output; in case the dither signal (D_{dither}) is 0, the modulator output (D_{out}) is the same as the comparator output (D_{on}) (or no dither is added), while in case the dither signal (D_{dither}) is 1, the modulator output is the reverse of the comparator output (D_{on}) (or effectively dither is added).

Appearance frequency of 1 for the dither signal (D_{dither}) can be adjusted by changing the amplitude and the center value of the input dither signal (D_{ind}). When the amplitude and the center value are very small, the frequency of the dither signal of 1 is low, and vice versa.

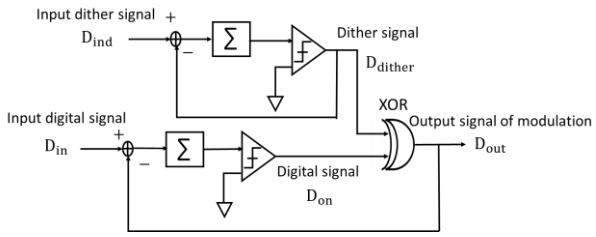

Fig. 2. Proposed ΔΣ DA modulator with digital dither

3. MATLAB Simulation Results

< 3.1 > Limit Cycle Suppression (10 bit case)

We have verified the effectiveness of the proposed

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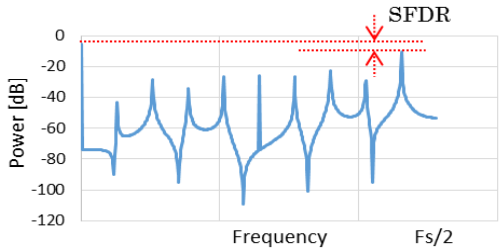
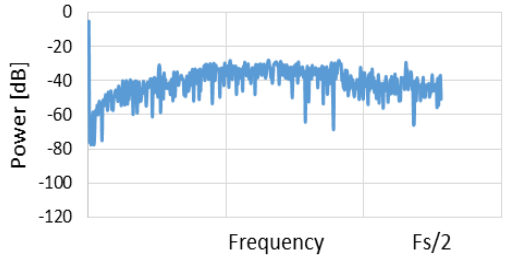
technique (Fig. 2). We use a sinusoidal signal (Dind) whose period is 10K-point for the dither generator and its amplitude and center values are controlled for limit cycle reduction. In addition, we have checked that the numbers of 1's at the modulator output are the same in both cases of with and without dither for DC input (full scale:-1 ~ +1) of Din.

Fig. 3 shows simulation results when the DC input of Din is 0.1. We see that the limit cycle of the proposed circuit with dither (Fig. 3 (b)) is lower than that without dither (Fig. 3 (a)), and also that Spurious Free Dynamic Range (SFDR) with dither (22.9dB) is higher than that without dither (5.4dB).

In a similar manner, Fig. 4 shows the amplitude and the center values of the input sine wave (Dind) adjusted according to the modulator DC input (Din) for limit cycle reduction. We compare SFDRs with dither and without dither and we see in Fig. 5 that it is improved for all range of the DC input (Din).

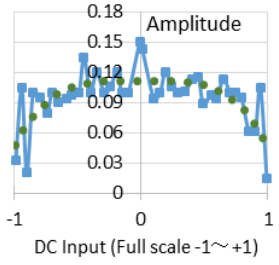


(a) Without dither

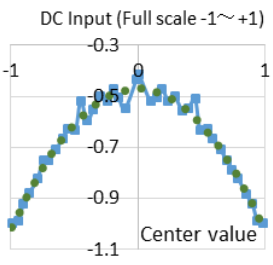


(b) Dither modulator sine wave input (Dind) of amplitude: 0.094, center value: -0.520.

Fig. 3. Power spectrum of ΔΣ modulator output in case that the DC input (Din) is 0.1.



(a) Amplitude



(b) Center value

Fig. 4. Dither generation modulator input sine wave for limit cycle reduction (Dot lines are approximation).

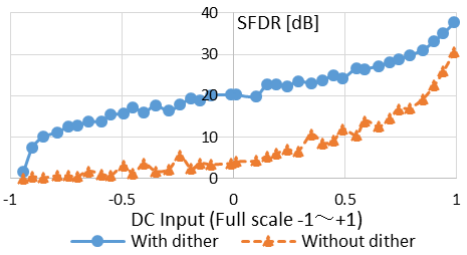
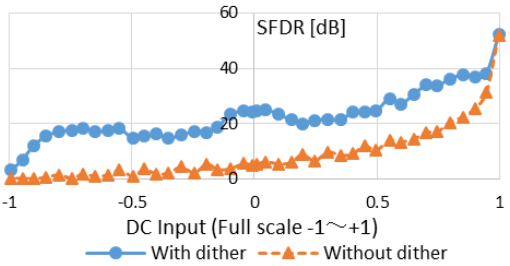


Fig. 5. SFDR comparison (simulation results)

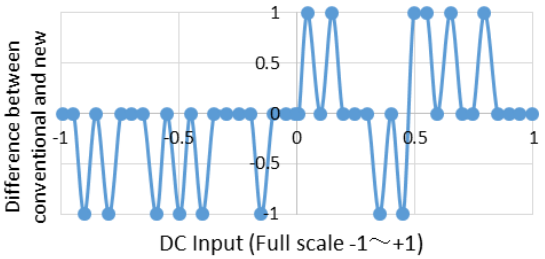
< 3.2 > Study on reduced circuit of the limit cycle (14, 16, 18-bit cases)

Section 3.1 describes the validation of the proposed algorithm. We modify this original method for ease of FPGA implementation; digital sinewave generation with controlled amplitude and center values is complicated for implementation, and here we replace a sinewave with a triangular wave for the dither modulator input.

Fig. 4 shows approximation graph to determine the amplitude and the center value of sine wave for a certain DC input, and there only DC input change is enough. We have simulated using this method in 14, 16, 18-bit cases, and their results are shown as Figs. 6, 7 and 8. We see in Fig. 6(a), 7, 8 that SFDR is improved for the DC input of full scale between -1 and +1. Fig. 6(b) shows the difference of the modulator output 1's numbers with and without the proposed dither in 14-bit case. We see that the proposed circuit maintains the DC linearity because the difference number of 1's is within a ±1 range. We also see in Figs. 7, 8 that the linearity is maintained in 16-bit and 18-bit cases.



(a) SFDR comparison



(b) Linearity

Fig. 6. Simulation results in 14-bit case.

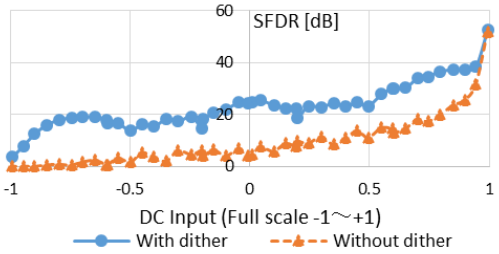


Fig. 7. SFDR simulation results in 16-bit case.

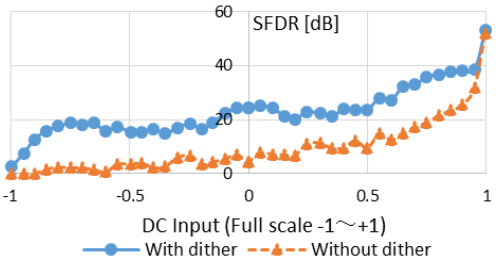


Fig. 8. SFDR simulation results in 18-bit case.

< 3.3 > FPGA design

Fig. 9 shows digital circuit design in Fig. 2, and it was implemented on an FPGA, based on the description in section 3.2. The amplitude of the triangular wave is 0.256 for design simplicity, and its center value is chosen as shown in Fig. 10 (see Fig. 4(b)). Also the DC input (Din) range is from -0.8 to +0.8.

Fig. 11 shows simulation results; we see in Fig. 11(a) that SFDR improves for the DC input from -0.8 to +0.8, and also Fig. 11(b) shows the difference between numbers of modulator output 1's with and without the proposed dither in 10-bit case and we see that the difference is within ±2. Fig. 12 shows the FPGA board.

4. Conclusion

We have proposed a new digital dither technique for limit cycle suppression and SFDR improvement in ΔΣ DA modulators. It uses an XOR gate at the modulator output and the digital dither is generated by another ΔΣD modulator or triangle wave generator (counter). The resolution of the DAC following the modulator is 1-bit (instead of multi-bit) thanks to XOR gate usage, and the overall SNR does not degrade because the dither is added at the output and hence it is noise-shaped. We have performed MATLAB simulation and FPGA implementation which verified the effectiveness of the proposed method.

References

[1] R. Schreier, G. C. Temes, Understanding Delta-Sigma Data Converters, Wiley-IEEE Press (2009).

[2] J. C. Candy, G. C. Temes (Editors), Oversampling Delta-Sigma Data Converters: Theory, Design, and Simulation, Wiley-IEEE Press (1991).

[3] D. Hyun, G. Fisher,``Limit Cycles and Pattern Noise in Single-Stage Single-Bit Delta-Sigma Modulators, '' IEEE Trans. Circuits and Systems I , pp. 646-656 (May 2002).

[4] S. R. Norsworthy, ``Effective Dithering of Sigma-Delta Modulators,'' IEEE ISCAS (May 1992).

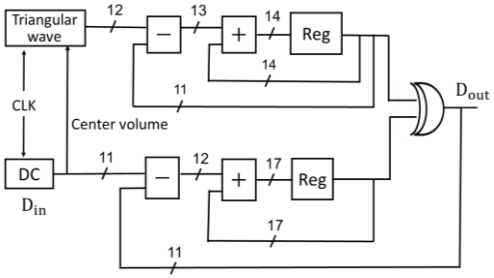


Fig. 9. Digital circuit design of the proposed modulator.

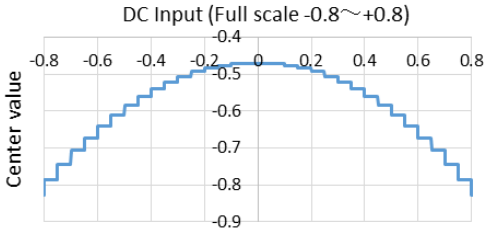
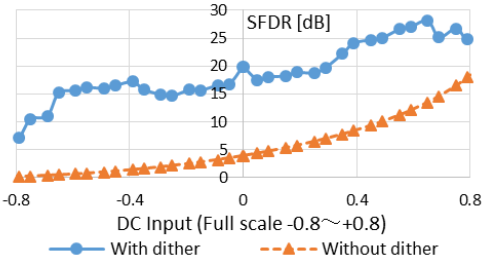
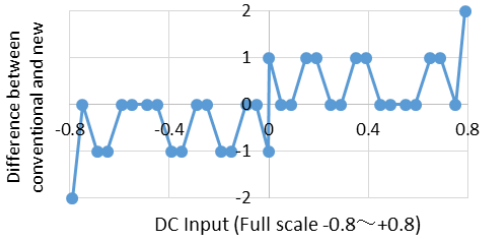


Fig. 10. Input triangular wave center value.



(a) SFDR comparison



(b) Difference between numbers of modulator output 1's with and without the proposed dither.

Fig. 11. FPGA simulation results of the circuit in Fig. 9.

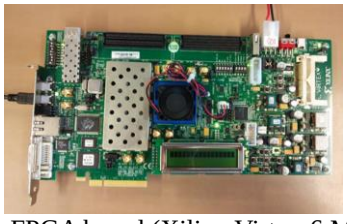
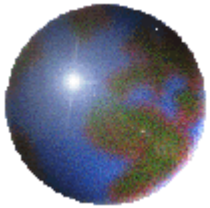


Fig. 12. FPGA board (Xilinx Virtex-6 ML605).

Spread-Spectrum Clocking in Switching Regulators to Reduce EMI



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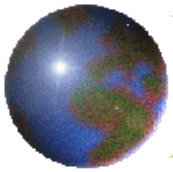
Sanyo Electric Co. Ltd., Japan



Contents

- Research Background and Goal
- Principle of DC-DC Converters
- Proposal of Noise Power Spectrum Spread Method in DC-DC Converters
- Implementation and Measurement Results
- Summary

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- Proposal of Noise Power Spectrum Spread Method in DC-DC Converters
- Implementation and Measurement Results
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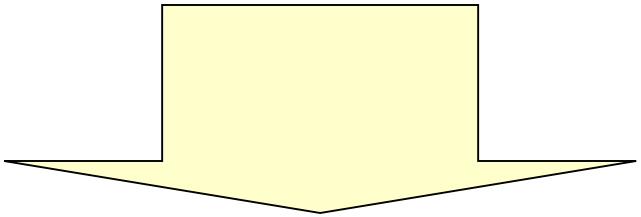
Research Background

- Mobile equipment prevails everywhere
- Mobile phone, Digital still camera, PDA



- Small size, High efficiency
- Multiple supply voltages
- Low-voltage supply

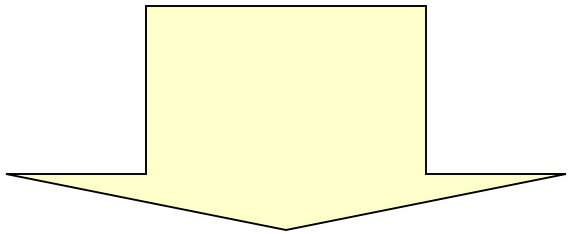
Features of Switching Regulator

- Merit
  - High efficiency
  - Continuously varying output voltage
  - Large output current
- Demerit
  - Coil is required. → bulky and costly
  - Switching noise

Research Goal

- We focus on a big problem of switching regulator:

  "Switching and harmonic noises"



Proposal of EMI reduction technique by spreading noise power spectrum

Contents

- Research Background and Goal
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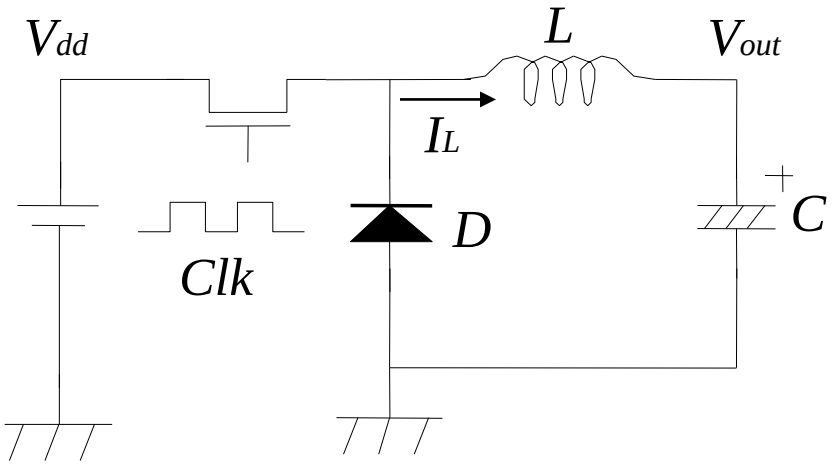
Principle of DC-DC Converter(1)



- In case Clk=ON

$$\Delta I_{L1} = \frac{V_{dd} - V_{out}}{L} \times T_{on}$$

- In case Clk=OFF

$$\Delta I_{L2} = - \frac{V_{out}}{L} \times T_{off}$$

$$V_{out} = \frac{T_{on}}{T} \bullet V_{dd}$$

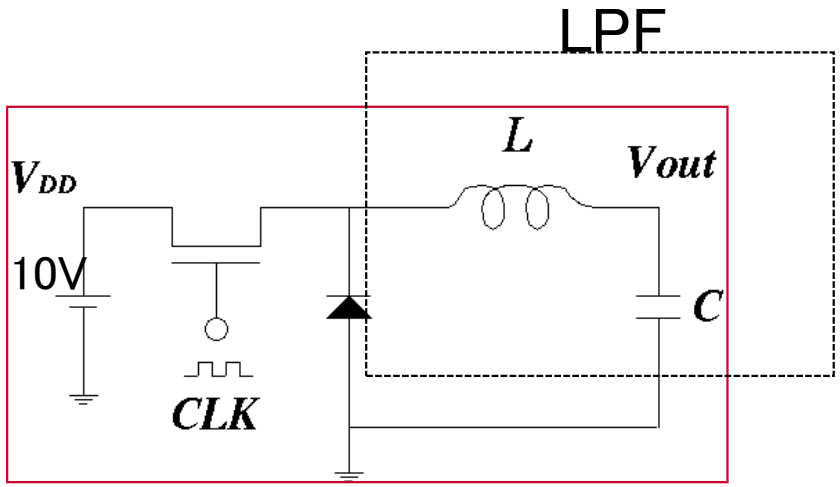
$$\Delta I_{L1} = \Delta I_{L2}$$

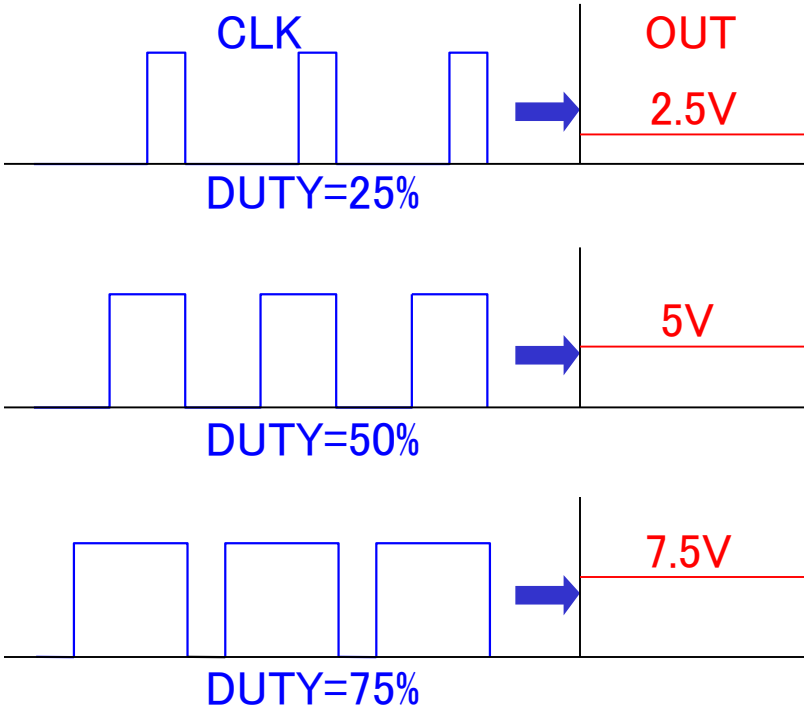
T; clock period

Output voltage *Vout* is determined by the clock duty.

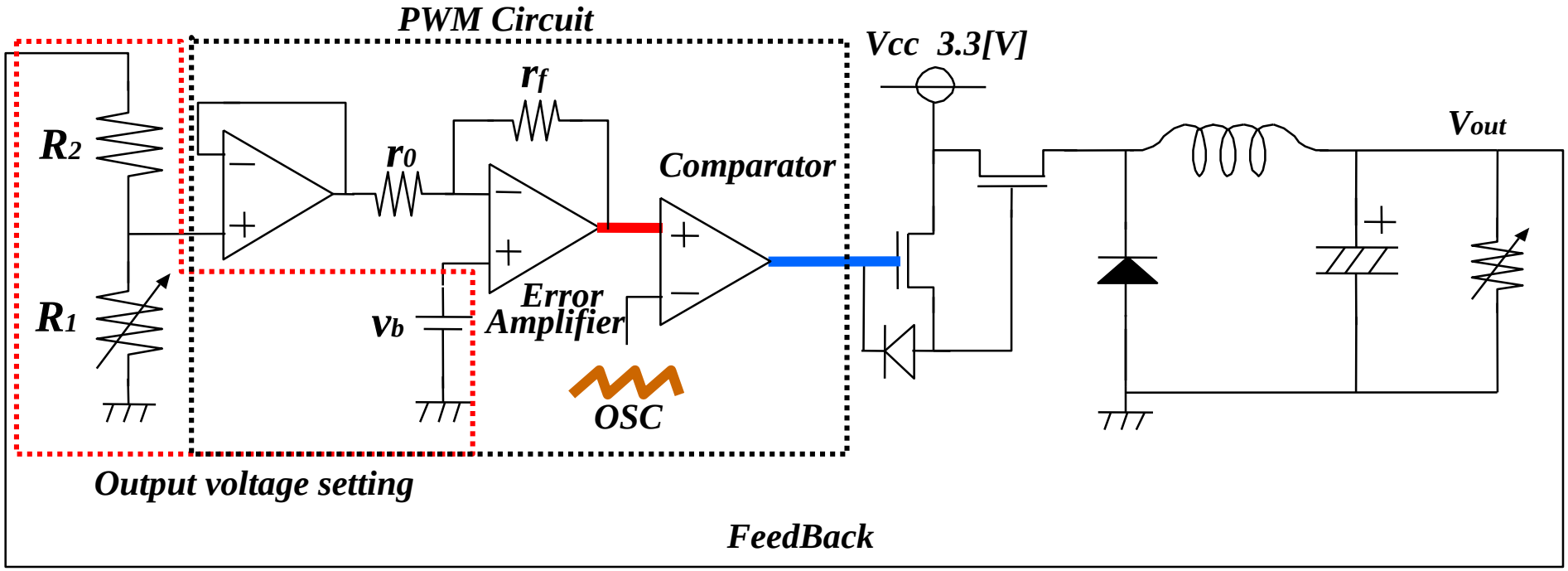
Principle of DC-DC Converter(2)

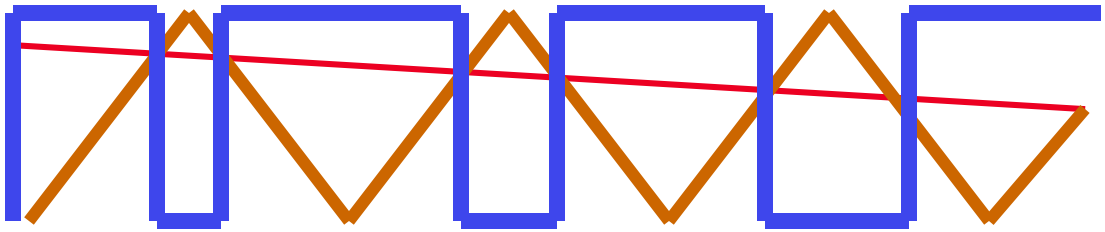
- Vdd: Input voltage
- CLK: Switching clock
- L, C: Low pass filter for smoothing
- Vout : Output voltage





DC-DC Converter with PWM Controller





Comparator output

Error amplifier output

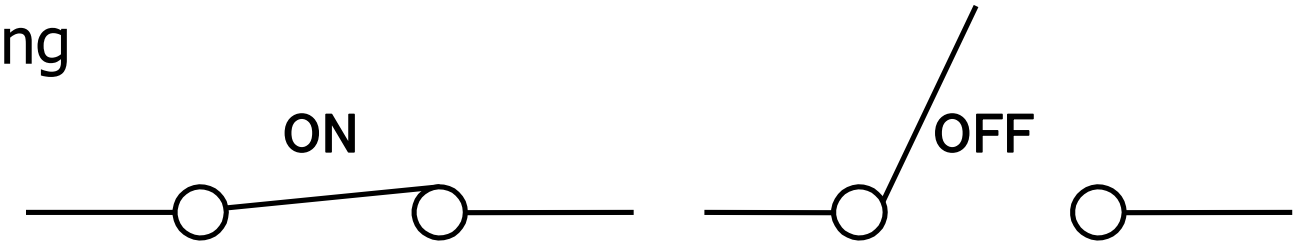
Triangular wave

Features of PWM Control

Advantage

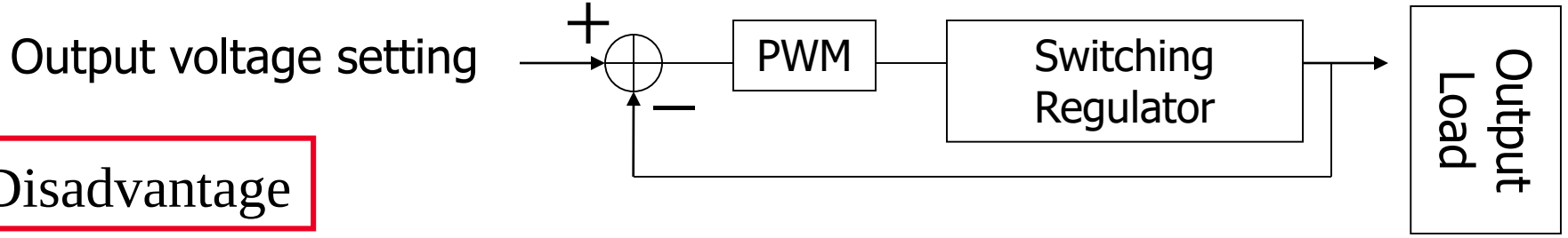
- ON/OFF switching

⇨ High efficiecy



- Negative feedback control

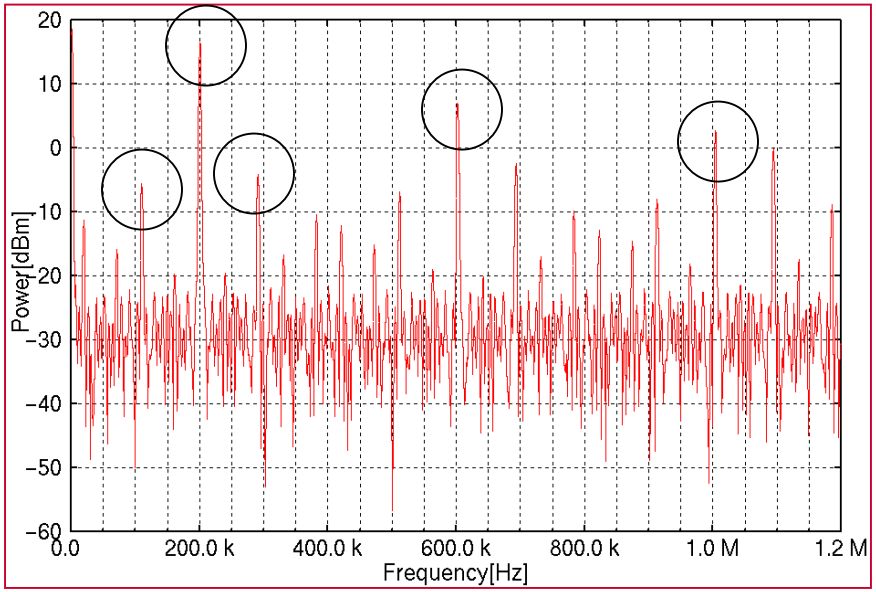
⇨ Output is stable regardless of output load.

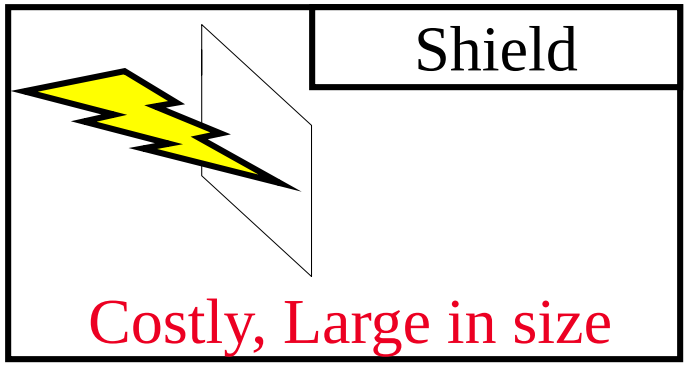


Disadvantage

- Synchronization with clock ⇨ Harmonic noises in specific frequencies

EMI and Switching Regulator





Shield is required
to meet EMI Regulations

Proposal of EMI reduction circuit

Contents

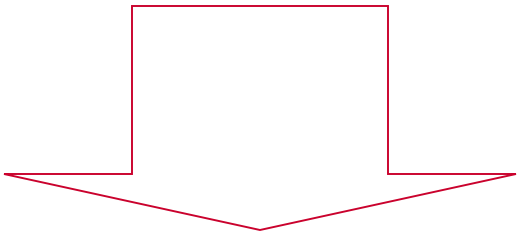
- Research Background and Goal
- Principle of DC-DC Converters
- Proposal of Noise Power Spectrum Spread Method in DC-DC Converters
- Implementation and Measurement Results
- Summary

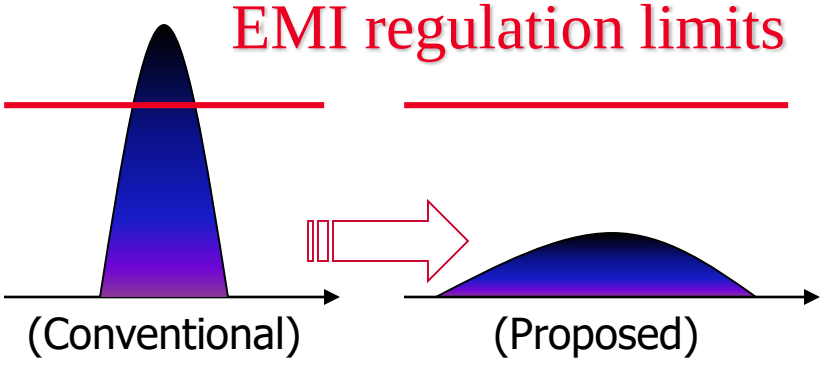
Proposed Method

Conventional DC-DC Converter +

Extra Digital Control Circuit

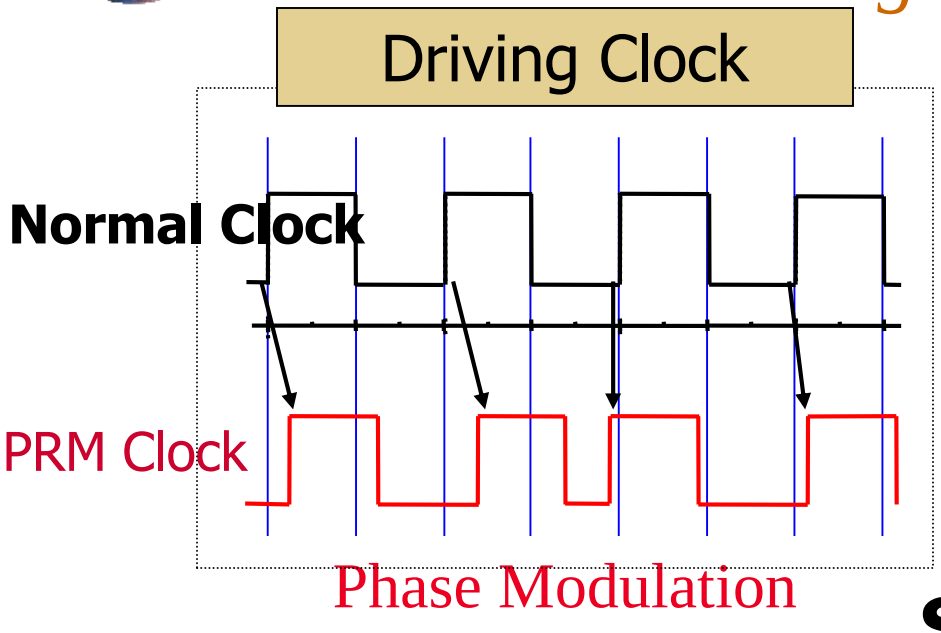
Generated switching noise power spectrum are in specific frequencies.

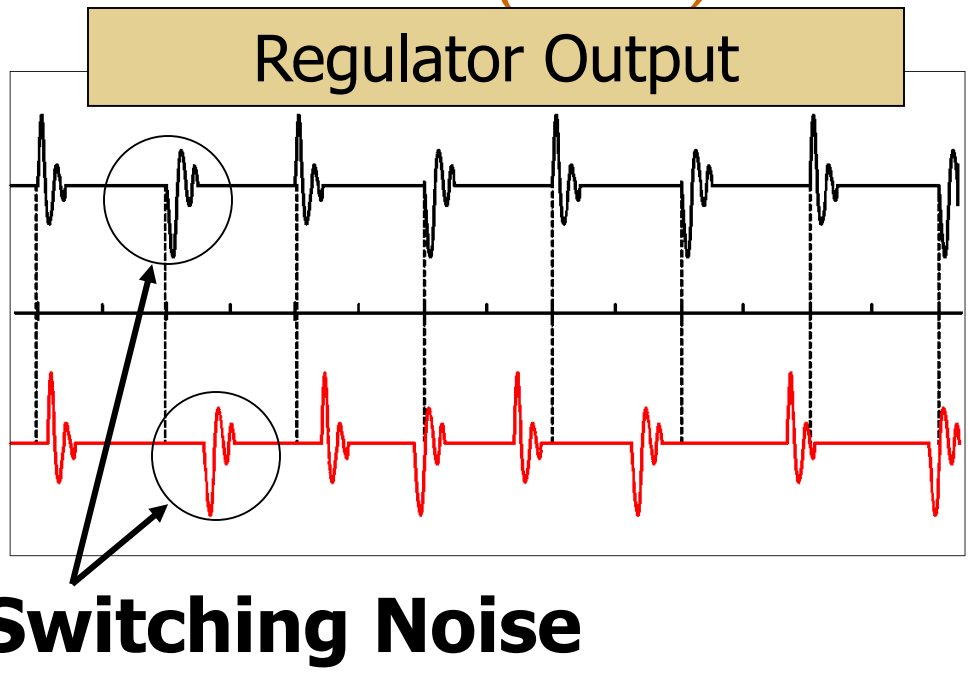




By spreading the spectrum of switching noise power, EMI reduction is realized.

Principle of Pseudo-Random Digital Modulation (PRM)





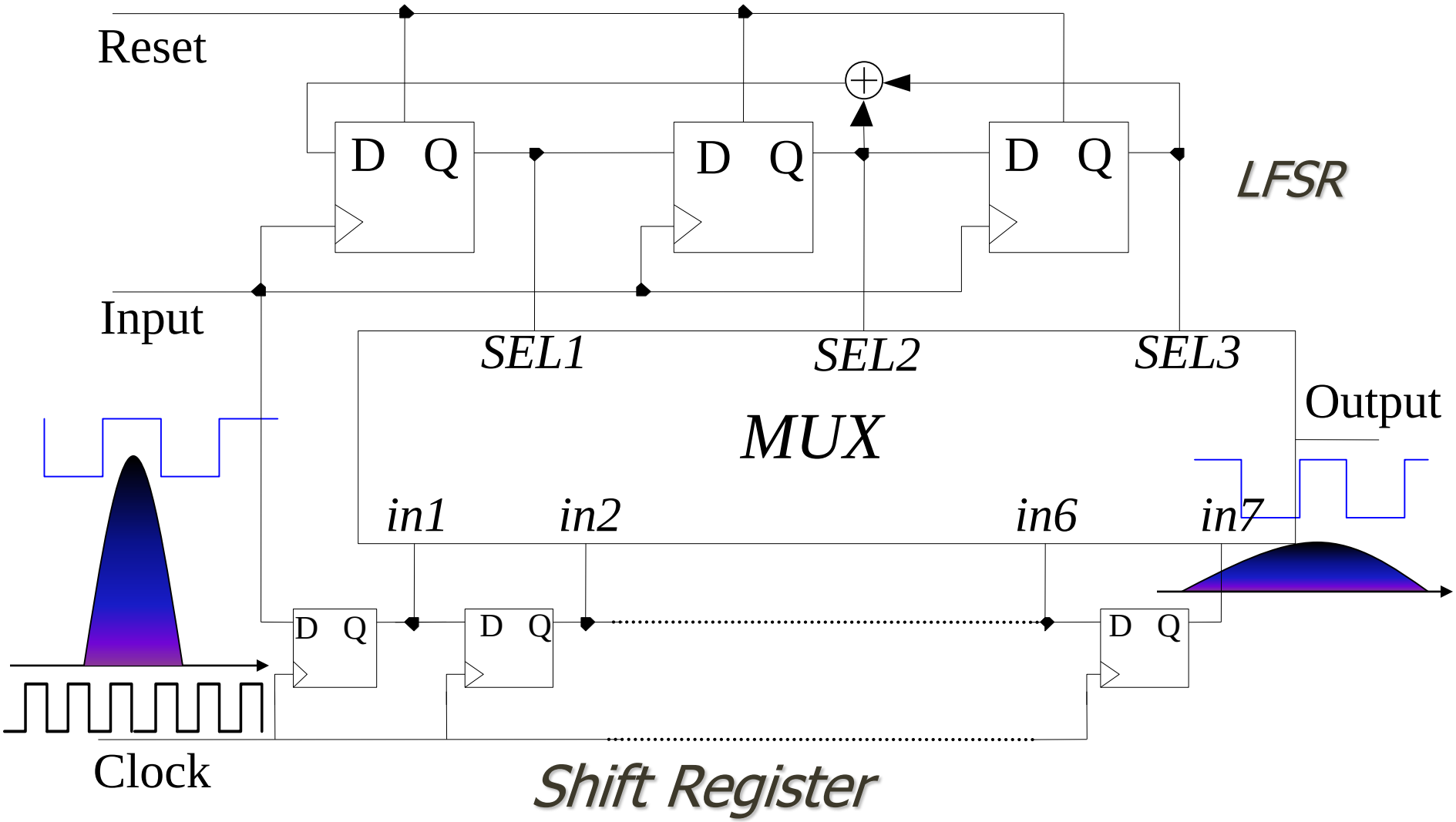
- Effect of $V = L\frac{di}{dt}$ ⇒ Large Switching Noises
- Switching Control with Pulse ⇒ Large Harmonic Noises

⇓

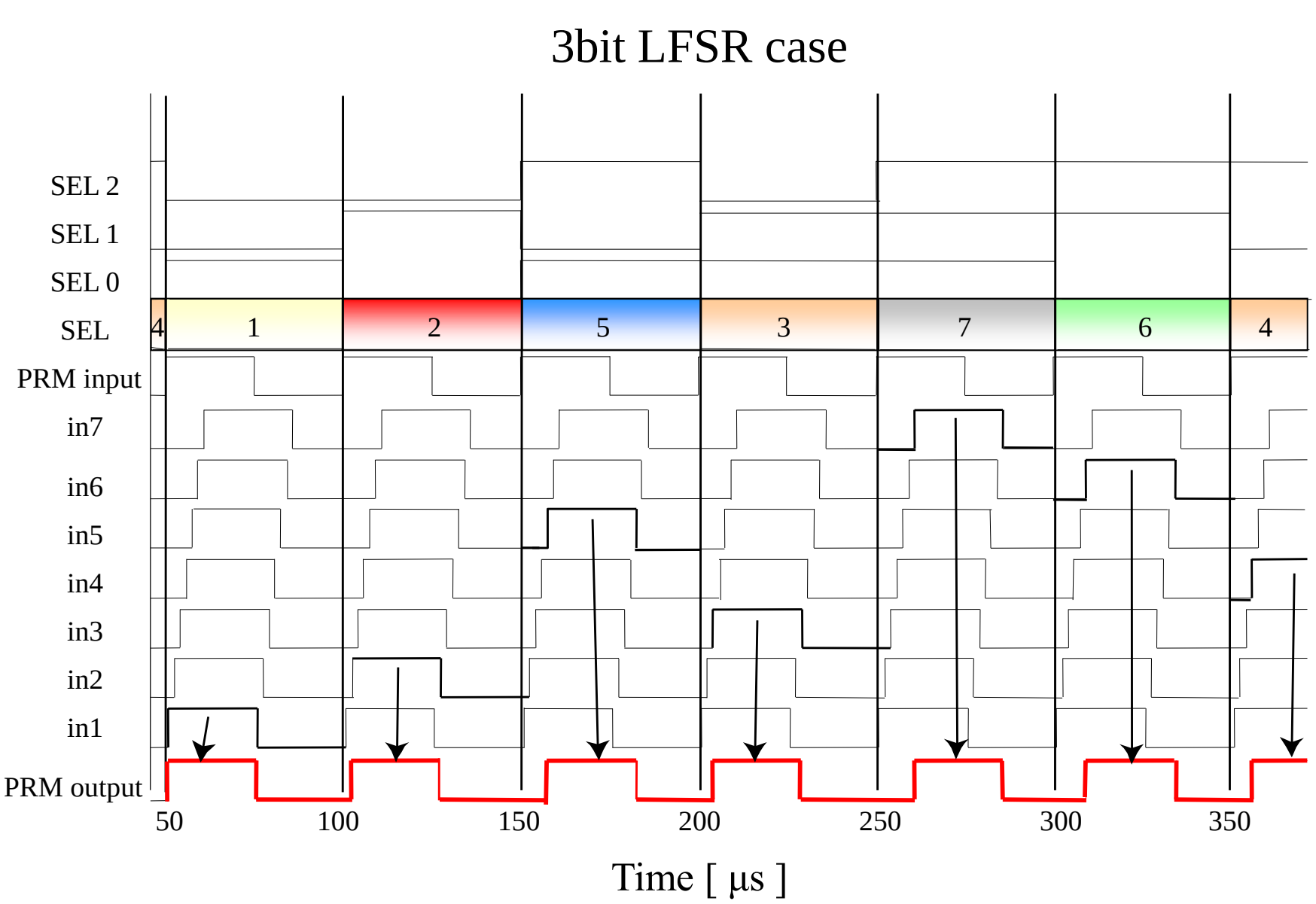
Pseudo-Random Spread Spectrum of Noise Power

PRM Circuit Implementation

- 3bit LFSR case -



PRM Timing Chart

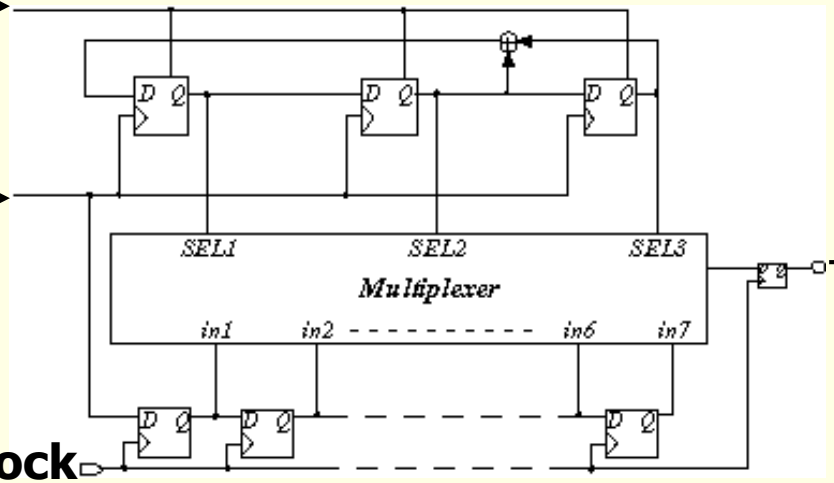


DC-DC Converter with PRM

Proposed PRM Circuit

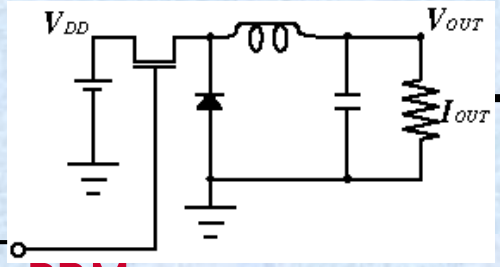
Reset

PRM input



Clock

DC-DC Converter Output



PRM Output

Power Circuit

DC-DC Converter

PWM output

PWM Controller

Control Circuit

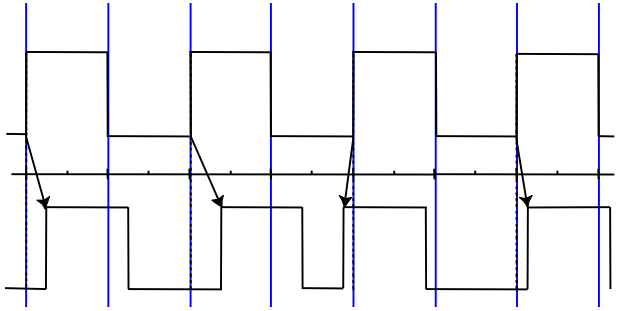
V_{OUT}

Conventional Circuit

(No need for modification)

Optimal Clock Phase Shift(1)

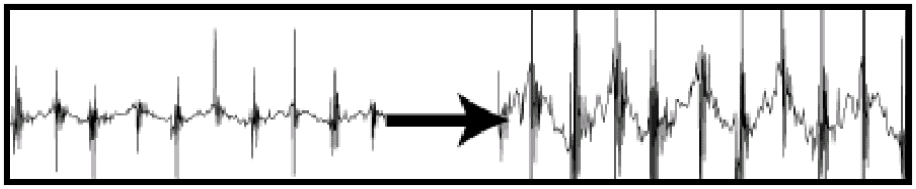
Normal clock (Conventional)



PRM clock (proposed)

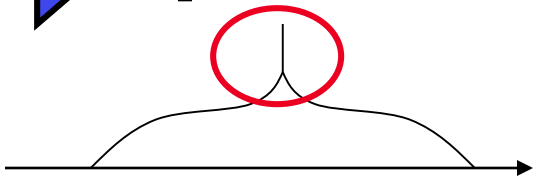
- When clock phase shift is too large,

output ripple becomes too large



- When clock phase shift is too small,

noise spectrum are not spread sufficiently.



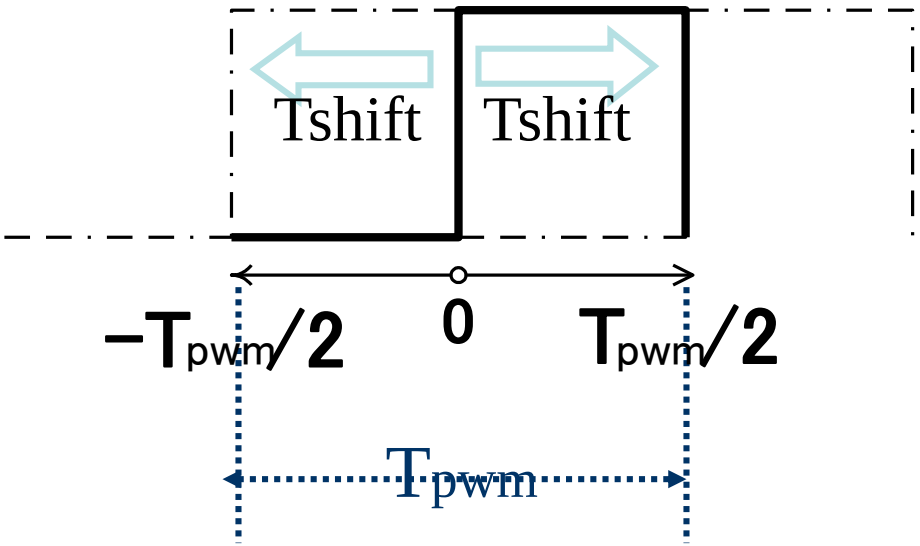
Optimal phase shift is obtained by measurement.

Optimal Clock Phase Shift(2)

Optimal value of maximum phase shift (T_{shift})

$$T_{shift} = \frac{T_{pwm}}{2}$$

T_{pwm}=PWM clock period



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FPGA Design

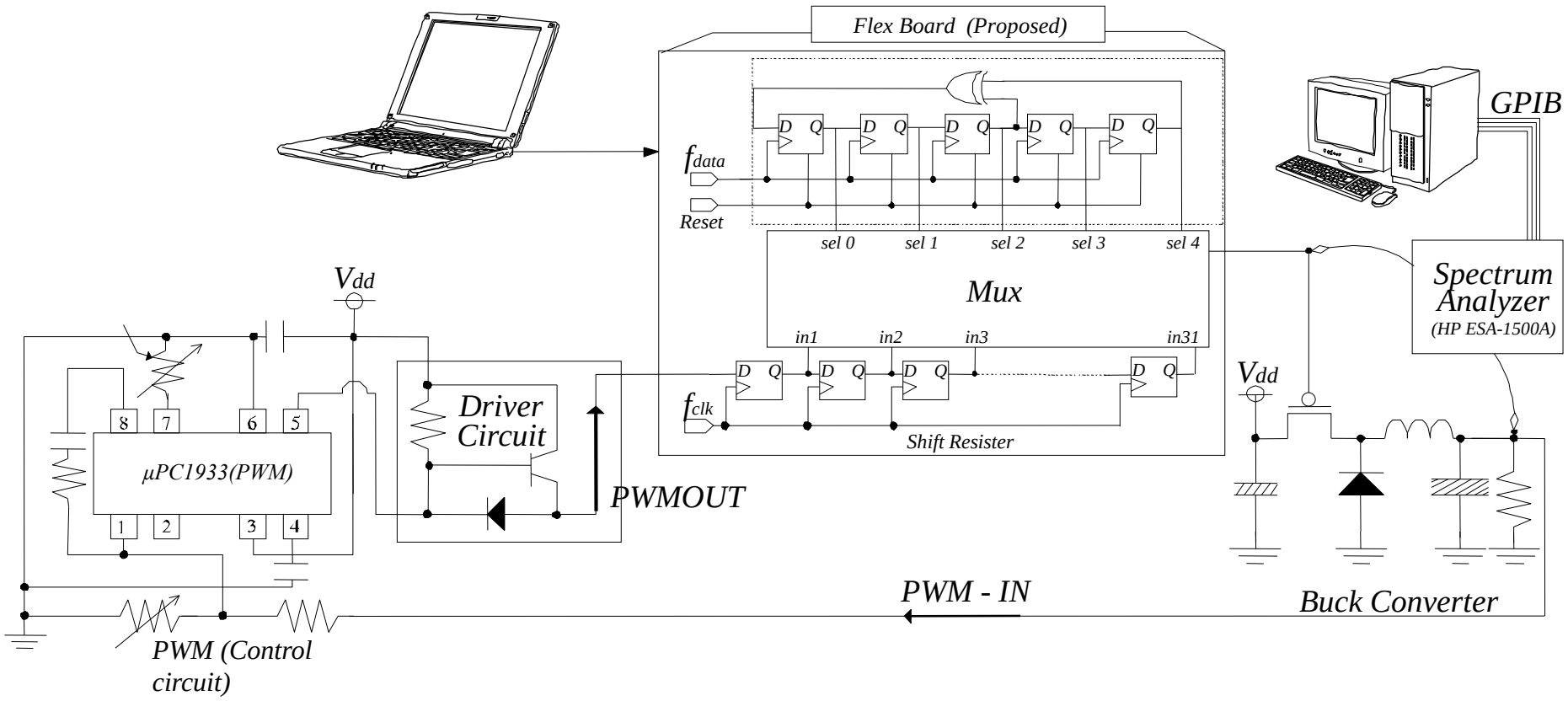
Evaluation Board

Technology:FLEX10K30EQC208 –3 (Altera)

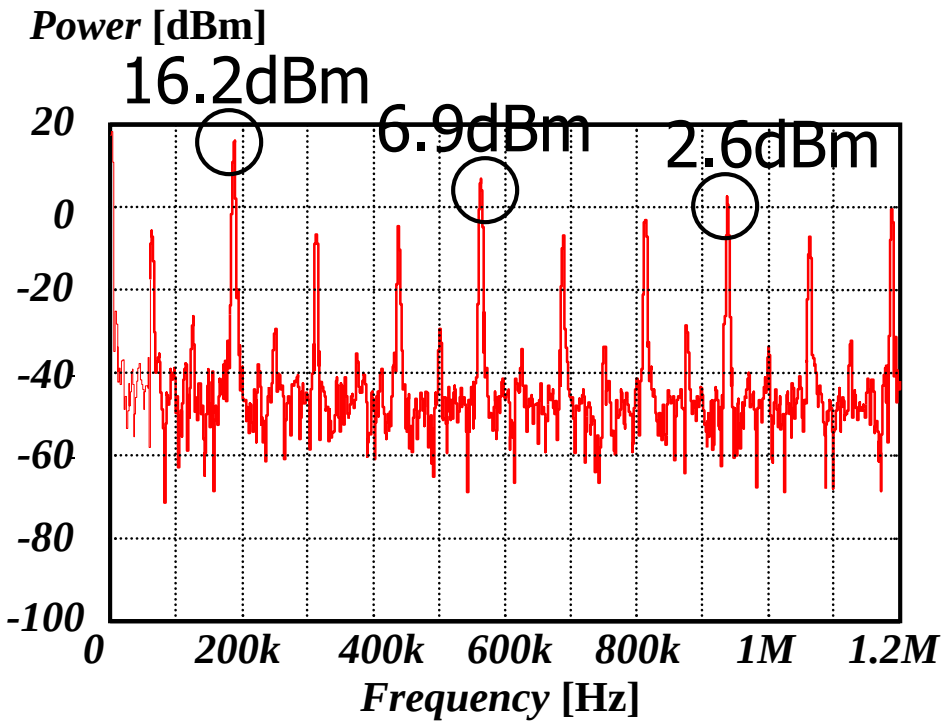
Design Item

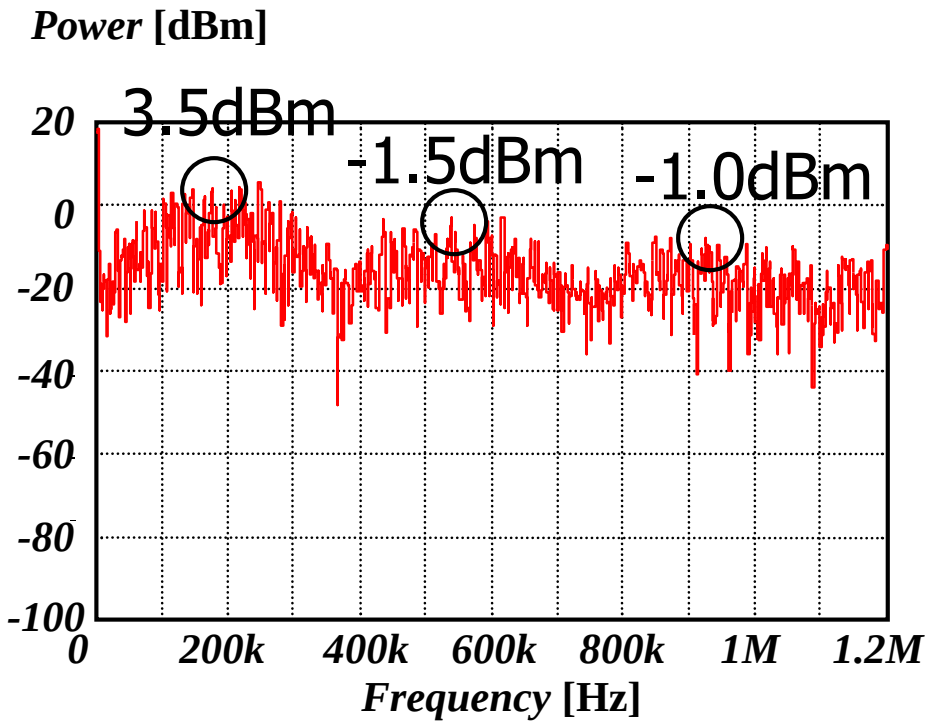
Item	Spec.
Spectrum Spread Method	Direct
Shift Register Clock	6MHz
PWM Input	187kHz
PN—code Control Clock	187kHz
Supply Voltage	3.3V
PN-code	M-Sequence
Code Length	31
The Number of DFFs	37

Measurement Setup



Measured Power Spectrum of Driving Clock





Power spectrum of normal clock

(Conventional)

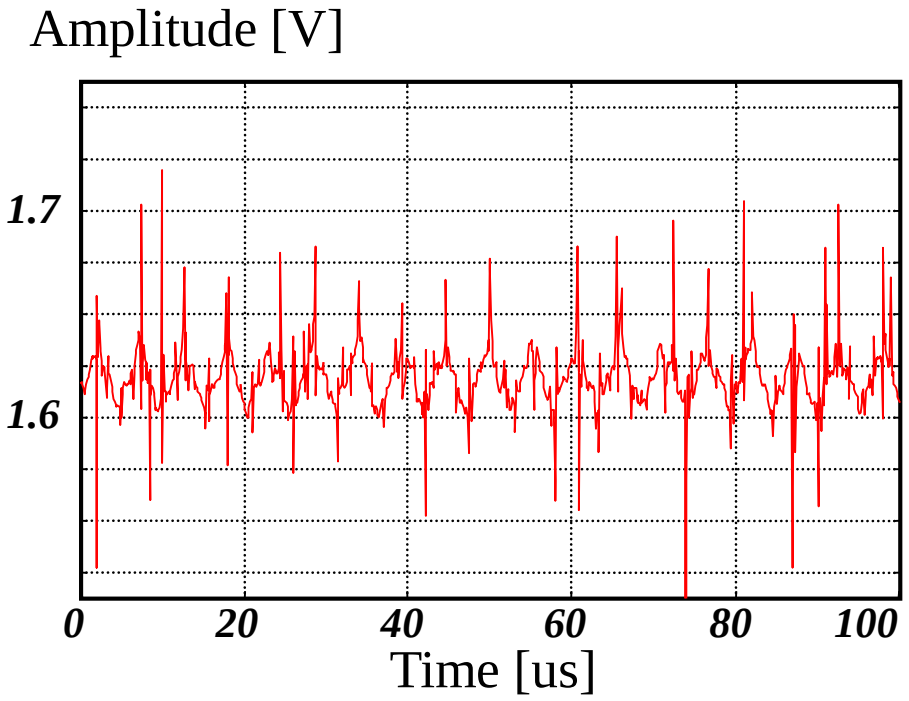
Power spectrum of PRM output clock with 5bit M-sequencer

(Proposed)

Maximum peak reduction by 12.7dBm

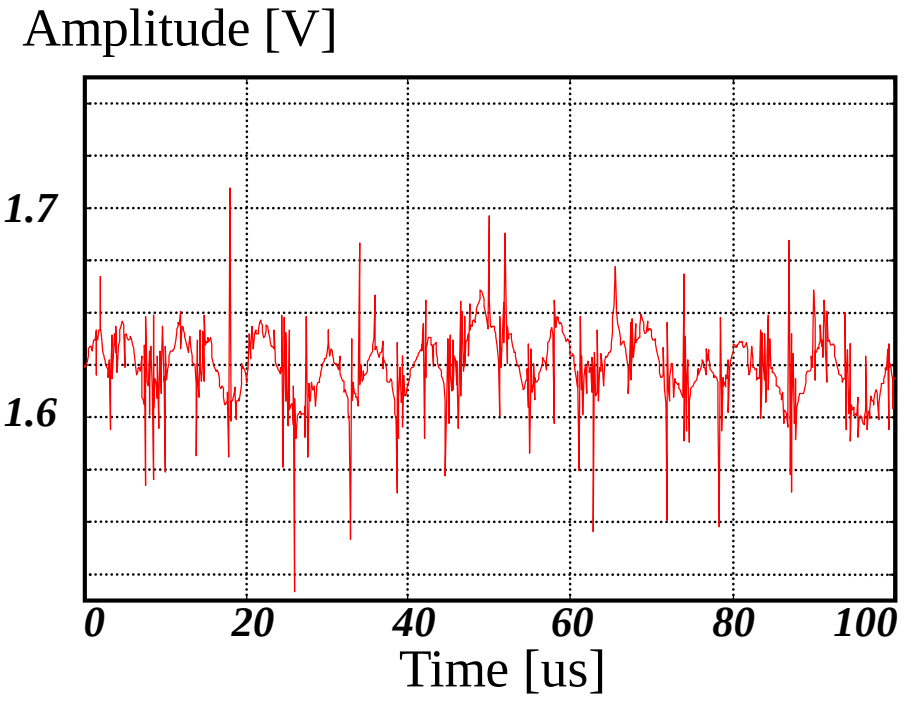
Measured Output Voltage Waveform of DC-DC Converter

Input voltage Vdd=3.3V, Clock duty = 50%



Output waveform with normal clock

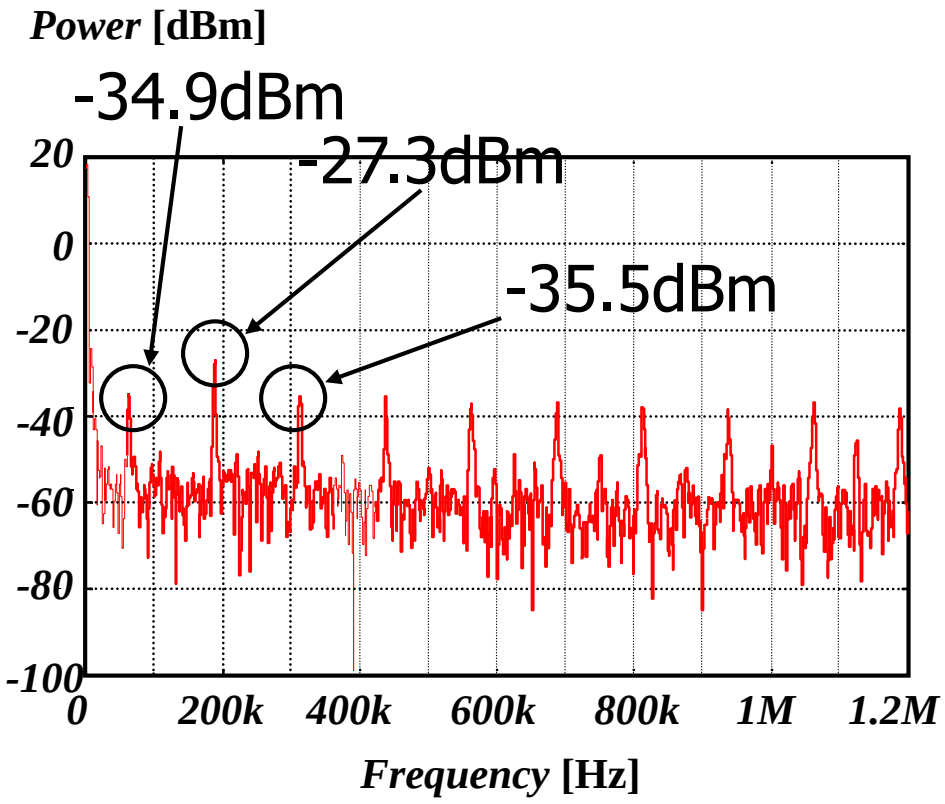
（Conventional)

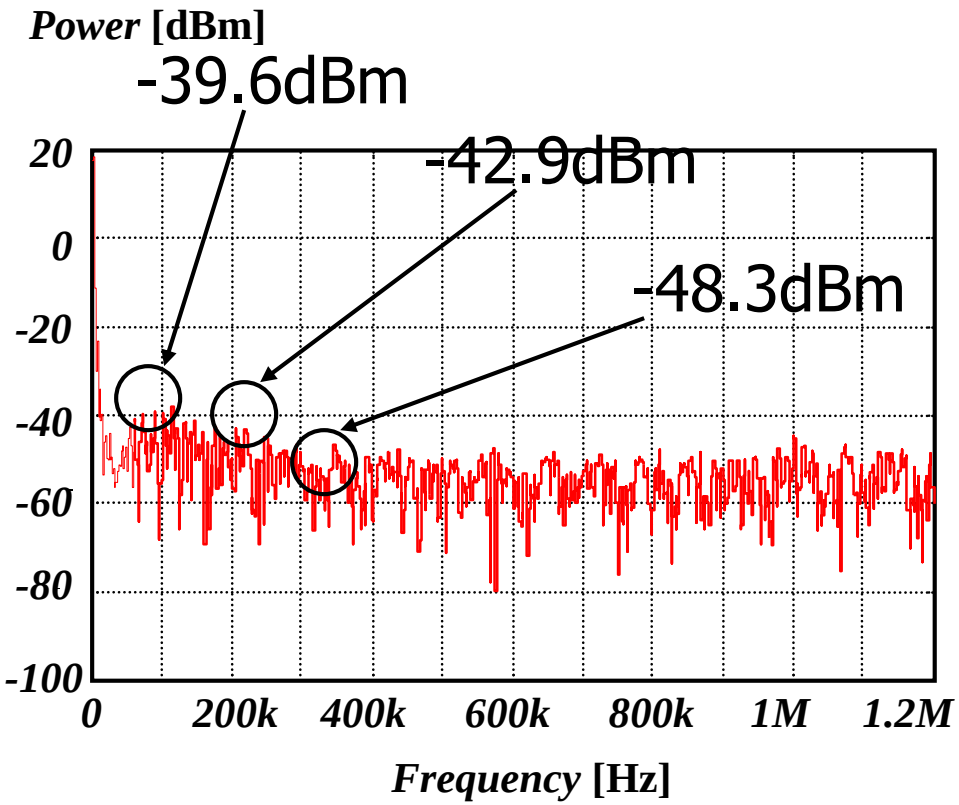


Output waveform with PRM clock.

(Proposed)

Measured Output Power Spectrum of DC-DC Converter



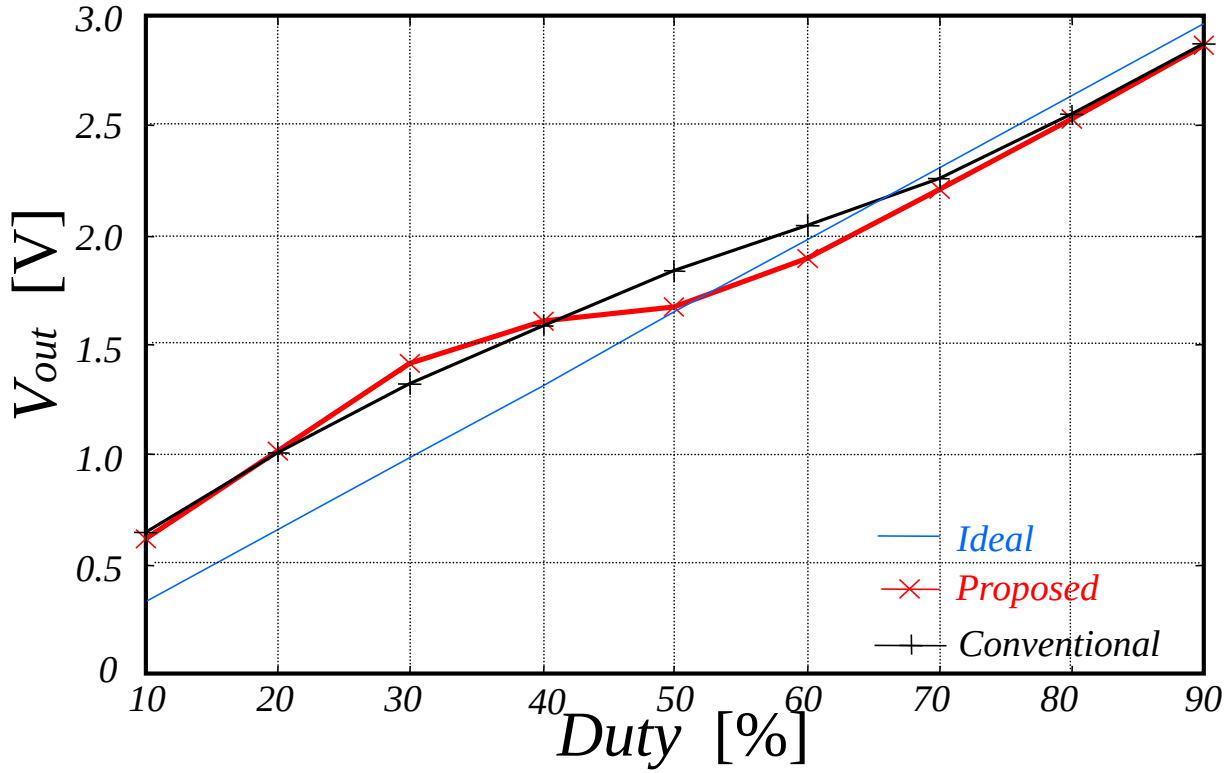


Output power spectrum with normal clock (Conventional)

Output power spectrum with PRM clock (Proposed)

Maximum peak reduction by 12．3dBm

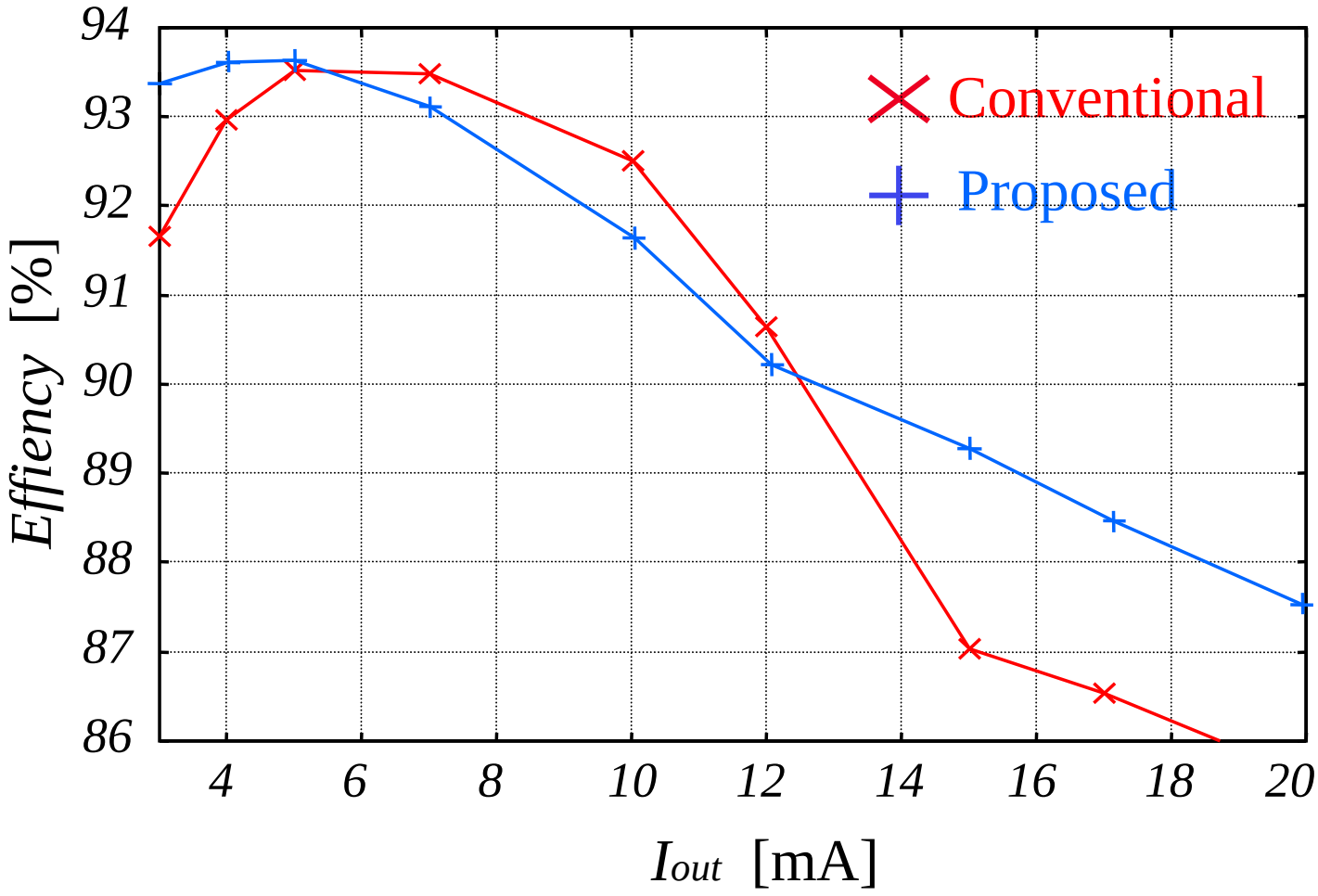
Clock Duty vs. Output Voltage



Match to the theoretical output voltage.

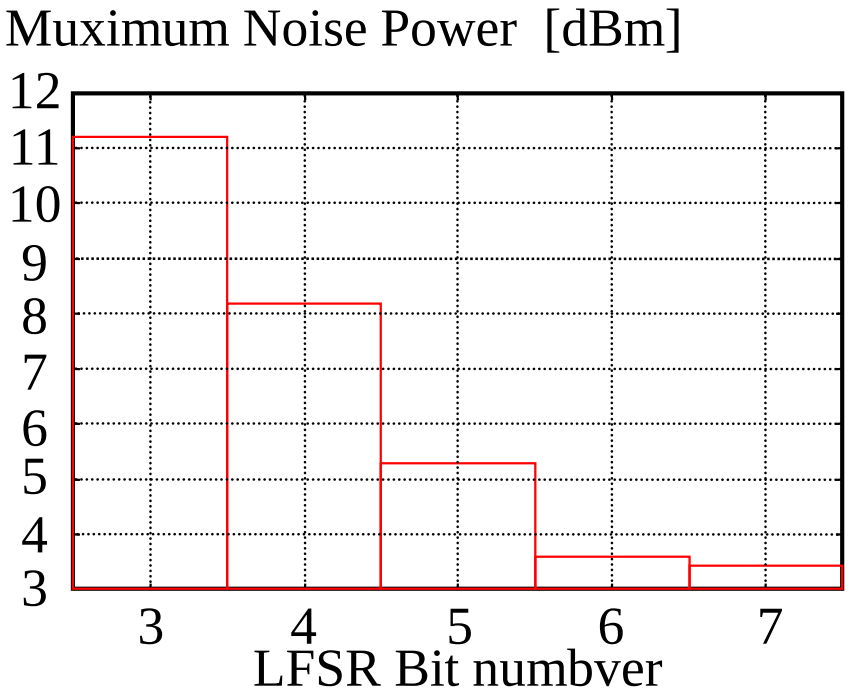
The proposed method does not affect the (average) output voltage.

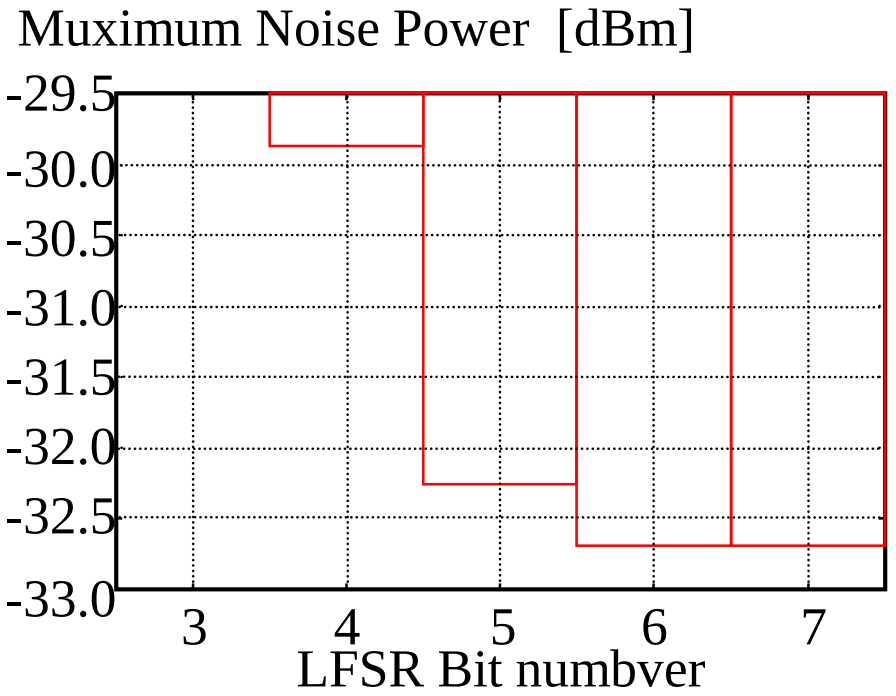
Efficiency vs. Output Current



The proposed method does not affect efficiency.

Peak Noise Power Spectrum vs. the Number of M-Sequencer Bits





Peak Noise Power Spectrum of Driving Clock

Peak Noise Power Spectrum of Switching Regulator Output

5-bit and 6-bit are reasonable trade-off.

Summary

- Proposal of Noise Power Spectrum Spread Technique
  - Addition of simple digital circuitry can realize EMI reduction.
    - Low cost, Low power
      - Robust against temperature variation, aging
  - No need for modification of the other parts.
  - Applicable also for voltage-boosting converter.

- Implementation with FPGA
- Confirmation of its effectiveness by measurements

Reduction by

Max. Peak	**12.3dBm**
Fundamental	**5.7dBm**
2nd-harmonics	**15.6dBm**
3rd-harmonics	**12.8dBm**