SEMICON® JAPAN

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Challenge for Analog Circuit Testing in Mixed-Signal SoC

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Contents

1. Introduction

Cost and Quality for Test Cost

- Analog portion continues to be difficult part of SoC test.
- Concept of “cost” and “quality” makes “issues and challenges of analog circuit testing in mixed-signal SoC” clear and logical.
- LSI testing technology reduces cost and improves quality simultaneously.

2. Review of Analog Circuit Testing in Mixed-Signal SoC

Management Strategy

- Strategy 1 :

  Use low cost ATE and develop analog BIST/BOST to make testing cost lower.

- Strategy 2 :

  Use high-end mixed-signal ATE as well as its associated services & know how.
  Fast time-to-market & no BIST can make profits much more than testing cost.

Save or Earn

ATE: Automatic Test Equipment

BIST: Built-In Self-Test, BOST: Built-Out Self-Testy

Low Cost Testing

Ideal : No testing

- Design guarantee
- 100% chips work well

Reality :

- Low cost ATE
- Short testing time
- Multi-site testing
- Minimum or no chip area penalty for BIST
- Extensive usage of BOST

A penny saved is a penny earned.

Test and Measurement are different

- Production Test : 100% Engineering

  Decision of “Go” or “No Go”

  For example, it can be performance comparison between DUT and “Golden Device”.

  - LSI testing is manufacturing engineering.

- Measurement : 50% Science, 50% Engineering

  Accurate performance evaluation of circuit

Measurement can be costly, but testing should be at low cost.

DUT: Device Under Test

Analog BIST

- BIST for digital : Successful
  BIST for analog : Not very successful
  ➡ Challenging research
- Digital test : Functionality ➡ Easy
  Analog test : Functionality & Quality ➡ Hard

Analog: parametric fault as well as fatal fault.

Prof. A. Chatterjee
Specification-based Test Alternative Test Defect-based Test

- In many cases
  - Analog BIST depends on circuit.
  - No general method like scan path in digital.
  - One BIST, for one parameter testing

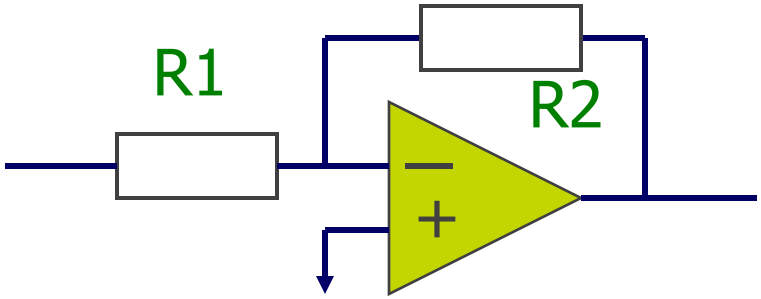
RF / High-Speed IO / Power Device Testing

- RF / HSIO / Power testing is different from analog testing technology.
- These testing technologies are other challenging areas.
- RF testing items examples:
  - EVM test
    - System level testing, GSM/EDGE
    - AM/PM distortion
    - Jitter, Phase noise

Robust Design and Testing

Robust design makes its testing difficult.

- Feedback suppresses parameter variation effects.



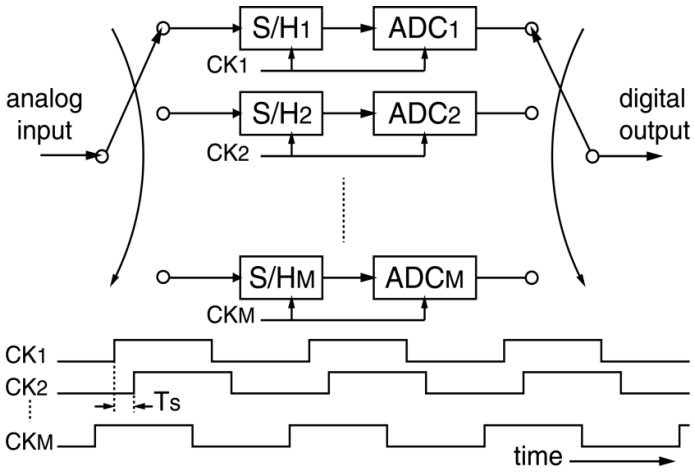
- Self-calibration and redundancy hide defects in DUT.
- Secure DUT is difficult to test.

Robust design (yield enhancement) and testing cost reduction are trade-off.

ATE for Mixed-Signal Testing

- Analog part is costly for development.
- Analog BIST is also beneficial
  for mixed-signal ATE manufacturer
- ATE must be designed with today's technology for tomorrow's higher performance chip testing.

Interleaved ADC used in ATE
to realize very high sampling rate
with today's ADCs



Low Cost ATE

- Digital ATE
  - No analog option such as
    Arbitrary Waveform Generator: AWG
  - Input/output are mainly digital.
- Replacement of analog ATE with digital ATE
  - Multi-site testing becomes possible.
  - Still short testing time is important.
- Secondhand ATE, In-house ATE
- ATE with well balanced modular hardware and software

Cooperation among Engineers

- Collaboration is important
  - Circuit designer
  - LSI testing engineer
  - ATE manufacturer engineer
  - Management
  - LSI testing researcher in academia
- Strong background of analog circuit design as well as LSI testing are required for analog testing research.

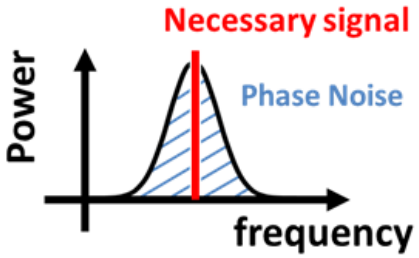
Collaboration with Socionext Inc., STARC and other related industries

3. Research Topics

Phase Noise Test with ΔΣ TDC

BOST solution

Phase noise in oscillator



Malfunction of electronic systems

- RF circuit & system
- ADC

Important

Phase noise test at low cost, in short time

Conventional

- Expensive : Spectrum analyzer
- Long : test time (~10seconds)

cost high

Proposed

Simple circuit

ΔΣ Time-to-Digital Converter

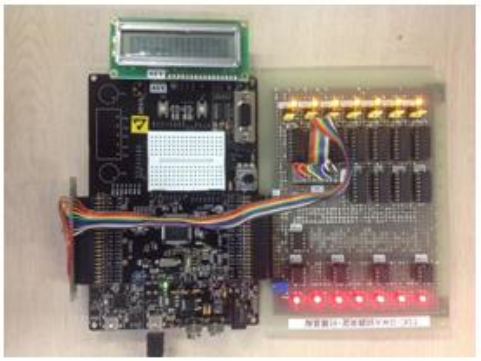
Low cost, high quality Phase noise test

[1] Y. Osawa, H. Kobayashi, "Phase Noise Measurement Techniques Using Delta-Sigma TDC", IEEE International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW'14), Porto Alegre, Brazil (Sept. 17-19, 2014).

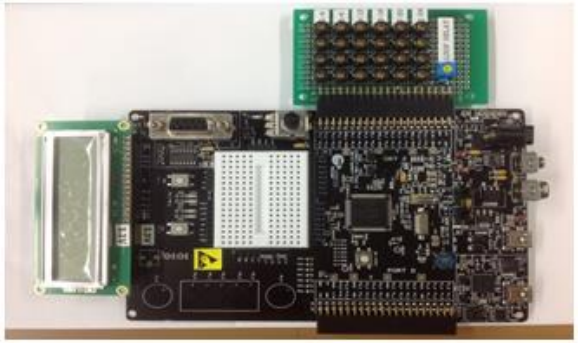
TDC BOSTs for Timing Signal Testing

BOST solution

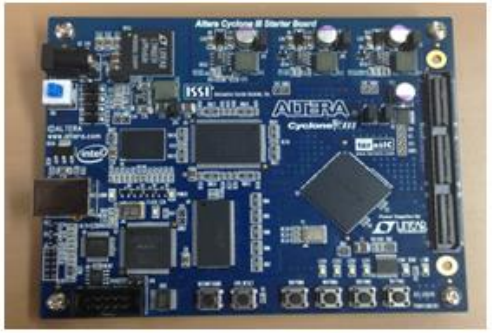
Single-bit ΔΣ TDC with analog FPGA



Multi-bit ΔΣ TDC with analog FPGA



Flash-type TDC with analog FPGA

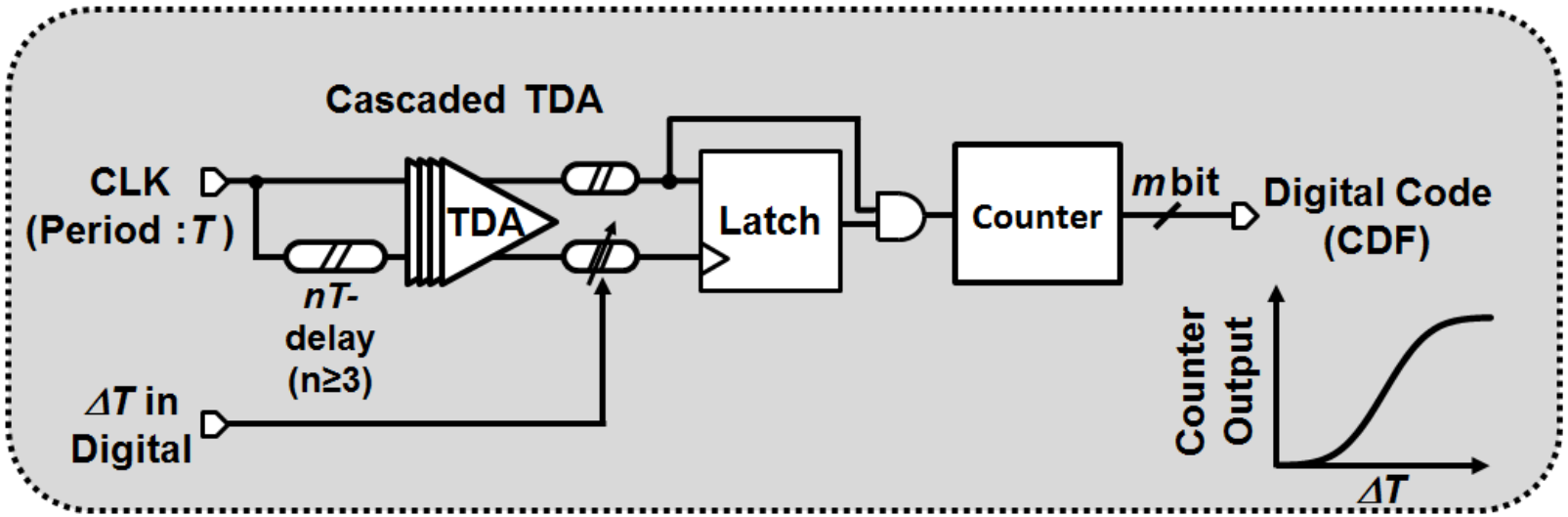


Flash-type TDC with digital FPGA

[2] R. Jiang, H. Kobayashi, Y. Ozawa, R. Shiota, K. Hatayama, et. al.,
"Successive Approximation Time-to-Digital Converter with Vernier-level Resolution",
IEEE International Mixed-Signal Testing Workshop, Catalunya, Spain (July 4-6, 2016).

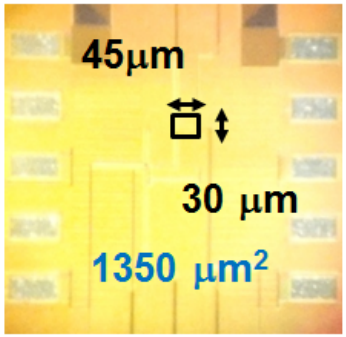
BIST solution

On-chip Jitter Measurement Circuit



Experiments show that
1.67 ps RMS timing jitter
can be measured

Process : 65 nm CMOS
Supply Voltage : 1.2 V

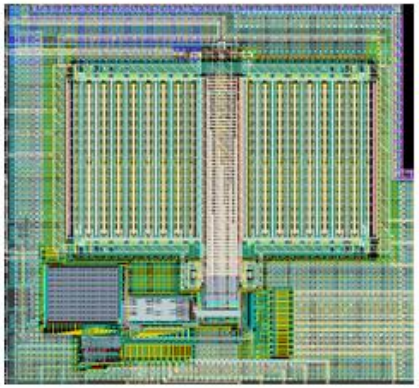


[3] K. Niitsu, H. Kobayashi , "CMOS Circuits to Measure Timing Jitter Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier with Duty-Cycle Compensation," IEEE Journal of Solid-State Circuits, Nov. 2012.

DFT for SAR ADC Linearity

BIST Solution

A high-resolution, low-sampling-rate ADC requires a long testing time for its linearity.



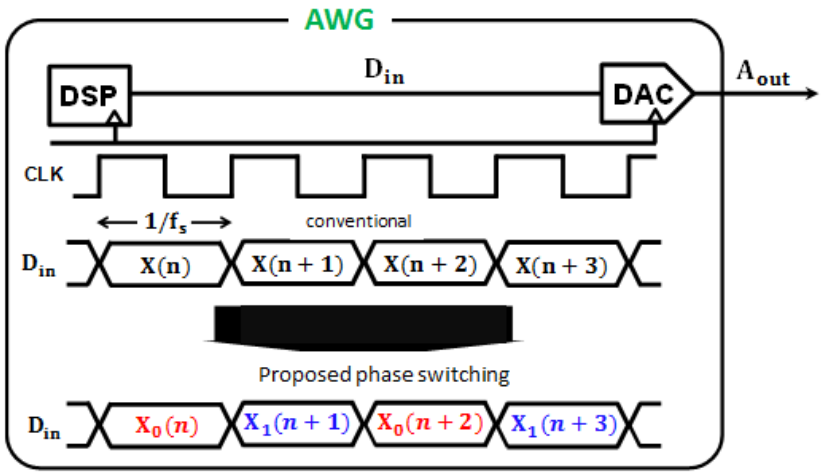
Shorten SAR ADC linearity test time.

10bit SAR ADC
TSMC 180nm
1.2×1.2mm^2

[4] T. Ogawa, H. Kobayashi,
"Design for Testability That Reduces Linearity Testing Time of SAR ADCs",
IEICE Trans. on Electronics (June 2011).

Low Cost ATE

Low IMD3 2-Tone Signal Generation with AWG for Communication Application ADC Testing

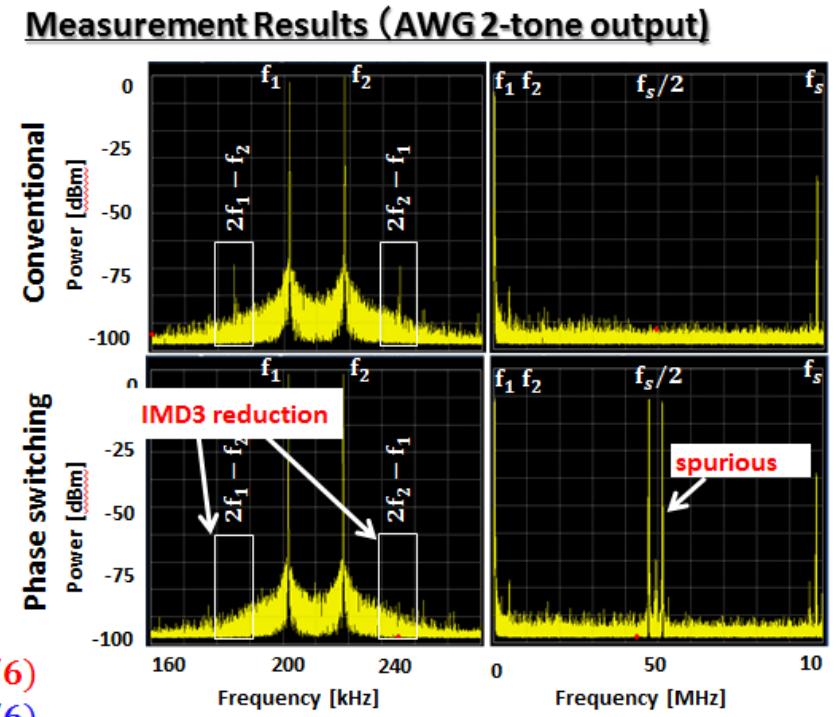


Conventional

$$X(n) = A\cos(2\pi f_1 n T_s) + A\cos(2\pi f_2 n T_s)$$

Proposed phase switching

$$X_0(n) = B\cos(2\pi f_1 n T_s + \pi/6) + B\cos(2\pi f_2 n T_s - \pi/6)$$
$$X_1(n) = B\cos(2\pi f_1 n T_s - \pi/6) + B\cos(2\pi f_2 n T_s + \pi/6)$$



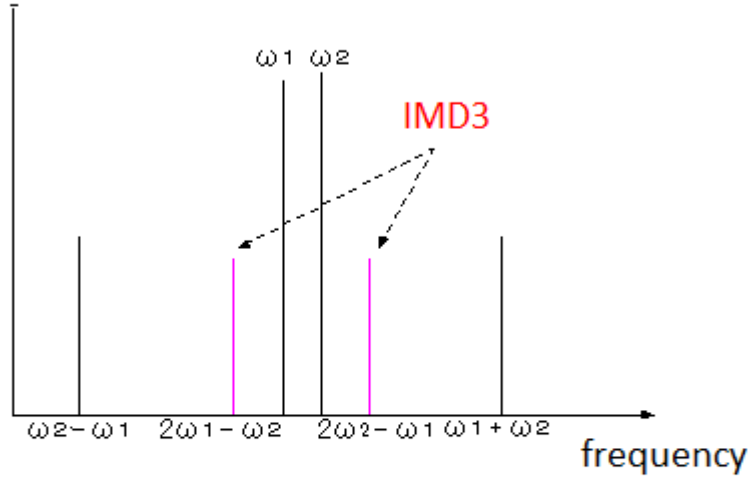
[5] K. Kato, H. Kobayashi,
"Two-Tone Signal Generation for Communication Application ADC Testing",
The 21st IEEE Asian Test Symposium, Niigata, Japan (Nov. 2012).

Algorithm

Multi-tone Curve Fitting Algorithm for Communication Application ADC

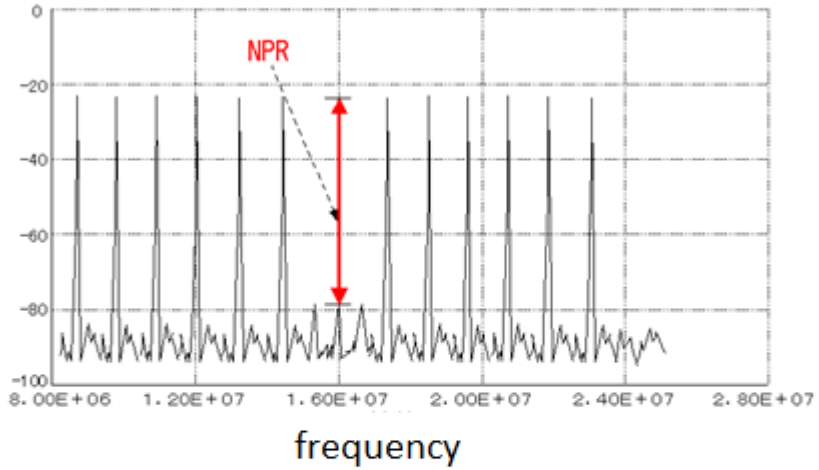
2-tone

Power spectrum



Multi-tone

Power spectrum



No need for expensive instruments

Noise Power Ratio: NPR

ADSL application ADC testing

[6] Y. Motoki, H. Kobayashi,
``Multi-Tone Curve Fitting Algorithms for Communication Application ADC Testing'',
Electronics and Communication in Japan: Part 2, Wiley Periodicals Inc. (2003).

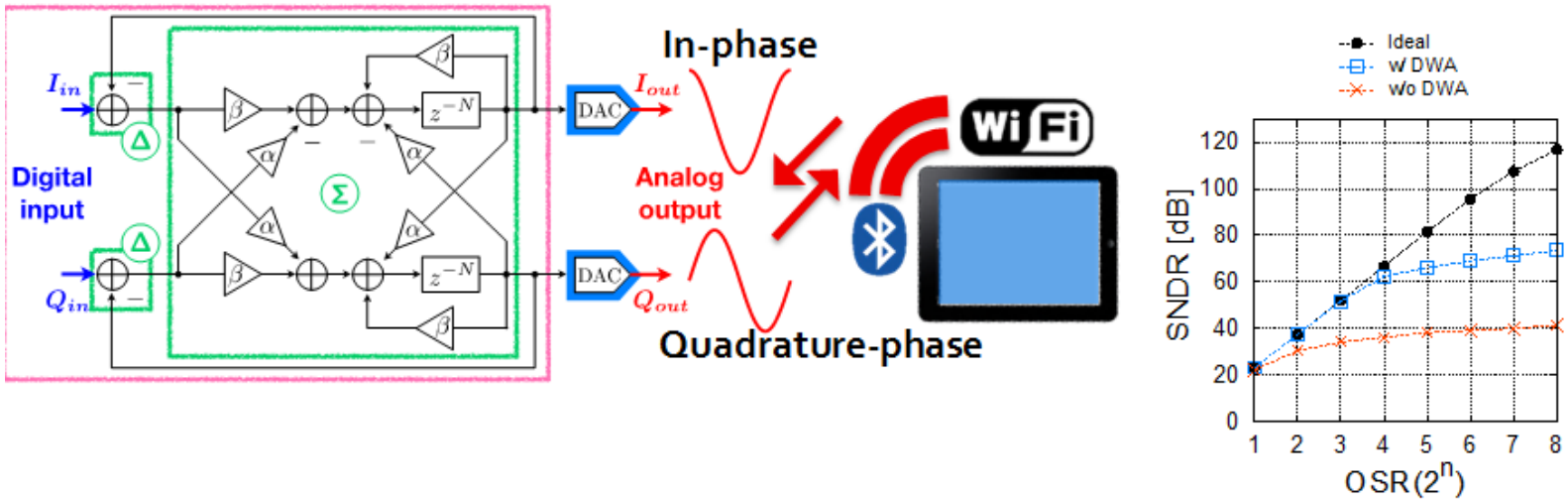
Complex Multi-Bandpass ΔΣ Modulator for I-Q Signal Generation

ATE for Mixed-Signal Testing

- Generation of high quality analog I-Q signals
- Testing of communication application ICs
- Digital rich

(Suitable to the realization with nano CMOS → Low cost)

ΔΣ modulation | Complex signal processing | Non-linear correction algorithm for Multi-bit DAC



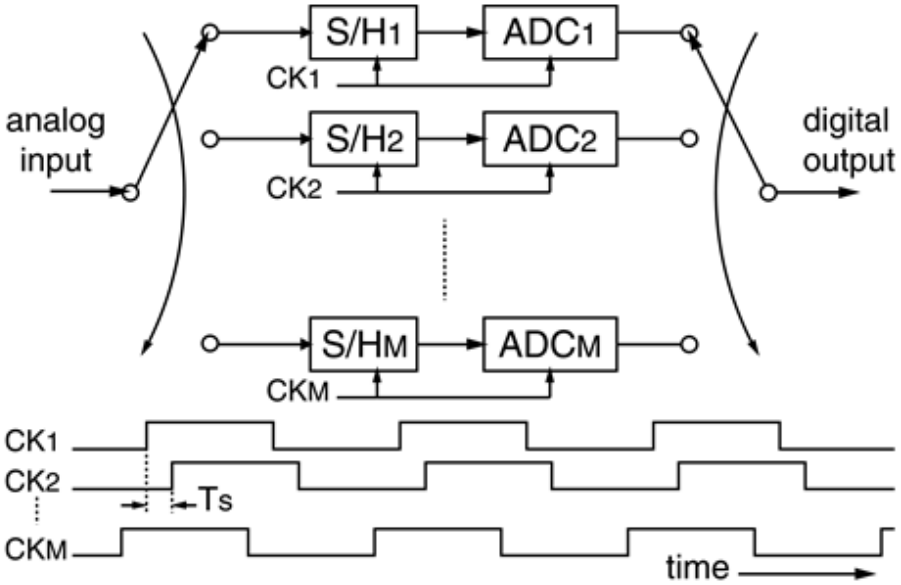
[7] M. Murakami, H. Kobayashi, " I-Q Signal Generation Techniques for Communication IC Testing and ATE Systems", IEEE International Test Conference,(Nov. 2016).

Time Interleaved ADC in ATE System

ATE for Mixed-Signal Testing

Channel ADC mismatch compensation

Cost effective high-speed ADC



[8] N. Kurosawa, H. Kobayashi,
``Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems",
IEEE Trans. on Circuits and Systems I (March 2001).

[9] R. Yi, H. Kobayashi,
Digital Compensation for Timing Mismatches in Interleaved ADCs",
IEEE 22nd Asian Test Symposium, Yilan, Taiwan, (Nov. 2013)

[10] K. Asami, H. Kobayashi, "Timing Skew Compensation Technique using Digital Filter with Novel Linear Phase Condition,"
IEEE International Test Conference, Austin (Nov. 2010).

4. Challenges & Conclusion

Challenges of Analog Testing

- Use all aspects of technologies
  - Circuit technique
  - Cooperation among BIST, BOST & ATE
    as well as software & network
  - Signal processing algorithm
  - Use resources in SOC
    such as μP core, memory, ADC/DAC

There is no science without measurement.

There is no production without test

No royal road to analog testing

Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems

N.Kurosawa, K.Maruyama, H.Kobayashi,

H.Sugawara and K.Kobayashi y

Gunma University, Japan y Teratec Corp. Japan

発表内容

1. 研究の目的
2. インターリーブADCの原理と問題点
3. ミスマッチが独立して存在する場合の影響
4. ミスマッチが同時に存在する場合の影響
5. 帯域ミスマッチの影響
6. まとめ

1.研究の目的

研究の目的

インターリーブ・アーキテクチャを用いて
最高速のADCを実現する場合の、
システム上の問題の理論解析を行う。

2.インターリーブADCの原理と問題点

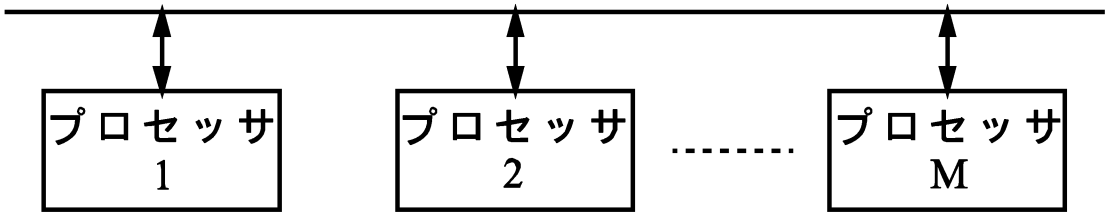
高速・高精度ADCの構成

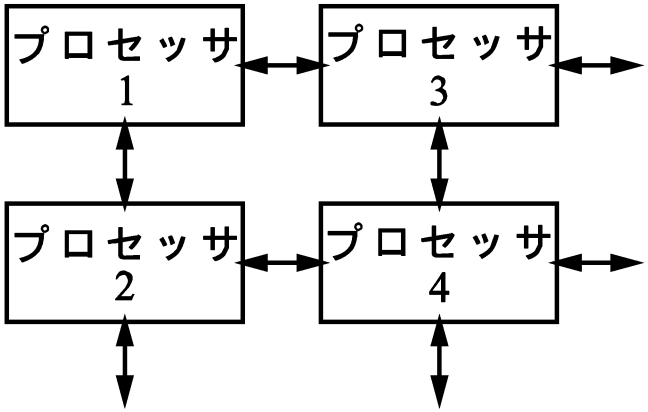
- 高速ADCの構成
  - 大部分の回路が比較的低い周波数のクロックで動作
  - 周波数の高い信号の発生が不要
  - 周波数の高い信号が不要
  - タイミングの問題が少ない(例:タイミングスキュー)
- 高精度ADCの構成
  - 高精度回路が不要
  - 大きなプロセス変動を許容
  - 低ノイズ回路・デバイスが不要

  例: デルタ・シグマADC
    - サブミクロンCMOSのアナログCMOS回路
    - 高精度回路が不要
    - 低ノイズ回路が不要

マルチプロセッサ構成

- デジタルの世界では、マルチプロセッサ構成は非常に一般的
  - 多くの低性能プロセッサ
  - 高性能を実現

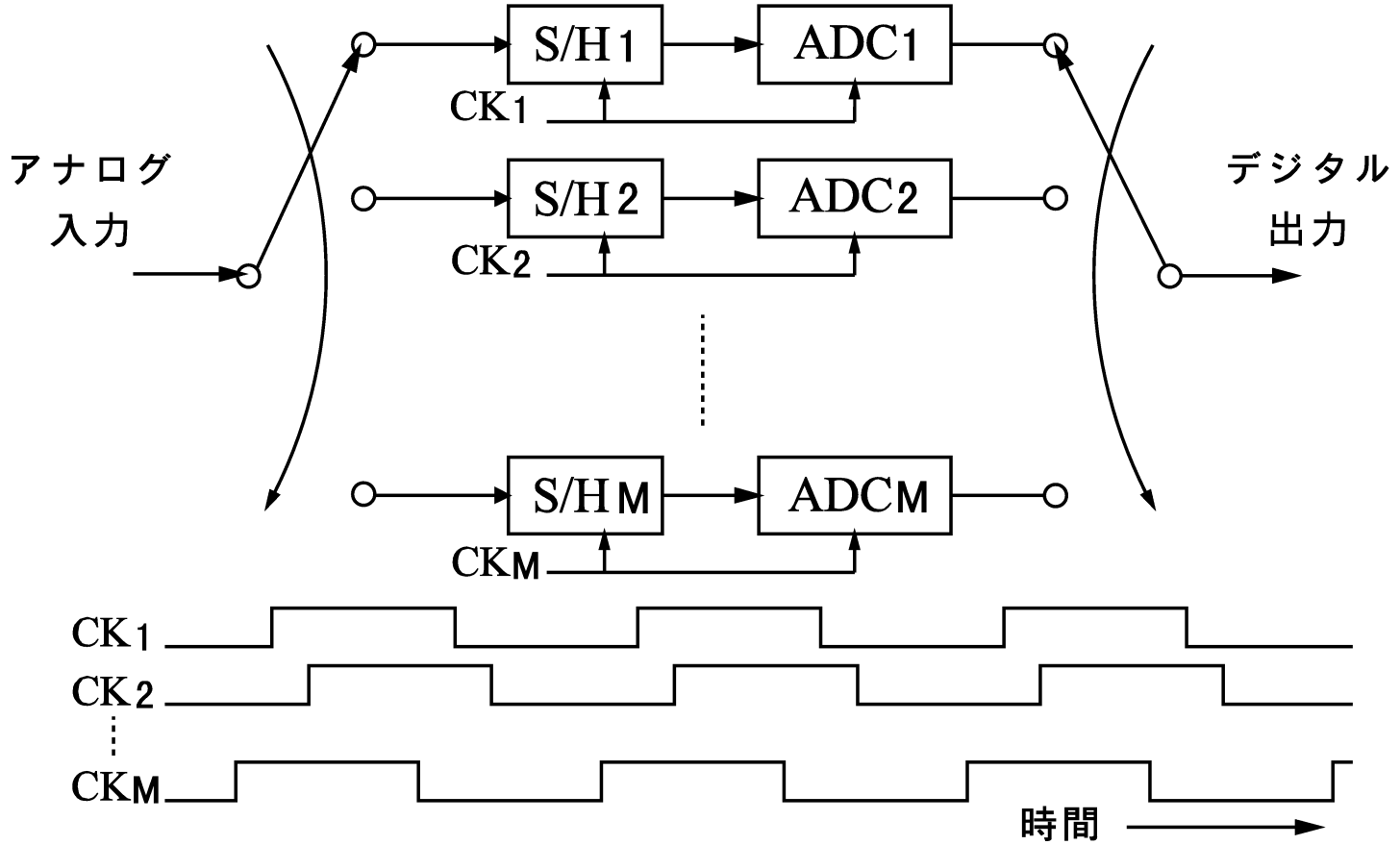




- 問題点
  - ソフトウエア開発の負担が重い
  - マルチプロセッサの性能 ¿ プロセッサ１個の M 倍の性能
    M ：プロセッサ数

インターリーブADCの原理と問題点

- M 個のADCのインターリーブで M 倍のサンプリングレートを実現
  - ± マルチプロセッサ構成の観点から、非常に効果的
  - ± サンプリングレートの高いADCに適している



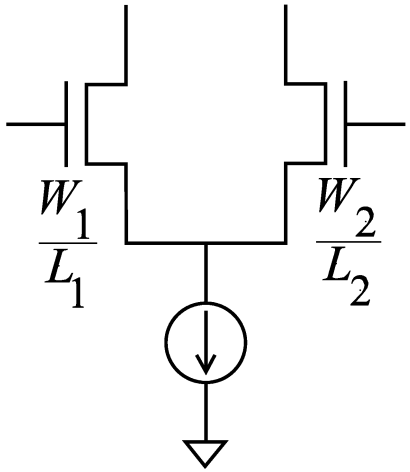
- チャネル間ミスマッチによってS/Nが低下
  通常キャリブレーションが必要

アナログ回路システムのミスマッチ

- **回路レベルのミスマッチ**

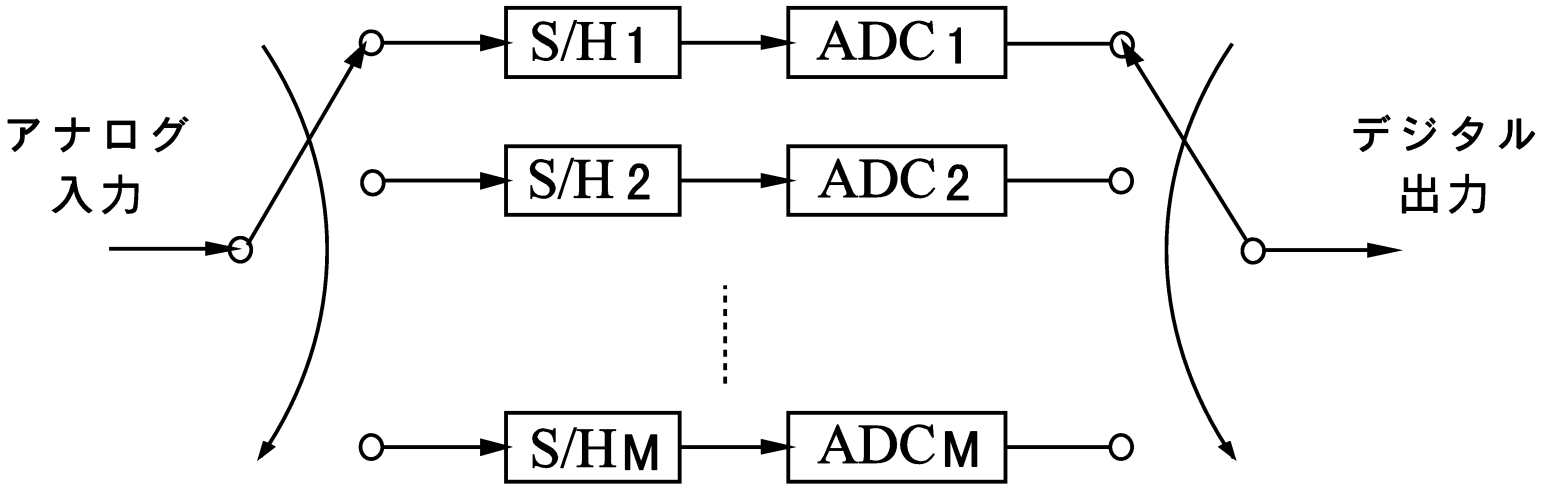
  例: 差動ペアのオフセット V_{os}

$$(V_{os})_{rms} = \frac{1}{WL}$$



- **システムレベルのミスマッチ**

  例: インターリーブ ADC **のチャネル間のミスマッチ**



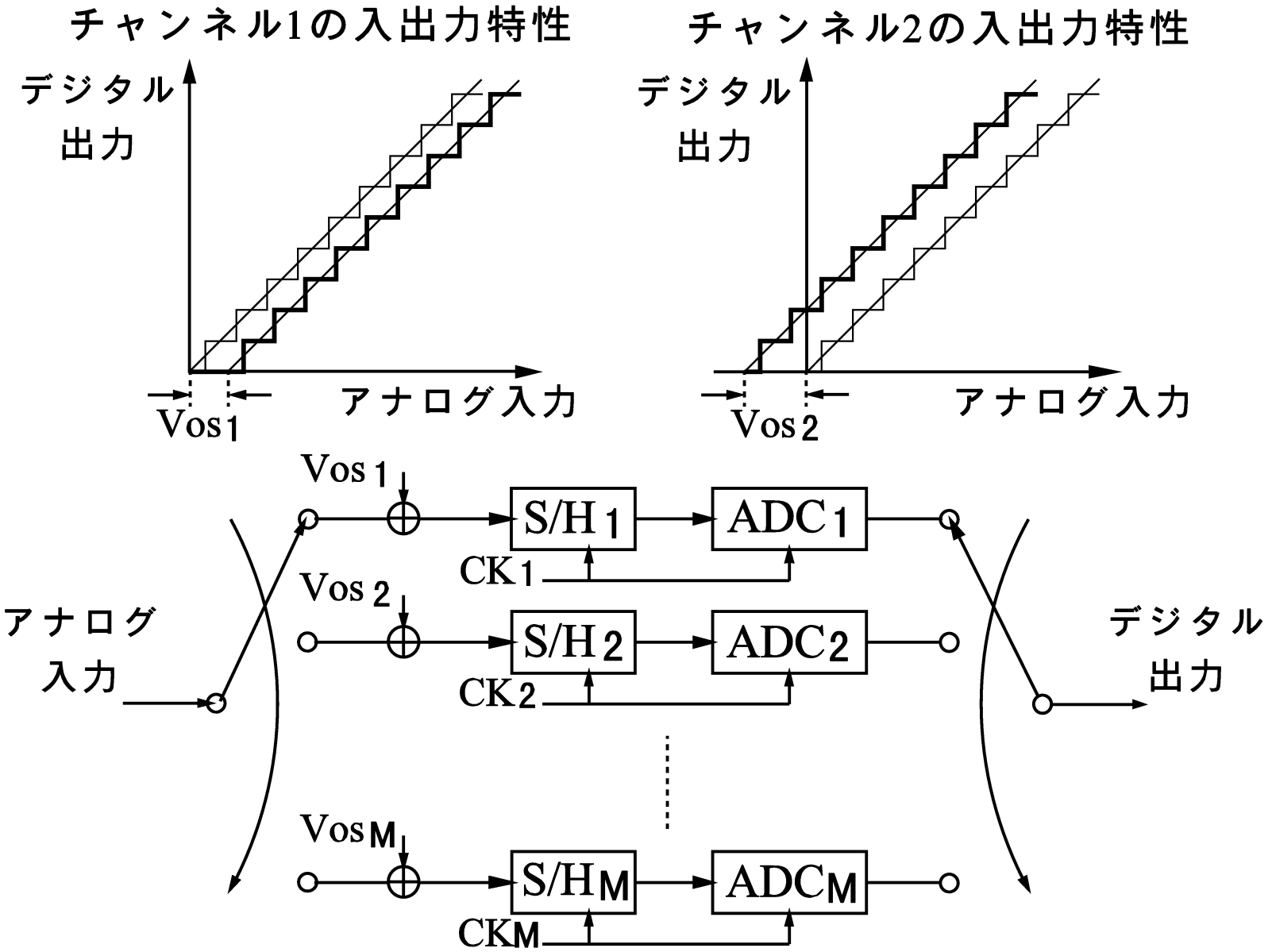
3. ミスマッチが独立して

存在する場合の影響

チャネル間ミスマッチの影響

- オフセットミスマッチの影響

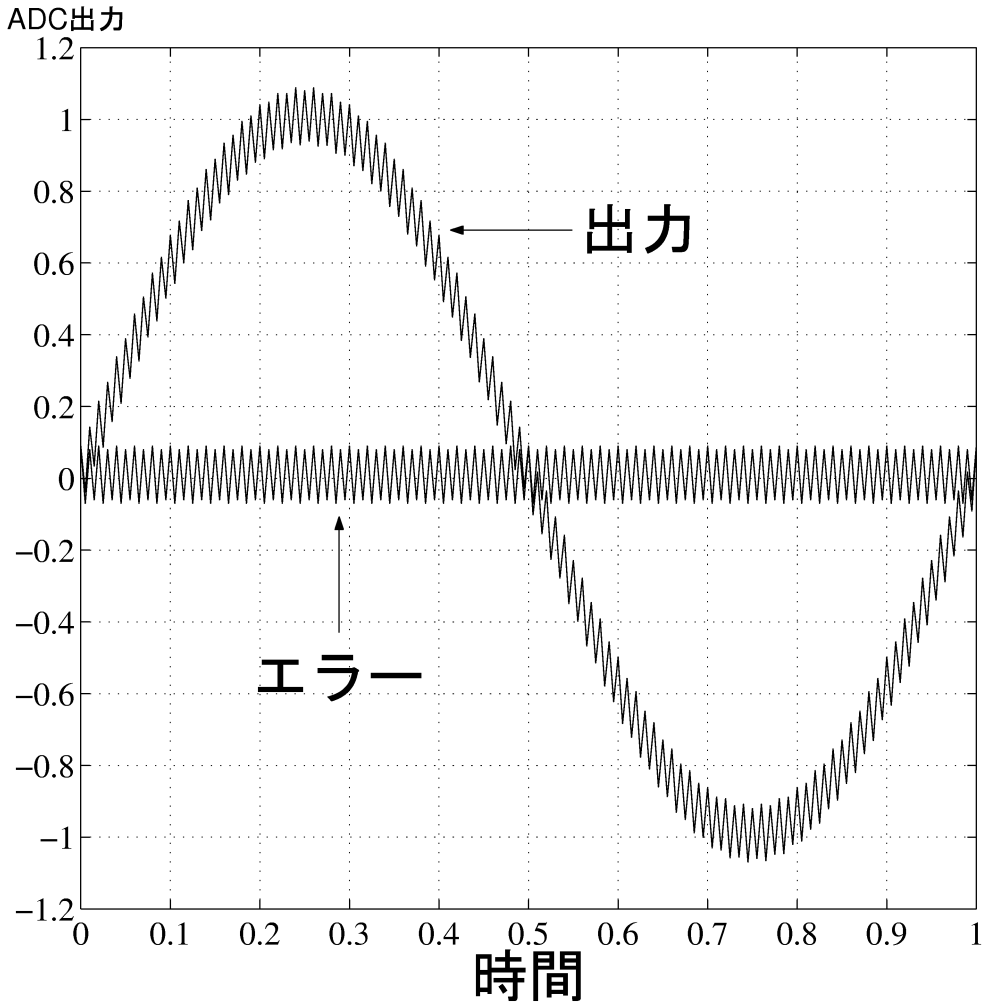
オフセットミスマッチのモデル



オフセットミスマッチの時間領域での影響

- パターンノイズ
  - ほぼ入力周波数と独立
  - 加算的ノイズ
  - f_S=M 周期
    - f_S : サンプリング周波数
    - M : チャンネル数
- 4チャンネルADCのシミュレーション
  - 正弦波入力

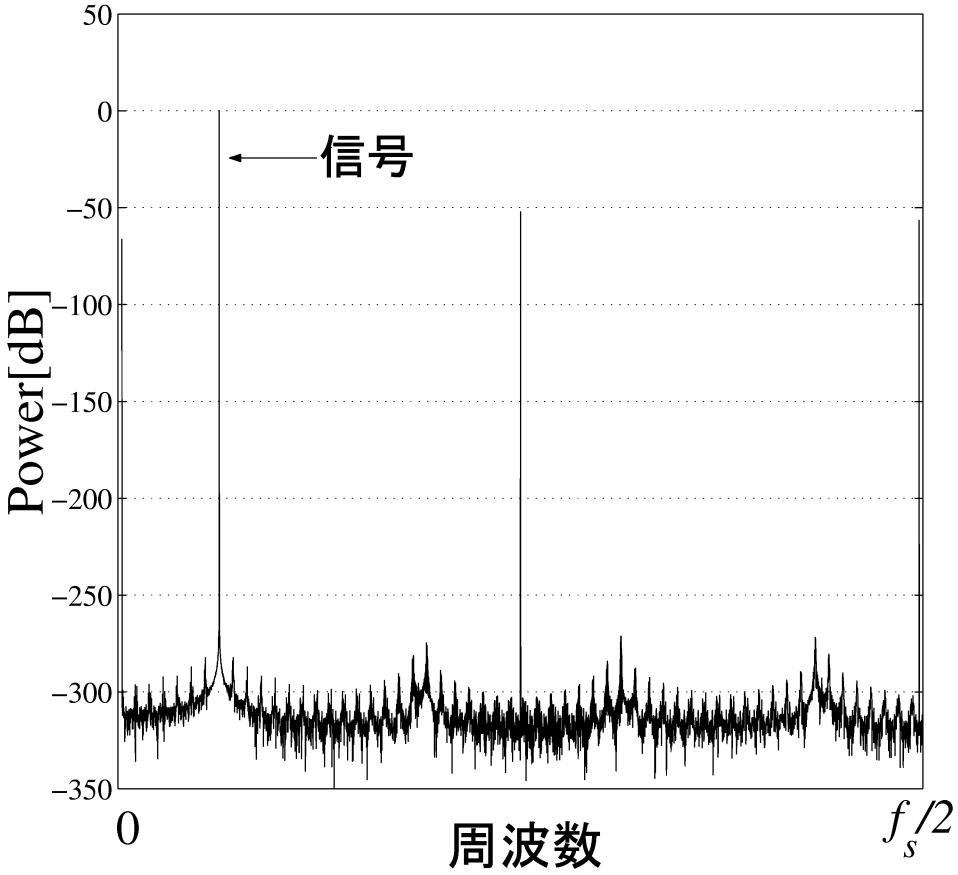
ADCシステムの出力とエラー



オフセットミスマッチの周波数領域での影響

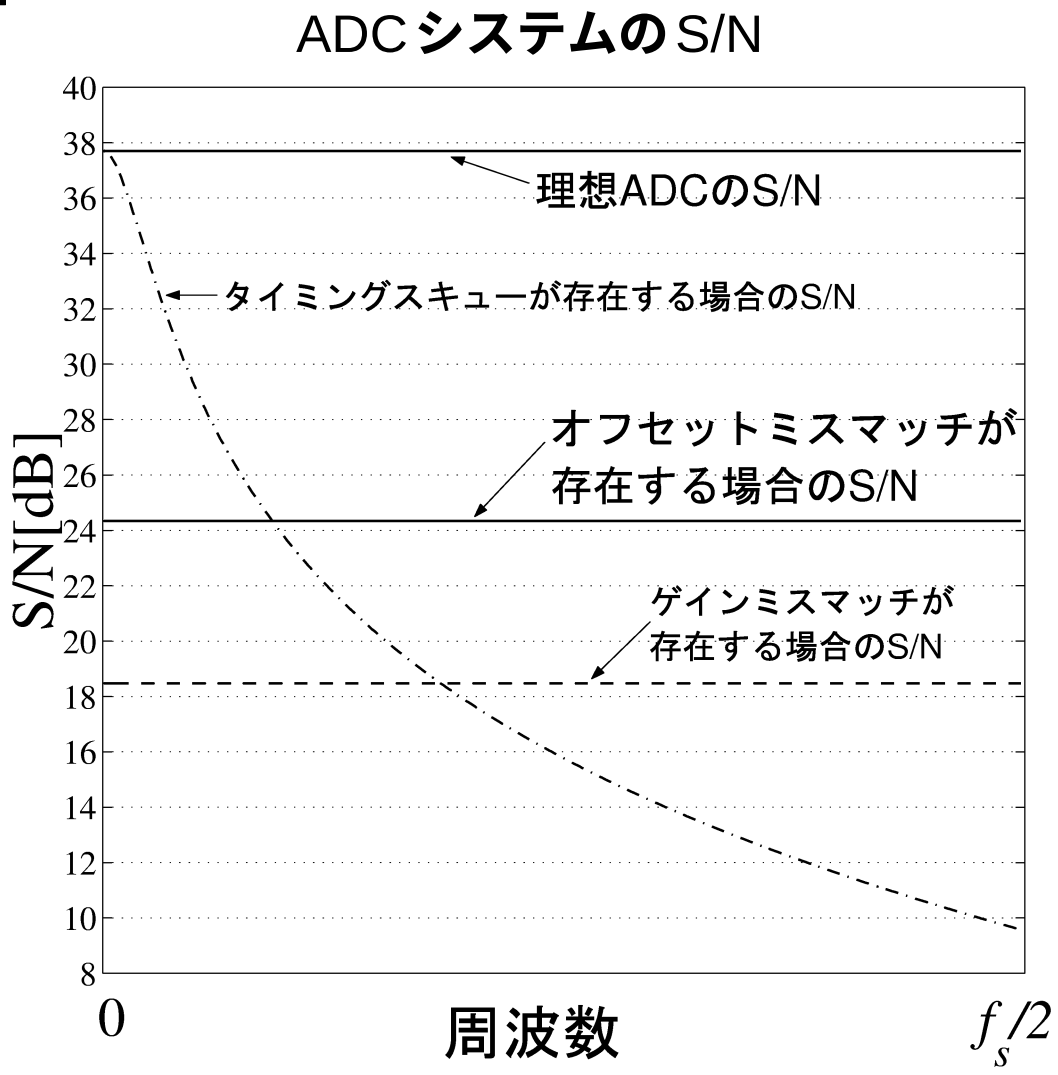
- パターンノイズの周波数
  - $\pm f_{noise} = k \times f_s / M$
    $k = 1; 2; 3; \cdots$
    f_s : サンプリング周波数
    M : チャンネル数
- 4チャンネルADCのシミュレーション
  - ± 8192点FFT

ADC出力のパワースペクトラム



オフセットミスマッチのS/Nへの影響

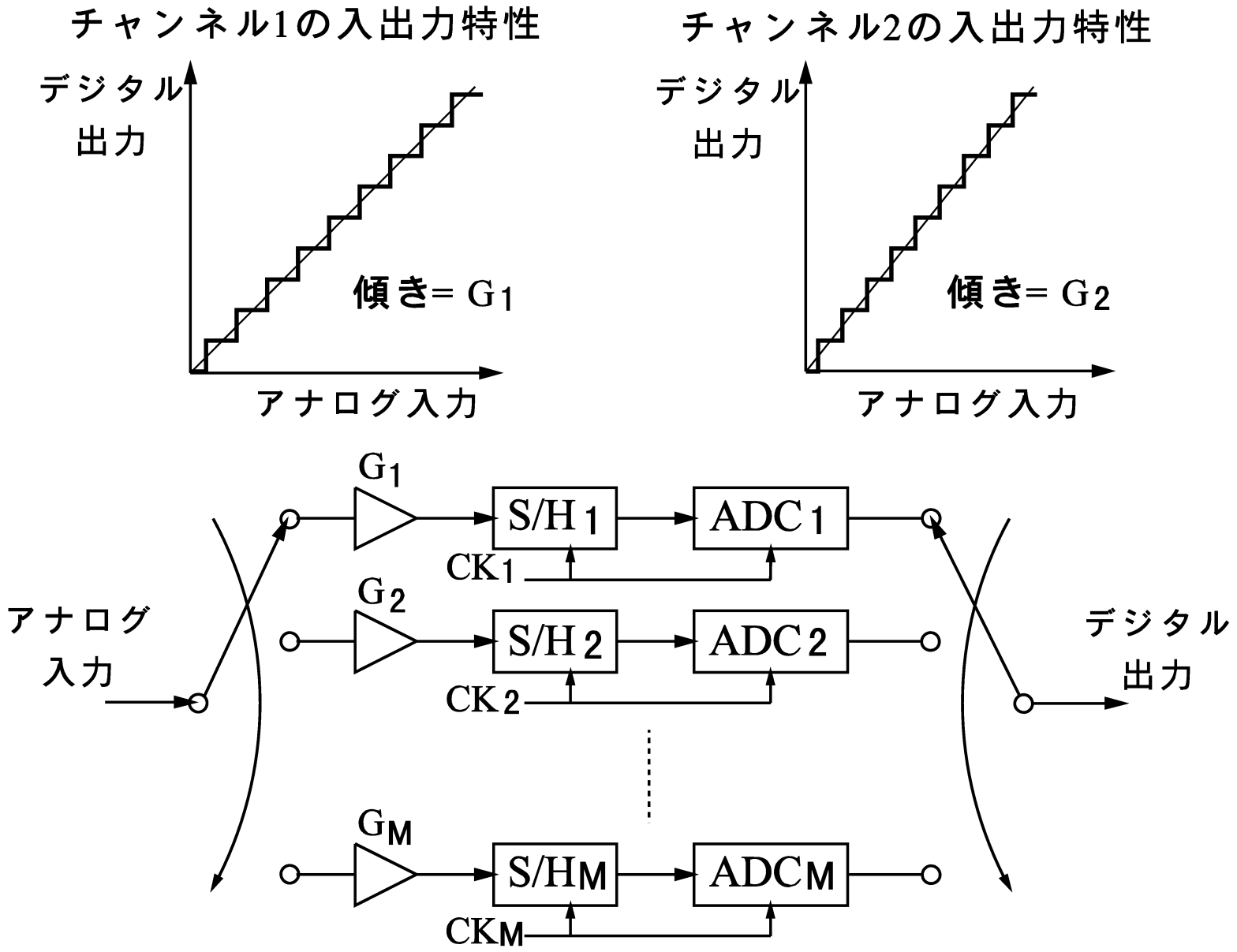
- 4チャンネル6ビットADCのシミュレーション
- オフセットミスマッチ：
  S/Nは入力周波数に独立
  ノイズレベルは入力振幅に独立



チャネル間ミスマッチの影響

- ゲインミスマッチの影響

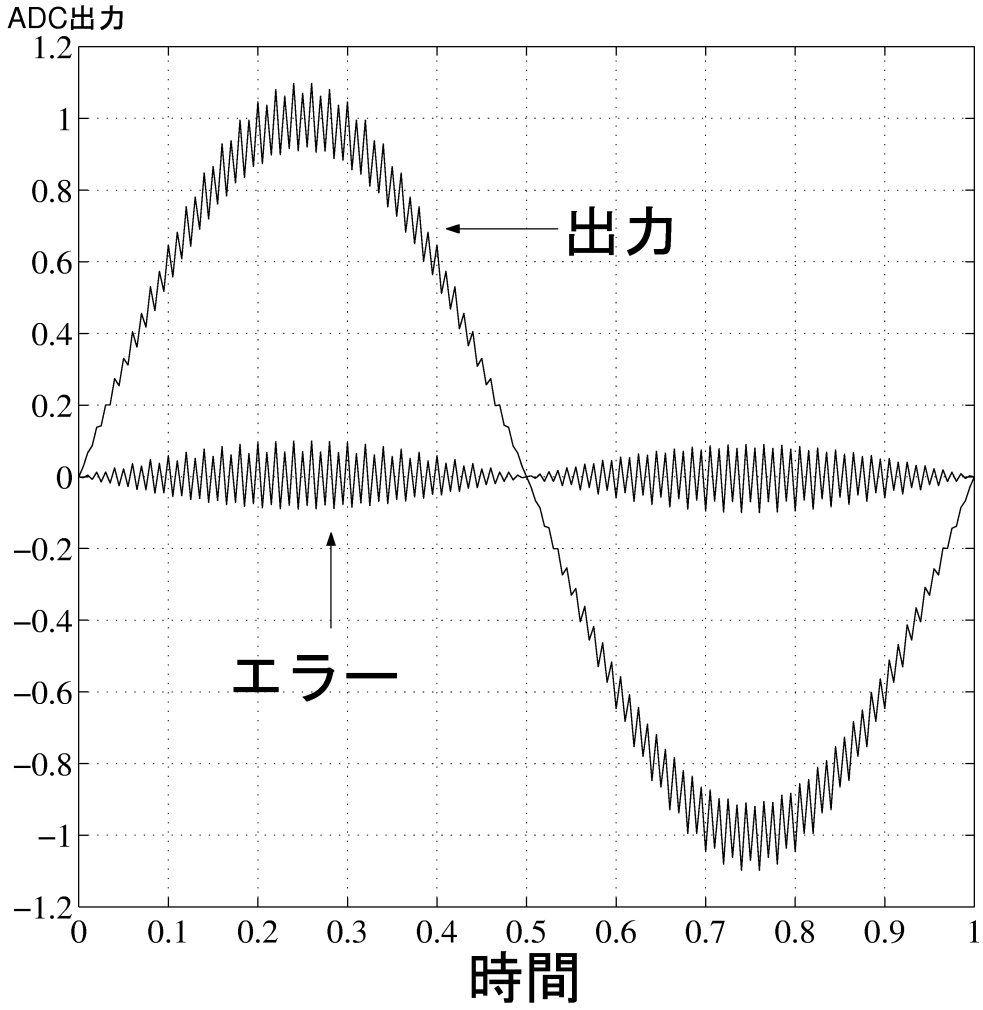
ゲインミスマッチのモデル



ゲインミスマッチの時間領域での影響

- パターンノイズ
  - ± 入力正弦波のピークでエラー最大
  - ± 乗算的ノイズ(AMノイズ)
- 4チャンネルADCのシミュレーション
  - ± 正弦波入力

ADCシステムの出力とエラー



ゲインミスマッチの周波数領域での影響

- パターンノイズの周波数

$$\pm \boxed{f_{noise} = f_{in} \S k \pounds f_s/M}$$

$$k = 1; 2; 3; ¢¢¢$$

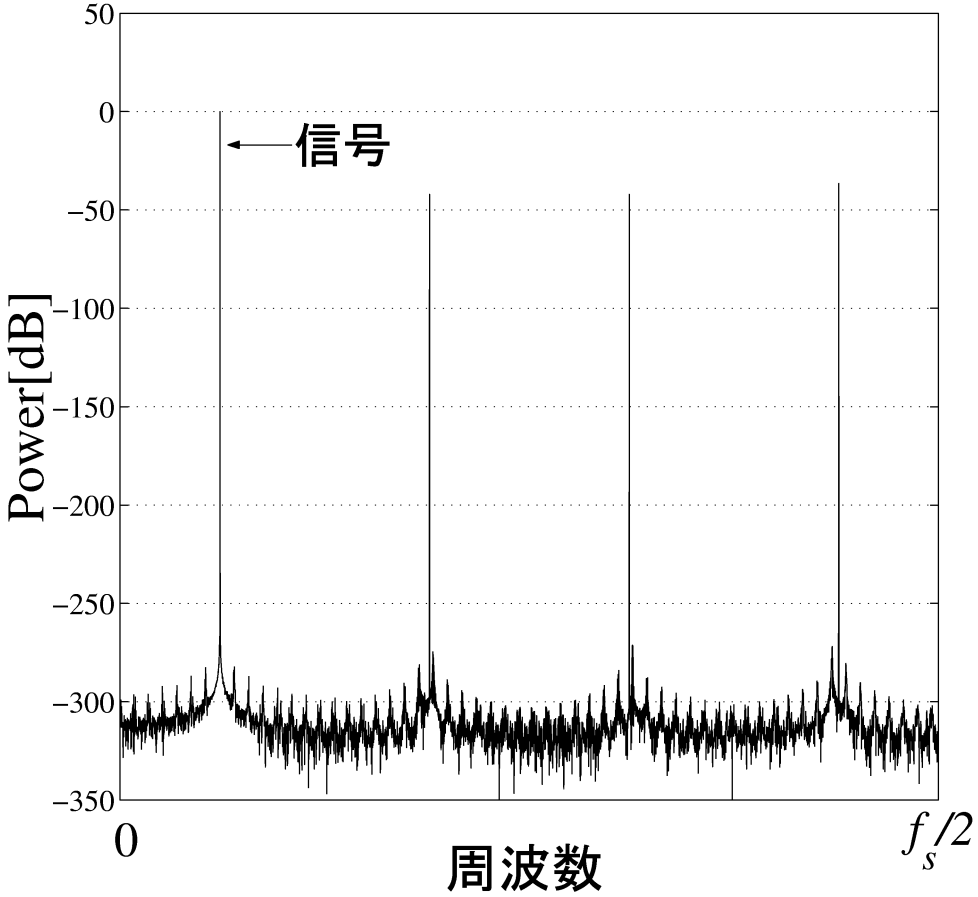
f_s : サンプリング周波数

f_{in} : 入力周波数

M : チャンネル数

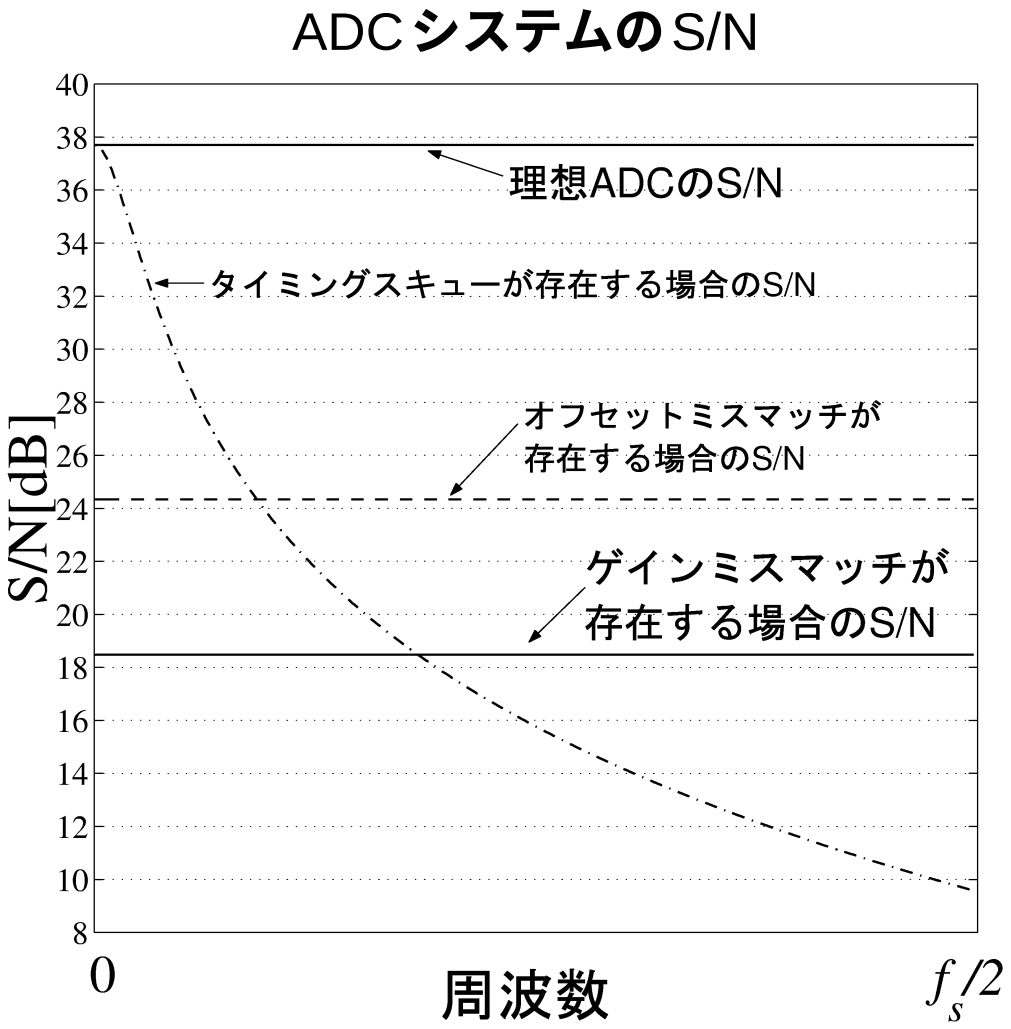
- 4チャンネルADCのシミュレーション
  - 8192点FFT

ADC出力のパワースペクトラム



ゲインミスマッチのS/Nへの影響

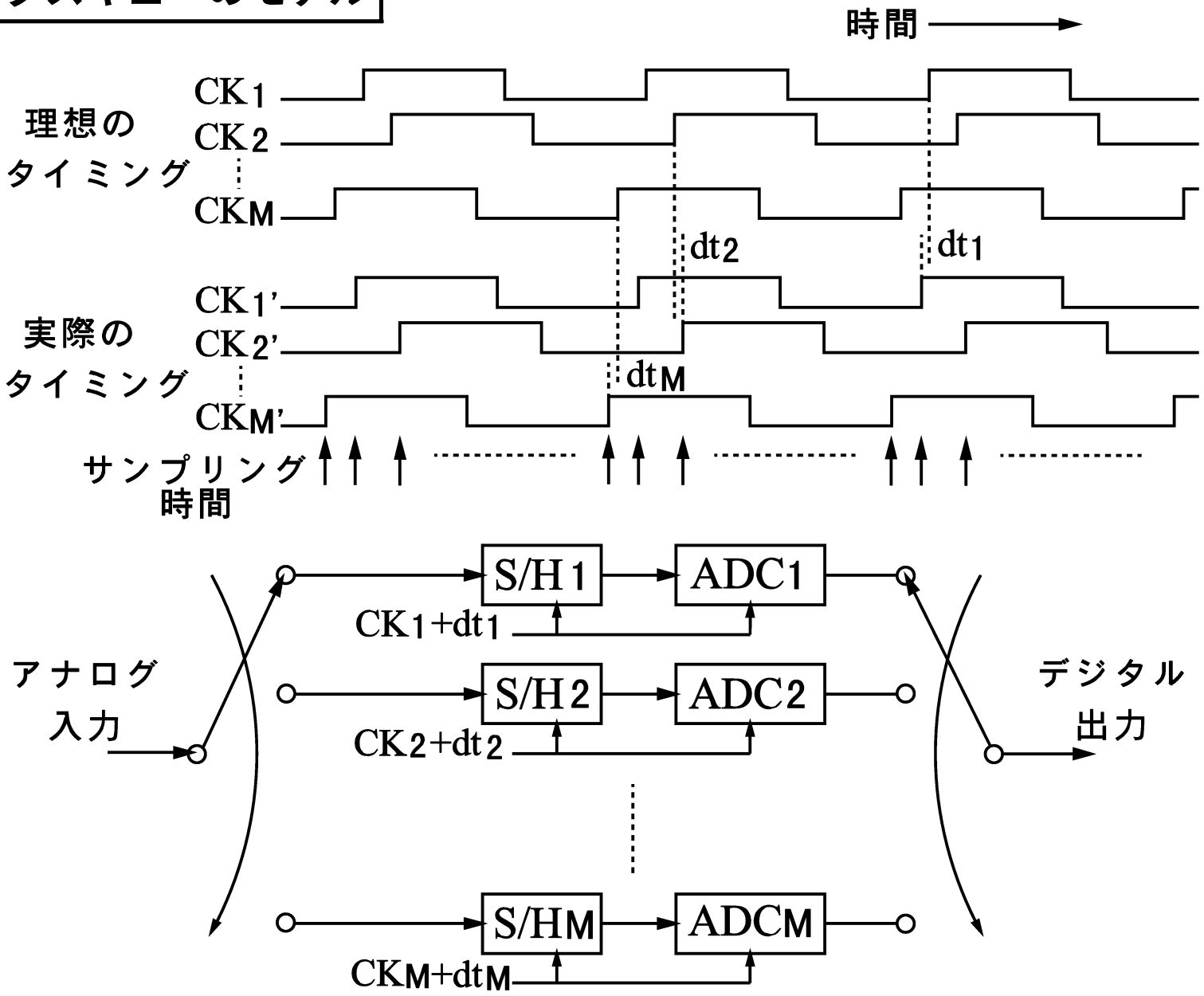
- 4チャンネル6ビットADCのシミュレーション
- ゲインミスマッチ：
  S/Nは入力周波数に独立
  入力振幅に独立



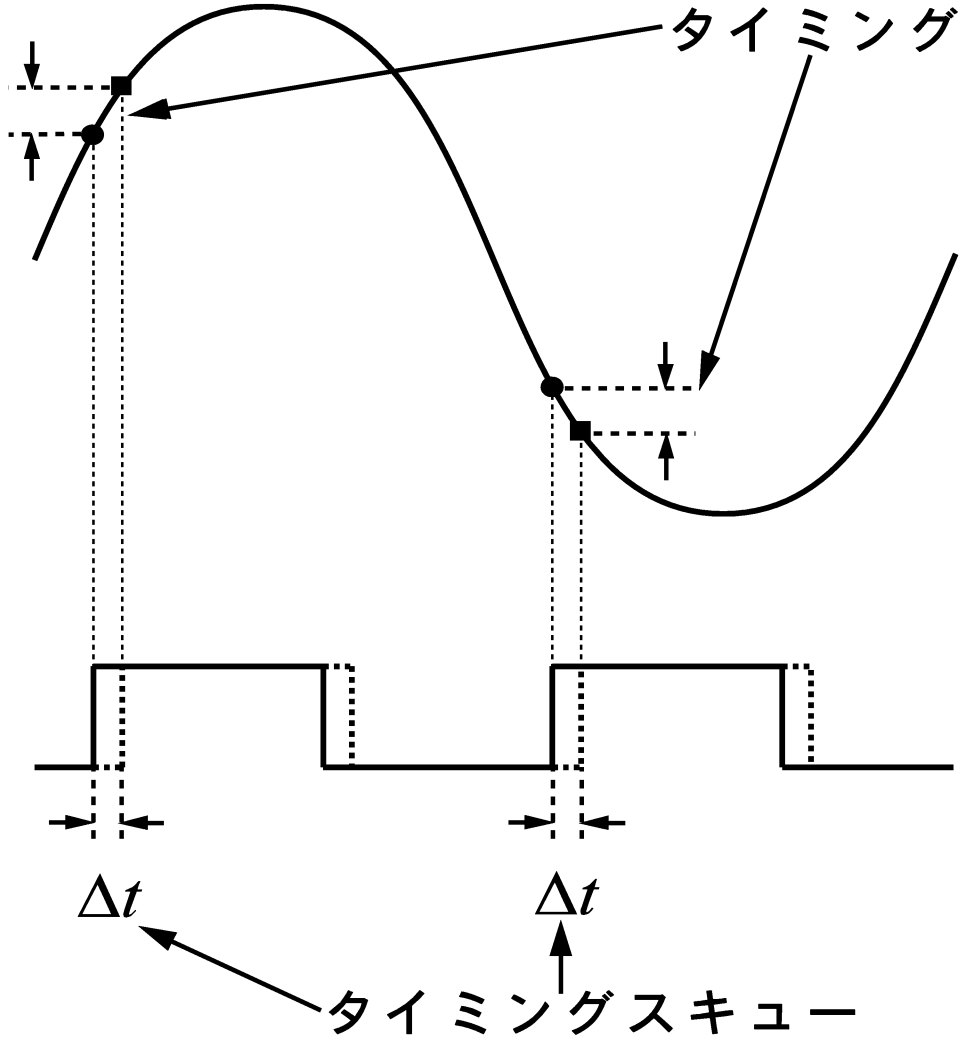
チャネル間ミスマッチの影響

- タイミングスキューの影響

タイミングスキューのモデル



タイミングスキューの出力への影響



理想クロック

タイミングスキューの
影響を受けたクロック

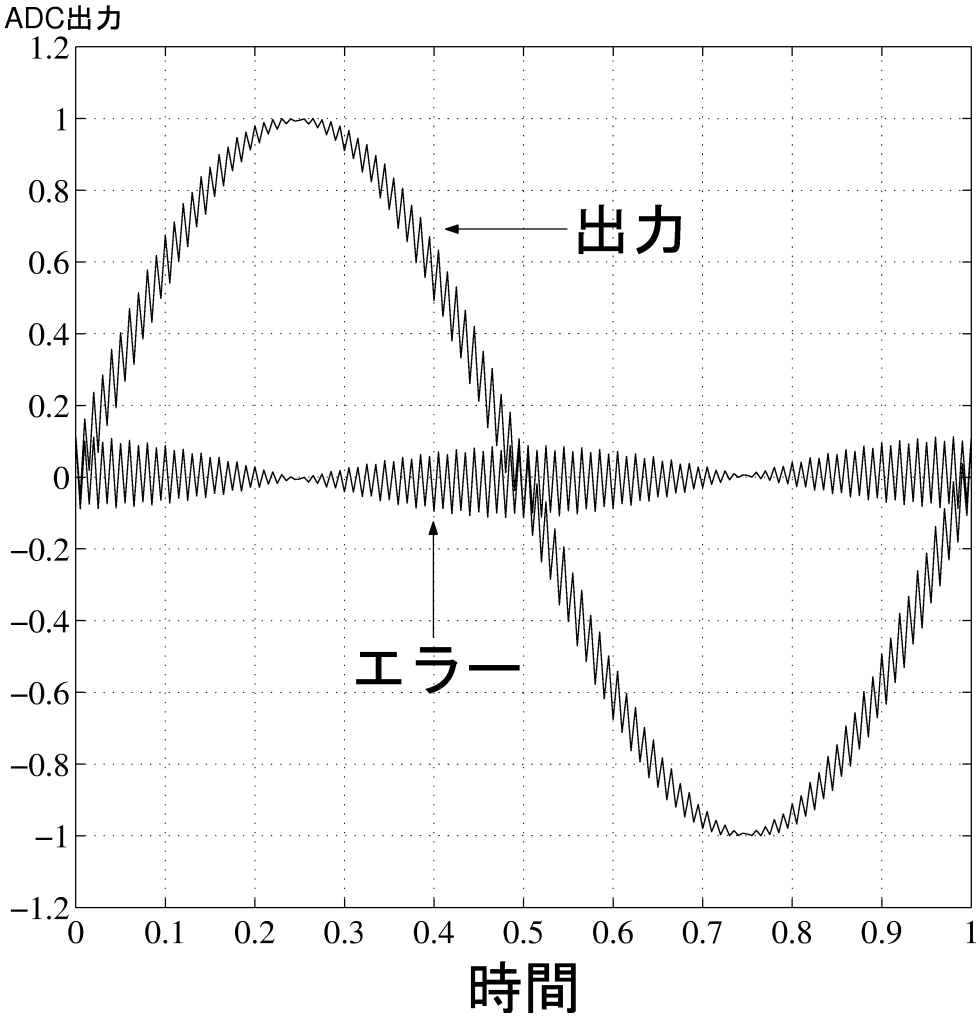
● 理想サンプリング点

■ タイミングスキューの
影響を受けたサンプリング点

タイミングスキューの時間領域での影響

- パターンノイズ
  - ± 入力正弦波のゼロ交差 (スルーレート最大) 付近で最大のエラー
  - ± ゲインミスマッチとは逆
  - ± PM ノイズ
- 4チャンネルADCのシミュレーション
  - ± 正弦波入力

ADCシステムの出力とエラー



タイミングスキューの周波数領域での影響

- パターンノイズの周波数
  - $f_{noise} = f_{in} \pm k \times f_s/M$

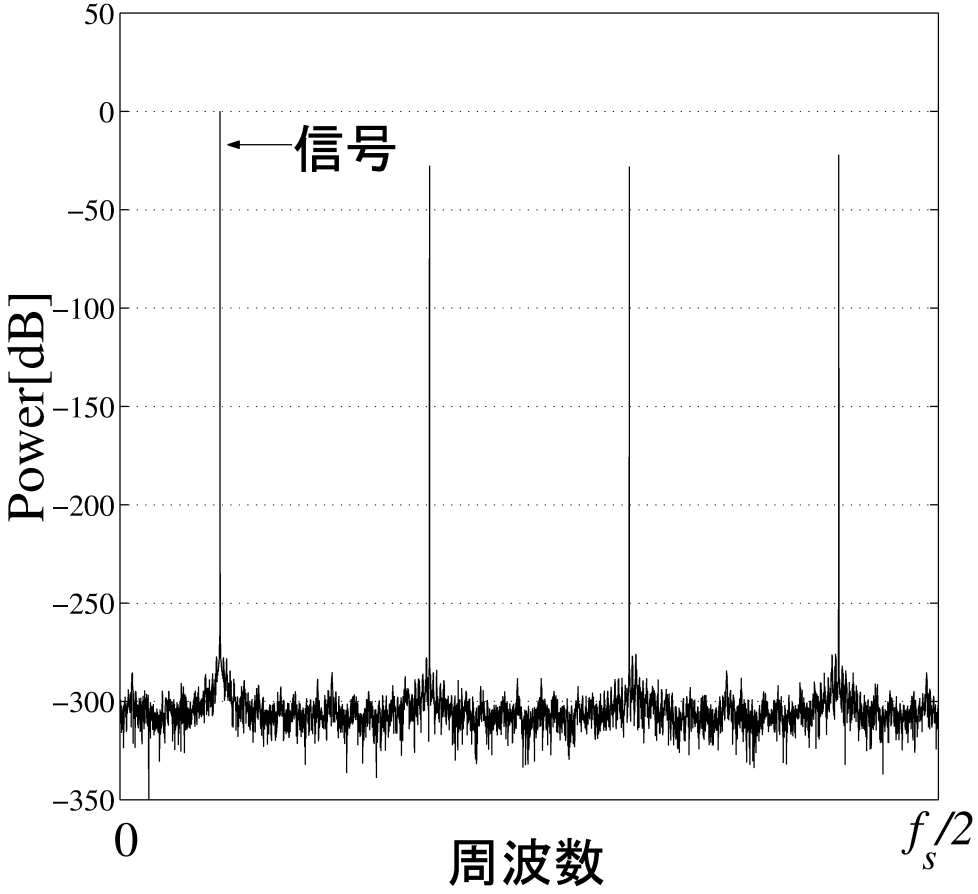
    $k = 1; 2; 3; \cdots$

    f_s : サンプリング周波数

    f_{in} : 入力周波数

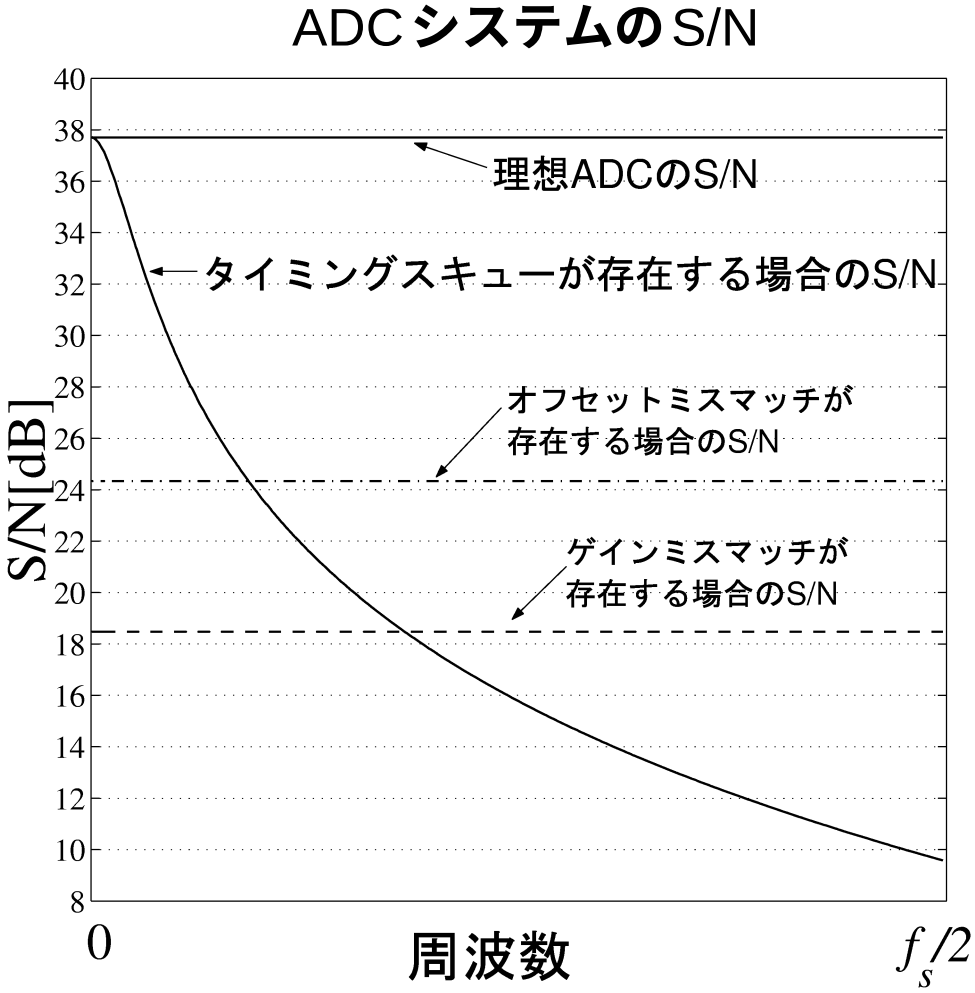
    M : チャンネル数
  - ゲインミスマッチの場合と同じ
- 4チャンネルADCのシミュレーション
  - 8192点FFT

ADC出力のパワースペクトラム



タイミングスキューのS/Nへの影響

- 4チャンネル6ビットADCのシミュレーション
- タイミングスキュー：
  S/Nは
  - 入力周波数が高くなると共に低下
  - 入力振幅に独立



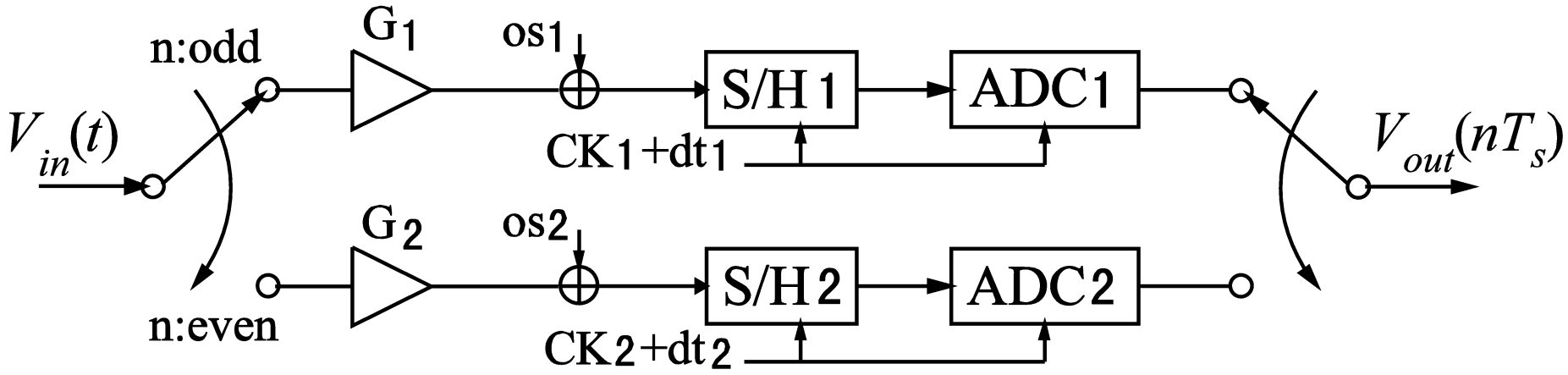
4. ミスマッチが同時に

存在する場合の影響

ミスマッチが同時に存在する場合の影響

- 2チャンネルADC

2ch ADCに複数のミスマッチが同時に存在する場合のモデル



$$V_{in}(t) = A\cos(2\pi f_{in} t)$$

$$V_{out}(nT_s) = \begin{cases} AG_1\cos\{2\pi f_{in}(nT_s + \Delta t_1)\} + os_1 & (n : \text{odd}) \\ AG_2\cos\{2\pi f_{in}(nT_s + \Delta t_2)\} + os_2 & (n : \text{even}) \end{cases}$$

$$= \begin{cases} AG(1-\Delta)\cos\left\{2\pi f_{in}\left(nT_s - \frac{\Delta t}{2}\right)\right\} + os_{cm} - os_{diff} & (n : \text{odd}) \\ AG(1+\Delta)\cos\left\{2\pi f_{in}\left(nT_s + \frac{\Delta t}{2}\right)\right\} + os_{cm} + os_{diff} & (n : \text{even}) \end{cases}$$

$$(n = 0, \pm 1, \pm 2, \cdots)$$

2ch ADC に複数のミスマッチが同時に存在する場合の出力

$$V_{out}(nT_s) = A_s \cos\left(2\pi f_{in} nT_s + \mu_s\right) + A_n \cos\left\{2\pi \left(f_{in} + \frac{1}{2} f_s\right) nT_s + \mu_n\right\} + os_{cm} + os_{diff} \cos\left\{2\pi \frac{1}{2} f_s nT_s\right\}$$

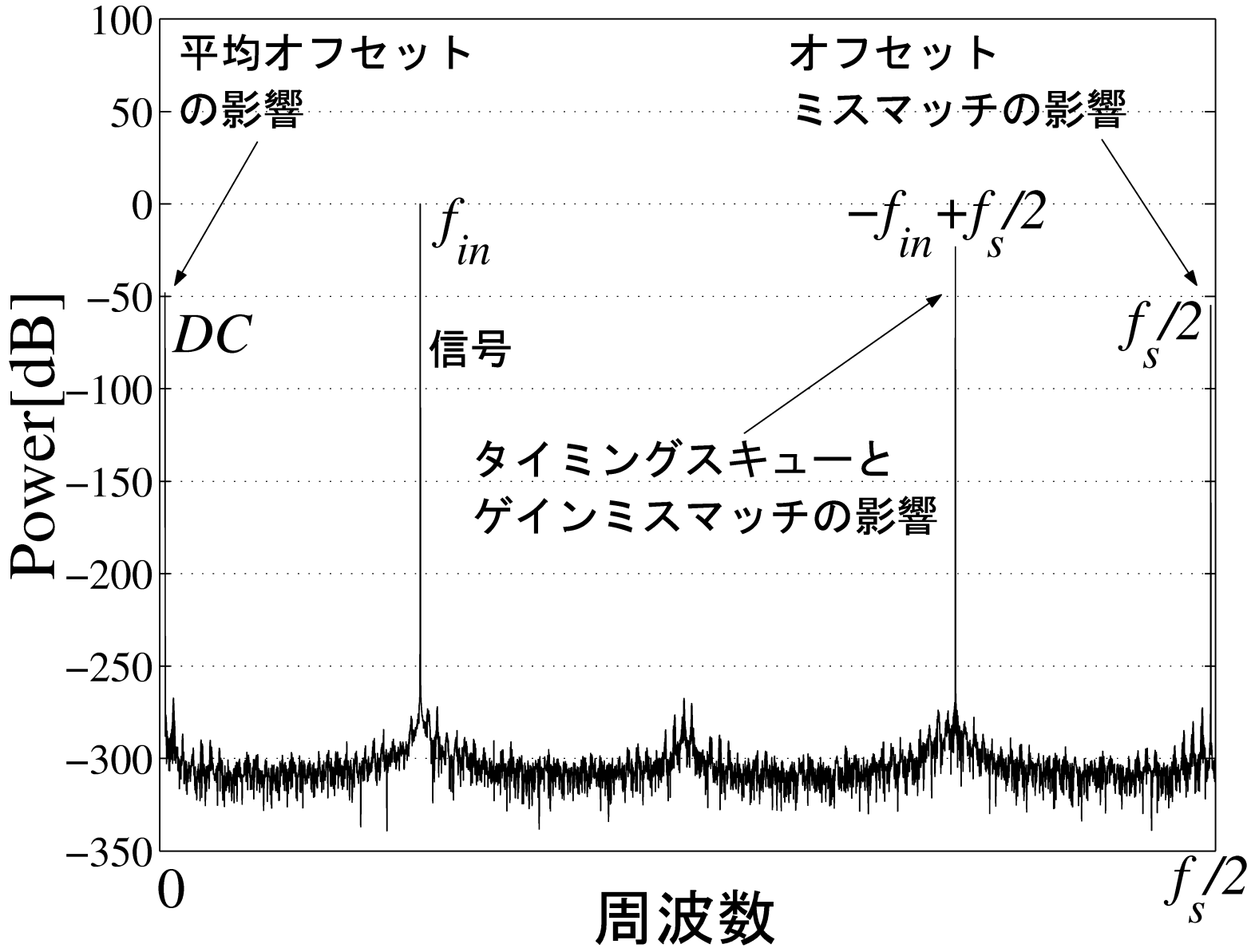
$$A_s = AG \sqrt{\frac{\cos^2(\pi f_{in} \pm t) + \alpha^2 \sin^2(\pi f_{in} \pm t)}{\alpha^2 \cos^2(\pi f_{in} \pm t) + \sin^2(\pi f_{in} \pm t)}}$$

$$A_n = AG \frac{\alpha^2 \cos^2(\pi f_{in} \pm t) + \sin^2(\pi f_{in} \pm t)}{\alpha^2 \cos^2(\pi f_{in} \pm t) + \sin^2(\pi f_{in} \pm t)}$$

$$\mu_s = \arctan\{\alpha \tan(\pi f_{in} \pm t)\}$$

$$\mu_n = \arctan\{\tan(\pi f_{in} \pm t) = \alpha\}$$

2ch ADCに複数のミスマッチが同時に存在する場合の出力のパワースペクトラム

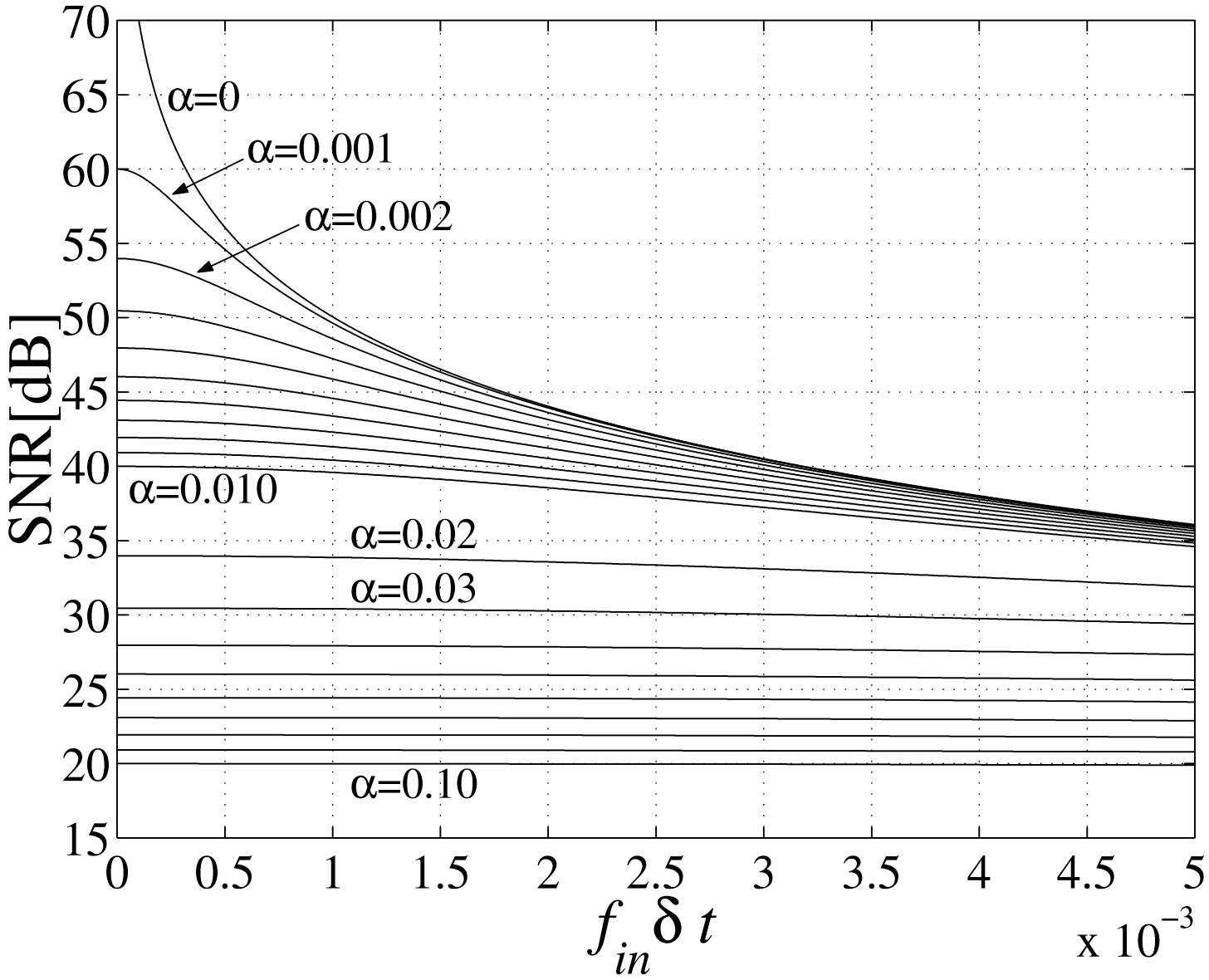


解析式と数値計算の結果が一致

＋

解析式の正当性を確認

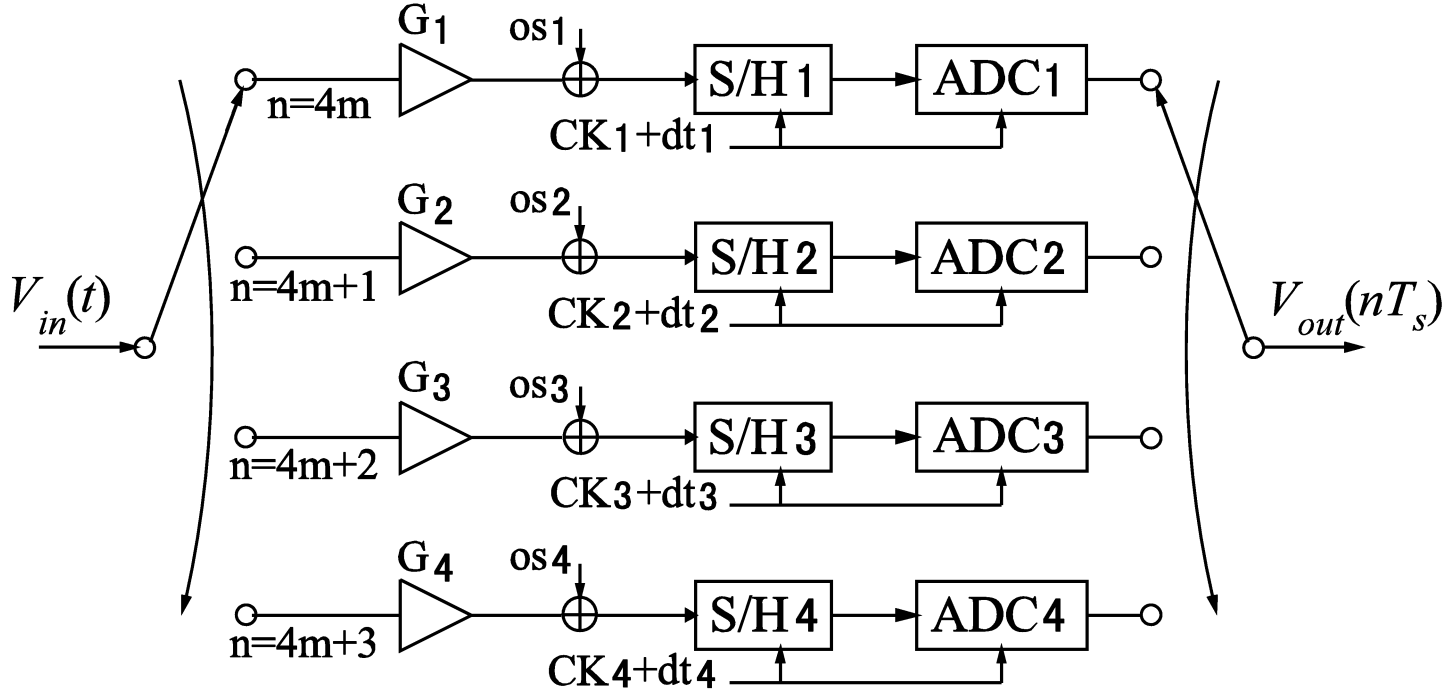
2ch ADC に複数のミスマッチが同時に存在する場合の SNR の低下



ミスマッチが同時に存在する場合の影響

- ４チャンネルADC

4ch ADCに複数のミスマッチが同時に存在する場合のモデル



$$V_{in}(t) = A\cos(2\pi f_{in} t)$$

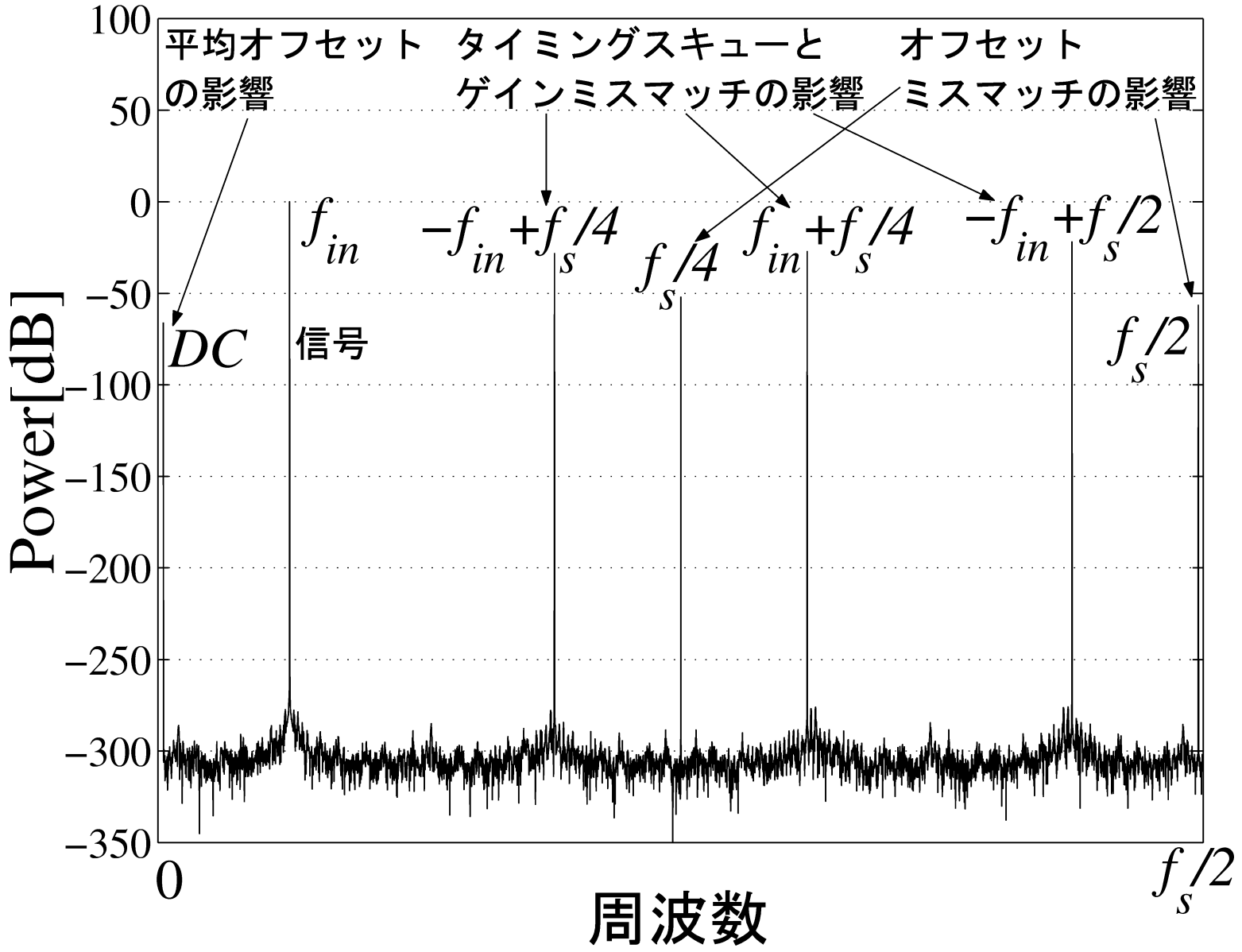
$$V_{out}(nT_s) = \begin{cases} AG_1\cos\{2\pi f_{in}(nT_s + \Delta t_1)\} + os_1 & (n = 4m) \\ AG_2\cos\{2\pi f_{in}(nT_s + \Delta t_2)\} + os_2 & (n = 4m+1) \\ AG_3\cos\{2\pi f_{in}(nT_s + \Delta t_3)\} + os_3 & (n = 4m+2) \\ AG_4\cos\{2\pi f_{in}(nT_s + \Delta t_4)\} + os_4 & (n = 4m+3) \end{cases}$$

$$(m = 0, \pm 1, \pm 2, \cdots)$$

4ch ADC に複数のミスマッチが同時に存在する場合の出力

$$
\begin{aligned}
V_{out}(nT_s) = {} & \sqrt{A_{sc}^2 + A_{ss}^2}\cos\left(2\pi f_{in} nT_s - \arctan\frac{A_{ss}}{A_{sc}}\right) \\
& + \sqrt{A_{n1c}^2 + A_{n1s}^2}\cos\left\{2\pi\left(f_{in} + \frac{1}{4}f_s\right)nT_s - \arctan\left(\frac{A_{n1s}}{A_{n1c}}\right)\right\} \\
& + \sqrt{A_{n2c}^2 + A_{n2s}^2}\cos\left\{2\pi\left(f_{in} + \frac{1}{2}f_s\right)nT_s - \arctan\left(\frac{A_{n2s}}{A_{n2c}}\right)\right\} \\
& + \sqrt{A_{n3c}^2 + A_{n3s}^2}\cos\left\{2\pi\left(f_{in} + \frac{3}{4}f_s\right)nT_s - \arctan\left(\frac{A_{n3s}}{A_{n3c}}\right)\right\} \\
& + \frac{1}{4}(os_1 - os_2 + os_3 - os_4)\cos\left(2\pi\frac{1}{2}f_s nT_s\right) \\
& + \frac{1}{2}\sqrt{(os_1 - os_3)^2 + (os_2 - os_4)^2}\cos\left\{2\pi\frac{1}{4}f_s nT_s - \arctan\left(\frac{os_2 - os_4}{os_1 - os_3}\right)\right\} \\
& + \frac{1}{4}(os_1 + os_2 + os_3 + os_4)
\end{aligned}
$$

4ch ADCに複数のミスマッチが同時に存在する場合の出力のパワースペクトラム

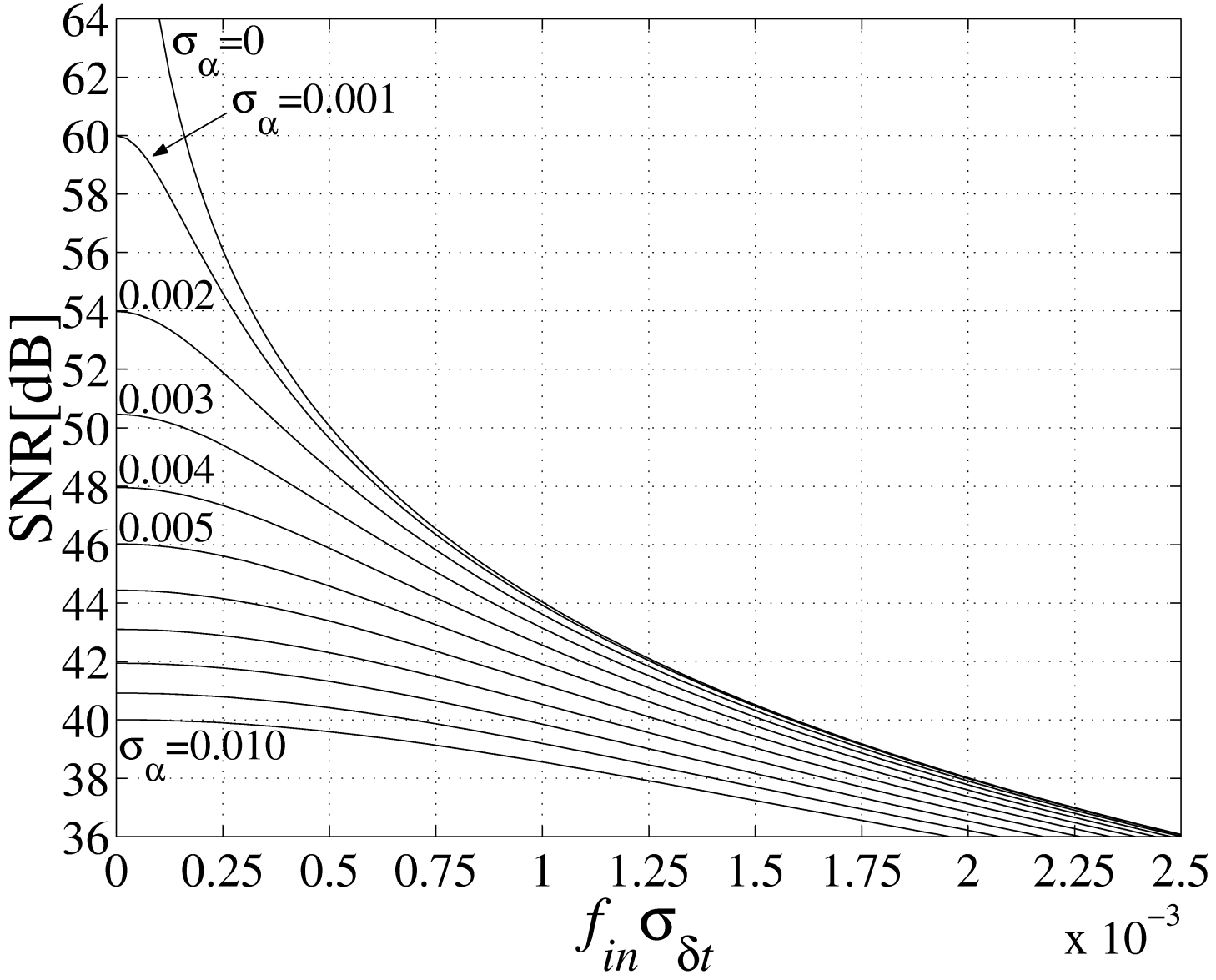


解析式と数値計算の結果が一致

＋

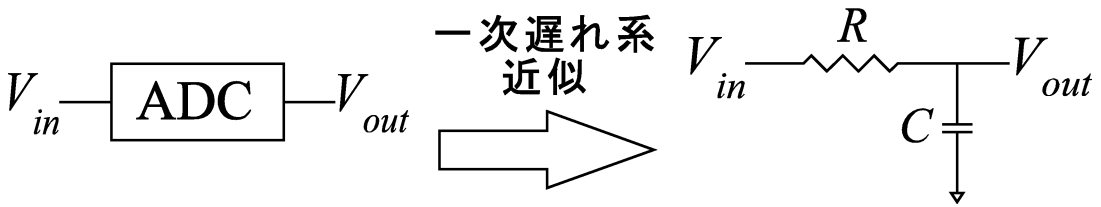
解析式の正当性を確認

4ch ADC に複数のミスマッチが同時に存在する場合の SNR の低下



5. 帯域ミスマッチの影響

ADCの一次遅れ系近似



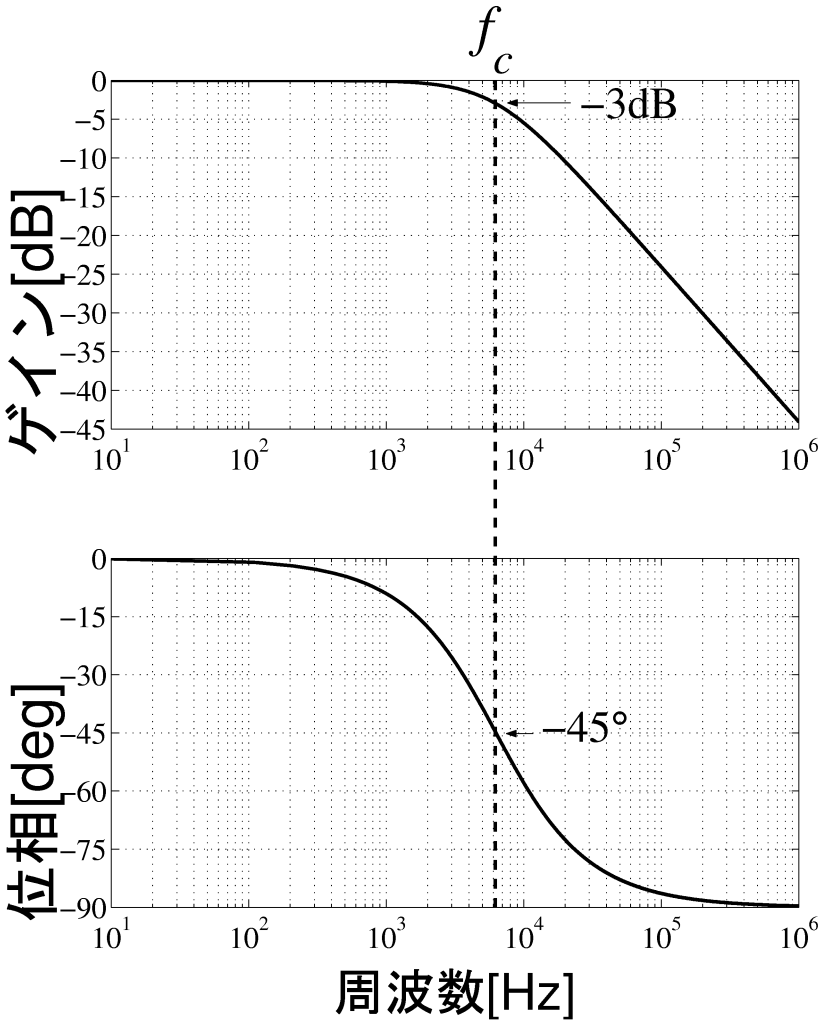
$$H(j2\pi f) = \frac{1}{1 + j f_{in}/f_c}$$

$$\text{ゲイン} \quad |H(j2\pi f)| = 1/\sqrt{1 + (f_{in}/f_c)^2}$$

$$\text{位相} \quad \angle H(j2\pi f) = -\arctan(f_{in}/f_c)$$

$V_{in}(t) = \cos(2\pi f_{in} t)$ **のとき**

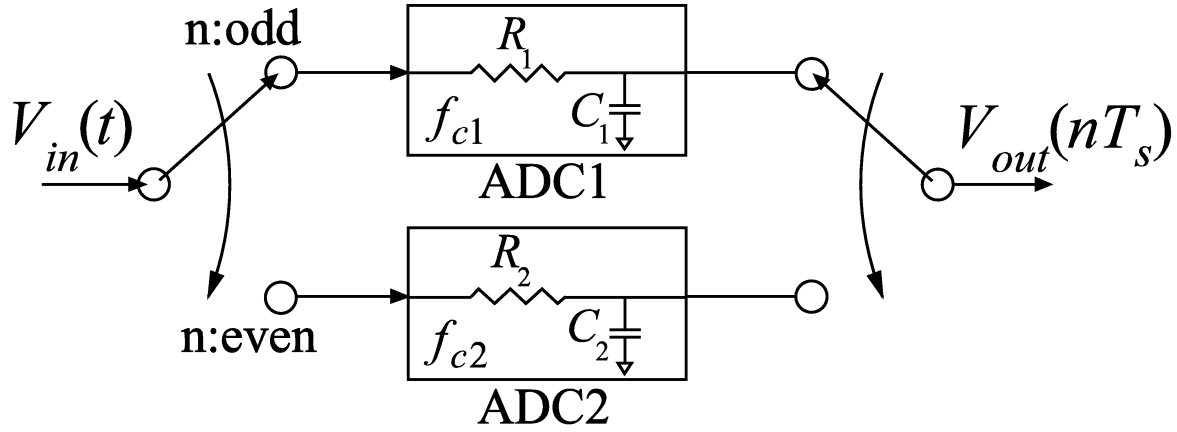
$$V_{outk}(nT_s) = G_k \cos(2\pi f_{in} n T_s + \mu_k)$$



帯域ミスマッチの影響

- 2チャンネルADC

2ch ADC に帯域のミスマッチが存在する場合のモデル



$$V_{in}(t) = A\cos(2\pi f_{in}t)$$

$$V_{out}(nT_s) = \begin{cases} A\sqrt{\dfrac{1}{1+(f_{in}/f_{c1})^2}}\cos\{2\pi f_{in}nT_s - \arctan(f_{in}/f_{c1})\} & (n:\text{odd}) \\ A\sqrt{\dfrac{1}{1+(f_{in}/f_{c2})^2}}\cos\{2\pi f_{in}nT_s - \arctan(f_{in}/f_{c2})\} & (n:\text{even}) \end{cases}$$

$$= \begin{cases} AG_1\cos(2\pi f_{in}nT_s + \mu_1) & (n:\text{odd}) \\ AG_2\cos(2\pi f_{in}nT_s + \mu_2) & (n:\text{even}) \end{cases} \qquad (n = 0, \pm 1, \pm 2, \cdots)$$

- **帯域のミスマッチ**
  - **ゲインと位相のミスマッチ**
  - **ゲインミスマッチとタイミングスキューに相似**
  - **ゲイン, 位相は周波数の関数**

2ch ADC に帯域のミスマッチが存在する場合の出力

$$V_{out}(nT_s) = A_s \cos(2\pi f_{in} nT_s + \mu_s) + A_n \cos\left(2\pi \left(\frac{1}{2}f_s - f_{in}\right) nT_s + \mu_n\right)$$

$$A_s = \frac{1}{2}A\sqrt{G_c^2\cos^2(\mu_d) + G_d^2\sin^2(\mu_d)}$$

$$A_n = \frac{1}{2}A\sqrt{G_c^2\sin^2(\mu_d) + G_d^2\cos^2(\mu_d)}$$

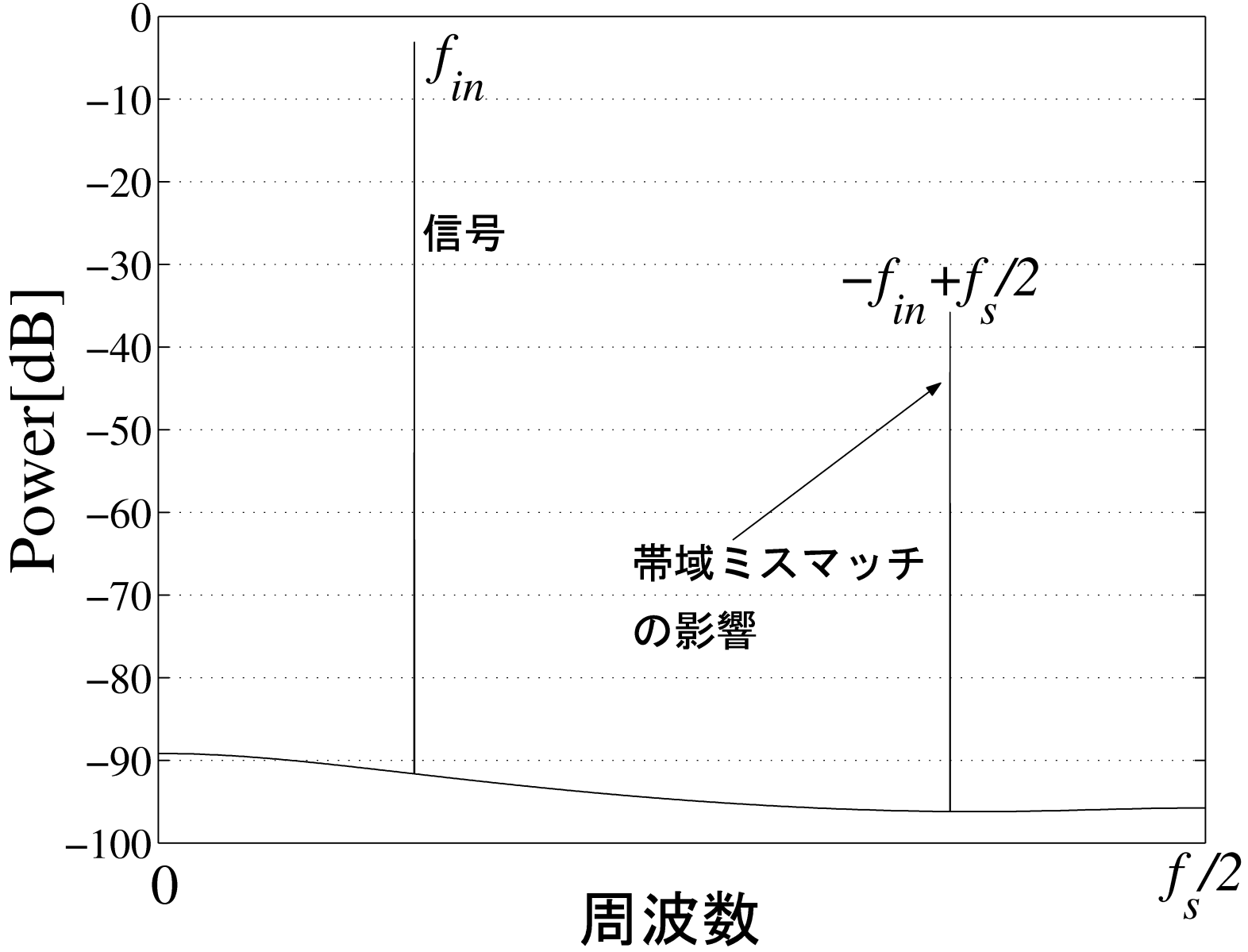
$$\mu_s = \arctan\left\{\frac{G_c\sin(\mu_c)\cos(\mu_d) + G_d\cos(\mu_c)\sin(\mu_d)}{G_c\cos(\mu_c)\cos(\mu_d) - G_d\sin(\mu_c)\sin(\mu_d)}\right\}$$

$$\mu_n = -\arctan\left\{\frac{G_c\cos(\mu_c)\sin(\mu_d) + G_d\sin(\mu_c)\cos(\mu_d)}{G_c\sin(\mu_c)\sin(\mu_d) - G_d\cos(\mu_c)\cos(\mu_d)}\right\}$$

$$G_c = G_1 + G_2;\ G_d = G_1 - G_2$$

$$\mu_c = (\mu_1 + \mu_2)/2;\ \mu_d = (\mu_1 - \mu_2)/2$$

2ch ADCに帯域のミスマッチが存在する場合の出力のパワースペクトラム



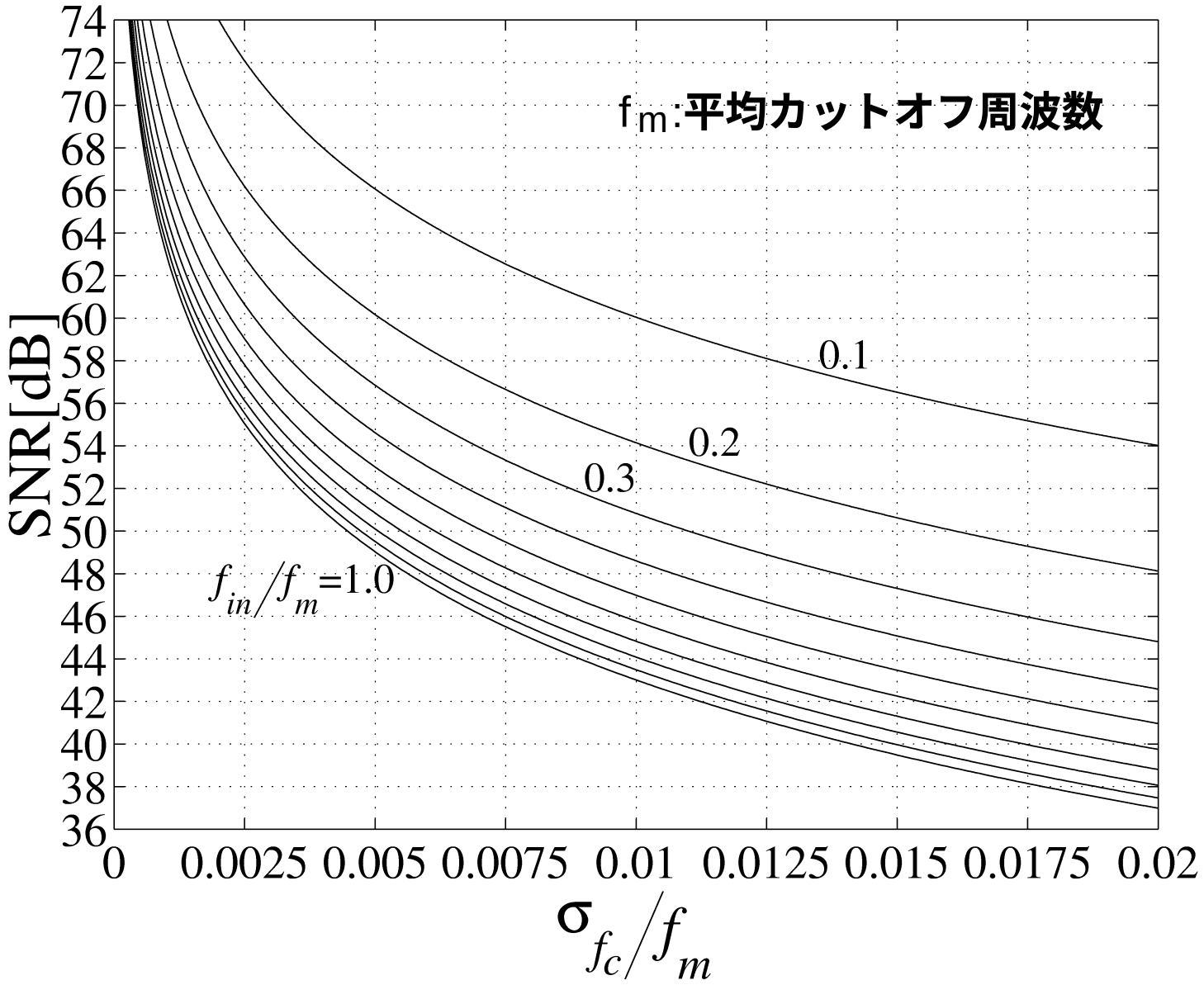
解析式と

Spiceシミュレーション結果が一致

＋

解析式の正当性を確認

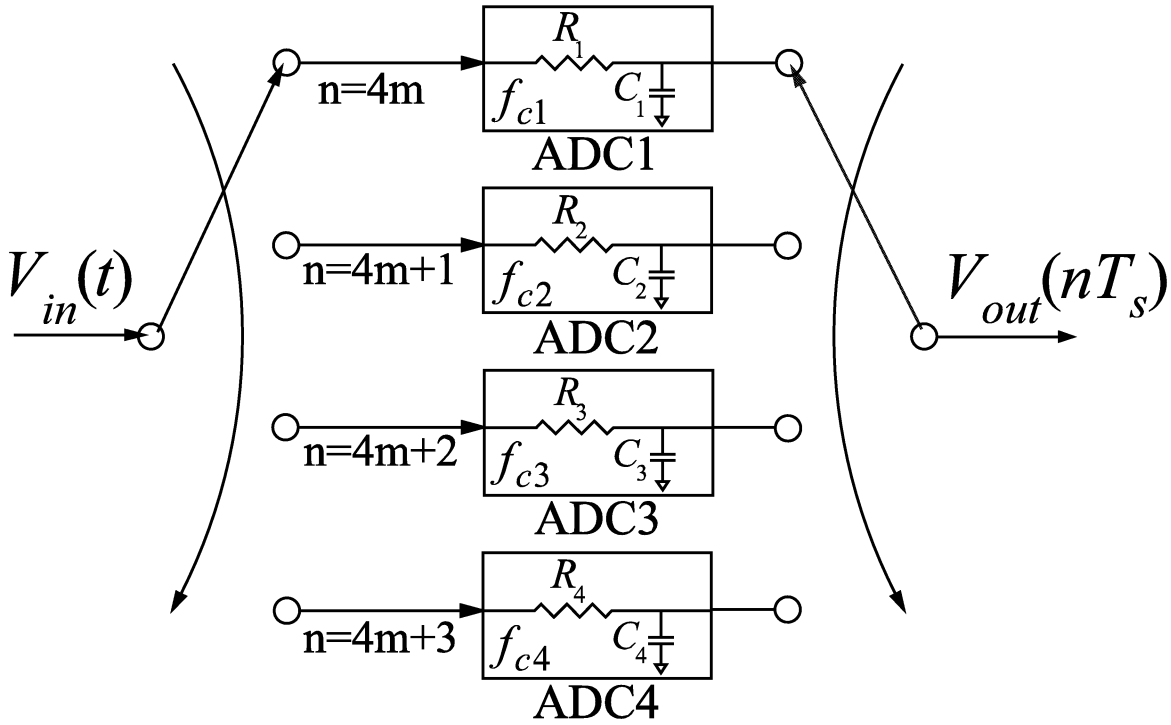
2ch ADCに帯域のミスマッチが存在する場合のSNRの低下



帯域ミスマッチの影響

- ４チャンネルADC

4ch ADCに帯域のミスマッチが存在する場合のモデル



$$V_{in}(t) = A\cos(2\pi f_{in} t)$$

$$V_{out}(nT_s) \approx \begin{cases} G_1\cos(2\pi f_{in} nT_s + \mu_1) & (n = 4m) \\ G_2\cos(2\pi f_{in} nT_s + \mu_2) & (n = 4m+1) \\ G_3\cos(2\pi f_{in} nT_s + \mu_3) & (n = 4m+2) \\ G_4\cos(2\pi f_{in} nT_s + \mu_4) & (n = 4m+3) \end{cases}$$

$(m = 0, \pm 1, \pm 2, \cdots)$

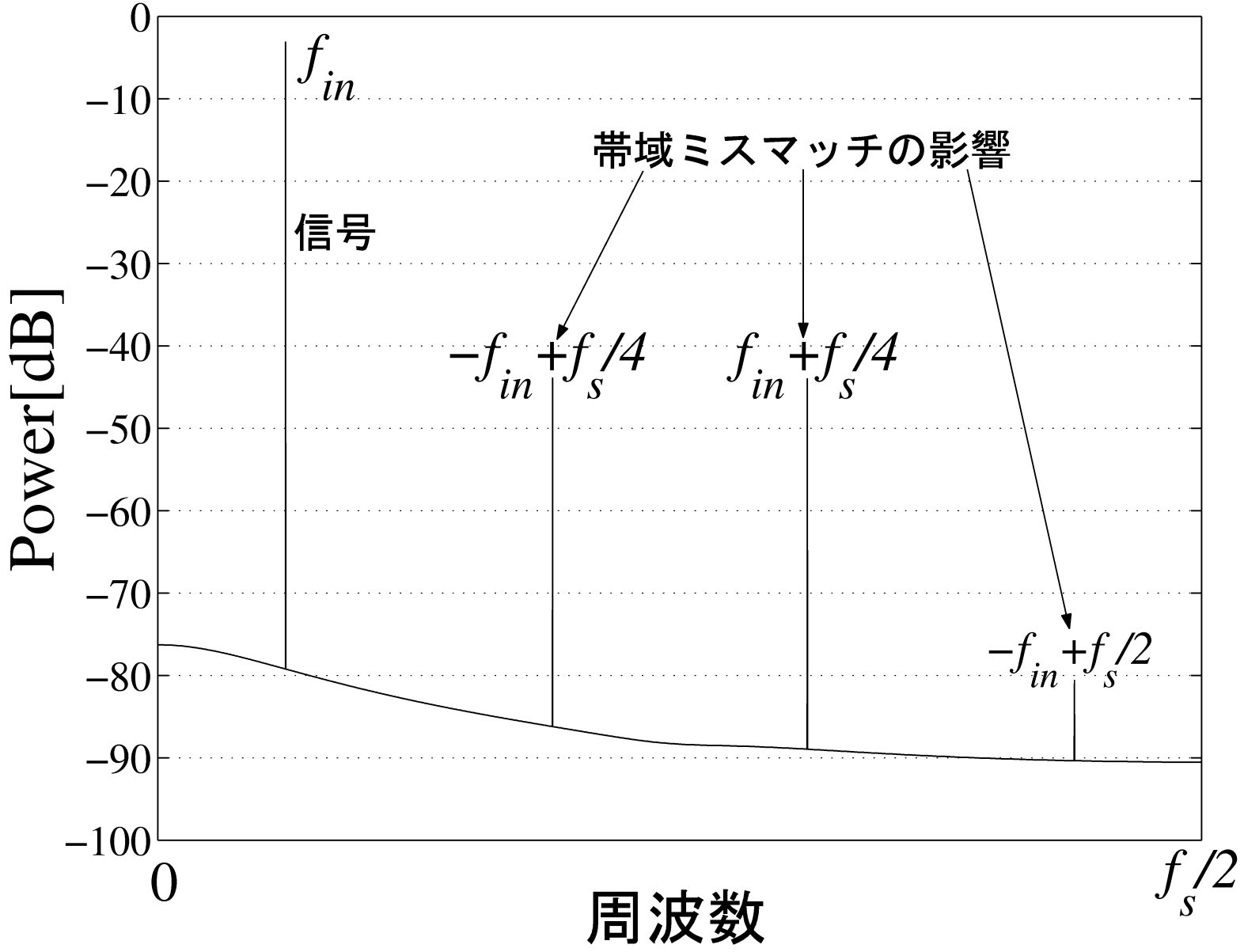
4ch ADC に帯域のミスマッチが存在する場合の出力

$$
\begin{aligned}
V_{out}(nT_s) = & \sqrt{A_{sc}^2 + A_{ss}^2}\cos\left(2\pi f_{in} nT_s - \arctan\frac{A_{ss}}{A_{sc}}\right) \\
& + \sqrt{A_{n1c}^2 + A_{n1s}^2}\cos\left\{2\pi\left(f_{in} + \frac{1}{4}f_s\right)nT_s - \arctan\left(\frac{A_{n1s}}{A_{n1c}}\right)\right\} \\
& + \sqrt{A_{n2c}^2 + A_{n2s}^2}\cos\left\{2\pi\left(f_{in} + \frac{1}{2}f_s\right)nT_s - \arctan\left(\frac{A_{n2s}}{A_{n2c}}\right)\right\} \\
& + \sqrt{A_{n3c}^2 + A_{n3s}^2}\cos\left\{2\pi\left(f_{in} + \frac{3}{4}f_s\right)nT_s - \arctan\left(\frac{A_{n3s}}{A_{n3c}}\right)\right\}
\end{aligned}
$$

Asc; Ass; An1c; An1s; An2c; An2s; An3c; An3s **は**

f_{in}; f_{c1}; f_{c2}; f_{c3}; f_{c4} **の関数**

4ch ADCに帯域のミスマッチが存在する場合の出力のパワースペクトラム



解析式と

Spiceシミュレーション結果が一致

＋

解析式の正当性を確認

6. まとめ

研究成果

インターリーブADCのミスマッチの影響について

- 複数のミスマッチが同時に存在する場合の解析式を導出
- 帯域のミスマッチが存在する場合の解析式を導出
- 実際のアプリケーションの80%以上をカバーする

  2チャンネルと4チャンネルについて解析

Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems

Naoki Kurosawa, Haruo Kobayashi, *Member, IEEE,* Kaoru Maruyama, Hidetake Sugawara, and Kensuke Kobayashi

***Abstract*—A time-interleaved A–D converter (ADC) system is an effective way to implement a high-sampling-rate ADC with relatively slow circuits. In the system, several channel ADCs operate at interleaved sampling times as if they were effectively a single ADC operating at a much higher sampling rate. However, mismatches such as offset, gain mismatches among channel ADCs as well as timing skew of the clocks distributed to them degrade *S/N* of the ADC system as a whole. This paper analyzes the channel mismatch effects in the time-interleaved ADC system. Previous analysis showed the effect for each mismatch *individually*, however in this paper we derive *explicit* formulas for the mismatch effects when *all* of offset, gain and timing mismatches exist together. We have clarified that the gain and timing mismatch effects interact with each other but the offset mismatch effect is independent from them, and this can be seen clearly in frequency domain. We also discuss the bandwidth mismatch effect. The derived formulas can be used for calibration algorithms to compensate for the channel mismatch effects.**

***Index Terms*—A–D converter, analog circuit, calibration, channel mismatch, interleave, track/hold circuit.**

I. Introduction

ELECTRONIC devices are continuously getting faster and accordingly, the need for instruments such as digitizing oscilloscopes and large scale integrated (LSI) circuit testers to measure their performance is growing. A–D converters (ADCs) incorporated in such instruments have to operate at a very high sampling rate. This paper studies theoretical issues of a time-interleaved ADC system where several channel ADCs operate at interleaved sampling times as if they were effectively a single ADC operating at a much higher sampling rate [1]–[7]. Fig. 1 shows such an ADC system where each M channel ADCs $(\mathrm{ADC}_1, \mathrm{ADC}_2, \ldots, \mathrm{ADC}_M)$ operates with one of M phase clocks $(CK_1, CK_2, \ldots, CK_M)$, respectively. The sampling rate of the ADC as a whole is M times the channel sampling rate. This time-interleaved ADC system is an effective way to implement a high-sampling-rate ADC with relatively slow circuits, and is widely used. Ideally, characteristics of channel ADCs should be identical and clock skew should be zero. However, in reality there are mismatches such as offset, gain mismatches among channel ADCs as well as timing skew of the clocks distributed to them, which cause so-called *pattern noise* and significantly degrade *S/N* (effective bits) of the ADC system as a whole. Hence calibration often has to be incorporated to ensure uniformity among the characteristics of the channels. It is important to clarify the issues of the interleaved ADC architecture for designing the system. This channel mismatch in the interleaved ADC system may be called as *system level mismatch* or *module level mismatch*, while, for example, a random offset voltage in a CMOS differential pair circuit due to device size and threshold voltage mismatches may be called as *circuit level mismatch*.

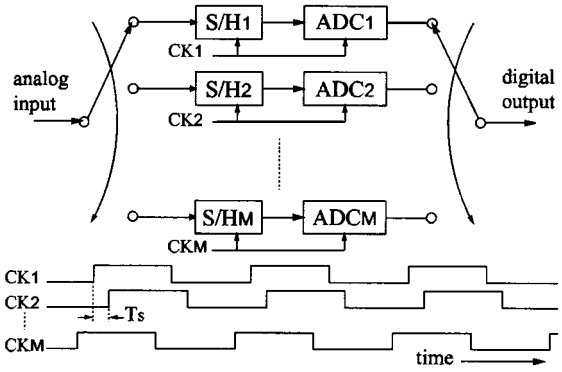


Fig. 1. Time-interleaved ADC system.

This paper first reviews interleaving issues, the effects of offset, gain and timing mismatches *individually* [4]–[11]. Then, we will derive *explicit* formulas for the mismatch effects when all of offset, gain and timing mismatches exist together, and show that the gain and timing mismatch effects interact each other but the offset mismatch effect is independent from them. We also analyze the bandwidth mismatch effect. The derived formulas can be used for calibration algorithms to compensate for the channel mismatch effects. In this paper, we concentrate on two-channel and four-channel interleaved systems because they cover most of the practical applications. Eight-channel or others may be sometimes used in practical situation, and the extension of the results here to an interleaved system of other channels is also possible.

Hereafter, we will use following notations:

M	number of channel ADCs in the ADC system;
f_{noise}	pattern noise frequency of the ADC output;
f_{in}	input frequency applied to the ADC system;
f_s	sampling frequency of the ADC system;
f_s/M	sampling frequency of each channel ADC.

II. Individual Channel Mismatch Effects

This section reviews the effects of offset, gain and timing mismatches *individually* in interleaved ADC systems [4]–[11].

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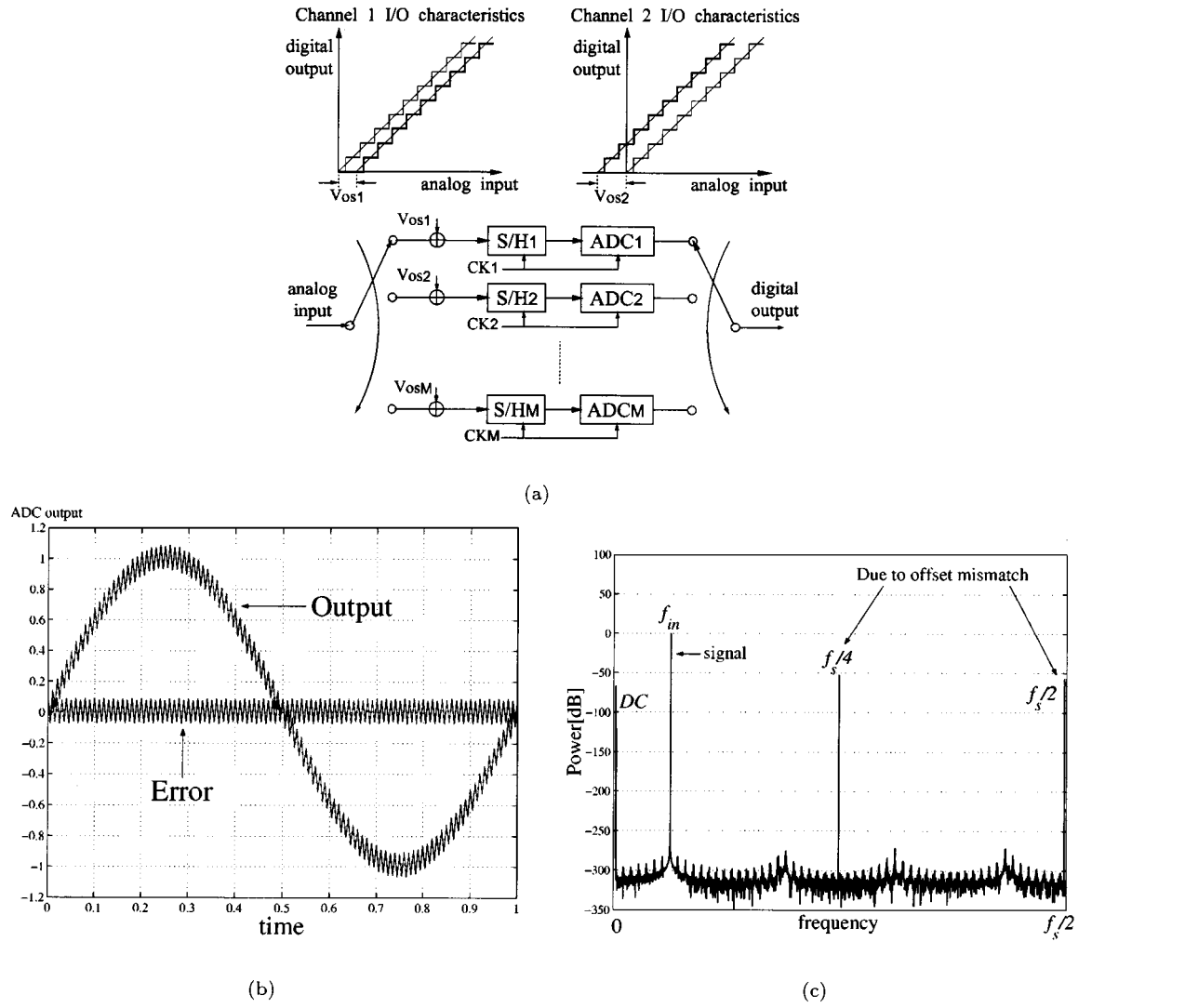

Fig. 2 Offset mismatch effect. (a) Offset mismatch model. Vos_k represents the offset of kth channel $(k = 1, 2, \cdots, M)$. (b) ADC output and error signals in time domain for a sinusoidal input. (c) ADC output power spectrum.

A. Offset Mismatch Effects

Suppose that the offsets of each channel are different and the other characteristics are identical (Fig. 2). This mismatch causes *fixed pattern noise* in the ADC system. For a dc input, each channel may produce a different output code and the period of this error signal is M/f_s. The pattern noise is almost independent of the input signal in time and frequency domains, and it is additive noise in time domain while in frequency domain it causes noise peaks at

$$f_{\text{noise}} = k \times f_s/M, \qquad k = 1, 2, 3, \ldots.$$

The *S/N* degradation of the ADC system (total pattern-noise power) due to the offset mismatch is constant regardless of the input frequency and amplitude (Fig. 3).

B. Gain Mismatch Effects

Suppose that the gains of each channel are different and the other characteristics are identical (Fig. 4). If a sinusoidal input

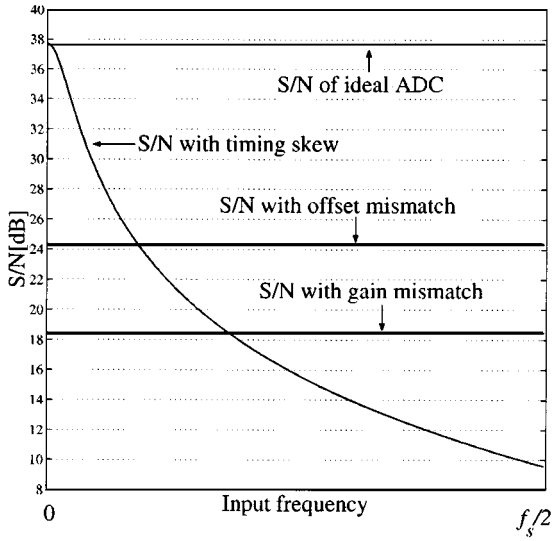

Fig. 3. Simulation results of *S/N* versus f_{in} of a four-channel 6-bit interleaved ADC system in offset, gain and timing mismatch cases.

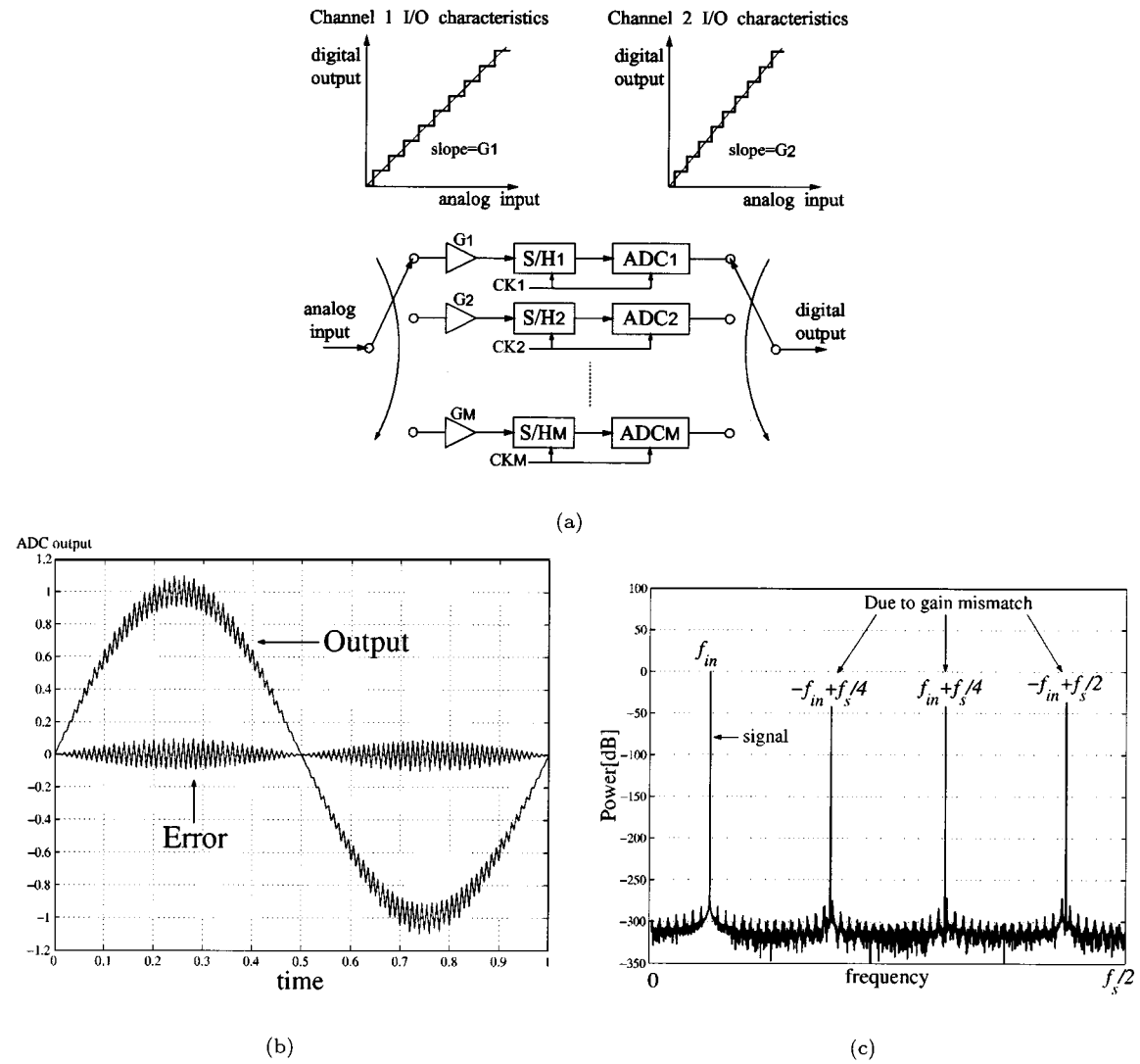

Fig. 4. Gain mismatch effect. (a) Gain mismatch model. G_k represents the gain of kth channel ($k = 1, 2, \ldots, M$). (b) ADC output and error signals in time domain for a sinusoidal input. (c) ADC output power spectrum.

signal is applied to the system, the largest difference in channel outputs occurs at the peaks of the sine wave. As with the offset mismatch case, the basic error occurs with a period of M/f_s but the magnitude of the error is modulated by the input frequency f_{in}. Thus, the pattern noise due to gain mismatch is multiplicative in time domain—which is like amplitude modulation (AM) noise—while noise spectrum peaks are at

$$f_{\text{noise}} = \pm f_{\text{in}} + \frac{k}{M} f_s, \qquad k = 1, 2, 3, \ldots.$$

f_{noise} depends on f_{in} (Fig. 4) while the *S/N* degradation of the ADC system due to the gain mismatch is independent of f_{in} (Fig. 3). Also, note that in the offset mismatch case, the *S/N* degradation (noise power) is independent of the amplitude of the input but in the gain mismatch case, it depends on the amplitude.

C. Clock Timing Error Effects

There are two kinds of timing errors in an interleaved ADC system, clock skew (systematic error) and clock jitter (random error). Clock jitter effects are unavoidable in any ADC system but the interleaved architecture also suffers from clock skew effects. Suppose that the clocks $CK_1, CK_2, \cdots, CK_M$ have skews $dt_1, dt_2, \cdots, dt_M$ (Fig. 5). This skew causes noise in the ADC system, and in the time domain the largest error occurs when the input signal has the largest slew rate, or crosses zero, which is like phase modulation (PM) noise (Fig. 6). The envelope of the error signal is the largest at the zero-crossings with a period of M/f_s. It is shifted by 90 deg compared to the gain mismatch case. In the frequency domain, as with the gain mismatch case, the basic error occurs with a period of M/f_s and the magnitude of the error is modulated by the input frequency f_{in}. The noise spectrum peaks are at

$$f_{\text{noise}} = \pm f_{\text{in}} + \frac{k}{M} f_s, \qquad k = 1, 2, 3, \ldots.$$

Note, that *S/N* degrades as f_{in} increases (Fig. 3).

Remark: In offset and gain mismatch cases, the signal power at the output keeps constant as f_{in} increases. On the other hand, in the timing skew case, the signal power at the output decreases as f_{in} increases, while the total power of the signal and the error at the output keeps constant.

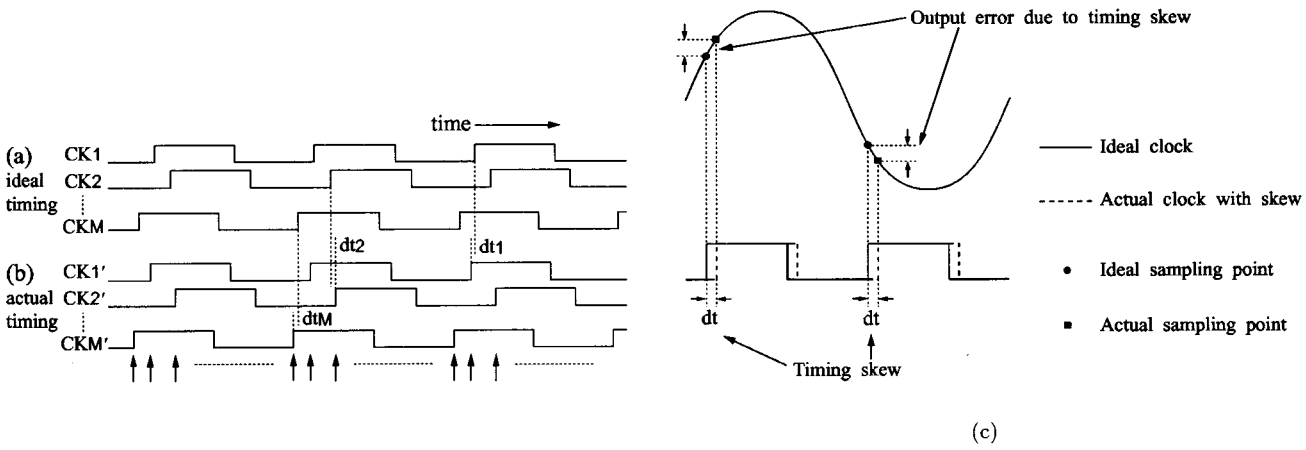

Fig. 5. Clock skew: (a) Ideal clock timing. (b) Clock timing with skews of $dt_1, dt_2, \ldots, dt_M$. (c) Timing skew causes error for the sampled data.

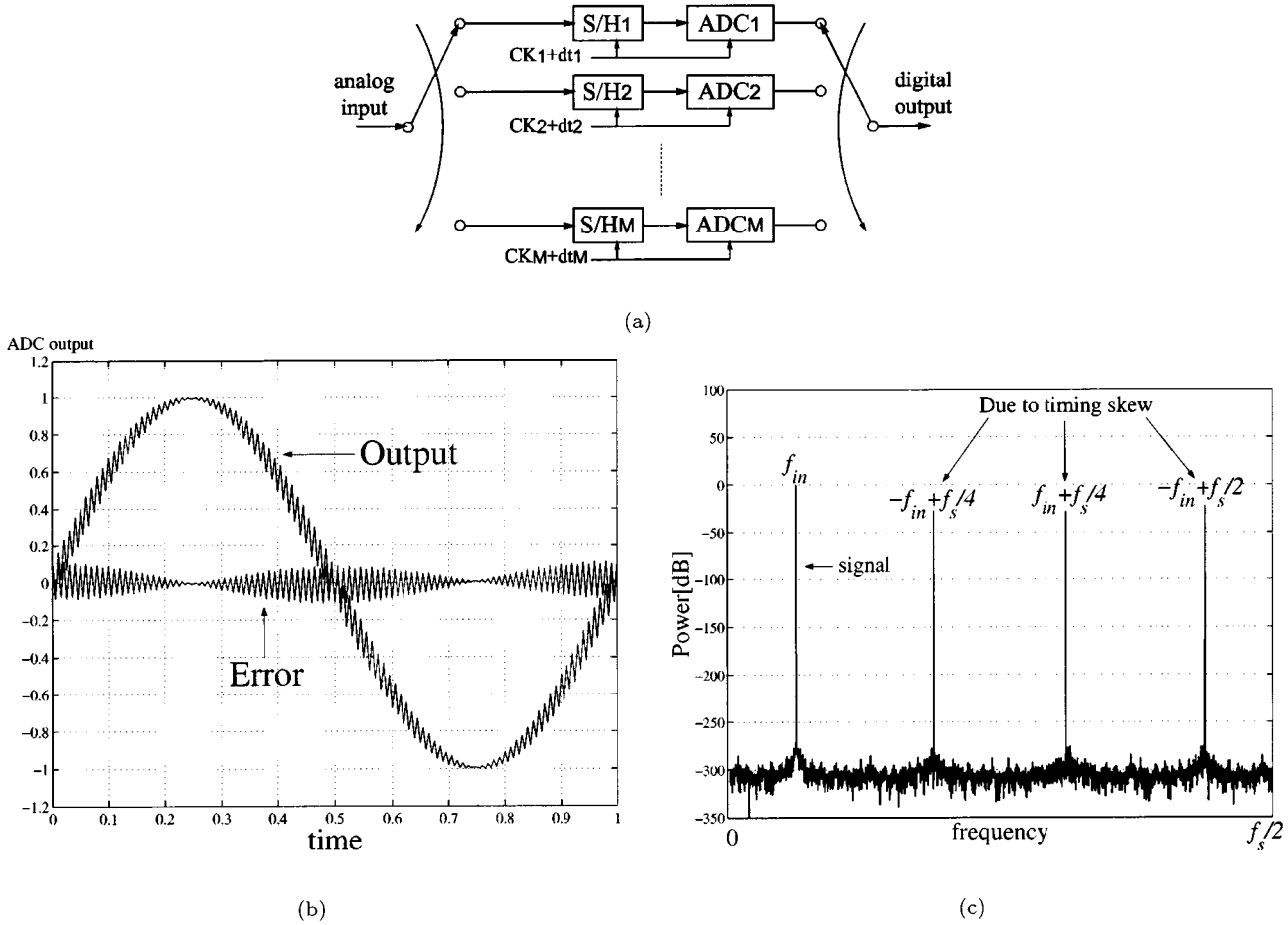

Fig. 6. Timing skew effect. (a) Timing skew model. dt_k represents the skew of kth clock ($k = 1, 2, \ldots, M$). (b) ADC output and error signals in time domain for a sinusoidal input. (c) ADC output power spectrum.

III. Combined Channel Mismatch Effects

In this section, we will derive *explicit* formulas for the mismatch effects when all of offset, gain and timing mismatches exist together, and show that the gain and timing mismatch effects interact each other but the offset mismatch effect is independent of them.

A. Two-channel Interleaved ADC ($M = 2$)

First, we consider a two-channel interleaved ADC system. Fig. 7 shows its configuration where each of two-channel ADCs (ADC_1, ADC_2) operates with one of two-phase clocks (Φ_1, Φ_2 with a period of $2T_s$), respectively. The sampling rate (f_s, where $f_s \triangleq 1/T_s$) of the ADC as a whole is twice the channel sampling rate. However, as mentioned before, this interleaved ADC

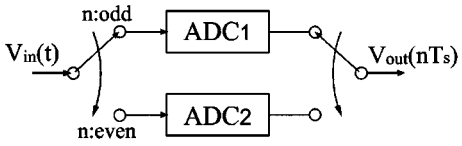

Fig. 7. Two-channel time-interleaved ADC system.

system suffers from channel mismatch effects [8], [9], [11]: gain mismatch, offset mismatch and timing mismatch. Ideally, ADC_1 and ADC_2 should be identical. However, in reality, their gains and offsets may be different from each other, and also the sampling timings may deviate from Φ_1 and Φ_2. Let the gains of ADC_1, ADC_2 be G_1, G_2 respectively, and their offsets be os_1, os_2 respectively. Also, let the sampling timing deviations from Φ_1 for ADC_1 and Φ_2 for ADC_2 be δt_1, δt_2 respectively. Suppose that the input to the ADC is a sinusoidal signal $V_{\mathrm{in}}(t) = A\cos(2\pi f_{\mathrm{in}} t)$. Then, the output of the two-channel interleaved system is given as follows:

$$V_{\mathrm{out}}(n) = \begin{cases} G_1 A\cos[2\pi f_{\mathrm{in}}(nT_s + \delta t_1)] + os_1 & (n\text{: odd}) \\ G_2 A\cos[2\pi f_{\mathrm{in}}(nT_s + \delta t_2)] + os_2 & (n\text{: even}). \end{cases} \tag{1}$$

Let

$$\begin{aligned} G &\triangleq (G_1 + G_2)/2 & \alpha &\triangleq (G_2 - G_1)/(2G) \\ \delta t_{cm} &\triangleq (\delta t_1 + \delta t_2)/2 & \delta t &\triangleq \delta t_2 - \delta t_1 \\ os_{cm} &\triangleq (os_1 + os_2)/2 & os_{\mathrm{diff}} &\triangleq (os_2 - os_1)/2. \end{aligned} \tag{2}$$

Without loss of generality, we choose the timing reference so that $\delta t_{cm} = 0$. Then, we obtain the following:

$$\begin{aligned} V_{\mathrm{out}}(nT_s) = {} & A_s\cos(2\pi f_{\mathrm{in}} nT_s + \theta_s) \\ & + A_n\cos\left[2\pi\left(-f_{\mathrm{in}} + \tfrac{1}{2} f_s\right) nT_s + \theta_n\right] \\ & + os_{cm} + \cos(\pi n) os_{\mathrm{diff}} \end{aligned} \tag{3}$$

where

$$\begin{aligned} A_s &\triangleq AG\sqrt{\cos^2(\pi f_{\mathrm{in}}\delta t) + \alpha^2\sin^2(\pi f_{\mathrm{in}}\delta t)} \\ A_n &\triangleq AG\sqrt{\alpha^2\cos^2(\pi f_{\mathrm{in}}\delta t) + \sin^2(\pi f_{\mathrm{in}}\delta t)} \\ \theta_s &\triangleq \arctan[\alpha\tan(\pi f_{\mathrm{in}}\delta t)] \\ \theta_n &\triangleq -\arctan[\tan(\pi f_{\mathrm{in}}\delta t)/\alpha]. \end{aligned}$$

Remark:

1) $V_{\mathrm{out}}(nT_s)$ given by (3) has four frequency components; the frequency of the first term in (3) is f_{in}, that of the second term is $-f_{\mathrm{in}} + (1/2)f_s$, the third one is 0 (dc) and the fourth one is $(1/2)f_s$. In other words, the first term corresponds to signal while the second term is due to gain and timing mismatches and the third term is caused by the average offset of ADC_1 and ADC_2 while the fourth term is caused by offset mismatch.
2) Equation (3) that we have newly derived considers the gain, offset and timing mismatches together and hence this is a very general result. However, in previous references [5], [6], [8]–[11] each channel mismatch effect in interleaved ADC systems is discussed only individually.
3) From (3) we see that the effects of gain and timing mismatch interact each other while the offset mismatch effect is independent.
4) Numerical simulations show that (1) and (3) match exactly; in both cases, the power at dc is −47.959 dB, the power and phase at f_{in} are −0.017 038 dB, 0.107 82 deg, those at $f_{\mathrm{in}} + f_s/2$ are −23.1736 dB, −64.439 deg and those at $f_s/2$ are −54.8945 dB, 0.0 deg with the simulation conditions in the caption of Fig. 8, where the simulated power spectrum is shown.
5) Fig. 9 shows numerical simulation result for the SNR due to gain mismatch and timing skew which would be useful for designing a two-channel interleaved system. In Fig. 9, the horizontal axis indicates timing skew δt normalized by the input frequency f_{in}, and the vertical axis shows the

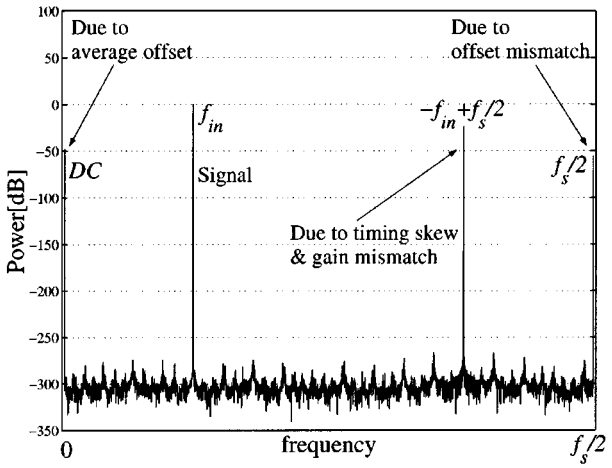

Fig. 8. Simulation result of a two-channel time-interleaved ADC system with channel mismatches which verifies the correctness of our derived equation (3). 8192-point FFT was performed with $A = 1$, $G = 1$, $f_{\mathrm{in}}/f_s = 997/8192$, gain mismatch of $\alpha = 0.03$, timing mismatch of $\delta t = 2.0 \times 10^{-5}$, average offset of $os_{cm} = 2.0 \times 10^{-3}$, and offset mismatch of $os_{\mathrm{diff}} = 9.0 \times 10^{-4}$ in (1) and (2).

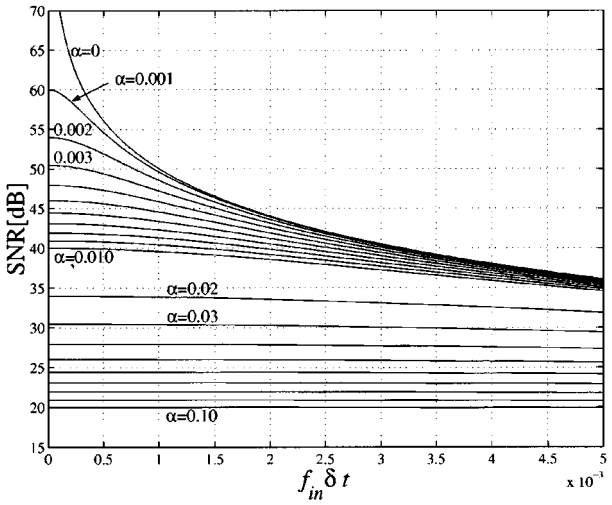

Fig. 9. Simulation result of SNR of a two-channel interleaved ADC system with gain mismatch (α) and timing skew (δt) based on (3).

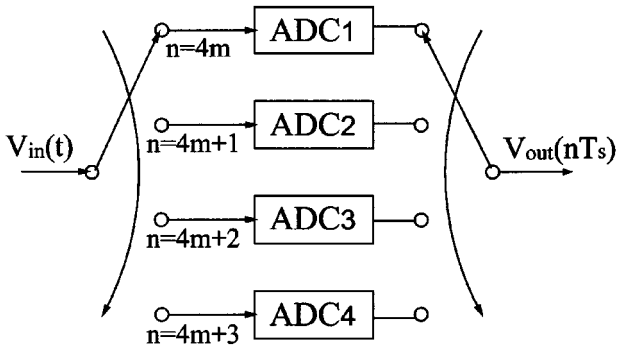

Fig. 10. Four-channel time-interleaved ADC system.

SNR of the two-channel interleaved ADC system with a parameter of gain mismatch α. For example we can see in Fig. 9 that gain matching better than 0.1% is required to obtain SNR better than 54 dB for $f_{\text{in}}\delta t \leq 0.5 \times 10^{-3}$. Note that the offset mismatch effect is not included in Fig. 9, however, it is independent of gain and timing mismatch effects and it can be simply added to them.

Fact 1: The total power P_{out1} of the signal and noise at the whole system output is given by

$$P_{\text{out1}} = \tfrac{1}{4}A^2(G_1^2 + G_2^2) + \tfrac{1}{2}(os_1^2 + os_2^2).$$

Proof: See Appendix III.

B. Four-channel Interleaved ADC $(M = 4)$

Next, we consider a four-channel interleaved ADC system, and Fig. 10 shows its configuration. Similarly, let the gains of ADC_1, ADC_2, ADC_3, ADC_4 be G_1, G_2, G_3, G_4, respectively, and their offsets be os_1, os_2, os_3, os_4, respectively. Also, let the sampling timing deviations be $\delta t_1, \delta t_2\, \delta t_3, \delta t_4$, respectively. Suppose that the input to the ADC is a sinusoidal signal $V_{\text{in}}(t) = A\cos(2\pi f_{\text{in}} t)$. Then, the output of the four-channel interleaved system is given as follows:

$$V_{\text{out}}(n) = \begin{cases} G_1 A\cos[2\pi f_{\text{in}}(nT_s + \delta t_1)] + os_1 & (n = 4m) \\ G_2 A\cos[2\pi f_{\text{in}}(nT_s + \delta t_2)] + os_2 & (n = 4m+1) \\ G_3 A\cos[2\pi f_{\text{in}}(nT_s + \delta t_3)] + os_3 & (n = 4m+2) \\ G_4 A\cos[2\pi f_{\text{in}}(nT_s + \delta t_4)] + os_4 & (n = 4m+3) \end{cases} \quad (4)$$

where $m = 0, \pm 1, \pm 2, \pm 3, \ldots$, and let

$$\begin{aligned} G_1 &\triangleq G(1+\alpha_1) & G_2 &\triangleq G(1+\alpha_2) \\ G_3 &\triangleq G(1+\alpha_3) & G_4 &\triangleq G(1+\alpha_4) \end{aligned} \quad (5)$$

where

$$G \triangleq \frac{G_1 + G_2 + G_3 + G_4}{4}.$$

Without loss of generality, we choose the timing reference so that

$$\delta t_1 + \delta t_2 + \delta t_3 + \delta t_4 = 0.$$

Then, we obtain the following:

$$\begin{aligned} &V_{\text{out}}(nT_s) \\ &= A_{s4}\cos\left(2\pi f_{\text{in}} nT_s - \arctan\frac{A_{ss}}{A_{sc}}\right) \\ &\quad + A_{n1}\cos\left[2\pi nT_s\left(f_{\text{in}} + \frac{1}{4}f_s\right) - \arctan\frac{A_{n1s}}{A_{n1c}}\right] \\ &\quad + A_{n2}\cos\left[2\pi nT_s\left(f_{\text{in}} + \frac{1}{2}f_s\right) - \arctan\frac{A_{n2s}}{A_{n2c}}\right] \\ &\quad + A_{n3}\cos\left[2\pi nT_s\left(f_{\text{in}} + \frac{3}{4}f_s\right) - \arctan\frac{A_{n3s}}{A_{n3c}}\right] \\ &\quad + \tfrac{1}{4}(os_1 - os_2 + os_3 - os_4)\cos\left[2\pi nT_s\left(\tfrac{1}{2}f_s\right)\right] \\ &\quad + \tfrac{1}{2}\sqrt{(os_1 - os_3)^2 + (os_2 - os_4)^2} \\ &\quad \times \cos\left[2\pi nT_s\left(\frac{1}{4}f_s\right) - \arctan\frac{os_2 - os_4}{os_1 - os_3}\right] \\ &\quad + (os_1 + os_2 + os_3 + os_4)/4 \end{aligned} \quad (6)$$

where

$$\begin{aligned} A_{s4} &\triangleq \sqrt{A_{sc}^2 + A_{ss}^2} & A_{n1} &\triangleq \sqrt{A_{n1c}^2 + A_{n1s}^2} \\ A_{n2} &\triangleq \sqrt{A_{n2c}^2 + A_{n2s}^2} & A_{n3} &\triangleq \sqrt{A_{n3c}^2 + A_{n3s}^2} \end{aligned}$$

and A_{sc}, A_{ss}, A_{n1c}, A_{n1s}, A_{n2c}, A_{n2s}, A_{n3c}, A_{n3s} are defined in Appendix I.

Remark:

1) Similar arguments described in two-channel case are valid for the four-channel case.
2) Numerical simulation shows that (4) and (6) match exactly; in both cases, the power at dc is -66.021[dB], the power and phase at f_{in} are $-0.041\,198$ [dB], 0.092 319 9 [deg], those at $-f_{\text{in}} + f_s/4$ are -27.164 [dB], 73.792 [deg], those at $f_s/4$ are -52.041 [dB], 0.0 [deg], those at $-f_{\text{in}} + f_s/2$ are -21.945 [dB], 80.336 [deg], those at $f_{\text{in}} + 3f_s/4$ are -28.296 [dB], -84.706 [deg] and those at $f_s/2$ are -56.478 [dB], 0.0 [deg] with the simulation conditions in the caption of Fig. 11, where the simulated power spectrum is shown.
3) Fig. 12 shows numerical simulation result for the SNR due to the gain mismatch and timing skew which would be useful for designing a four-channel interleaved system, as similar to Fig. 9 in two-channel case.

Fact 2: The total power P_{out2} of the signal and noise at the whole system output is given by

$$\begin{aligned} P_{\text{out2}} = \tfrac{1}{8}A^2(G_1^2 + G_2^2 + G_3^2 + G_4^2) \\ + \tfrac{1}{4}(os_1^2 + os_2^2 + os_3^2 + os_4^2). \end{aligned}$$

Proof: See Appendix III

IV. Bandwidth Mismatch Effect

In this section, we will introduce a rather new problem, *bandwidth mismatch*, in an interleaved ADC or an interleaved sampling system, and then we will derive the explicit formulas for its effects. Many electrical circuits can be approximated by a

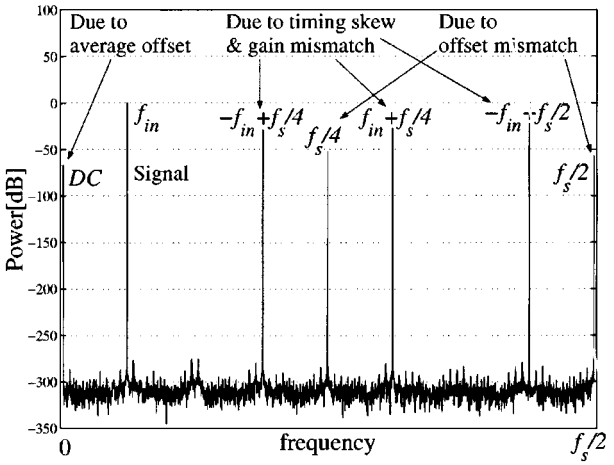

Fig. 11. Simulation result of a four-channel time-interleaved ADC system with channel mismatches which verifies the correctness of our derived equation (6). 8192-point FFT was performed with $A = 1, G = 1, f_{\rm in}/f_s = 499/8192$, gain mismatches of ($\alpha_1 = 0.03, \alpha_2 = -0.02, \alpha_3 = 0.0$ and $\alpha_4 = -0.01$), timing mismatches of ($\delta t_1 = 5.0 \times 10^{-5}, \delta t_2 = -2.0 \times 10^{-5}, \delta t_3 = 0.0$ and $\delta t_4 = -3.0 \times 10^{-5}$), and offset mismatches of ($os_1 = 2.0 \times 10^{-3}$, $os_2 = 1.0 \times 10^{-3}, os_4 = -3.0 \times 10^{-3}$ and $os_5 = 1.0 \times 10^{-3}$) in eqs. (4) and (5).

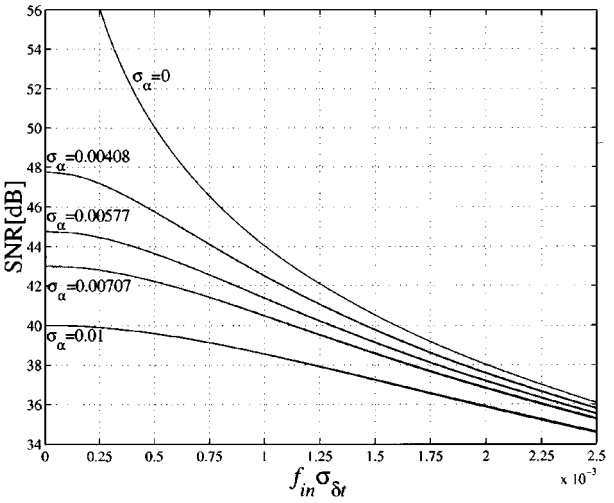

Fig. 12. Simulation result of SNR of a four-channel interleaved ADC system with gain mismatch (gain deviation of $\sigma_\alpha \triangleq \sqrt{(\alpha_1^2 + \alpha_2^2 + \alpha_3^2 + \alpha_4^2)/4}$) and timing skew (timing skew deviation of $\sigma_{\delta t} \triangleq \sqrt{(\delta t_1^2 + \delta t_2^2 + \delta t_3^2 + \delta t_4^2)/4}$) based on equation (6).

first-order system (Fig. 13). A typical example is an open-loop track/hold circuit in track mode, where the ON-resistance of the sampling switch and the hold capacitor constitute a first-order RC circuit. Here we assume that kth channel ADC is approximated by a first-order system and its bandwidth is given by f_{ck}, which can be mismatched among channels while there are no mismatches of offset, dc gain and timing discussed in the previous sections. (The reader may argue that the approximation of an ADC to a first-order system might be too inaccurate, however, for a track/hold circuit in track mode this approximation is very reasonable and hence the discussion in this section is applicable at least to interleaved sampling systems which consist of an array of track/hold circuits.) Setting the dc gain of

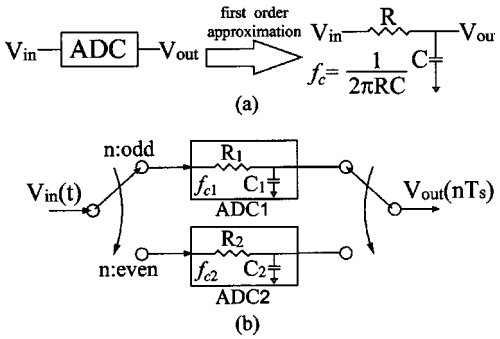

Fig. 13. Bandwidth mismatch model. (a) Approximation of an ADC to the first-order system. (b) Bandwidth mismatch model in two-channel case.

each channel to one, without loss of generality, and then the frequency transfer function $H_k(j2\pi f)$ of kth channel is given by

$$H_k(j2\pi f) = 1/(1 + jf/f_{ck})$$

and for the input of $V_{\rm in}(t) = A\cos(2\pi f_{\rm in}t)$, the output $V_{{\rm out}k}(nT_s)$ of kth channel is given by

$$V_{{\rm out}k}(nT_s) = G_k A\cos(2\pi f_{\rm in}nT_s + \theta_k)$$

where

$$G_k = 1\Big/\sqrt{1 + (f_{\rm in}/f_{ck})^2} \tag{7}$$

$$\theta_k = -\arctan(f_{\rm in}/f_{ck}). \tag{8}$$

We see that the mismatch of the bandwidth f_{ck} among channels ($k = 1, 2, \cdots, n$) causes G_k and θ_k mismatches. Note that G_k and θ_k are functions of the input frequency $f_{\rm in}$ as well as the bandwidth f_{ck}, and also note that when $f_{\rm in} = 0$, $G_k = 1$ and $\theta_k = 0$. Then, we will call the mismatch of G_k as *ac gain mismatch* and also the mismatch of θ_k as *ac phase mismatch*. Remark that the ac gain mismatch is different from the gain mismatch discussed in Sections II and III in that ac gain mismatch depends on $f_{\rm in}$ but the gain mismatch discussed before does not. Also, note that the ac phase mismatch due to the bandwidth mismatch is a *nonlinear* function of the input frequency $f_{\rm in}$ while the phase mismatch due to the timing skew is its *linear* function.

A. Two-Channel Interleaved ADC ($M = 2$)

We consider a two-channel interleaved ADC system, where the bandwidth of each channel is given by f_{c1} and f_{c2} respectively [Fig. 13(b)]. Then, when an input of $V_{\rm in}(t) = A\cos(2\pi f_{\rm in}t)$ is applied, the output of the interleaved system is given by

$$V_{\rm out}(n) = \begin{cases} G_1 A\cos(2\pi f_{\rm in}nT_s + \theta_1) & (n\text{: odd}) \\ G_2 A\cos(2\pi f_{\rm in}nT_s + \theta_2) & (n\text{: even}) \end{cases} \tag{9}$$

where G_1, G_2, θ_1 and θ_2 are defined in (7) and (8). Then we can obtain the following formulas:

$$V_{\rm out}(nT_s) = B_s\cos(2\pi f_{\rm in}nT_s + \theta_s) + B_n\cos[2\pi(-f_{\rm in} + f_s/2)nT_s + \theta_n] \tag{10}$$

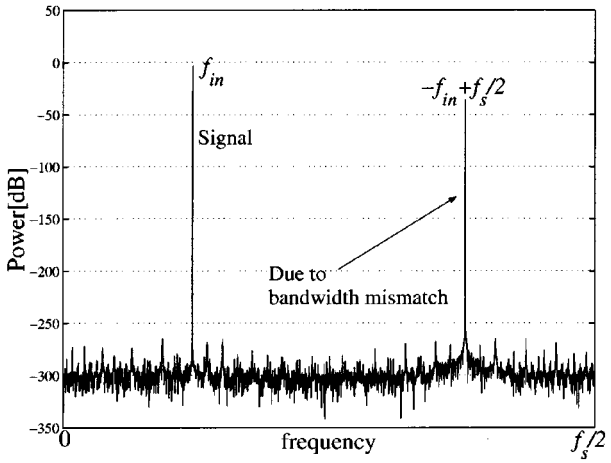

Fig. 14. Simulation result of a two-channel time-interleaved ADC system with bandwidth mismatch which verifies the correctness of our derived equation (10). Here $A = 1$, $f_{c1}/f_s = 3200/(8192\pi)$, $f_{c2}/f_s = 3000/(8192\pi)$, $f_{\rm in}/f_s = 997/8192$ are used, and 8192-point FFT is performed.

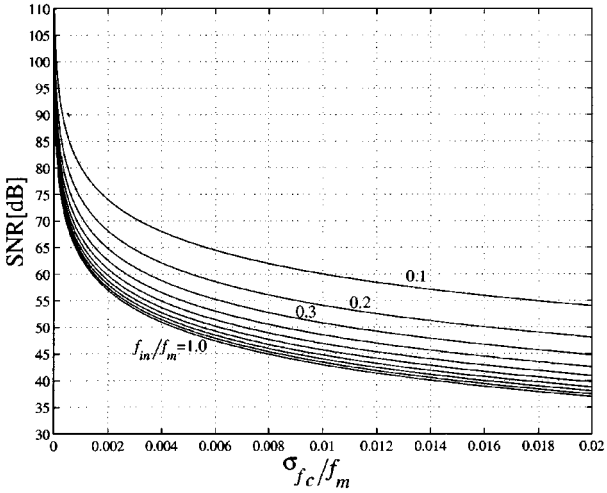

Fig. 15. Simulation result of SNR of a two-channel interleaved ADC system with bandwidth mismatch based on (10). Here, $f_m \triangleq (f_{c1} + f_{c2})/2$ (average cut-off frequency) and $\sigma_{f_c} \triangleq |f_{c1} - f_{c2}|/2$ (cut-off frequency deviation between two channels). $f_{\rm in}/f_s = 997/8192$ is used and 8192-point FFT is performed.

where

$$
\begin{aligned}
B_s &\triangleq \tfrac{1}{2} A\sqrt{G_c^2\cos^2(\theta_d) + G_d^2\sin^2(\theta_d)} \\
B_n &\triangleq \tfrac{1}{2} A\sqrt{G_c^2\sin^2(\theta_d) + G_d^2\cos^2(\theta_d)} \\
\theta_s &\triangleq \arctan\left[\frac{G_c\sin(\theta_c)\cos(\theta_d) + G_d\cos(\theta_c)\sin(\theta_d)}{G_c\cos(\theta_c)\cos(\theta_d) - G_d\sin(\theta_c)\sin(\theta_d)}\right] \\
\theta_n &\triangleq \arctan\left[\frac{G_c\cos(\theta_c)\sin(\theta_d) + G_d\sin(\theta_c)\cos(\theta_d)}{G_c\sin(\theta_c)\sin(\theta_d) - G_d\cos(\theta_c)\cos(\theta_d)}\right] \\
G_d &\triangleq G_1 - G_2 \qquad G_c \triangleq G_1 + G_2 \\
\theta_d &\triangleq (\theta_1 - \theta_2)/2 \qquad \theta_c \triangleq (\theta_1 + \theta_2)/2.
\end{aligned}
$$

Also, SNR due to the bandwith mismatch is given by

$$\text{SNR} = 10\log_{10}(B_s^2/B_n^2)\ \text{dB}.$$

Remark:

1) Numerical simulation shows that (9) and (10) match exactly; in both cases the power and phase at $f_{\rm in}$ are -2.8844 [dB], -44.127 [deg] and that at $-f_{\rm in} + f_s/2$ is -35.852 [dB], -1.7165 [deg]. with the simulation conditions in the caption of Fig. 14, where the simulated power spectrum is shown.
2) Fig. 15 shows numerical simulation result for SNR versus $|f_{c1} - f_{c2}|/(f_{c1} + f_{c2})$ due to the bandwidth mismatch, which would be useful for the designer to know how much bandwidth mismatch is tolerable for a specified SNR. Note that our simulation shows that SNR does not depend on $f_{\rm in}/f_s$.

Fact 3: The total power $P_{\rm out3}$ of the signal and noise at the whole system output is given by

$$P_{\rm out3} = \frac{1}{4}A^2\left[\frac{1}{1+(f_{\rm in}/f_{c1})^2} + \frac{1}{1+(f_{\rm in}/f_{c2})^2}\right].$$

Proof: See Appendix III.

B. Four-channel Interleaved ADC ($M = 4$)

Next, we consider a four-channel interleaved ADC system, where the bandwidth of each channel is given by f_{c1}, f_{c2} f_{c3} and f_{c4} respectively. Then when the input of $V_{\rm in}(t) = A\cos(2\pi f_{\rm in}t + \theta)$ is applied, the output of the interleaved system is given by

$$V_{\rm out}(nT_s) = \begin{cases} G_1 A\cos(2\pi f_{\rm in}nT_s + \theta_1) & (n = 4m) \\ G_2 A\cos(2\pi f_{\rm in}nT_s + \theta_2) & (n = 4m+1) \\ G_3 A\cos(2\pi f_{\rm in}nT_s + \theta_3) & (n = 4m+2) \\ G_4 A\cos(2\pi f_{\rm in}nT_s + \theta_4) & (n = 4m+3) \end{cases} \tag{11}$$

where

$$\theta + \tfrac{1}{4}(\theta_1 + \theta_2 + \theta_3 + \theta_4) = 0$$

and $G_1, G_2, G_3, G_4, \theta_1, \theta_2, \theta_3$ and θ_4 are defined in (7) and (8). Then, we can obtain the following formulas:

$$
\begin{aligned}
&V_{\rm out}(nT_s) \\
&\quad = B_{s4}\cos\left[2\pi f_{\rm in}nT_s - \arctan\frac{B_{ss}}{B_{sc}}\right] \\
&\qquad + B_{n1}\cos\left[2\pi\left(f_{\rm in} + \frac{1}{4}f_s\right)nT_s - \arctan\frac{B_{n1s}}{B_{n1c}}\right] \\
&\qquad + B_{n2}\cos\left[2\pi\left(f_{\rm in} + \frac{1}{2}f_s\right)nT_s - \arctan\frac{B_{n2s}}{B_{n2c}}\right] \\
&\qquad + B_{n3}\cos\left[2\pi\left(f_{\rm in} + \frac{3}{4}f_s\right)nT_s - \arctan\frac{B_{n3s}}{B_{n3c}}\right]
\end{aligned} \tag{12}
$$

where

$$
\begin{aligned}
B_{s4} &\triangleq \sqrt{B_{sc}^2 + B_{ss}^2} \qquad B_{n1} \triangleq \sqrt{B_{n1c}^2 + B_{n1s}^2} \\
B_{n2} &\triangleq \sqrt{B_{n2c}^2 + B_{n2s}^2} \qquad B_{n3} \triangleq \sqrt{B_{n3c}^2 + B_{n3s}^2}
\end{aligned}
$$

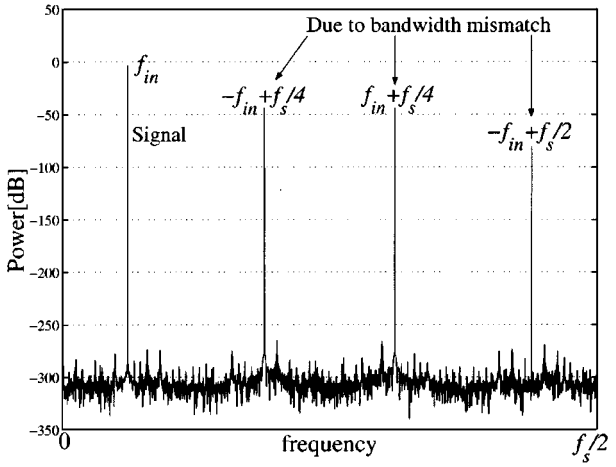

Fig. 16. Simulation result of a four-channel time-interleaved ADC system with bandwidth mismatch which verifies the correctness of our derived equation. (12). Here, $A = 1$, $f_{c1}/f_s = 1575/(8192\pi)$, $f_{c2}/f_s = 1600/(8192\pi)$, $f_{c3}/f_s = 1550/(8192\pi)$, $f_{c4}/f_s = 1525/(8192\pi)$, $f_{\rm in}/f_s = 499/8192$ are used, and 8192-point FFT is performed.

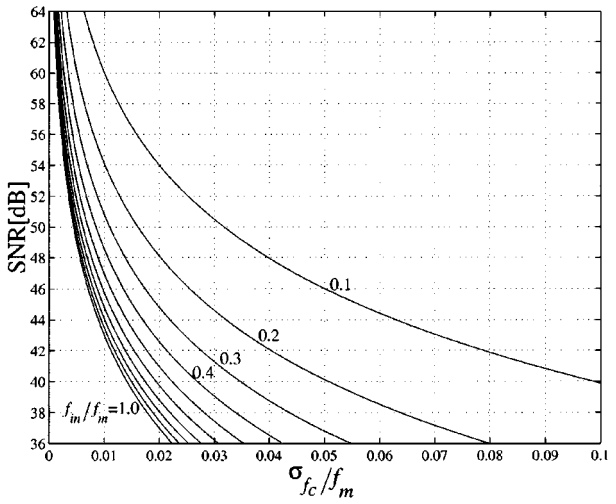

Fig. 17. Simulation result of SNR of a four-channel interleaved ADC system with bandwidth mismatch based on (12). Here we consider the case that $f_{c1} < f_{c2} < f_{c3} < f_{c4}$ and $f_{c2} - f_{c1} = f_{c3} - f_{c2} = f_{c4} - f_{c3}$. In the graph $f_m \triangleq (f_{c1} + f_{c2} + f_{c3} + f_{c4})/4$ (average cut-off frequency) and $\sigma_{f_c} \triangleq \sqrt{(f_{c1} - f_m)^2 + (f_{c2} - f_m)^2 + (f_{c3} - f_m)^2 + (f_{c4} - f_m)^2)/4}$ (cut-off frequency deviation among four channels). 8192-point FFT is performed, and $f_{\rm in}/f_s = 997/8192$ is used.

and B_{sc}, B_{ss}, B_{n1c}, B_{n1s}, B_{n2c}, B_{n2s}, B_{n3c} and B_{n3s} are defined in Appendix II. The SNR is given by

$$\text{SNR} = 10\log_{10}\frac{B_s^2}{B_{n1}^2 + B_{n2}^2 + B_{n3}^2}\ \text{dB}.$$

Remark:

1) Numerical simulation shows that (11) and (12) match exactly; in both cases, the power and phase at $f_{\rm in}$ are -3.0260 [dB], 0.004 601 13 [deg], those at $-f_{\rm in} + f_s/4$ are -43.980 [dB], -26.670 [deg], those at $-f_{\rm in} + f_s/2$ are -80.880 [dB], $-0.202\,41$[deg] and those at $-f_{\rm in} + 3f_s/4$ are -43.979 [dB], -63.540 [deg] with the simulation conditions in the caption of Fig. 16, where the simulated power spectrum is shown.
2) Fig. 17 shows numerical simulation result for SNR versus (cut-off frequency deviation among four channels)/(average cut-off frequency) due to the bandwidth mismatch, which would be useful for the designer to know how much bandwidth mismatch is tolerable for a specified SNR. Note that our simulation shows that SNR does not depend on $f_{\rm in}/f_s$.

Fact 4: The total power $P_{\rm out4}$ of the signal and noise at the whole system output is given by

$$P_{\rm out4} = \frac{1}{8}A^2\left[\frac{1}{1+(f_{\rm in}/f_{c1})^2} + \frac{1}{1+(f_{\rm in}/f_{c2})^2} + \frac{1}{1+(f_{\rm in}/f_{c3})^2} + \frac{1}{1+(f_{\rm in}/f_{c4})^2}\right].$$

Proof: See Appendix III.

V. Conclusion

We have analyzed the channel mismatch effects in the time-interleaved ADC system, and derived *explicit* formulas for the mismatch effects when *all* of offset, gain and timing mismatches exist together. We have clarified that the gain and timing mismatch effects interact with each other but the offset mismatch effect is independent of them. Also, we discussed the bandwidth mismatch effect (ac mismatch effect). We have shown several graphs calculated from these formulas, which are useful for the designer to know how much mismatch is tolerable for a specified SNR. Finally, we remark that we are investigating the following as on-going projects for the time-interleaved ADC system:

- Combined channel mismatch effects for all four of offset, gain, timing and bandwidth.
- Channel linearity mismatch effects.[12]
- Algorithms to measure mismatch values and compensate for them.

Appendix I

This appendix gives definitions of A_{sc}, A_{ss}, A_{n1c}, A_{n1s}, A_{n2c}, A_{n2s}, A_{n3c}, and A_{n3s} used in Section III-B.

$$\begin{aligned}
A_{sc} \triangleq &+\tfrac{1}{4}A(G_1+G_3)\cos(\phi)\cos(\phi_{13})\\
&+\tfrac{1}{4}A(G_2+G_4)\cos(\phi)\cos(\phi_{24})\\
&-\tfrac{1}{4}A(G_1-G_3)\sin(\phi)\sin(\phi_{13})\\
&+\tfrac{1}{4}A(G_2-G_4)\sin(\phi)\sin(\phi_{24})\\
A_{ss} \triangleq &-\tfrac{1}{4}A(G_1+G_3)\sin(\phi)\cos(\phi_{13})\\
&+\tfrac{1}{4}A(G_2+G_4)\sin(\phi)\cos(\phi_{24})\\
&-\tfrac{1}{4}A(G_1-G_3)\cos(\phi)\sin(\phi_{13})\\
&-\tfrac{1}{4}A(G_2-G_4)\cos(\phi)\sin(\phi_{24})\\
A_{n1c} \triangleq &-\tfrac{1}{4}A(G_1+G_3)\sin(\phi)\sin(\phi_{13})\\
&+\tfrac{1}{4}A(G_2+G_4)\cos(\phi)\sin(\phi_{24})\\
&+\tfrac{1}{4}A(G_1-G_3)\cos(\phi)\cos(\phi_{13})\\
&-\tfrac{1}{4}A(G_2-G_4)\sin(\phi)\cos(\phi_{24})
\end{aligned}$$

$$
\begin{aligned}
A_{n1s} \triangleq & -\tfrac{1}{4} A(G_1+G_3)\cos(\phi)\sin(\phi_{13}) \\
& +\tfrac{1}{4} A(G_2+G_4)\sin(\phi)\sin(\phi_{24}) \\
& -\tfrac{1}{4} A(G_1-G_3)\sin(\phi)\cos(\phi_{13}) \\
& +\tfrac{1}{4} A(G_2-G_4)\cos(\phi)\cos(\phi_{24}) \\
A_{n2c} \triangleq & +\tfrac{1}{4} A(G_1+G_3)\cos(\phi)\cos(\phi_{13}) \\
& -\tfrac{1}{4} A(G_2+G_4)\cos(\phi)\cos(\phi_{24}) \\
& -\tfrac{1}{4} A(G_1-G_3)\sin(\phi)\sin(\phi_{13}) \\
& -\tfrac{1}{4} A(G_2-G_4)\sin(\phi)\sin(\phi_{24}) \\
A_{n2s} \triangleq & -\tfrac{1}{4} A(G_1+G_3)\sin(\phi)\cos(\phi_{13}) \\
& -\tfrac{1}{4} A(G_2+G_4)\sin(\phi)\cos(\phi_{24}) \\
& -\tfrac{1}{4} A(G_1-G_3)\cos(\phi)\sin(\phi_{13}) \\
& +\tfrac{1}{4} A(G_2-G_4)\cos(\phi)\sin(\phi_{24}) \\
A_{n3c} \triangleq & -\tfrac{1}{4} A(G_1+G_3)\sin(\phi)\sin(\phi_{13}) \\
& -\tfrac{1}{4} A(G_2+G_4)\cos(\phi)\sin(\phi_{24}) \\
& +\tfrac{1}{4} A(G_1-G_3)\cos(\phi)\cos(\phi_{13}) \\
& +\tfrac{1}{4} A(G_2-G_4)\sin(\phi)\cos(\phi_{24}) \\
A_{n3s} \triangleq & -\tfrac{1}{4} A(G_1+G_3)\cos(\phi)\sin(\phi_{13}) \\
& -\tfrac{1}{4} A(G_2+G_4)\sin(\phi)\sin(\phi_{24}) \\
& -\tfrac{1}{4} A(G_1-G_3)\sin(\phi)\cos(\phi_{13}) \\
& -\tfrac{1}{4} A(G_2-G_4)\cos(\phi)\cos(\phi_{24})
\end{aligned}
$$

where

$$
\begin{aligned}
\phi &\triangleq \tfrac{1}{2}\pi f_{\text{in}}(\delta t_1 - \delta t_2 + \delta t_3 - \delta t_4) \\
\phi_{13} &\triangleq \pi f_{\text{in}}(\delta t_1 - \delta t_3) \qquad \phi_{24} \triangleq \pi f_{\text{in}}(\delta t_2 - \delta t_4).
\end{aligned}
$$

APPENDIX II

This appendix gives definitions of B_{sc}, B_{ss}, B_{n1c}, B_{n1s}, B_{n2c}, B_{n2s}, B_{n3c} and B_{n3s} used in Section IV-B.

$$
\begin{aligned}
B_{sc} \triangleq & +\tfrac{1}{4} A(G_1+G_3)\cos(\theta)\cos(\theta_{13}) \\
& +\tfrac{1}{4} A(G_2+G_4)\cos(\theta)\cos(\theta_{24}) \\
& -\tfrac{1}{4} A(G_1-G_3)\sin(\theta)\sin(\theta_{13}) \\
& +\tfrac{1}{4} A(G_2-G_4)\sin(\theta)\sin(\theta_{24}) \\
B_{ss} \triangleq & -\tfrac{1}{4} A(G_1+G_3)\sin(\theta)\cos(\theta_{13}) \\
& +\tfrac{1}{4} A(G_2+G_4)\sin(\theta)\cos(\theta_{24}) \\
& -\tfrac{1}{4} A(G_1-G_3)\cos(\theta)\sin(\theta_{13}) \\
& -\tfrac{1}{4} A(G_2-G_4)\cos(\theta)\sin(\theta_{24}) \\
B_{n1c} \triangleq & -\tfrac{1}{4} A(G_1+G_3)\sin(\theta)\sin(\theta_{13}) \\
& +\tfrac{1}{4} A(G_2+G_4)\cos(\theta)\sin(\theta_{24}) \\
& +\tfrac{1}{4} A(G_1-G_3)\cos(\theta)\cos(\theta_{13}) \\
& -\tfrac{1}{4} A(G_2-G_4)\sin(\theta)\cos(\theta_{24}) \\
B_{n1s} \triangleq & -\tfrac{1}{4} A(G_1+G_3)\cos(\theta)\sin(\theta_{13}) \\
& +\tfrac{1}{4} A(G_2+G_4)\sin(\theta)\sin(\theta_{24}) \\
& -\tfrac{1}{4} A(G_1-G_3)\sin(\theta)\cos(\theta_{13}) \\
& +\tfrac{1}{4} A(G_2-G_4)\cos(\theta)\cos(\theta_{24}) \\
B_{n2c} \triangleq & +\tfrac{1}{4} A(G_1+G_3)\cos(\theta)\cos(\theta_{13}) \\
& -\tfrac{1}{4} A(G_2+G_4)\cos(\theta)\cos(\theta_{24}) \\
& -\tfrac{1}{4} A(G_1-G_3)\sin(\theta)\sin(\theta_{13}) \\
& -\tfrac{1}{4} A(G_2-G_4)\sin(\theta)\sin(\theta_{24}) \\
B_{n2s} \triangleq & -\tfrac{1}{4} A(G_1+G_3)\sin(\theta)\cos(\theta_{13}) \\
& -\tfrac{1}{4} A_4(G_2+G_4)\sin(\theta)\cos(\theta_{24}) \\
& -\tfrac{1}{4} A(G_1-G_3)\cos(\theta)\sin(\theta_{13}) \\
& +\tfrac{1}{4} A(G_2-G_4)\cos(\theta)\sin(\theta_{24}) \\
B_{n3c} \triangleq & -\tfrac{1}{4} A(G_1+G_3)\sin(\theta)\sin(\theta_{13}) \\
& -\tfrac{1}{4} A(G_2+G_4)\cos(\theta)\sin(\theta_{24}) \\
& +\tfrac{1}{4} A(G_1-G_3)\cos(\theta)\cos(\theta_{13}) \\
& +\tfrac{1}{4} A(G_2-G_4)\sin(\theta)\cos(\theta_{24}) \\
B_{n3s} \triangleq & -\tfrac{1}{4} A(G_1+G_3)\cos(\theta)\sin(\theta_{13}) \\
& -\tfrac{1}{4} A(G_2+G_4)\sin(\theta)\sin(\theta_{24}) \\
& -\tfrac{1}{4} A(G_1-G_3)\sin(\theta)\cos(\theta_{13}) \\
& -\tfrac{1}{4} A(G_2-G_4)\cos(\theta)\cos(\theta_{24})
\end{aligned}
$$

where

$$
\begin{aligned}
\theta &\triangleq \tfrac{1}{4}(\theta_1 - \theta_2 + \theta_3 - \theta_4) \\
\theta_{13} &\triangleq \tfrac{1}{2}(\theta_1 - \theta_3) \qquad \theta_{24} \triangleq \tfrac{1}{2}(\theta_2 - \theta_4).
\end{aligned}
$$

APPENDIX III

This appendix gives brief proofs of Facts 1, 2, 3 and 4.

Proof of Fact 1: It follows from (3) that the total output power P_{out1} is given by

$$
\begin{aligned}
P_{\text{out1}} &= \tfrac{1}{2}(A_s^2 + A_n^2) + os_{cm}^2 + os_{\text{diff}}^2 \\
&= \tfrac{1}{2} A^2 G^2 (1+\alpha^2) + \tfrac{1}{4}[(os_1+os_2)^2 + (os_1-os_2)^2] \\
&= \tfrac{1}{4} A^2 (G_1^2 + G_2^2) + \tfrac{1}{2}(os_1^2 + os_2^2).
\end{aligned}
$$

Proof of Fact 2: It follows from (6) that the total output power P_{out2} is given by

$$
\begin{aligned}
P_{\text{out2}} &= \tfrac{1}{2}(A_{s4}^2 + A_{n1}^2 + A_{n2}^2 + A_{n3}^2) \\
&\quad + \tfrac{1}{16}(os_1 - os_2 + os_3 - os_4)^2 \\
&\quad + \tfrac{1}{8}[(os_1 - os_3)^2 + (os_2 - os_4)^2] \\
&\quad + \tfrac{1}{16}(os_1 + os_2 + os_3 + os_4)^2 \\
&= \tfrac{1}{8} A^2 (G_1^2 + G_2^2 + G_3^2 + G_4^2) \\
&\quad + \tfrac{1}{4}(os_1^2 + os_2^2 + os_3^2 + os_4^2).
\end{aligned}
$$

Proof of Fact 3: It follows from (10) that the total output power P_{out3} is given by

$$
\begin{aligned}
P_{\text{out3}} &= \tfrac{1}{2}(B_s^2 + B_n^2) \\
&= \tfrac{1}{8}(G_c^2 + G_d^2) \\
&= \tfrac{1}{8}[(G_1 - G_2)^2 + (G_1 + G_2)^2] \\
&= \tfrac{1}{4}(G_1^2 + G_2^2) \\
&= \frac{1}{4} A^2 \left[\frac{1}{1 + (f_{\text{in}}/f_{c1})^2} + \frac{1}{1 + (f_{\text{in}}/f_{c2})^2} \right].
\end{aligned}
$$

Proof of Fact 4: It follows from (12) that the total output power $P_{\text{out}4}$ is given by

$$\begin{aligned} P_{\text{out}4} &= \tfrac{1}{2}\left(B_{s4}^2 + B_{n1}^2 + B_{n2}^2 + B_{n3}^2\right) \\ &= \frac{1}{8}A^2\left[\frac{1}{1+(f_{\text{in}}/f_{c1})^2} + \frac{1}{1+(f_{\text{in}}/f_{c2})^2} \right. \\ &\qquad \left. + \frac{1}{1+(f_{\text{in}}/f_{c3})^2} + \frac{1}{1+(f_{\text{in}}/f_{c4})^2}\right]. \end{aligned}$$

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Digital Compensation for Timing Mismatches in Interleaved ADCs

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- Time Interleaved ADC System
- Proposed Calibration System
- Simulation Results
- Extension to 4ch Interleaved ADCs
- Conclusion

Contents

Research Background & Objective

ATE System

Background

High-speed sampling time-interleaved ADC for ATE system

Timing skew ➡ Big issue

Error compensation of timing skew effects

Conventional

Analog method + Digital method

Objective

Proposal

Full digital method

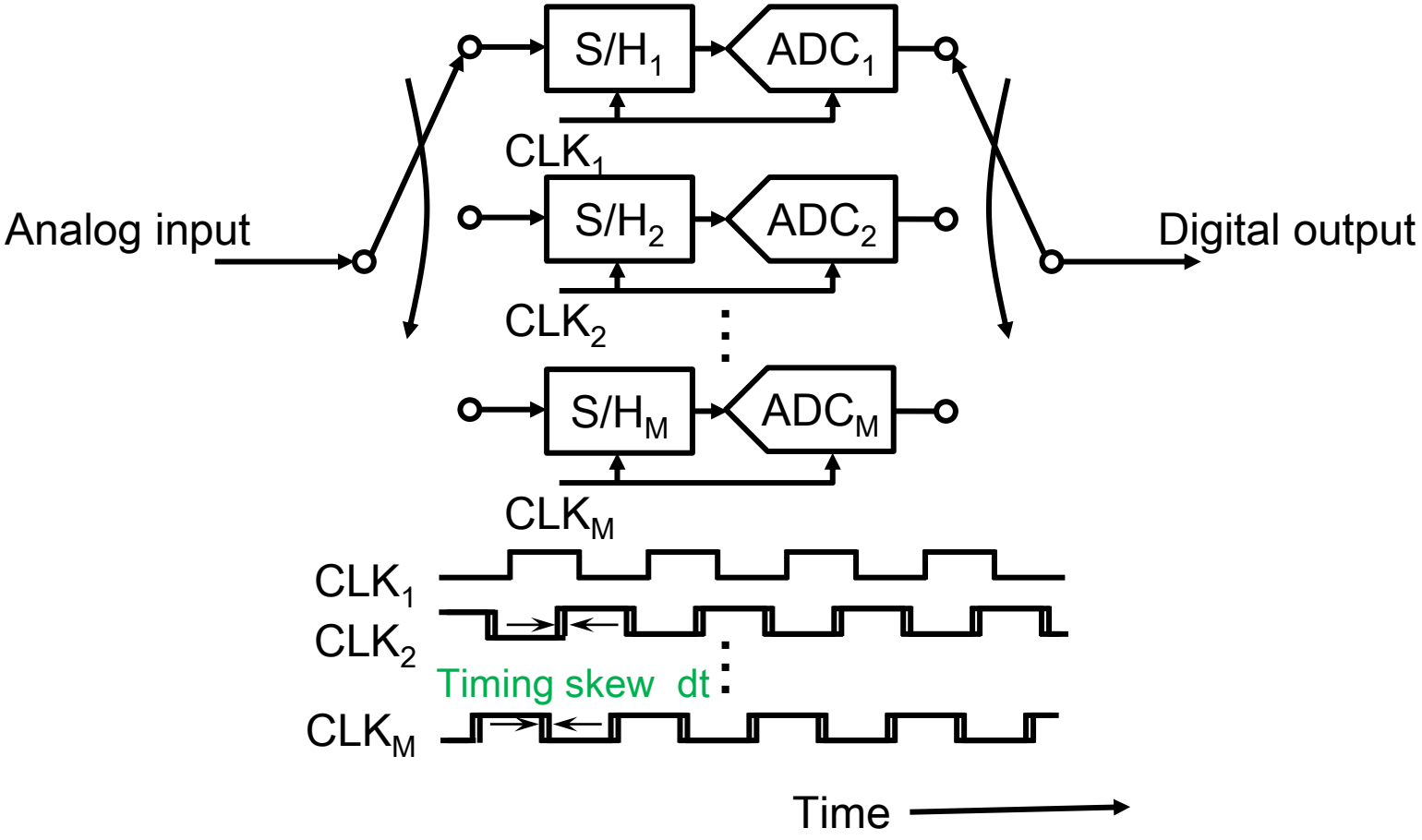
High accuracy, Stable, Reliable

Contents

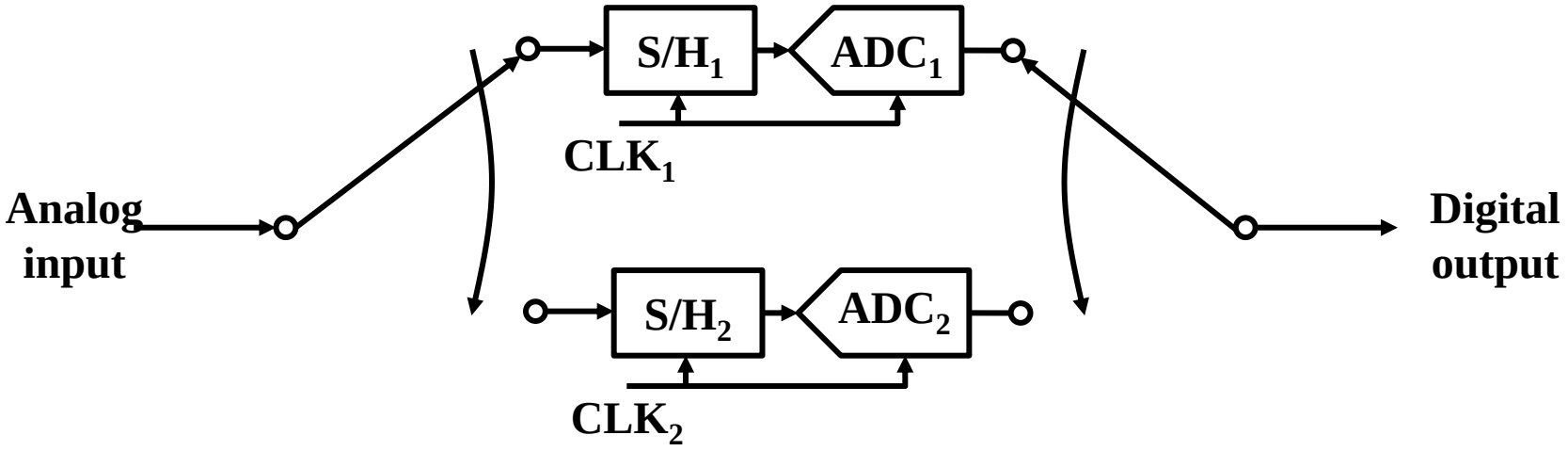
Principle of Time-Interleaved ADC

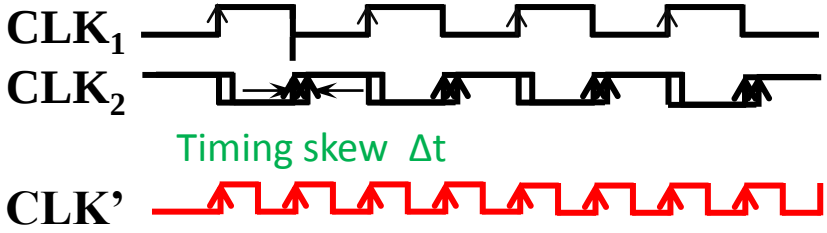
M times sampling rate with M-channel ADCs

➡ High-speed sampling



2-channel Interleaved ADC



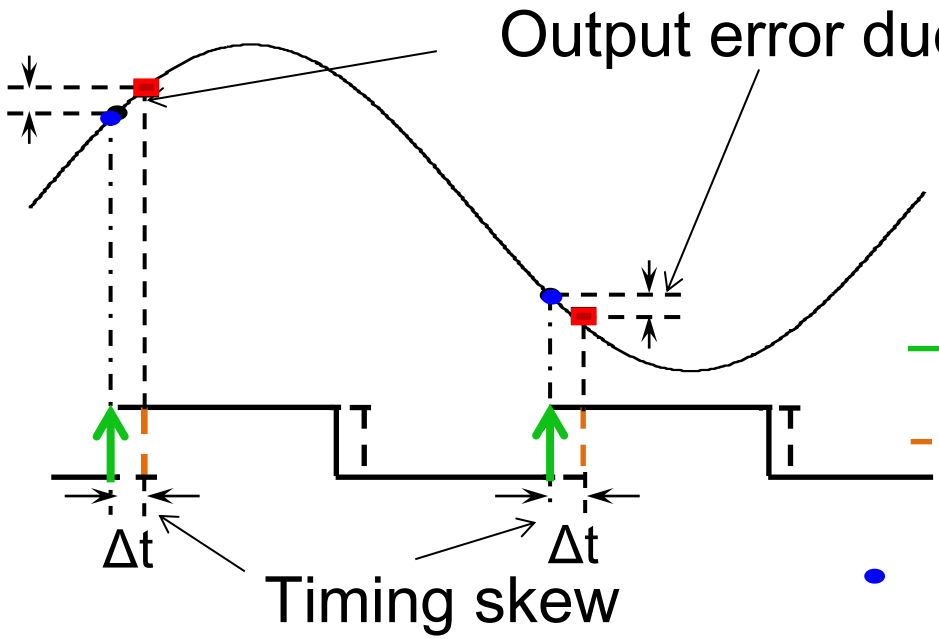


CLK1 reference

CLK2 delayed by half period

2 times sampling rate

Timing Error in Sampling



Ideal clock

Actual clock

Ideal sampling points

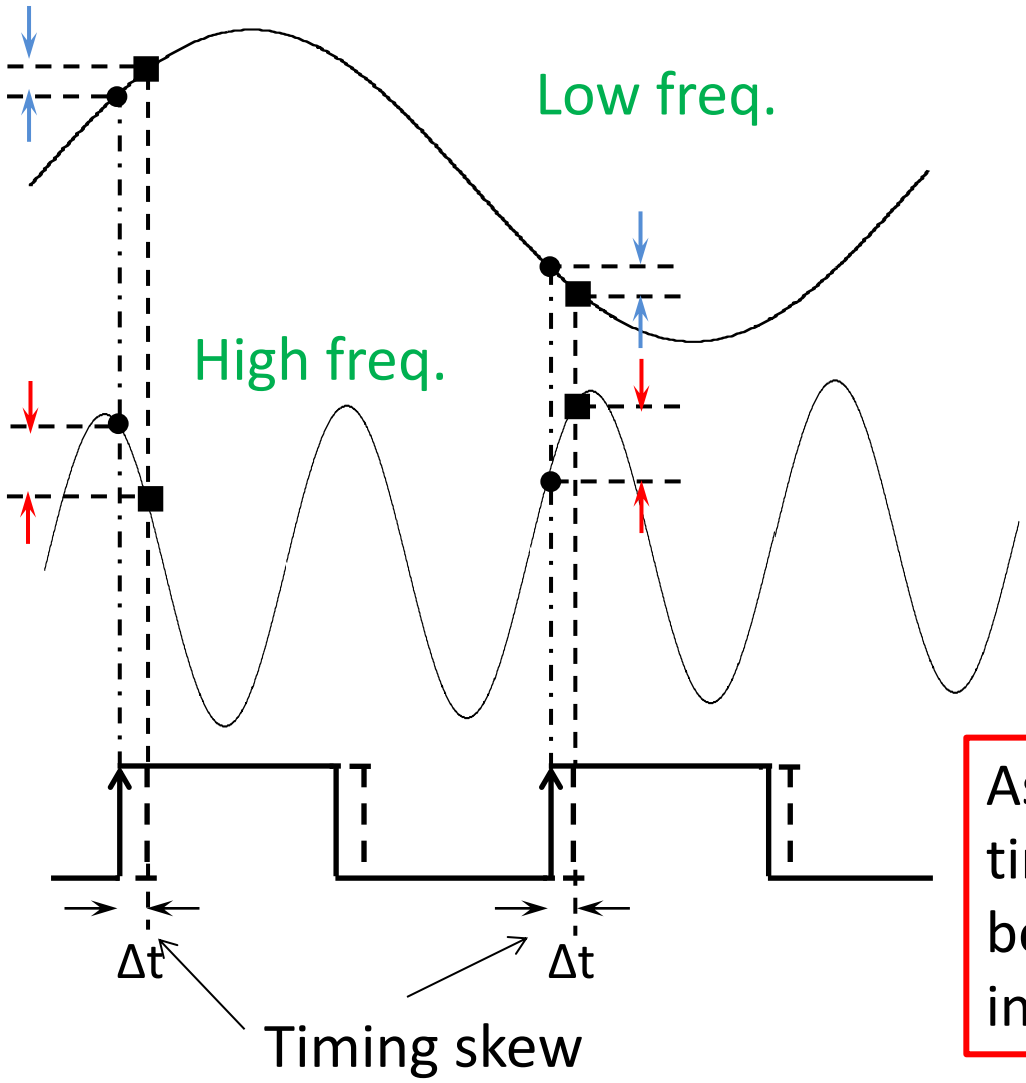
Actual sampling points

Timing error (horizontal error)

↓

Sampled voltage error (vertical error)

Input Frequency & Output



Input freq. ⬆

Output error ⬆

As input frequency increases, timing skew problem becomes serious in interleaved ADC.

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Proposed Calibration System

- Full digital
- Timing Skew Detection
  - Cross-correlation of two channel ADC outputs
- Timing Skew Effect Compensation
  - Delay linear digital filter
- Calibration Control
  - Successive approximation algorithm
  - Foreground calibration

Cross-Correlation

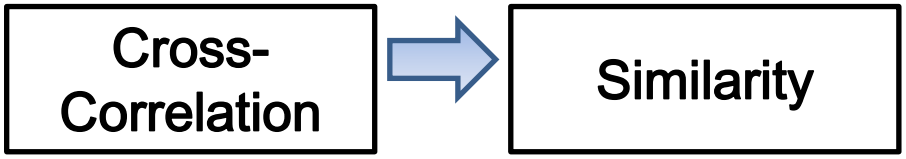
Continuous-time signal

$$(f * g)(t) = \int_{-\infty}^{\infty} f^*(\tau) g(t+\tau) d\tau$$

Discrete-time signal

$$(f * g)(m) = \sum_{m=-\infty}^{\infty} f^*[n] g[n+m]$$

The similarity of two time series signals f, g



Correlation of R(0)and R(1)

CH1 ADC output: $f[n]$

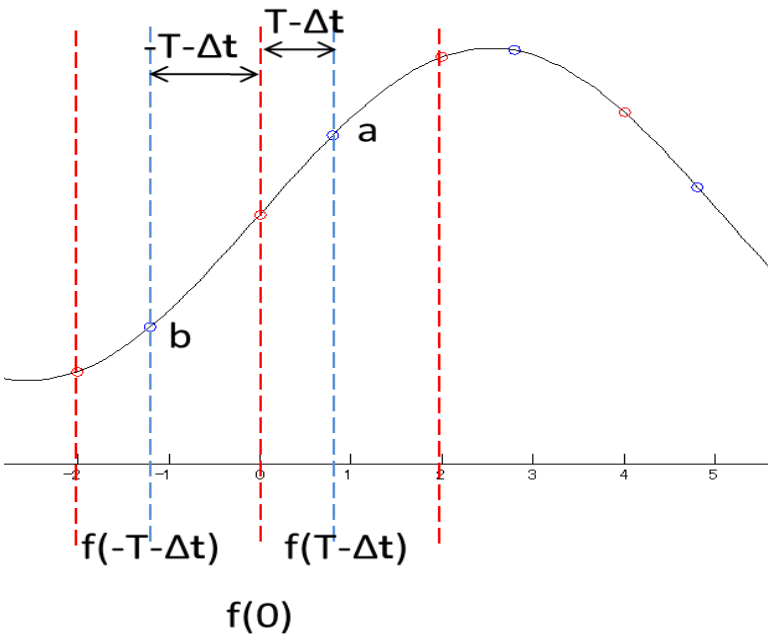
CH2 ADC output: $g[n] = f[n+T-\Delta t]$

lag 0,

$$R(0) = R_{ff}[0] = \lim_{n\to\infty} \frac{1}{n} \sum_{-n}^{n} f[n] f[n+T-\Delta t]$$

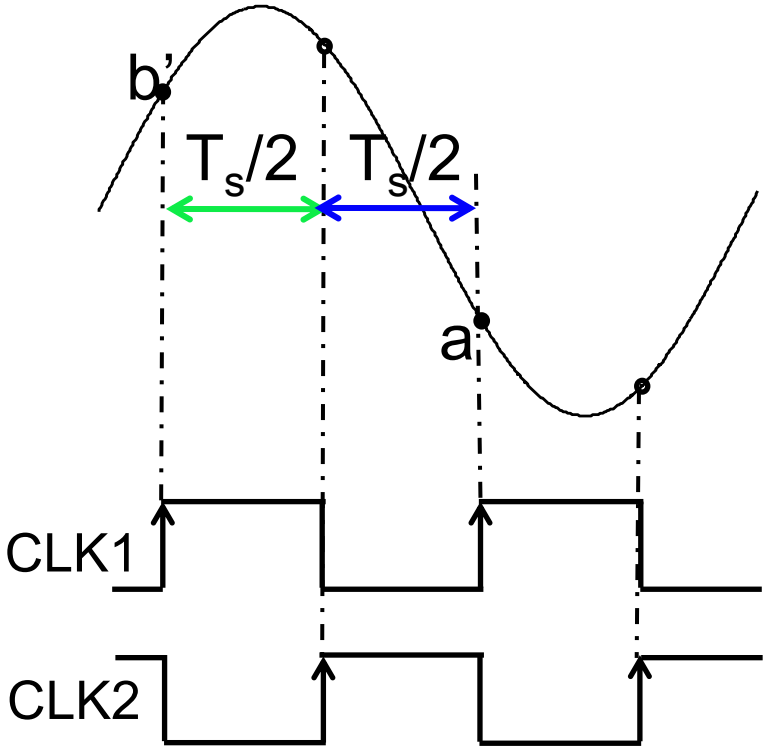
lag 1,

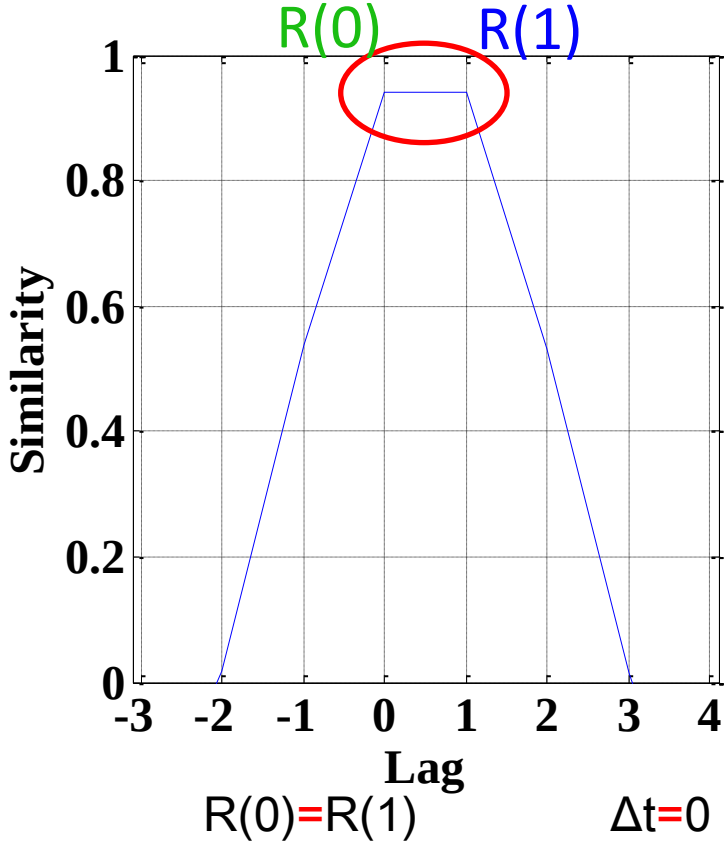
$$R(1) = R_{ff}[-2T] = \lim_{n\to\infty} \frac{1}{n} \sum_{-n}^{n} f[n] f[n-T-\Delta t]$$



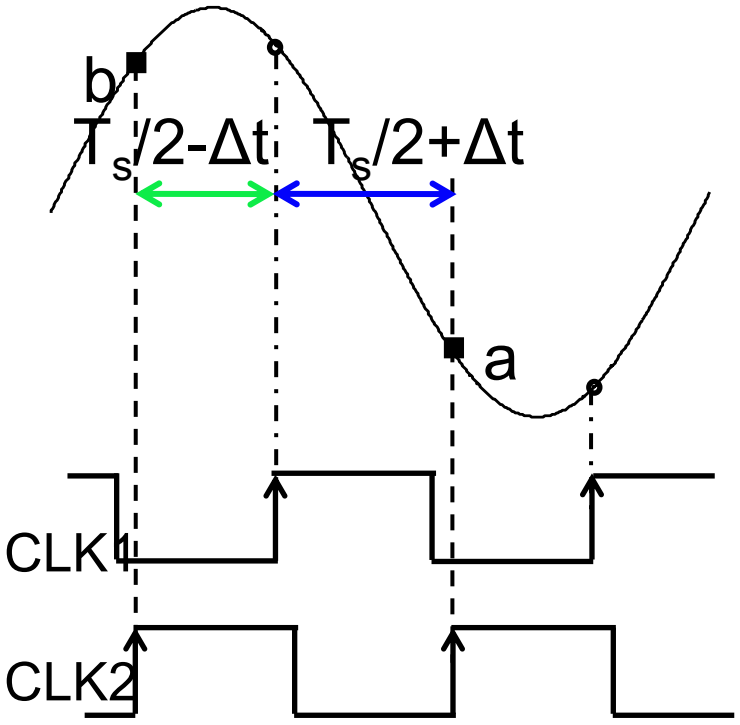
Timing skew Δt

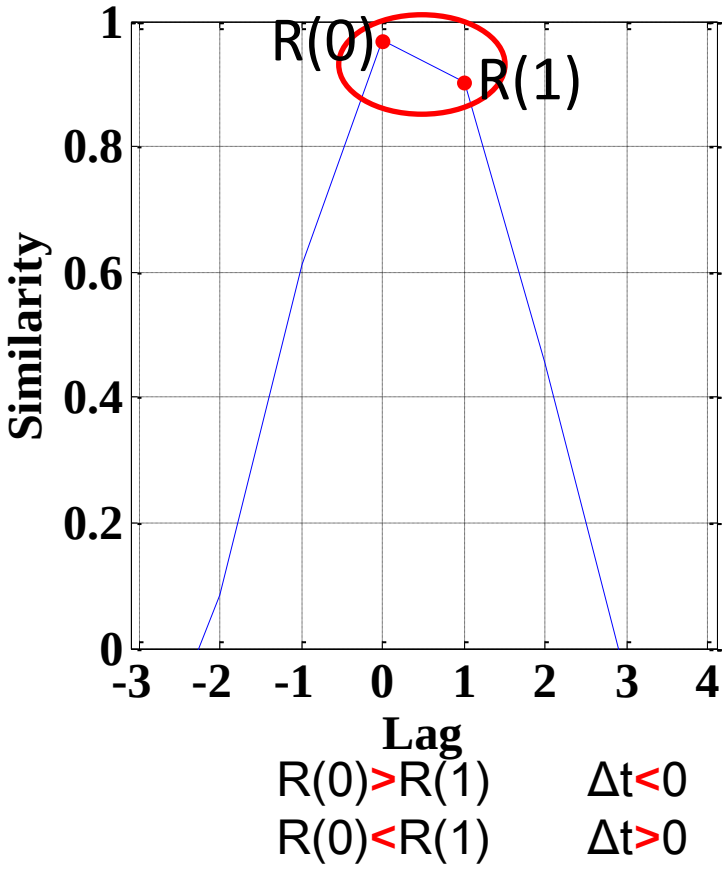
Cross-Correlation without Timing Skew





Cross-Correlation with Timing Skew





R(0)>R(1) Δt<0

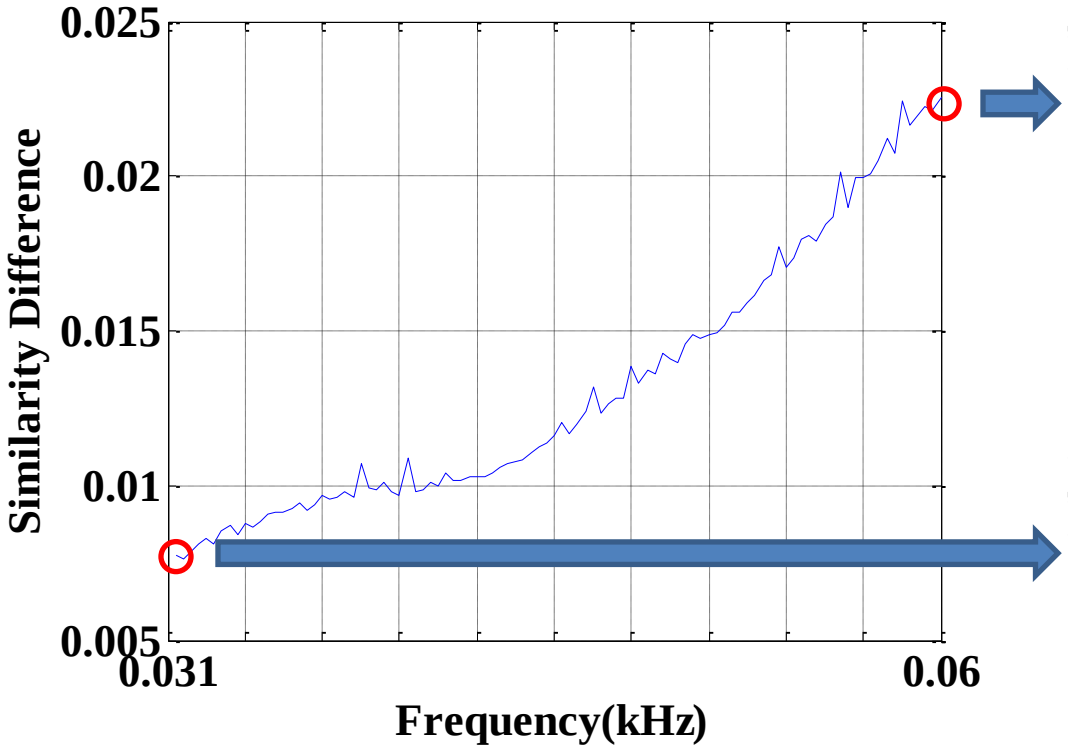
R(0)<R(1) Δt>0

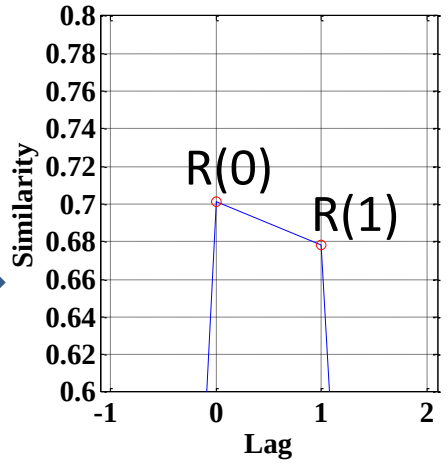
cross-correlation value ⇒ Sign of Δt (Δt >0 or Δt <0)

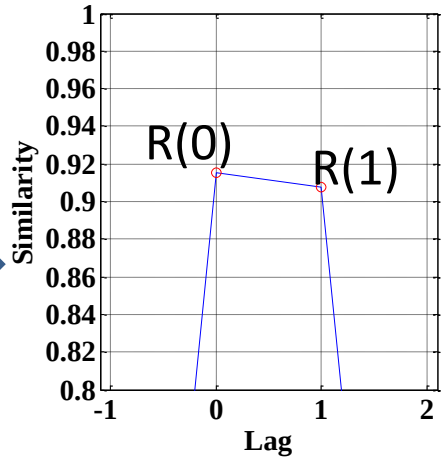
Magnitude of |Δt|

Calibration Input Frequency & Correlation Sensitivity

Δt=-0.02Ts



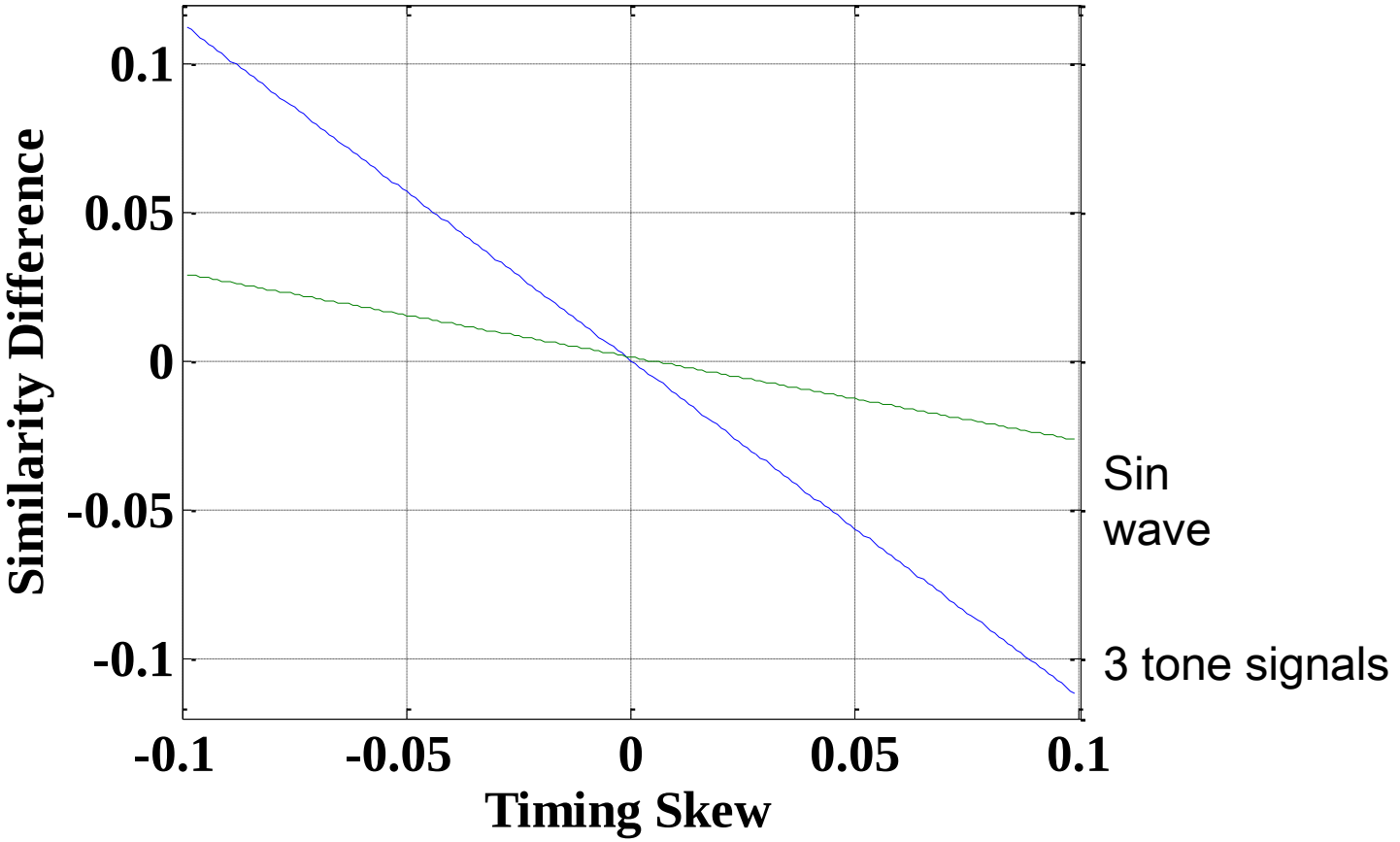




Frequency ⬆ ➡ Difference between R(0) and R(1) ⬆

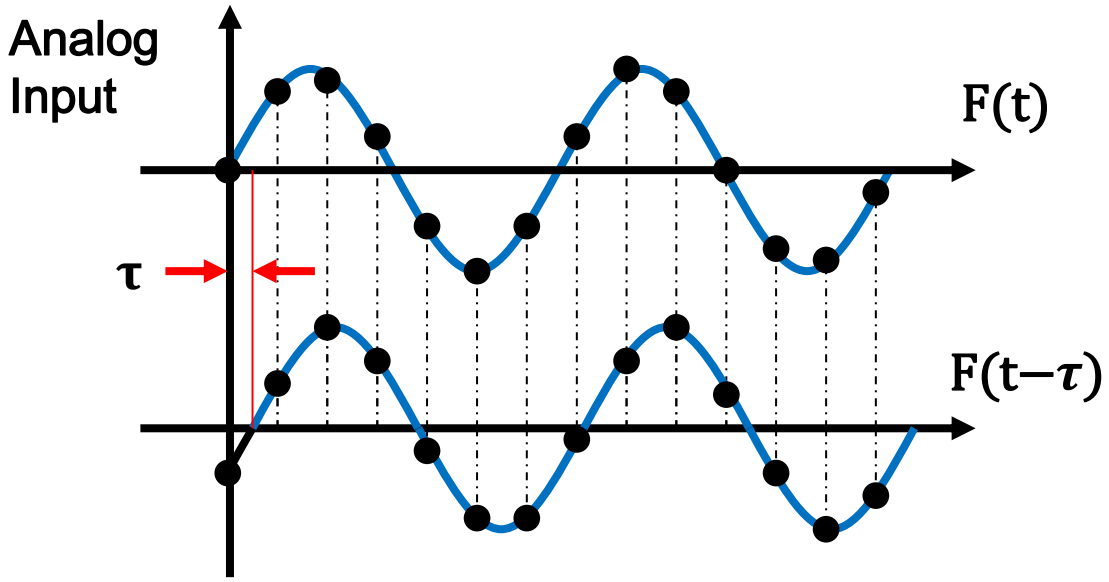
Timing Skew Detection

Calibration Input Signal & Correlation Sensitivity



- 3-tone is more sensitive than 1-tone.
- For 3-tone, minimize random phase and crest factor

Linear Phase Delay Digital Filter



Linear phase ⇒ maintain time-domain waveform

Conventional Linear-Phase Digital Filter :

Group delay time resolution $T_s/2$

Proposed Linear-Phase Delay Digital Filter [1] :

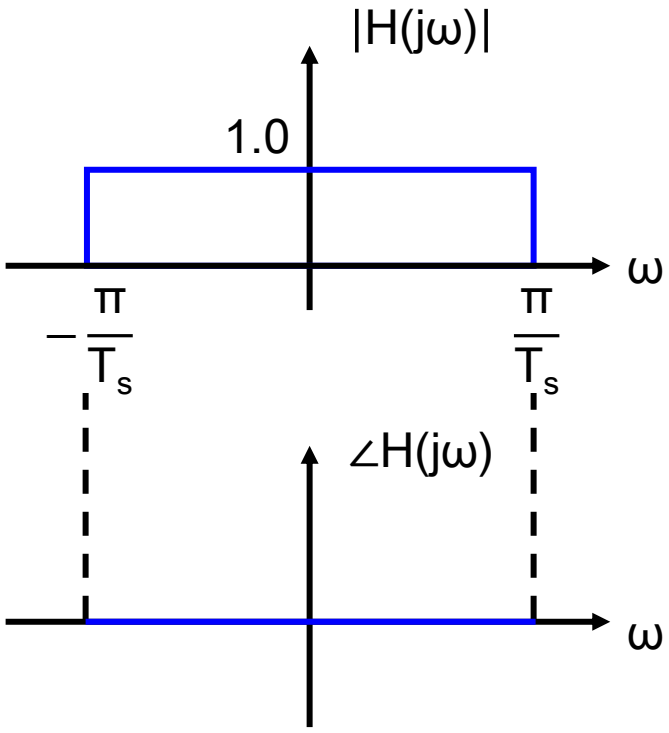
Arbitrary small time resolution τ

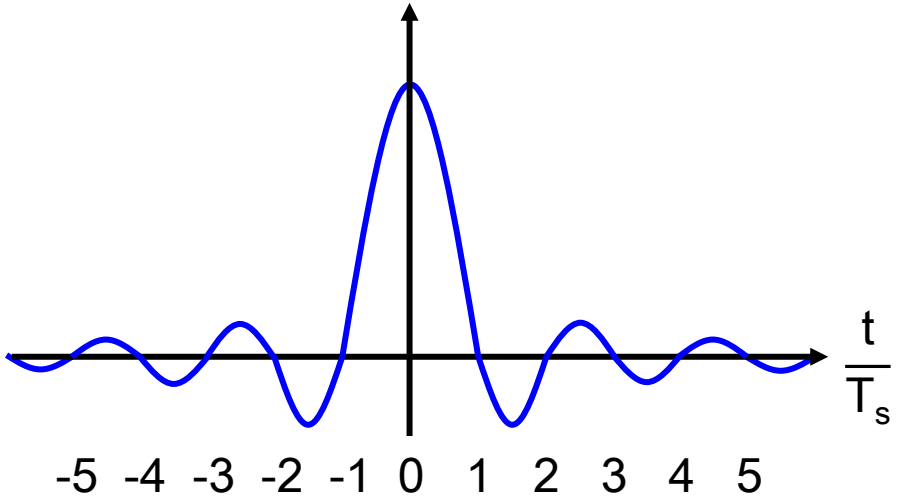
[1] K. Asami, et. al., "Timing Skew Compensation Technique using Digital Filter with Novel Linear Phase Condition," IEEE International Test Conference (Nov. 2010).

Ideal Filter

Inverse Fourier Transform

Frequency response → Impulse response



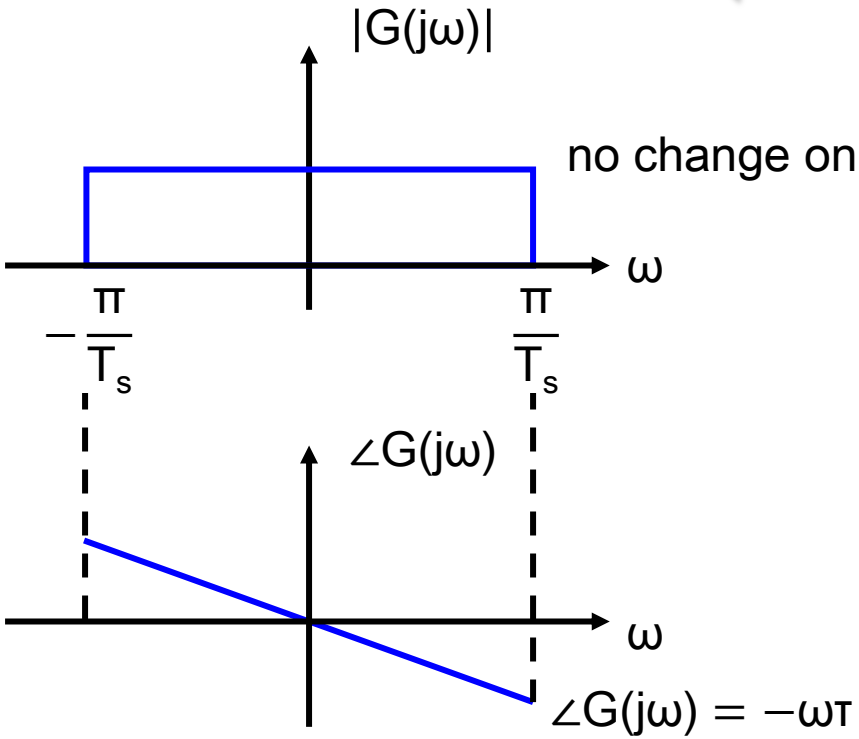


$$h(t)=\frac{1}{T_s}\,\mathrm{sinc}\left(\pi\frac{t}{T_s}\right)$$

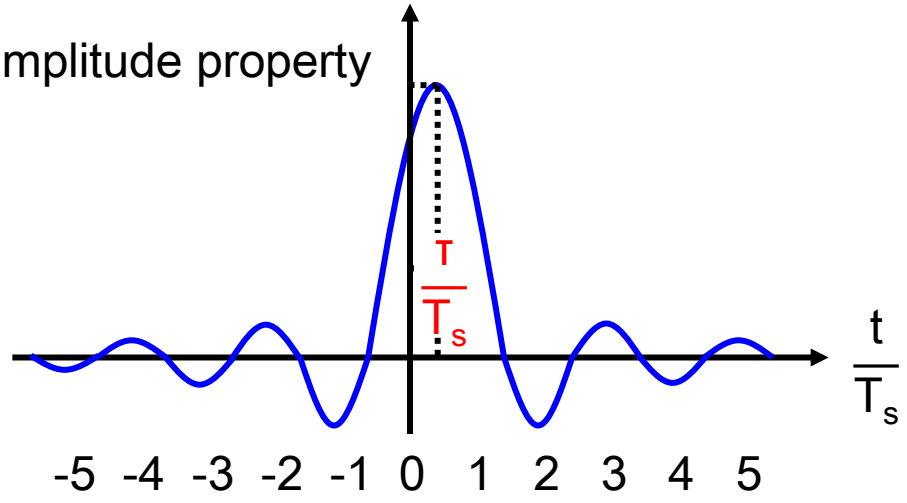
Time Shift of Ideal Filter

Fourier transform

Frequency response ⟵ Impulse response



no change on amplitude property



$$g(t) = h(t-\tau)$$
$$= \frac{1}{T_s}\mathrm{sinc}\left(\pi\frac{t-\tau}{T_s}\right)$$

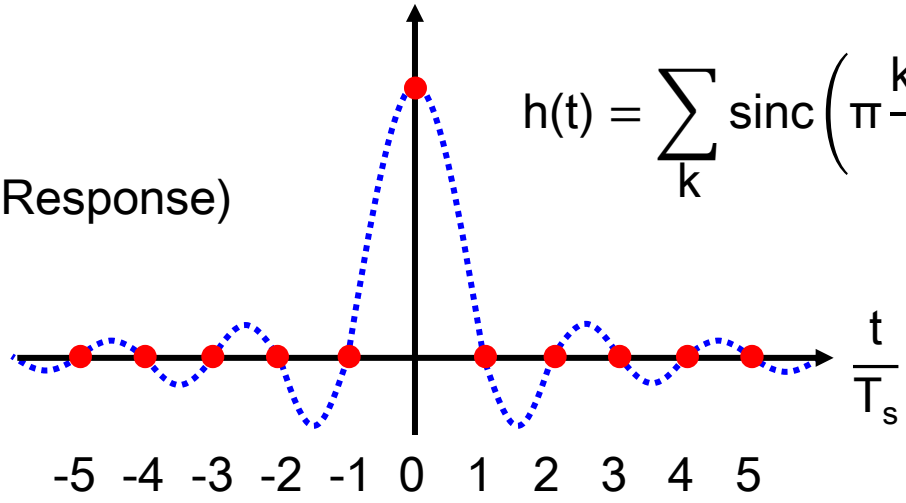
Linear phase is maintained.

Impulse response is time-shifted by, τ

Delay Digital Filter Coefficients

FIR(Finite Impulse Response) Filter

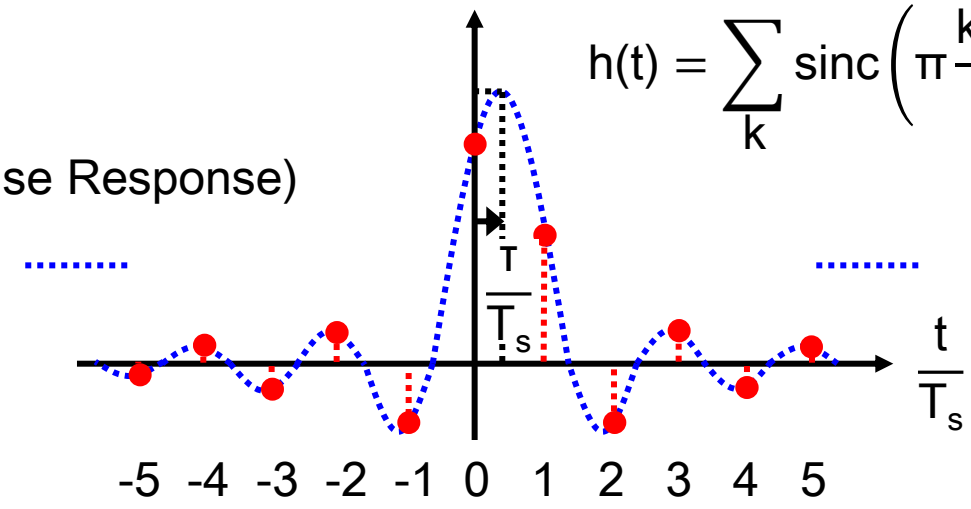
$$h(t) = \sum_k \mathrm{sinc}\left(\pi \frac{k \cdot T_s}{T_s}\right) \delta\left(t - k \cdot T_s\right)$$



Time-shift

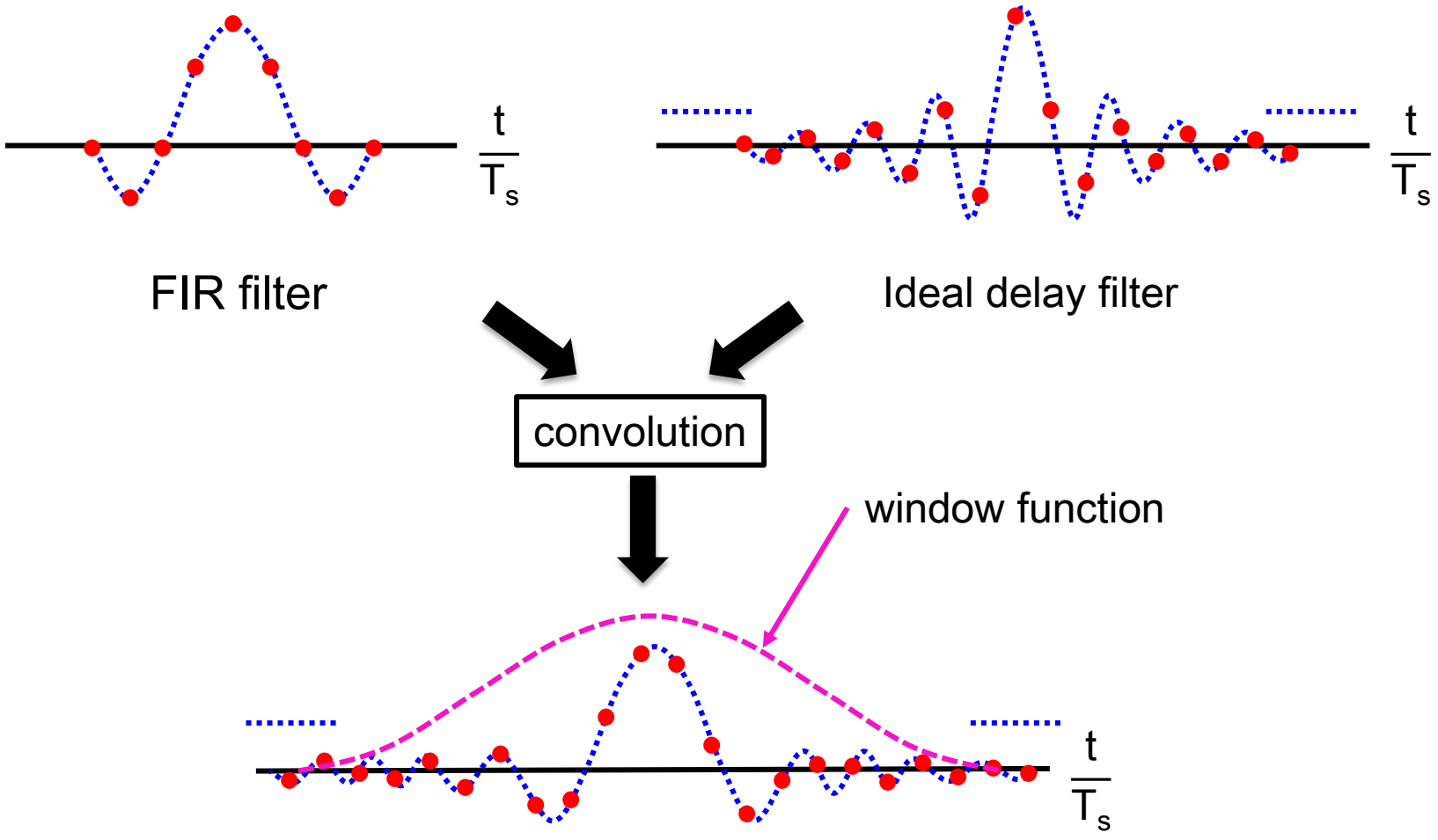
IIR(Infinite Impulse Response) Filter

$$h(t) = \sum_k \mathrm{sinc}\left(\pi \frac{k \cdot T_s - \tau}{T_s}\right) \delta\left(t - k \cdot T_s\right)$$



Ideal delay filter

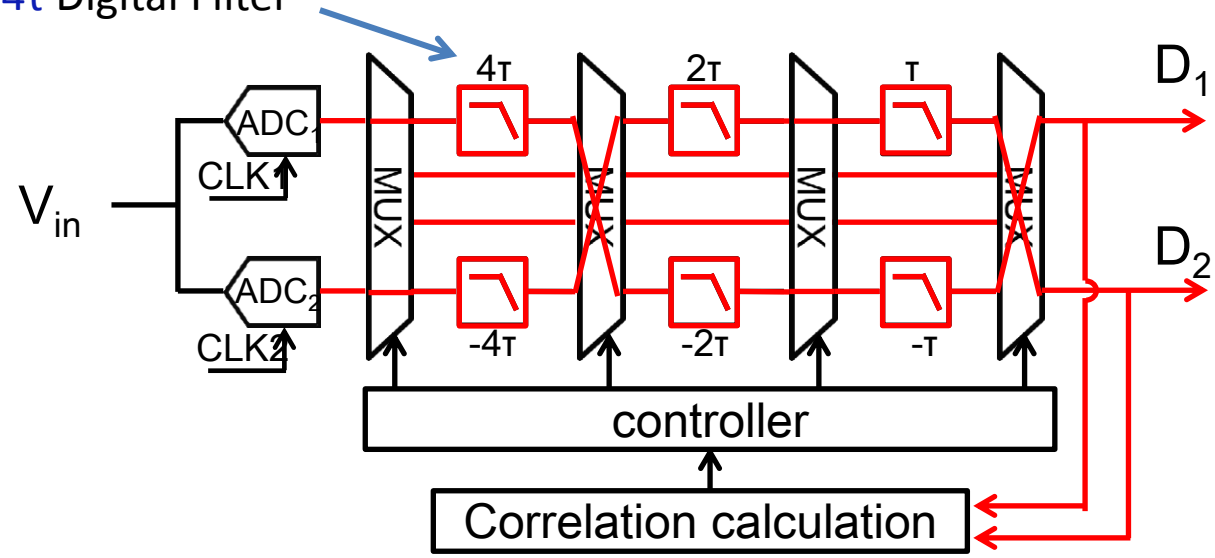
Design of Linear-Phase Delay Digital Filter

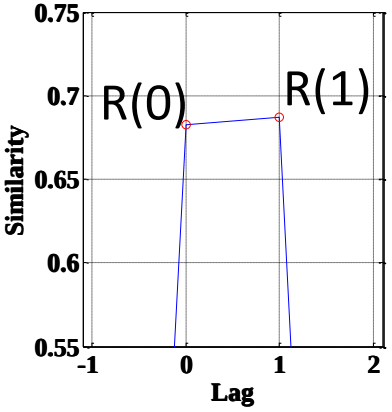


Linear phase Digital Delay Filter

Proposed System

Delay 4τ Digital Filter

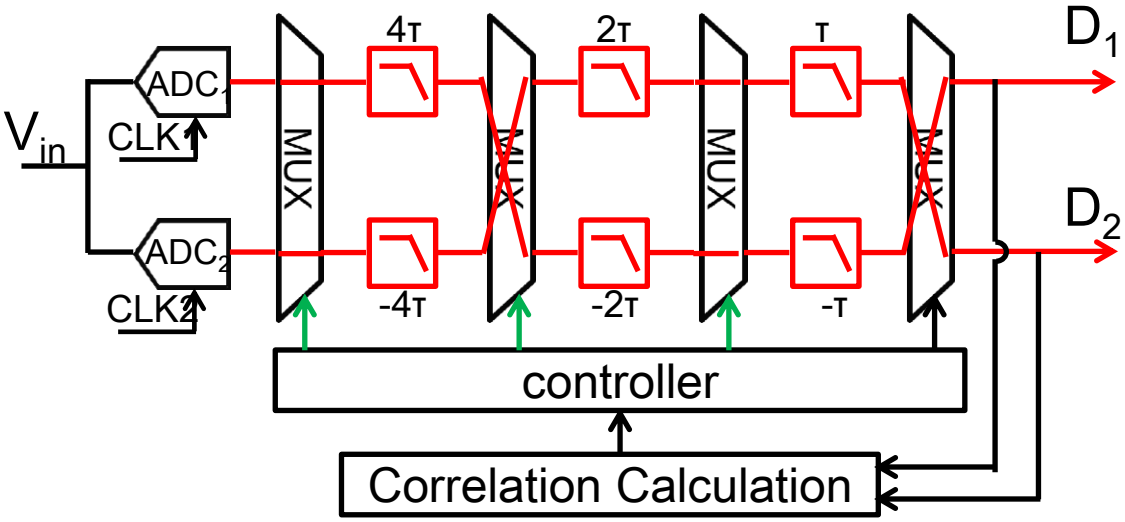




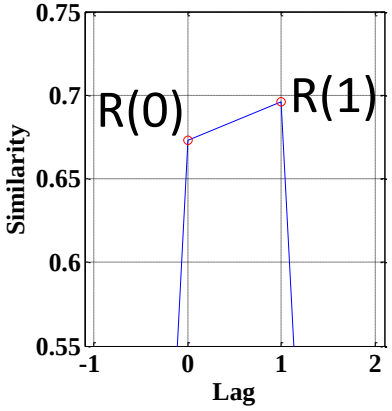
compare the correlation value of the lag 1 and lag 0
R(0)≠R(1)
Δt≠0

delay CH1 -4τ
delay CH2 -4τ

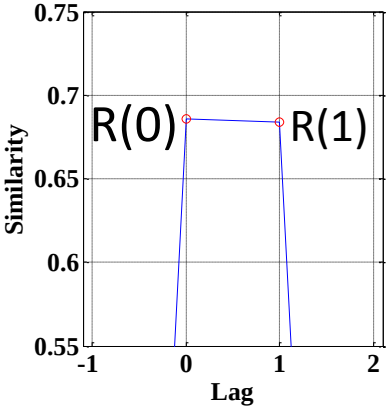
Calibration Done



before calibration



after calibration

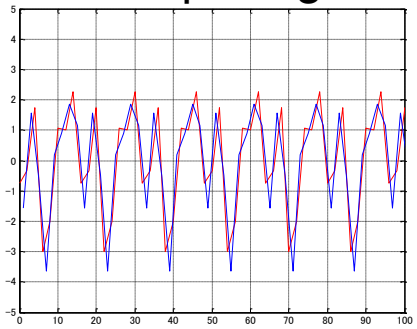


Binary-search, successive approximation

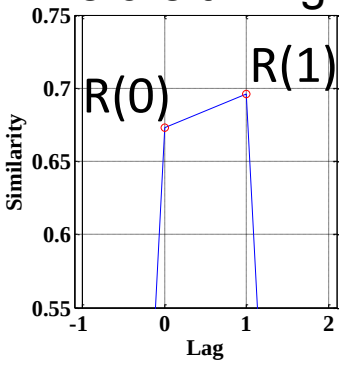
Contents

Simulation Results (1)

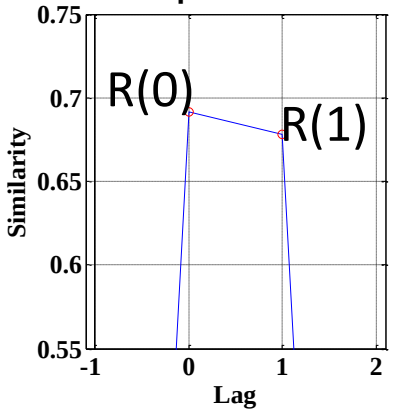
3-tone Input signal



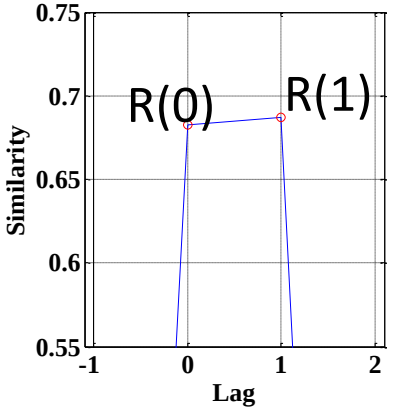
Before timing skew calibration



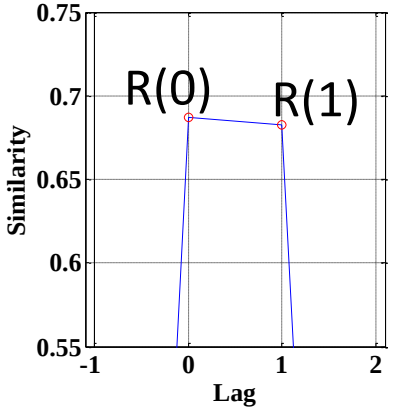
After step1 calibration



After step2 calibration



After step3 calibration

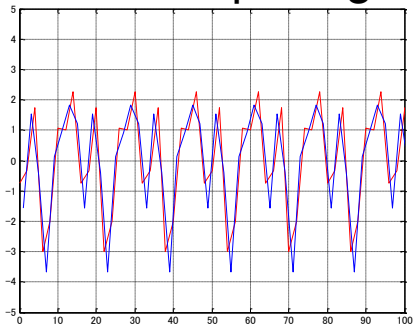


Confirm the performance of timing skew calibration

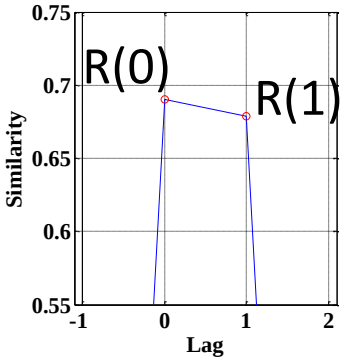
timing skew	+ 0.02 Ts
filter tap	21
window function	Blackman
T	0.001 Ts

Simulation Results (2)

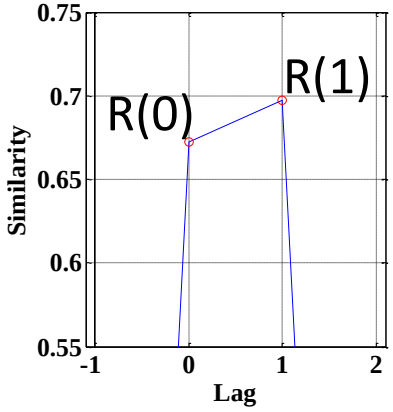
3-tone Input signal



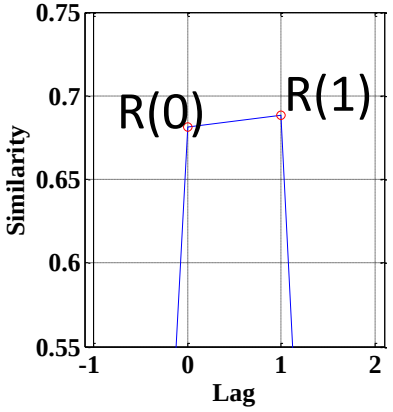
Before skew calibration



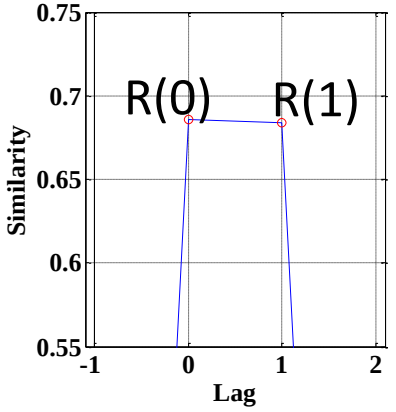
After step1 calibration



After step2 calibration



After step3 calibration

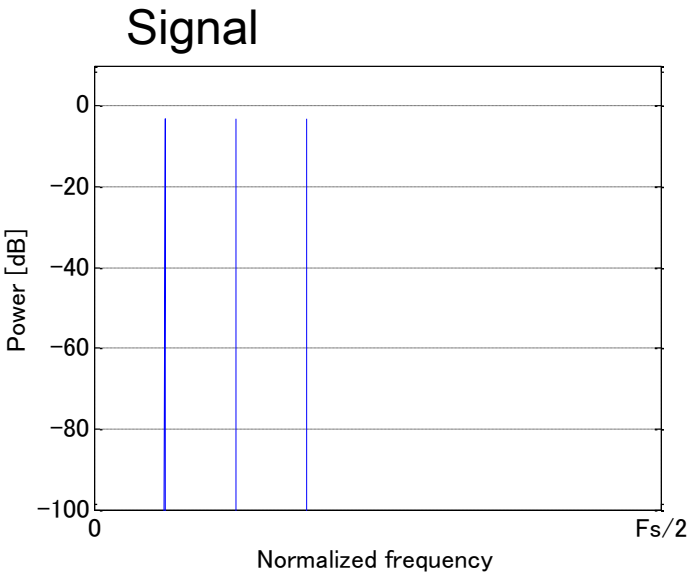


Confirm the performance of timing skew calibration

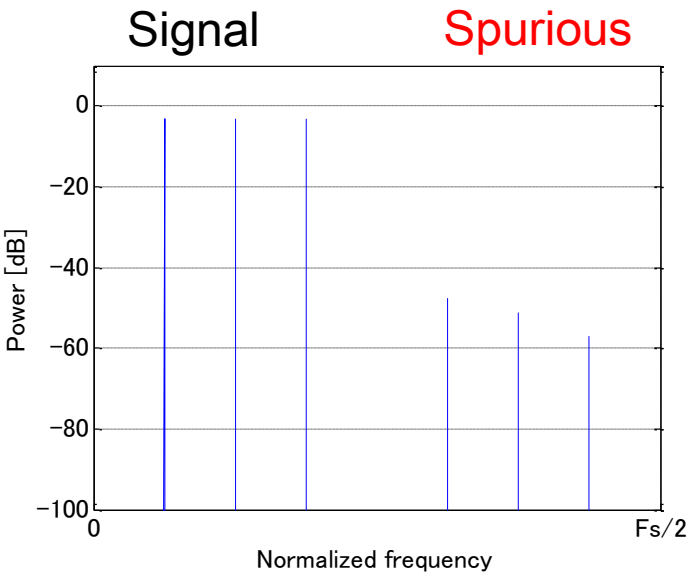
timing skew	- 0.01 Ts
filter tap	21
window function	Blackman
T	0.001 Ts

Power Spectrum of Interleaved ADC Output without/with Timing Skew

3-tone signal without skew

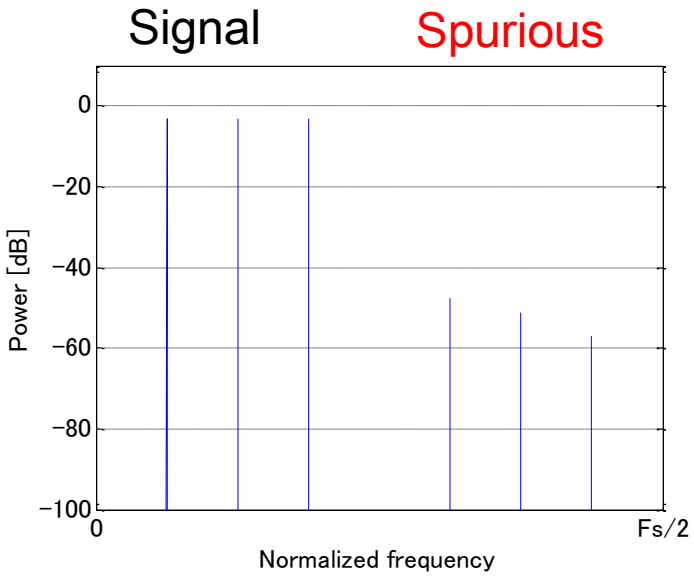


3-tone signal with skew

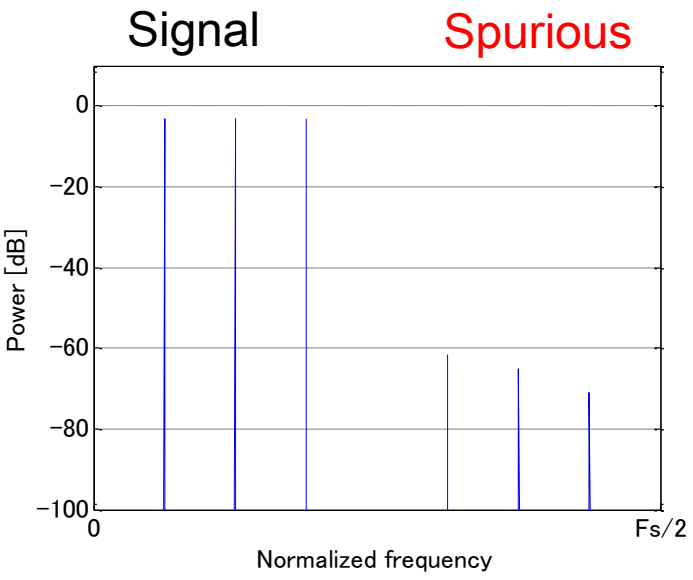


Power spectrum before/after Calibration

Before skew calibration



After skew calibration



Spurious components are reduced by proposed calibration

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4-Channel Case Extension Method

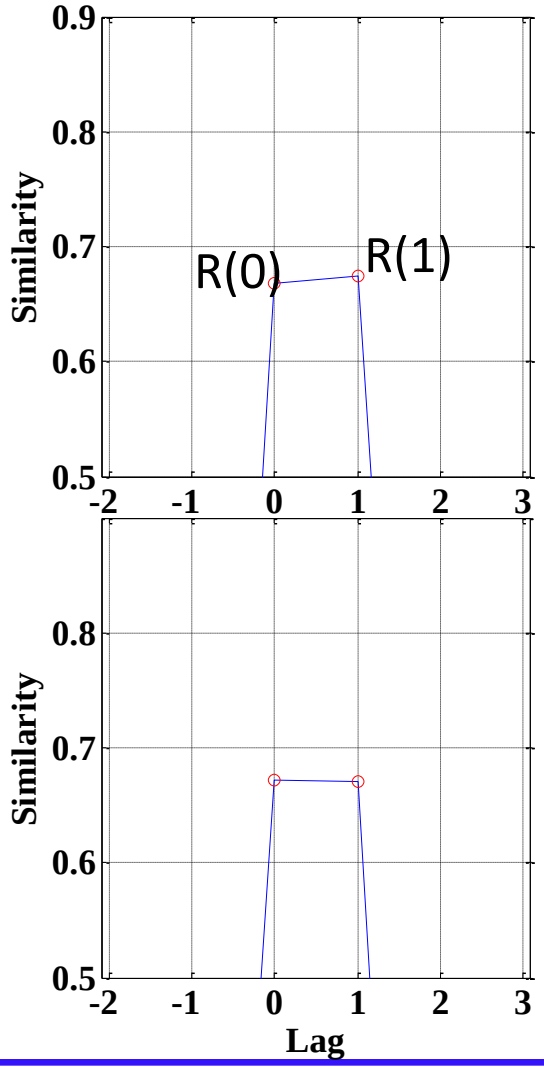
Ch1/ch3 calibration

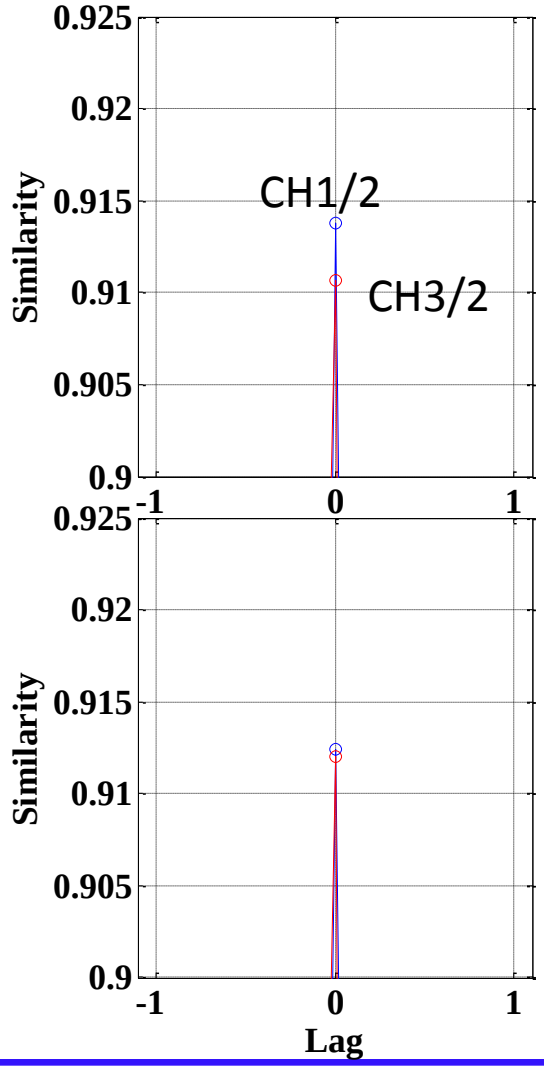
Ch2 calibration

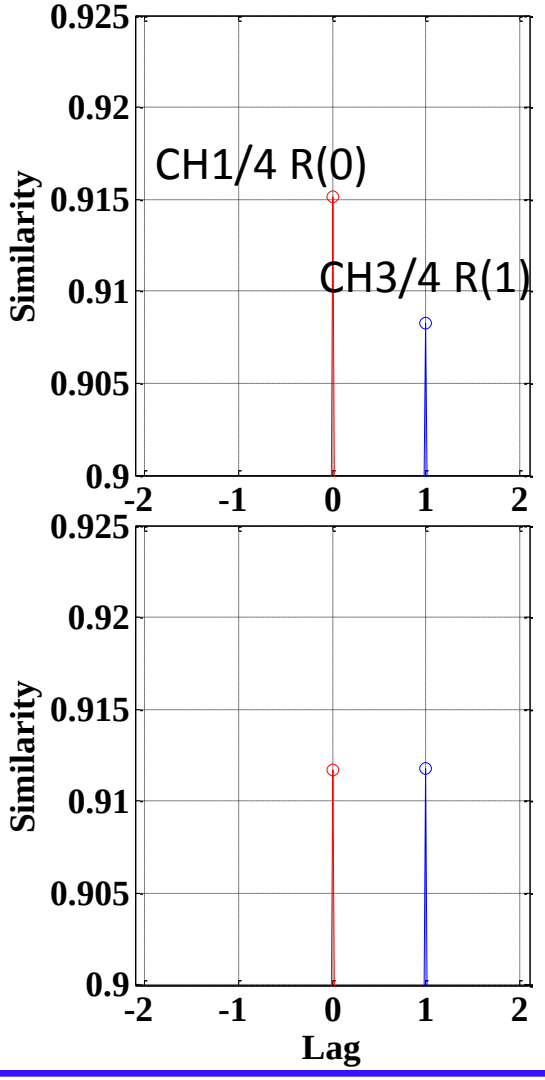
Ch4 calibration

Before calibration

After calibration

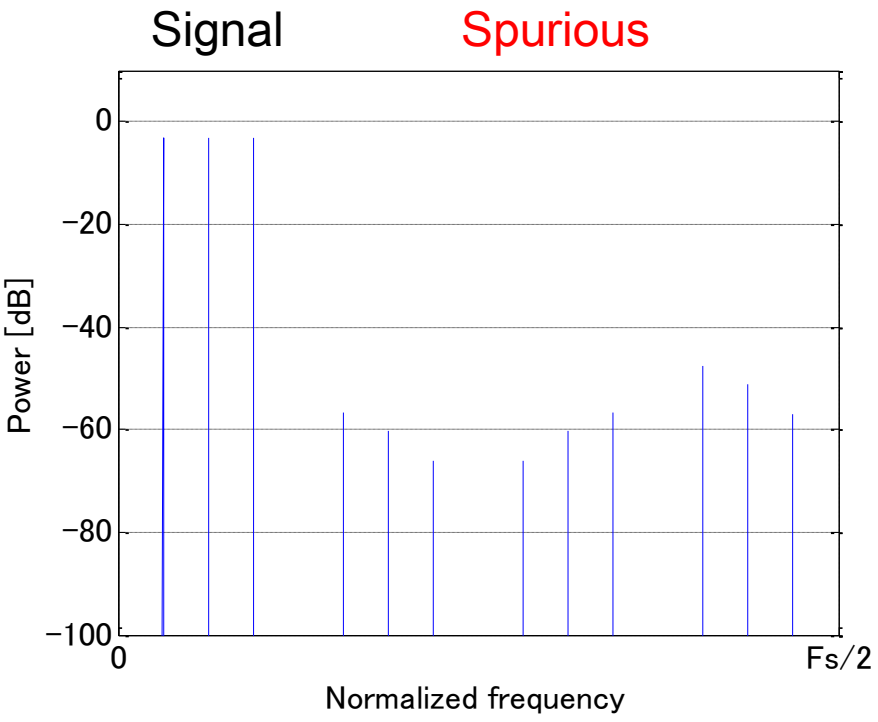




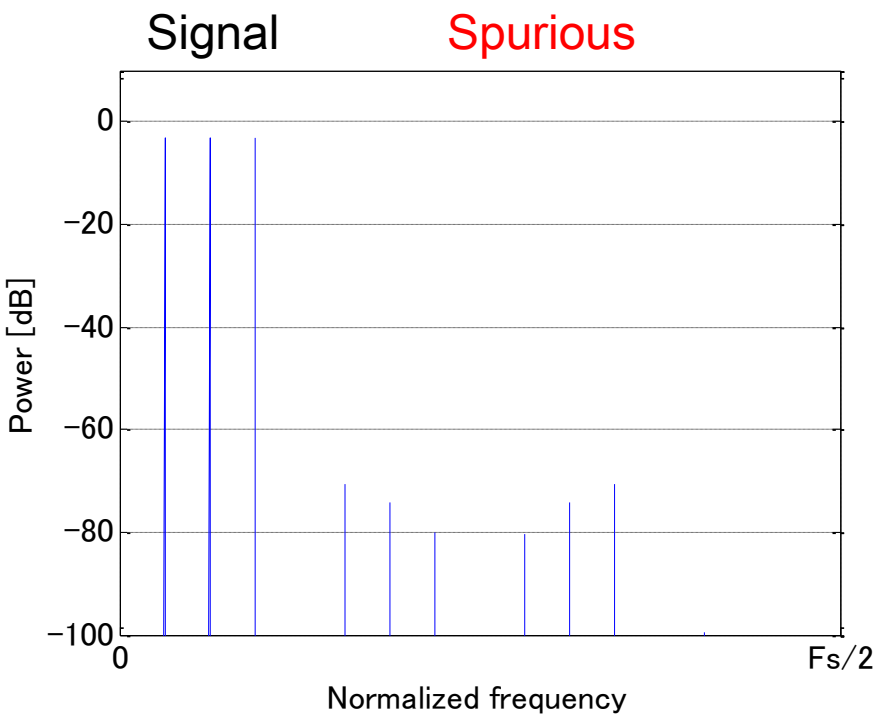


Simulation Results - Power Spectrum

Before calibration



After calibration



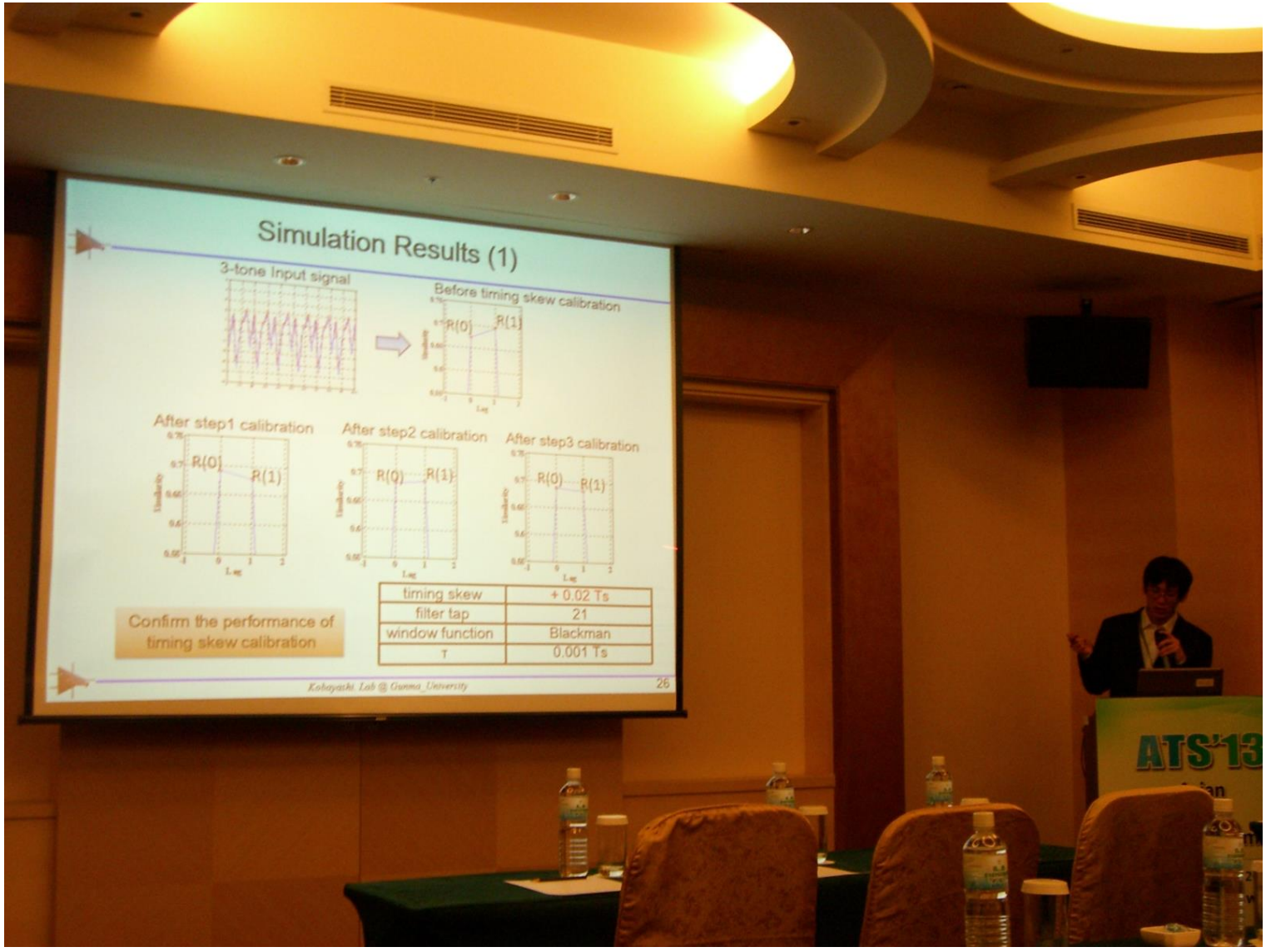
Contents

Conclusion

Proposal of timing skew calibration in interleaved ADC

- Full digital
- Timing Skew Detection
  - Cross-correlation of two channel ADC outputs
  - Effective for high frequency, multi-tone input
- Timing Skew Effect Compensation
  - Delay linear–phase digital filter
- Calibration Control
  - Successive approximation algorithm
  - Foreground calibration
- Verified with MATLAB simulation in 2-channel, 4-channel cases.

Presented by呉明輝（Minghui Wu）

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