Session B2 Analog Circuit 2

Kunming, China (Nov. 4, 2020)

Invited Paper

Analog/Mixed-Signal Circuit Testing Technologies in IoT Era

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Contents

- Research Background
- Analog/Mixed-Signal Circuit Testing
- Operational Amplifier Testing
- ADC Linearity Testing
- Analog Signal Generation with AWG
- Waveform Sampling Technique
- Timing Testing
- Challenges and Conclusion

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Hot Applications in IC Industry

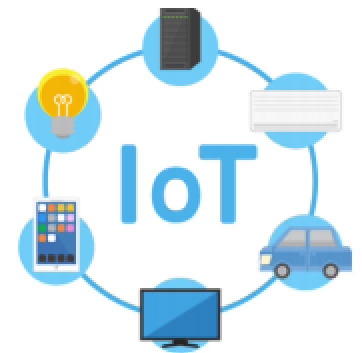
- Automotive application

  ppm (parts per million) → ppb (parts per billion)

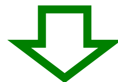
  low quality → out of business

- IoT systems

  A lot of sensors, interface analog circuits



High reliability, Low cost system



High quality, low cost testing of LSI is important !

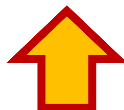
Test and Measurement are different

LSI test and measurement

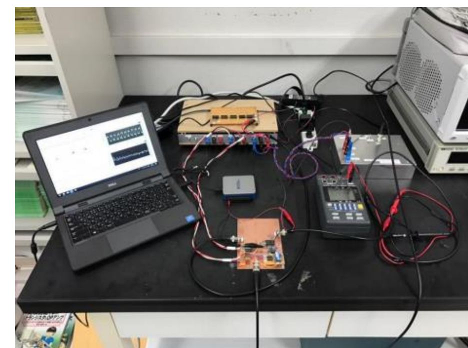
- **Production Test :**

  Decision of "Go" or "No Go"

  LSI testing → manufacturing engineering.



Today's focus



- **Measurement / Characterization**

  Accurate performance evaluation of circuit

IC Testing Technologies

- Analog/mixed-signal portions continue to be difficult part of SoC test.

  → most troublesome parts

- LSI testing technology reduces cost and improves quality simultaneously.
- Additional benefits of testing:

Improvement of

- Yield
- Reliability
- Security
- Diagnosis

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Management Strategy

- Strategy 1 :

  Use low cost ATE and develop analog BIST/BOST to make testing cost lower.

- Strategy 2 :

  Use high-end mixed-signal ATE as well as its associated services & know how.
  Fast time-to-market & no BIST can make profits much more than testing cost.

Save or Earn

ATE: Automatic Test Equipment

BIST: Built-In Self-Test, BOST: Built-Out Self-Test

Low Cost Testing

- Low cost ATE

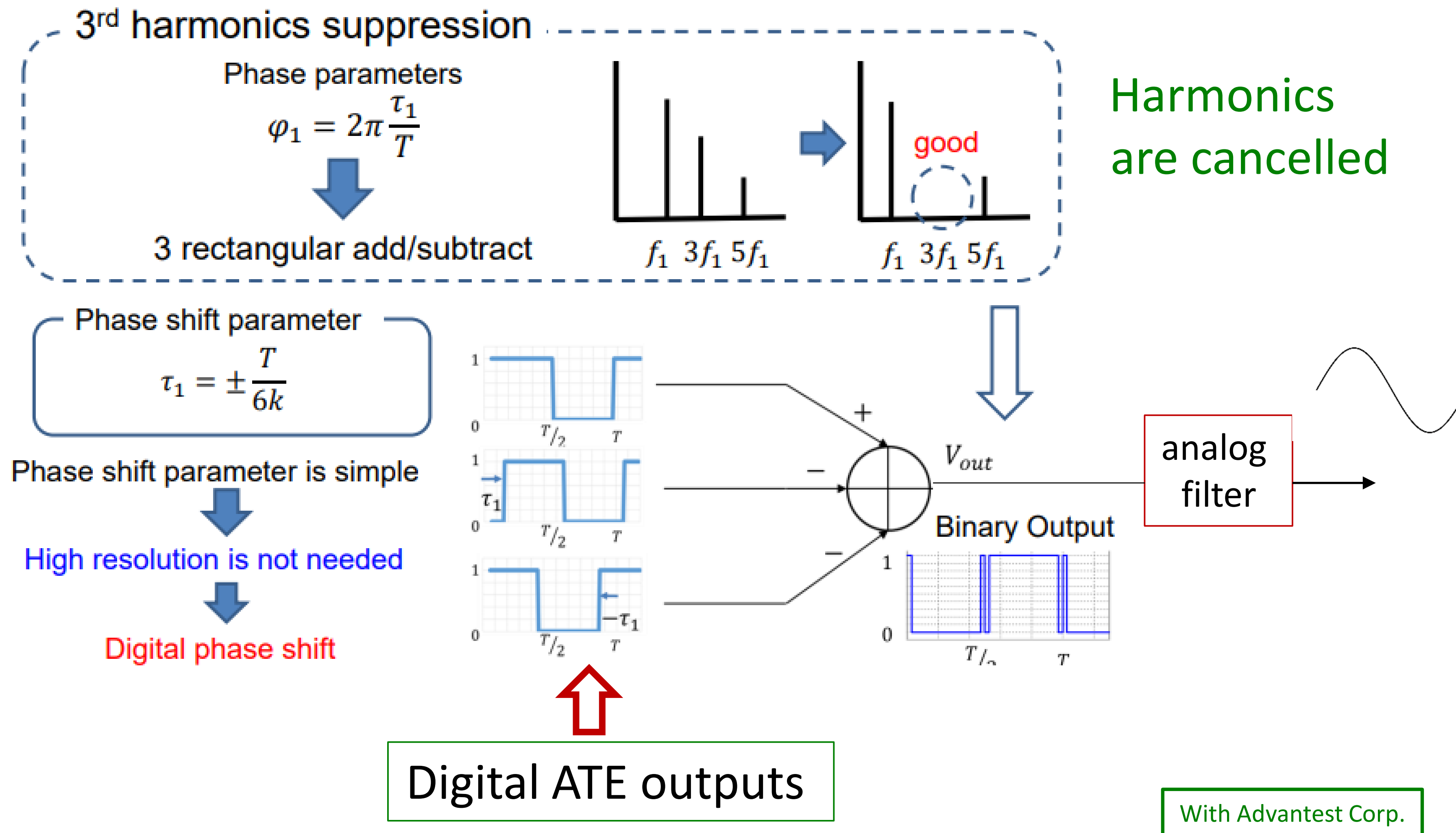
A penny saved is a penny earned.

Digital ATE

- No analog option such as Arbitrary Waveform Generator: AWG
- Input/output are mainly digital.

- Short testing time
- Multi-site testing
- Minimum or no chip area penalty for BIST
- Extensive usage of BOST

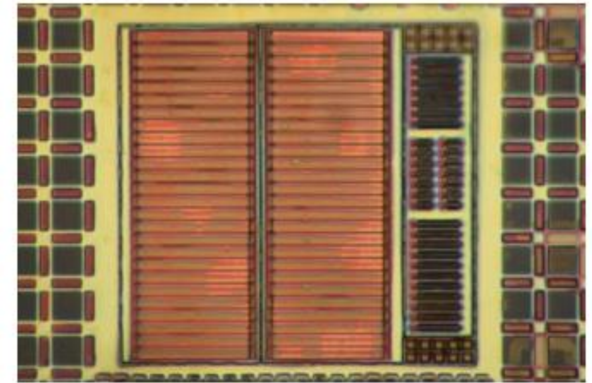
Sine Wave Generation with Digital ATE



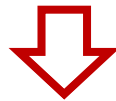
[1] M. Kawabata, K. Asami, S. Shibuya, T. Yanagida, H. Kobayashi, "Low-Distortion Signal Generation for Analog/Mixed-Signal Circuit Testing Using Digital ATE", The First International Test Conference in Asia, Taipei, Taiwan (Sept. 2017)

Hot Topics in Analog/Mixed-Signal Circuit Testing

- Analog fault model
- Analog fault simulation
- Analog test coverage
- Defect-based analog test



Analog IC



Very difficult,
but automotive industry strongly demands

Analog BIST

- BIST for digital : Successful

  BIST for analog : Not very successful

  ➡ Challenging research

- Digital test : Functionality ➡ Easy

  Analog test : Functionality & Quality ➡ Hard

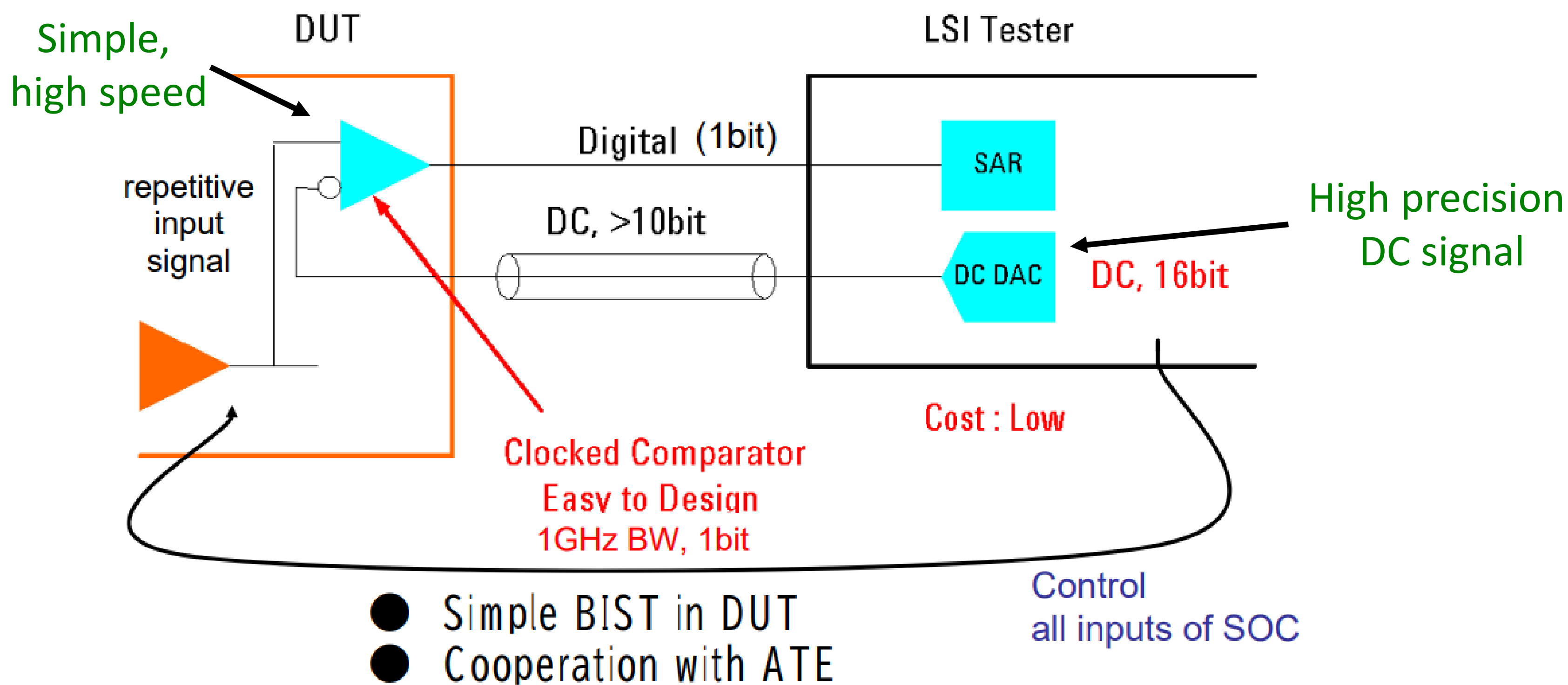
Analog: parametric fault as well as fatal fault.

Prof. A. Chatterjee

Specification-based Test ↔ Alternative Test ↔ Defect-based Test

- In many cases
  - Analog BIST depends on circuit.
  - No general method like scan path in digital.
  - One BIST, for one parameter testing

Cooperation of Analog BIST and ATE



Output signals from SoC can be repetitive by controlling all inputs to SOC with ATE

→ No need for T/H circuit in front of SAR ADC

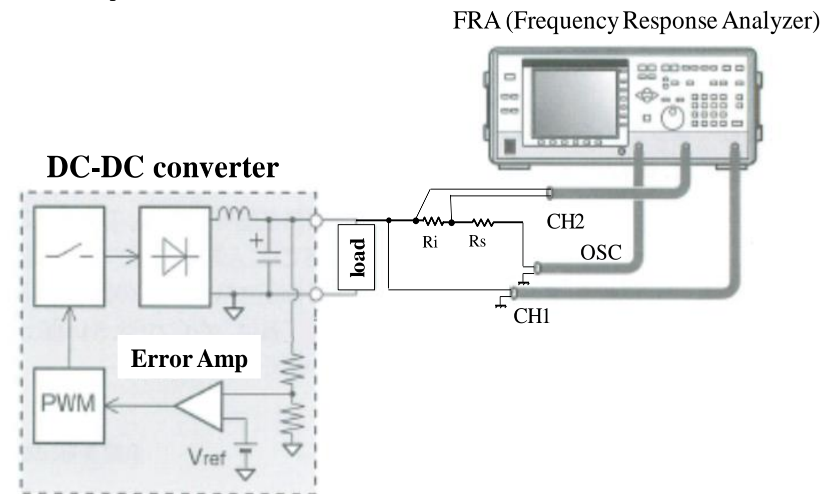
→ Wideband signal testing is possible

[2] T. Komuro, N. Hayasaka, H. Kobayashi, H. Sakayori,
"A Practical BIST Circuit for Analog Portion in Deep Sub-Micron CMOS System LSI'',
International Symposium on Circuits and Systems (ISCAS) (May.2005).

RF / High-Speed IO / Power Circuit Testing

- RF / HSIO / Power circuit testing is different from each other as well as analog testing technology.
- These are also challenging areas.
- Power supply circuit test example:

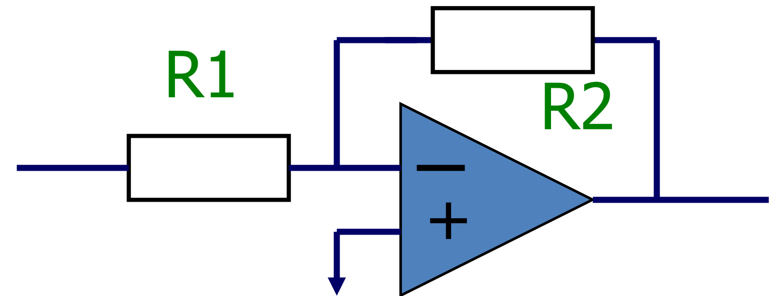
- Power supply circuit stability test without breaking the loop



[3] N. Tsukiji, Y. Kobori, H. Kobayashi, "A Study on Loop Gain Measurement Method Using Output Impedance in DC-DC Buck Converter ", IEICE Trans. Communications, (Sep. 2018).

Robust Design and Testing

Robust design makes its testing difficult.



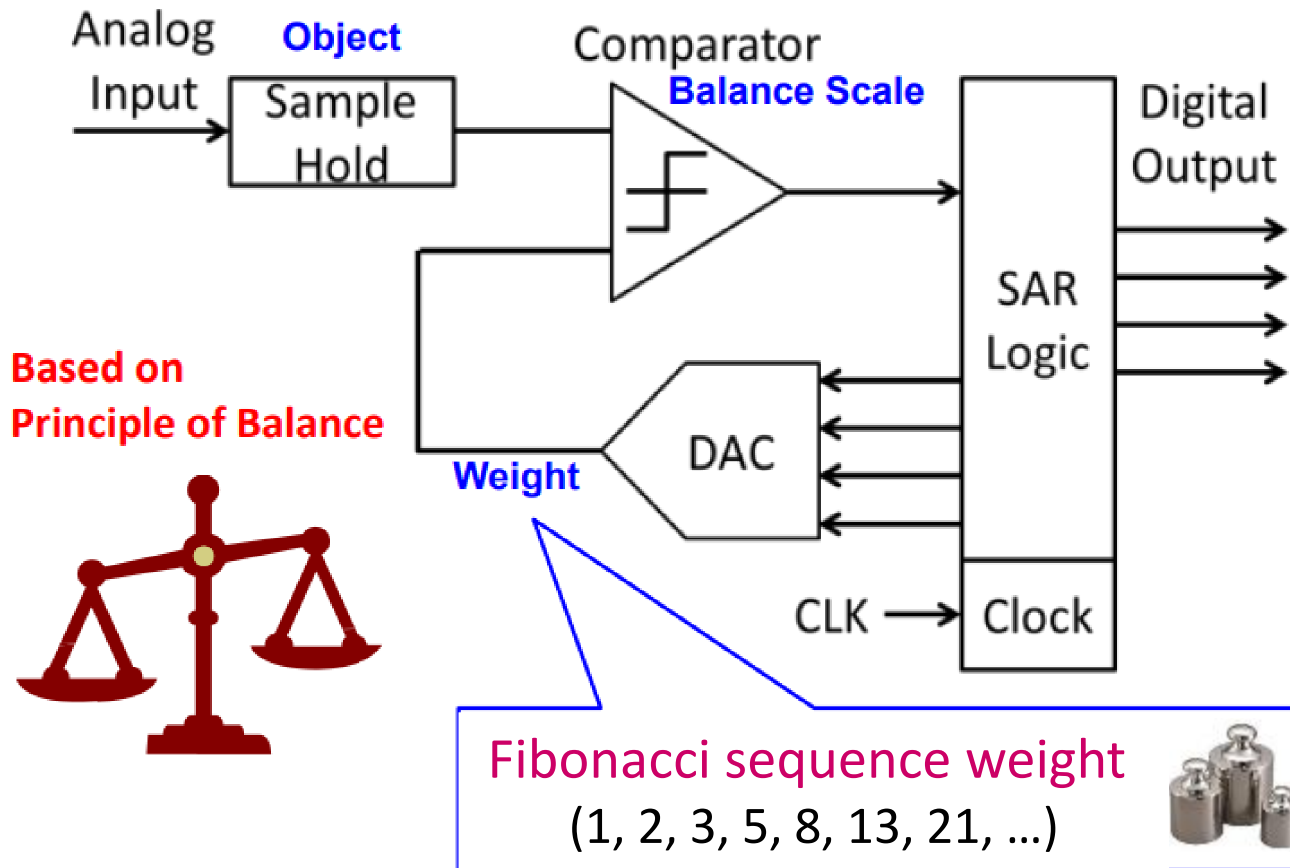
- Feedback suppresses parameter variation effects.
- Self-calibration and redundancy hide defects in DUT.
- Secure IC is difficult to test.

Trojan

[4] T. Yagi, H. Kobayashi, Y. Tan, S. Ito, S. Uemori, N. Takai, T. J. Yamaguchi, "Production Test Consideration for Mixed-Signal IC with Background Calibration", IEEJ Trans. Electrical and Electronic Engineering (Nov. 2010).

Redundancy SAR ADC Design Example

Reliable circuit ↔ Test difficulty



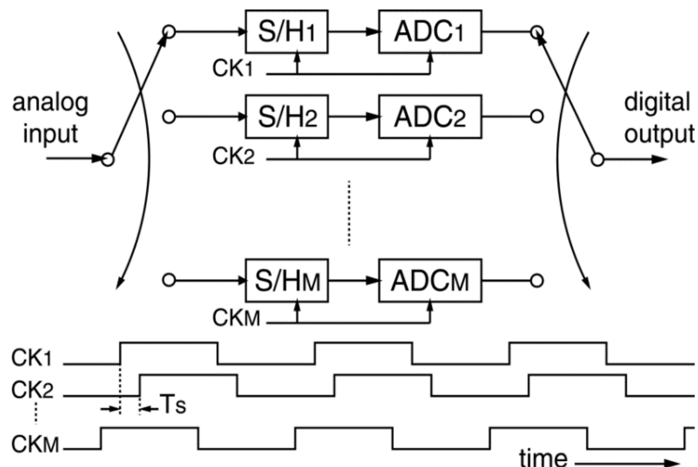
Fibonacci sequence weight
(1, 2, 3, 5, 8, 13, 21, ...)

[5] Y. Kobayashi, H. Kobayashi, et. al.,
"Redundant SAR ADC Algorithms for Reliability Based on Number Theory",
First IEEE International Workshop on Automotive Reliability & Test- ART Workshop (Nov. 2016)
[6] T. Ogawa, H. Kobayashi, "SAR ADC That is Configurable to Optimize Yield,"
IEEE Asia Pacific Conference on Circuits and Systems, Kuala Lumpur, Malaysia (Dec. 2010).

ATE for Mixed-Signal IC Testing

- Analog part of ATE is costly for development.
- Analog BIST is also beneficial for mixed-signal ATE manufacturer
- ATE must be designed with today's technology for tomorrow's higher performance chip testing.

Interleaved ADC used in ATE
to realize very high sampling rate
with today's ADCs



[7] R. Yi, M. Wu, K. Asami, H. Kobayashi, et. al.,
"Digital Compensation for Timing Mismatches in Interleaved ADCs",
IEEE 22nd Asian Test Symposium, Yilan, Taiwan, (Nov. 2013)

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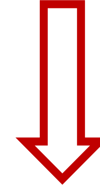
IoT System and OP amp

- OP amp with smaller than μV-order offset is a key component of IoT system



Its guarantee at production test

IoT Sensor Network

Sensor

Sonar, Pressure, Geomagnetic, Soil

Accelerator, Humidity, Temperature, Sounds

Gyro, Flow, Illuminance, Image

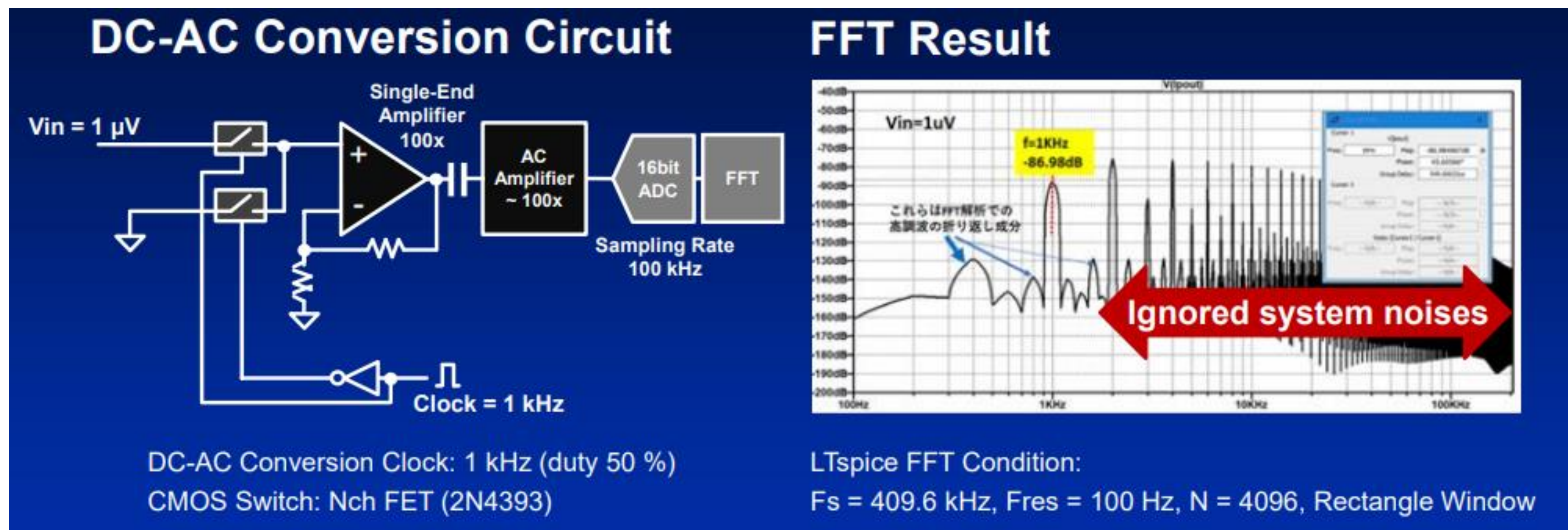
OP-Amp → LPF → ADC → MCU → Wi-Fi

µV-order Voltage Measurement

- µV-order OP amp offset voltage testing in short time at low cost.
- DC-AC conversion

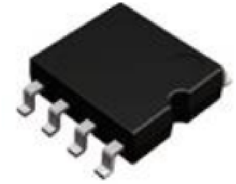
  ➡ No influence by DC noise, drift, thermal effects

- Applicable to multi-site testing



[8] Y. Sasaki,, T. Nakatani, H. Kobayashi, et. al., "Accurate and Fast Testing Technique of Operational Amplifier DC Offset Voltage in µV-order by DC-AC Conversion“, 3rd International Test Conference in Asia (Sept. 2019).

OP amp test with Null Method



Low-cost , high-quality testing of operation amplifier

Goal

Null Method → Apply for mass production testing

Null Method

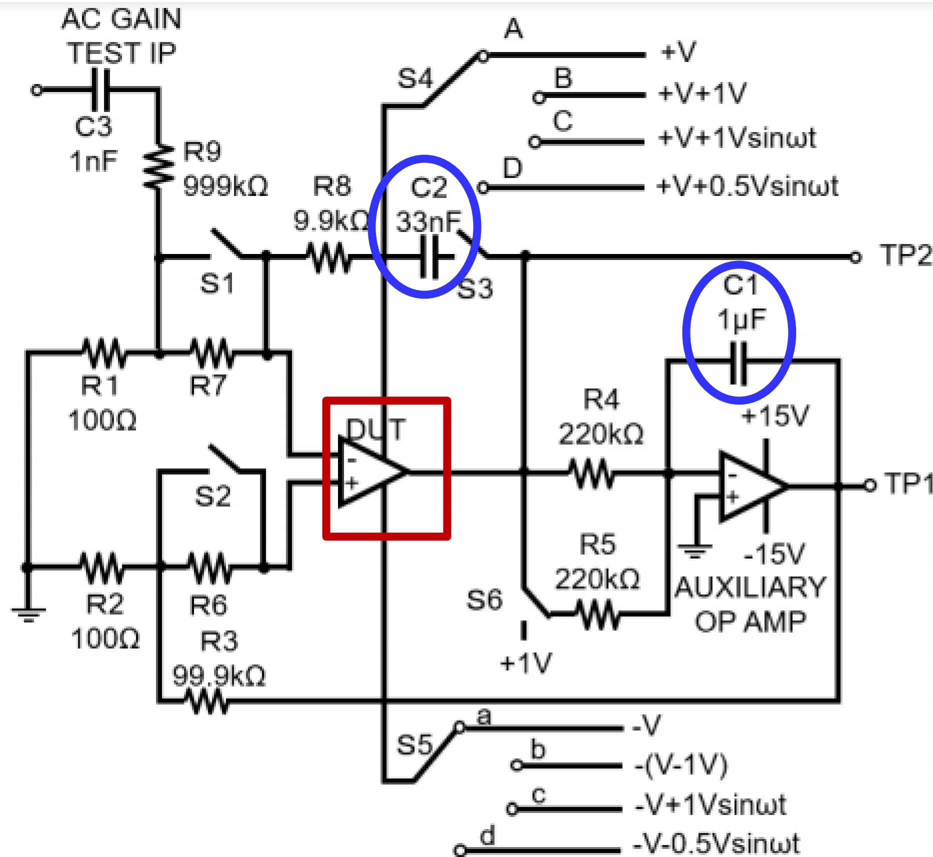
Measurement time : Long

Mass production testing : Difficult

1 second test time for
1 US dollar chip

Good capacitor value selection ➡ Fast, stable operation

Null Method Circuit



Operational Amplifier Measurement Circuit using the Null Method

Source：Analog Dialogue Vol 45 Apr.2011 Analog Devices

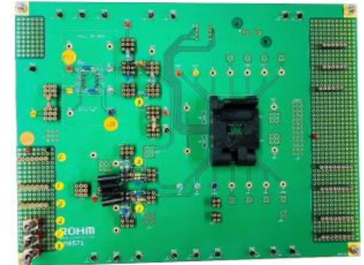
Switches (S1,.., S6)

- Offset
- Bias Current
- DC gain
- AC gain
- DC CMRR
- DC PSRR
- AC CMRR
- AC PSRR etc.

can be measured accurately

Accurate but slow !

Experiment & Simulation Verification



Our prototype

- Optimization of phase compensation constants

  C_1=1nF, C_2=0.1μF

  Null Circuit → Fast and Stable

- Null Circuit : Change of signal application point depending on the measurement item

- Switching C_1 and C_2 depending on the measurement item

  Settling time reduction → ≒ 1/10

Null method → Production testing

[9] R. Aoki, S. Katayama, Y. Sasaki, K. Machida, T. Nakatani, J. Wang, A. Kuwana, K. Hatayama, H. Kobayashi, K. Sato, T. Ishida, T. Okamoto, T. Ichikawa, "Evaluation of Null Method for Operational Amplifier Short-Time Testing", 13th IEEE International Conference on ASIC, Chongqing, China (Oct. 2019)

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ADC Testing (DC Linearity)

- DC linearity test is the most important in many cases of ADC under test.
  - Precise ramp generation is challenging.
  - High resolution ADC ➡ long testing time
- DC testing time is proportional to number of codes / sampling frequency

  large / slow

ADC Testing (AC Performance)

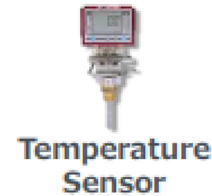
- ADC AC performance testing
  - Sampling clock jitter
  - High frequency input signal
- We have to build low clock jitter system and apply high frequency input signal. No alternative method so far.

ΔΣADC INL Test

Target

Product	:24bit 6.8sps Delta-Sigma ADC
Test Item	:INL
Final Product	

Air Flow Sensor

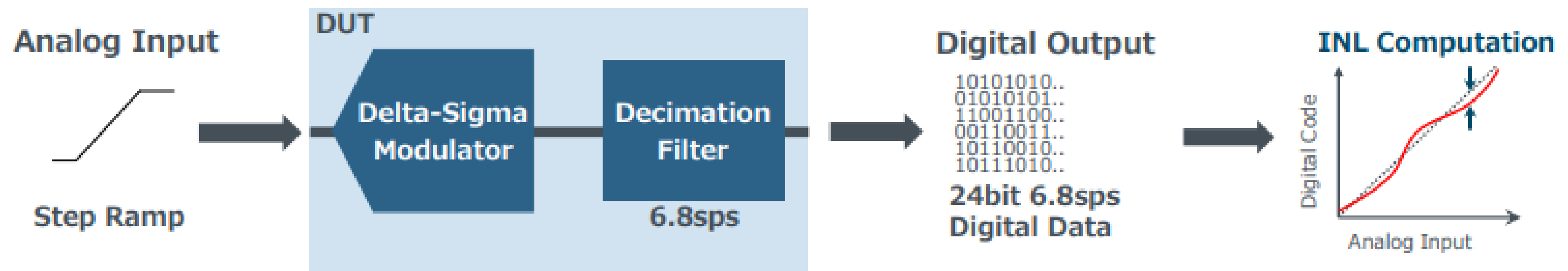

Temperature Sensor

Pressure Sensor

Strain Gauge

INL: Integral Non-Linearity

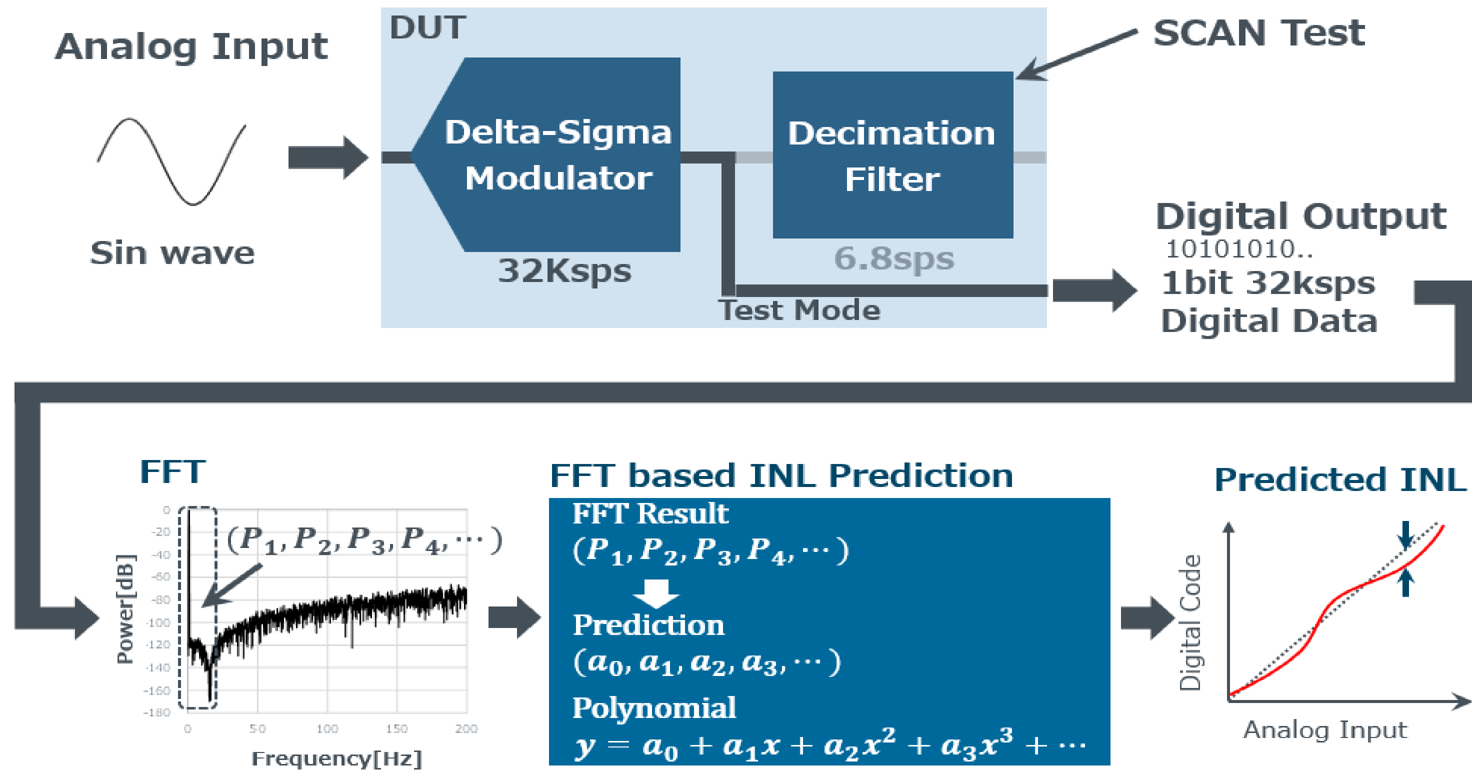
Problems of direct method



$$TestTime = 2^{24} * \frac{1}{6.8} * n = 685[\mathrm{h}] * n \qquad n = \frac{Samples}{Code}$$

Test Time will be 685[h]. Is it acceptable?

Proposed ΔΣADC INL Test Method



Test Time Estimation

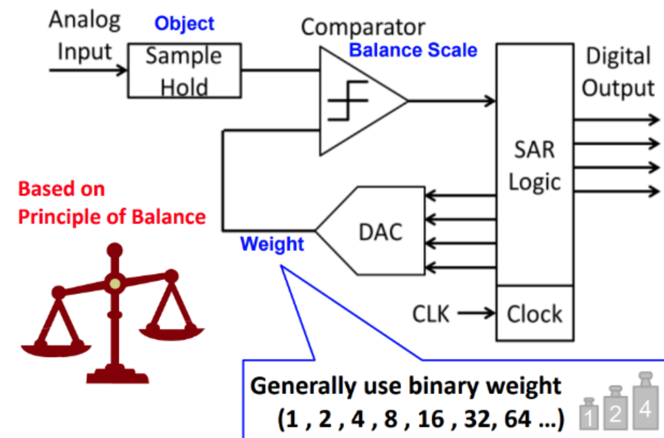
Conventional $TestTime = 685[\mathrm{h}]$

Proposed $TestTime = 34[\mathrm{sec}](2^{20}\mathrm{point})$

[10] J.-L. Wei, K. Sato, H. Kobayashi, et. al. , "High-Resolution Low-Sampling-Rate ΔΣADC Linearity Short-Time Testing Algorithm", 13th IEEE ASICON, Chongqing, China (Oct. 2019)

DFT for SAR ADC Linearity

A high-resolution, low-sampling rate ADC requires a long test time for its linearity.

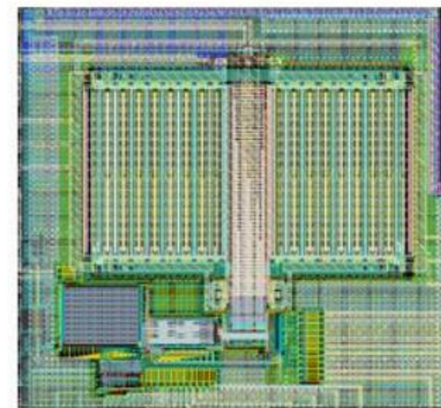


Shorten SAR ADC linearity test time.

For a 12-bit SAR ADC, its linearity test time
→ 1/4

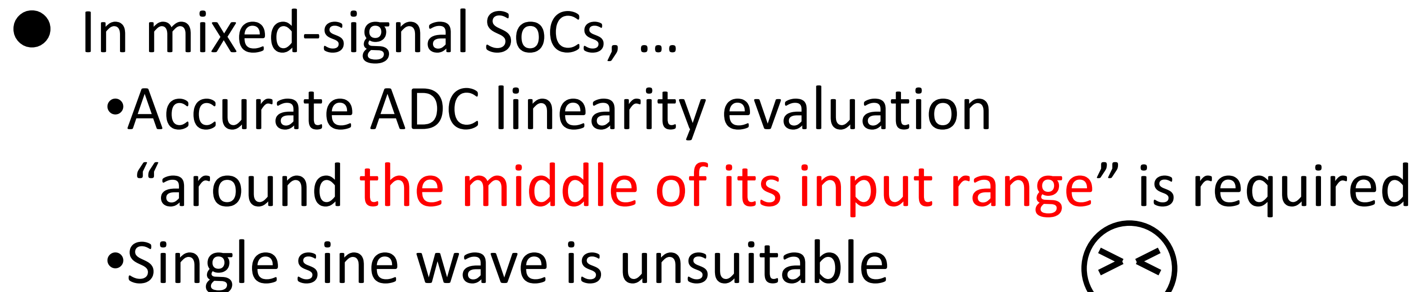
DFT: Design for Testability

[11] T. Ogawa, H. Kobayashi, et. al., "Design for Testability That Reduces Linearity Testing Time of SAR ADCs", IEICE Trans. Electronics (June 2011).

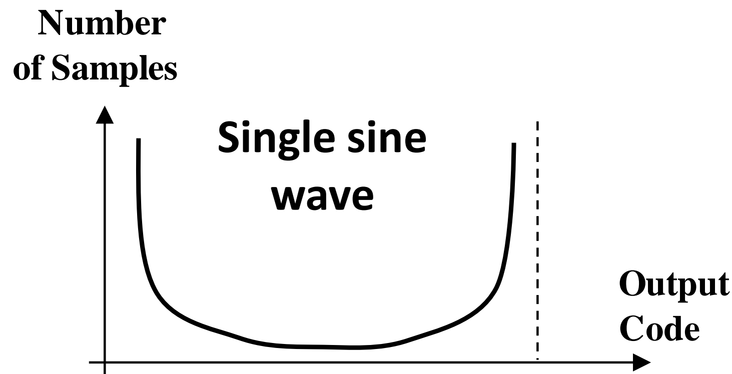


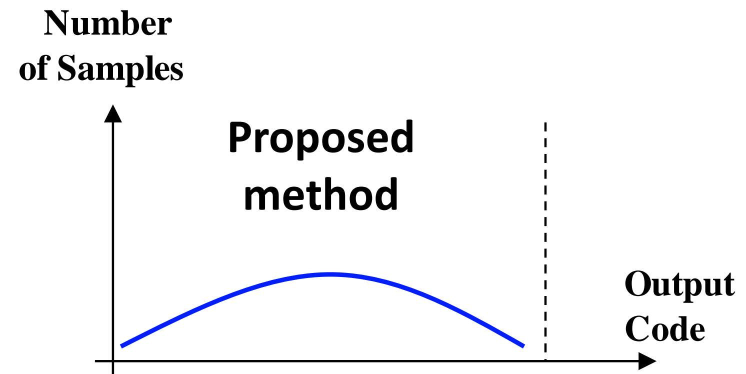
Our SAR ADC
TSMC 180nm
1.2mmx1.2mm

Analog Signal Generation for ADC Histogram Test

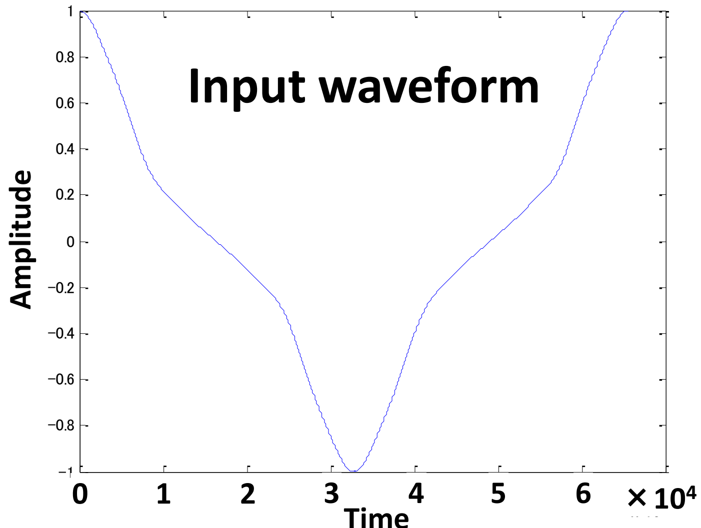


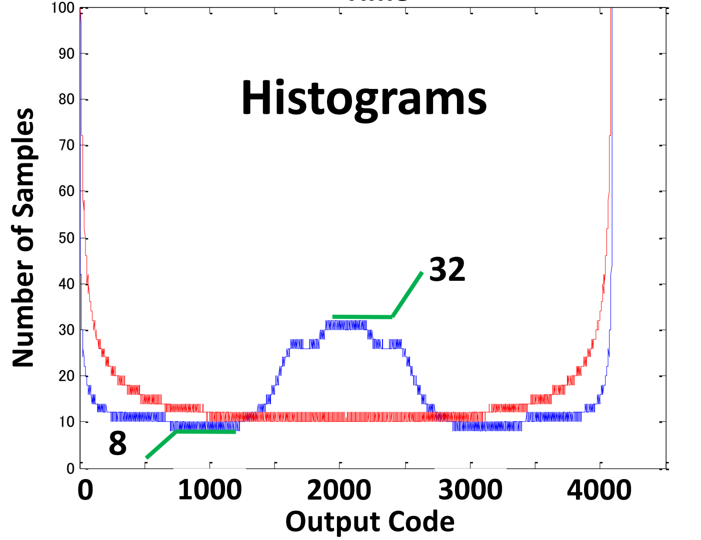
This Work





ADC Histogram Test with Multi-tone





Proposed

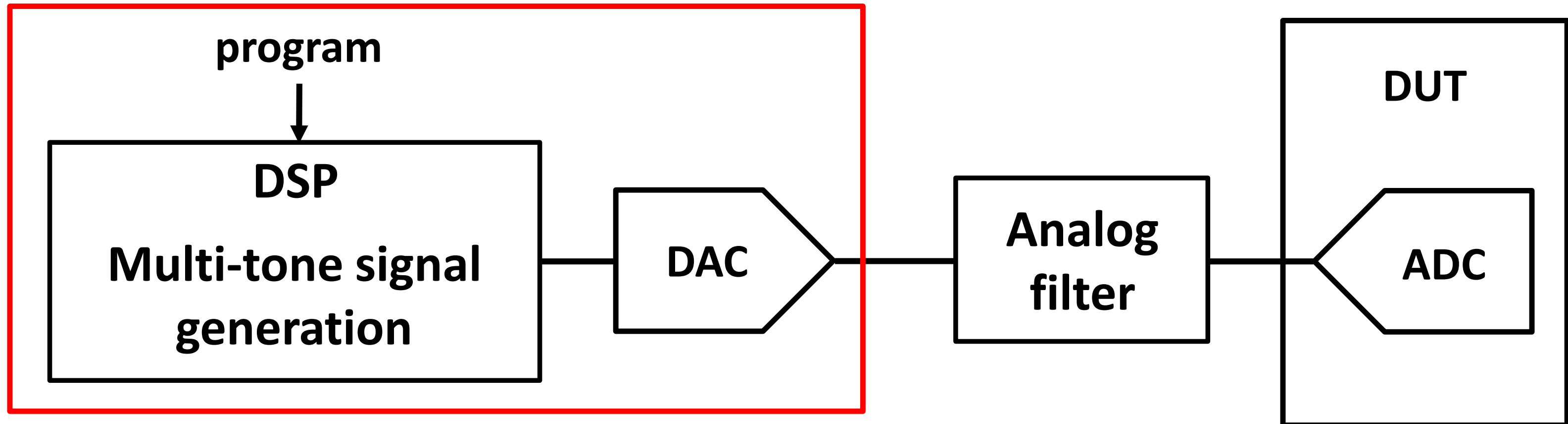
$$V_n = \frac{\cos((2n-1)\omega t)}{(2n-1)^2} \qquad n=1,2,\cdots$$

$$V_{in} = \frac{4}{\pi}\left(V_1 + 2.6\cdot V_2 + 1.8\cdot V_3 + 1.4\cdot V_6 + 1.2\cdot V_7\right)$$

Linearity test time reduction

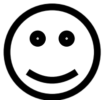
[12] S. Uemori, H. Kobayashi, et. al.,"ADC Linearity Test Signal Generation Algorithm", IEEE Asia Pacific Conference on Circuits and Systems, Kuala Lumpur, Malaysia (Dec. 2010)

Architecture for Generating Proposed Test Signal



- DSP program : Multi-tone sine wave
- Analog filter : Harmonics removal

As a result ...



- Histogram for the middle of ADC input range can be high.

ADC linearity test time → 1/2

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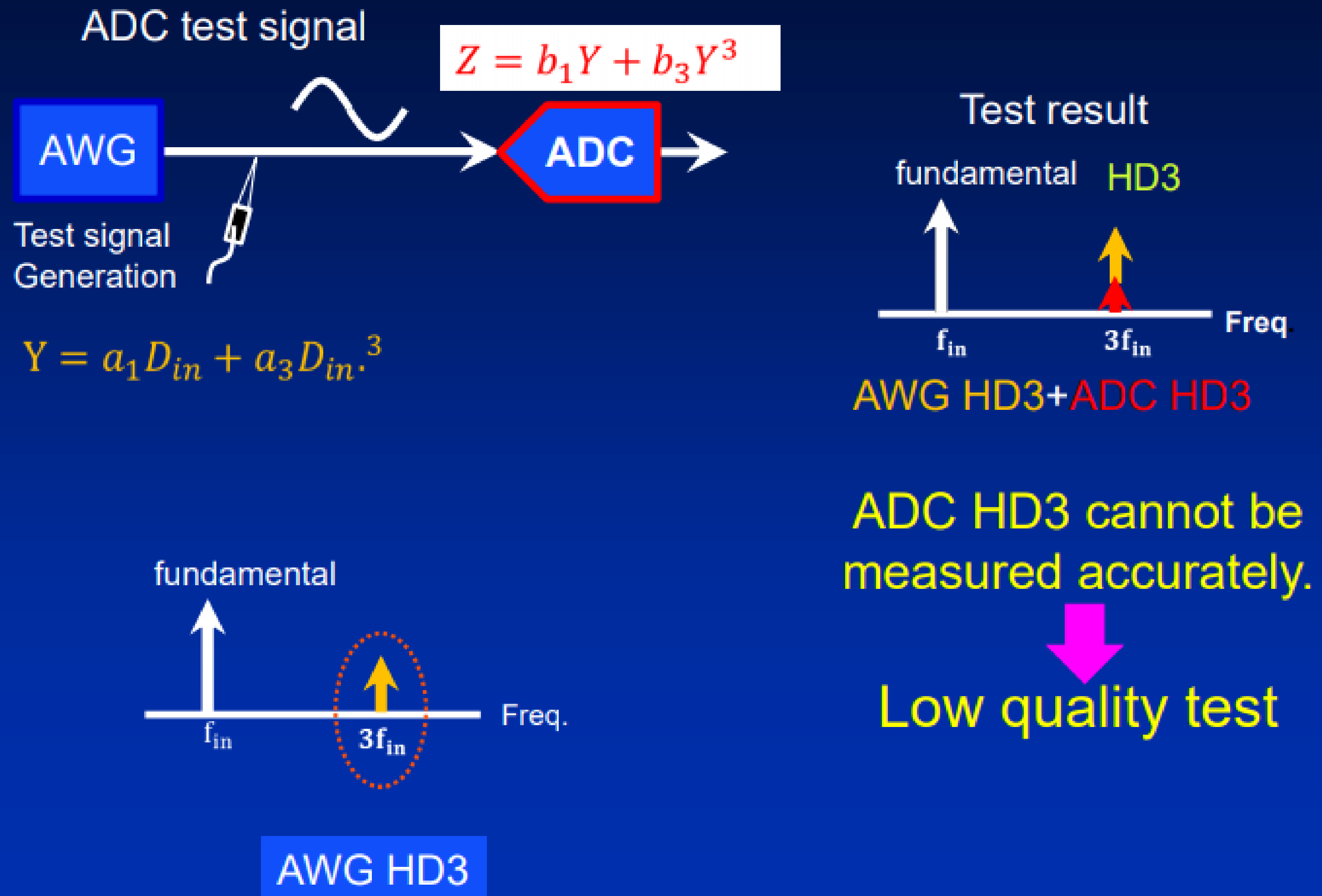
Signal Generation for Analog Circuit Test

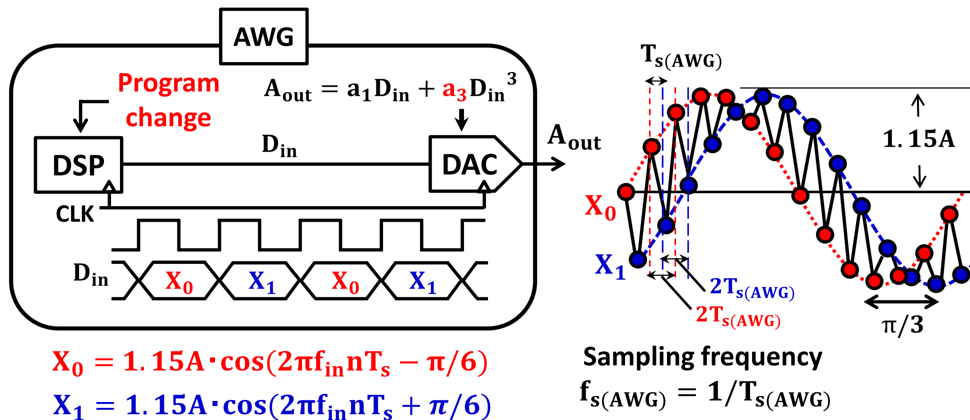


AWG: Arbitrary Waveform Generator

Low-Distortion Sine Wave Generation

- Low-distortion sine-wave generation using Arbitrary Waveform Generator (AWG)
- Compensation of AWG nonlinearity by digital pre-distortion
- ADC test signal

Phase switching method

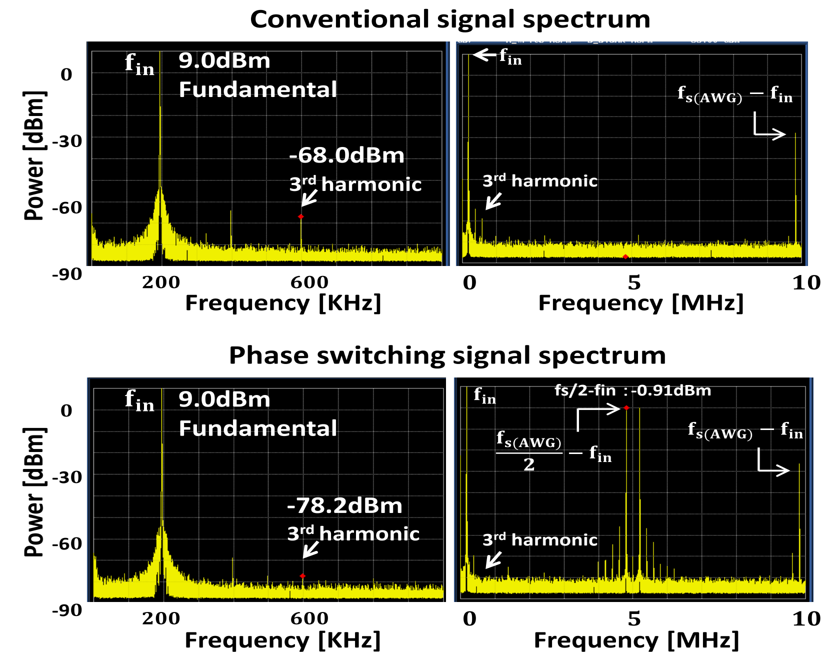


$X_0 = 1.15A \cdot \cos(2\pi f_{in} n T_s - \pi/6)$

$X_1 = 1.15A \cdot \cos(2\pi f_{in} n T_s + \pi/6)$

Sampling frequency

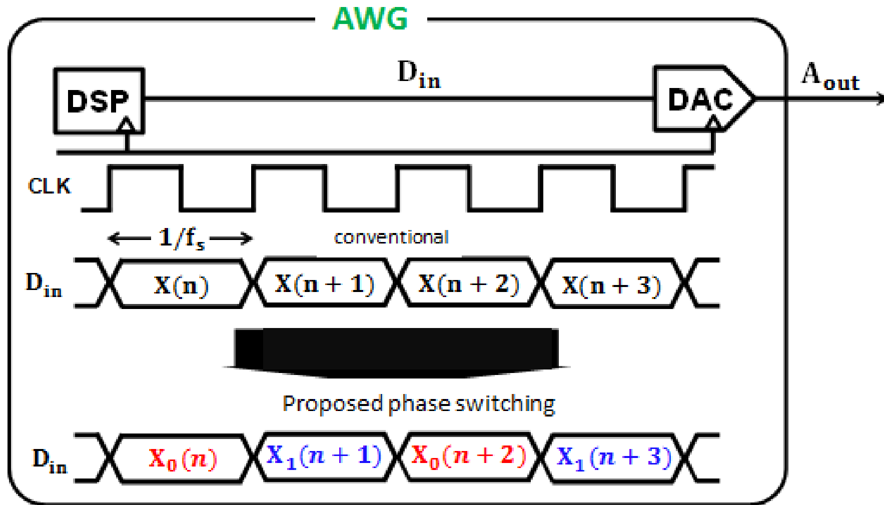
$f_{s(AWG)} = 1/T_{s(AWG)}$



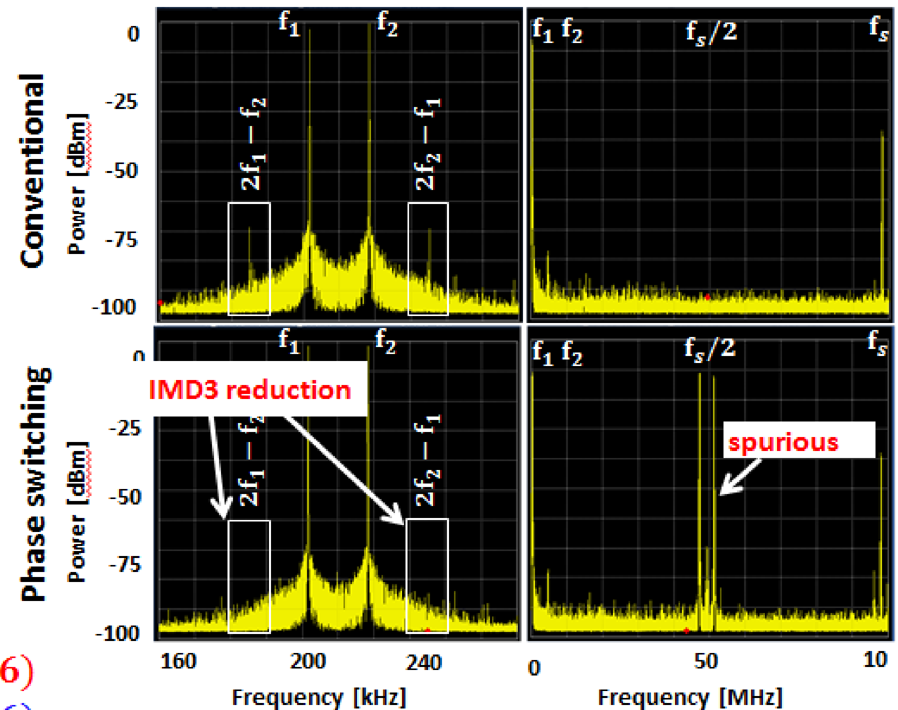
[13] F. Abe, Y. Kobayashi, K. Sawada, K. Kato, O. Kobayashi, H. Kobayashi, "Low-Distortion Signal Generation for ADC Testing," IEEE International Test Conference (Oct. 2014).

Low IMD3 2-Tone Signal Generation with AWG for Communication Application ADC Testing

IMD: Intermodulation Distortion



Measurement Results (AWG 2-tone output)



Conventional

$$X(n) = A\cos(2\pi f_1 nT_s) + A\cos(2\pi f_2 nT_s)$$

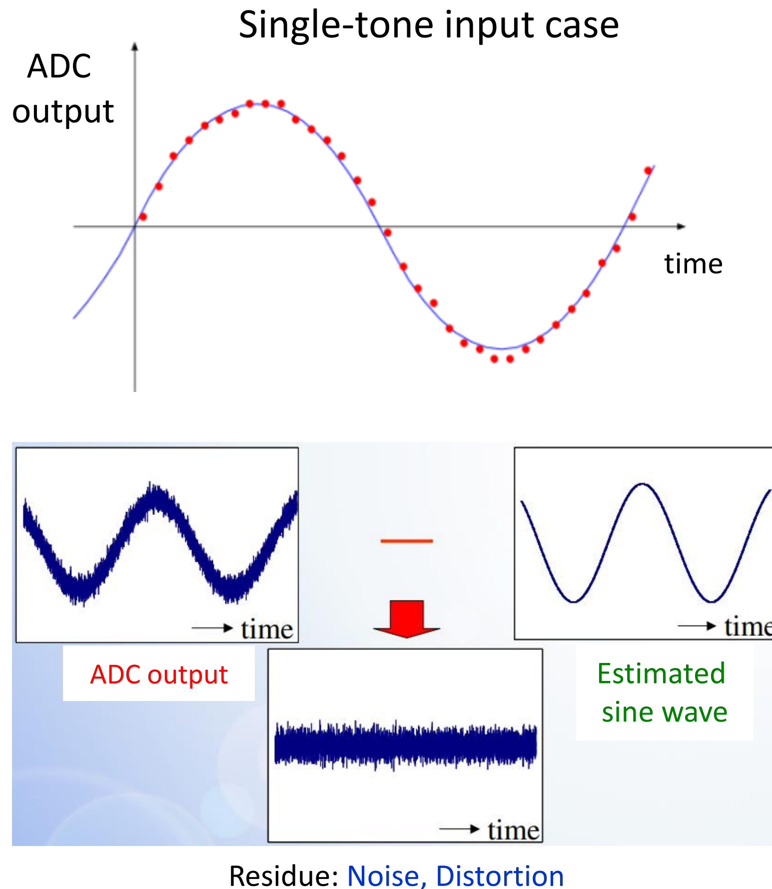
Proposed phase switching

$$X_0(n) = B\cos(2\pi f_1 nT_s + \pi/6) + B\cos(2\pi f_2 nT_s - \pi/6)$$

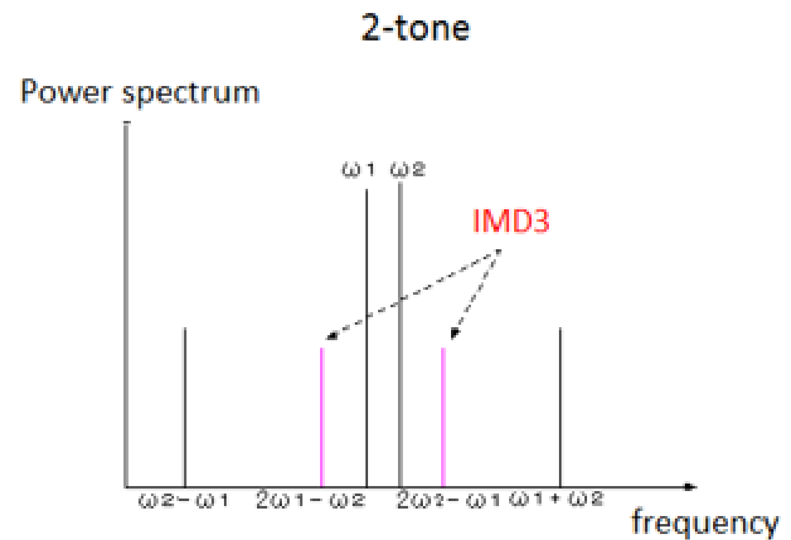
$$X_1(n) = B\cos(2\pi f_1 nT_s - \pi/6) + B\cos(2\pi f_2 nT_s + \pi/6)$$

[14] K. Kato, H. Kobayashi, et. al.,
"Two-Tone Signal Generation for Communication Application ADC Testing",
The 21st IEEE Asian Test Symposium, Niigata, Japan (Nov. 2012).

Two-tone Curve Fitting Algorithm for Communication Application ADC Testing



Residue: Noise, Distortion



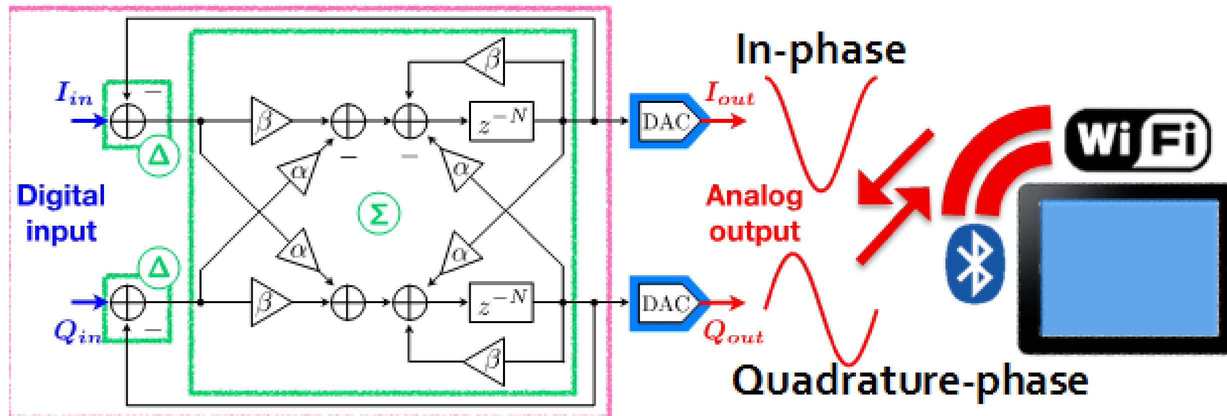
[15] Y. Motoki, H. Sugawara, H. Kobayashi, et. al.,
"Multi-Tone Curve Fitting Algorithms for Communication Application ADC Testing",
Electronics and Communication in Japan: Part 2, Wiley Periodicals Inc. (2003).

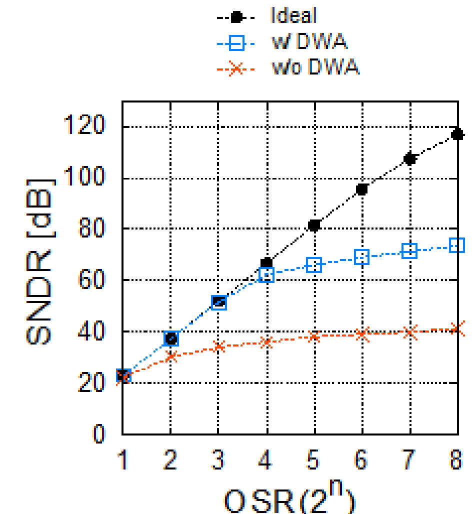
Complex Multi-Bandpass ΔΣ Modulator for I-Q Signal Generation

- **Generation of high quality analog I-Q signals**
- **Testing of communication application ICs**
- **Digital rich**

(Suitable to the realization with nano CMOS → Low cost)

ΔΣ modulation	Complex signal processing	Non-linear correction algorithm for Multi-bit DAC





[16] M. Murakami, H. Kobayashi, et. al.,
"I-Q Signal Generation Techniques for Communication IC Testing and ATE Systems",
IEEE International Test Conference, Fort Worth, TX (Nov. 2016).

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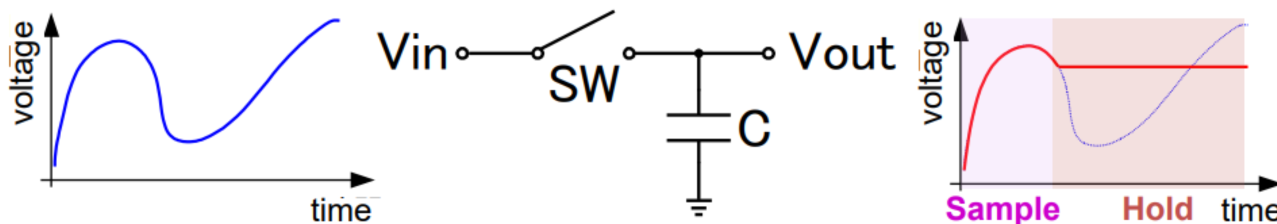
- Analog Signal Generation with AWG
- **Waveform Sampling Technique**
- Timing Testing
- Challenges and Conclusion

Waveform Sampling Technology

- Waveform sampling is important for analog signal test.
- Many issues for high performance sampling circuit
  - Noise, Distortion
  - Bandwidth
  - Jitter, Aperture time
  - Sampling clock rate
  - Power

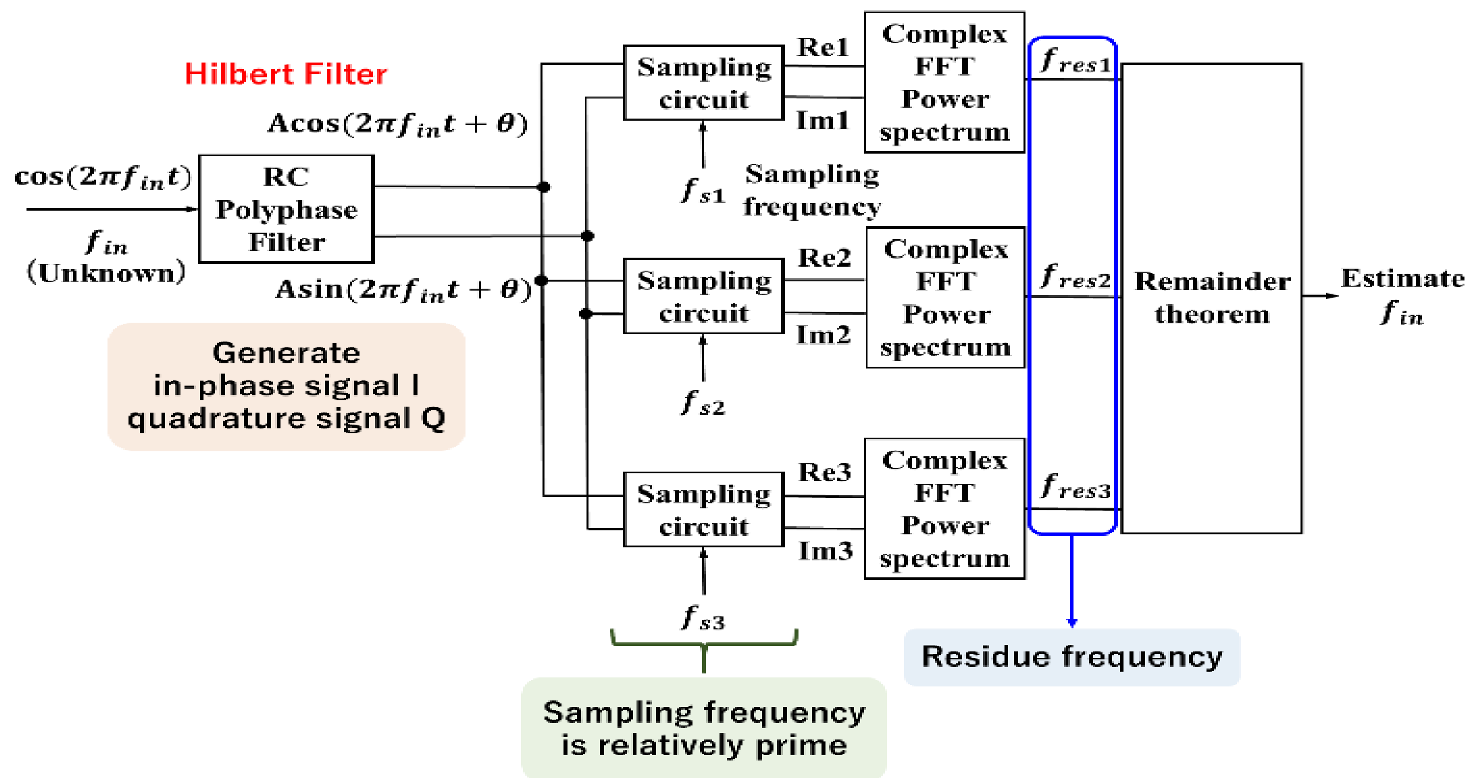
■Open-loop S/H circuit:
Switch and Capacitor



Residue Sampling Circuit

- Proactive usage of aliasing by waveform sampling
- Multiple low-rate sampling circuits

→ High-frequency waveform sampling



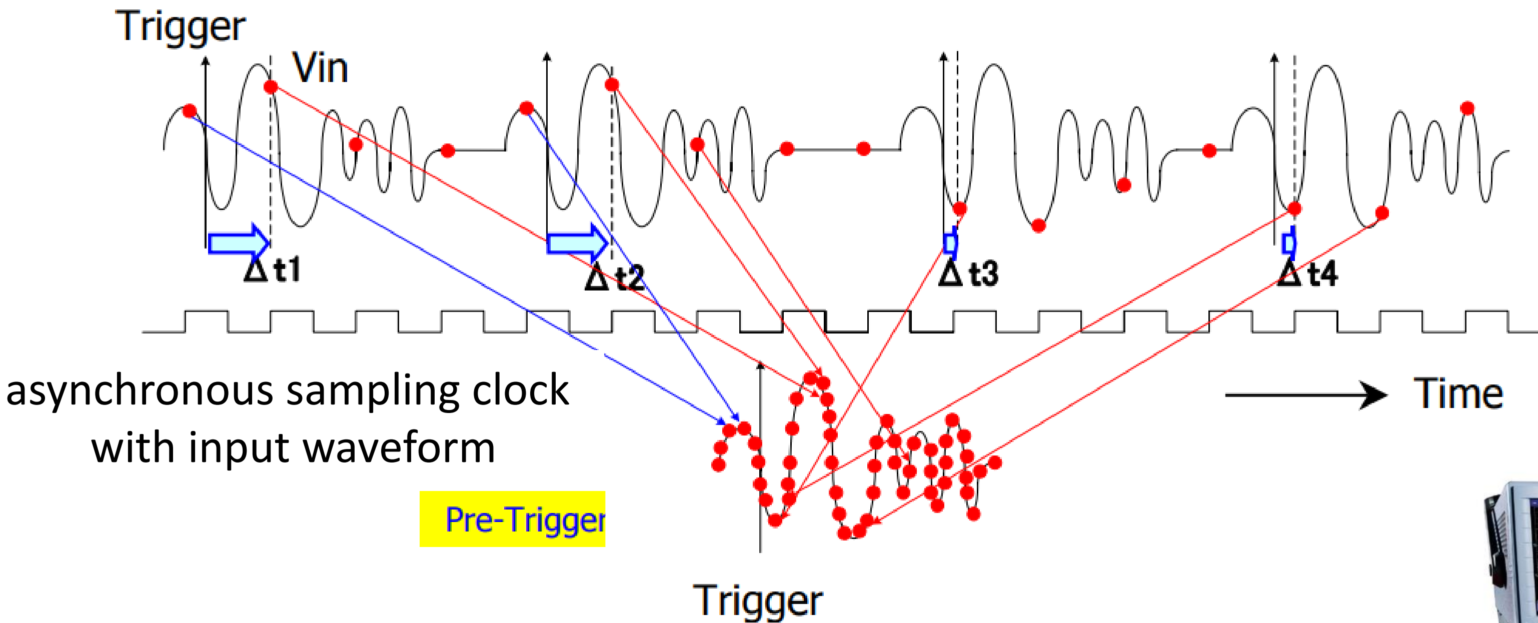
[17] Y. Abe, S. Katayama, C. Li, A. Kuwana, H. Kobayashi, "Frequency Estimation Sampling Circuit Using Analog Hilbert Filter and Residue Number System", 13th IEEE International Conference on ASIC, Chongqing, China (Oct. 2019).

Equivalent-Time Sampling in Testing

- Production Test :

  Input signal is controllable

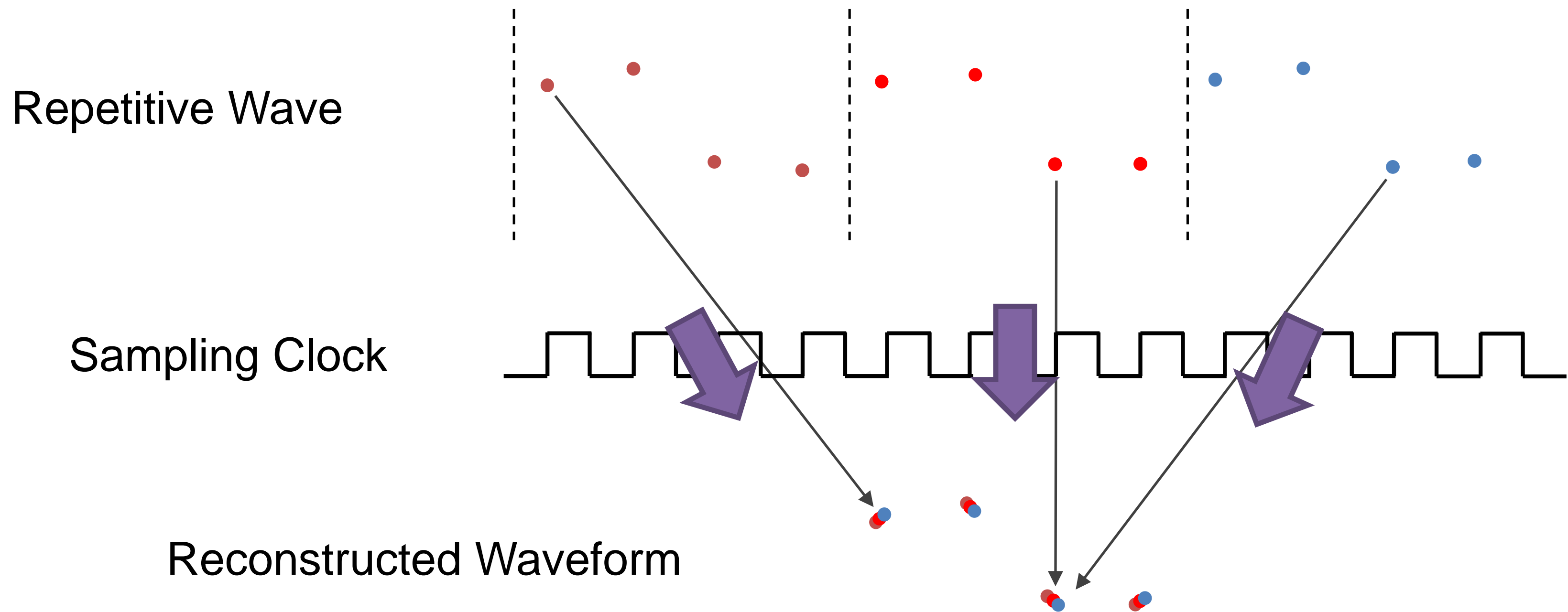
Waveform reconstruction of repetitive signal



Sampling oscilloscope

- Measurement : Input signal is unknown

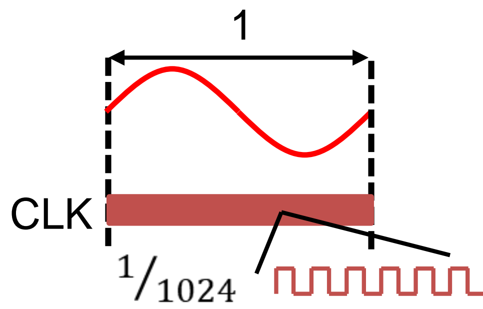
Waveform Missing Phenomena

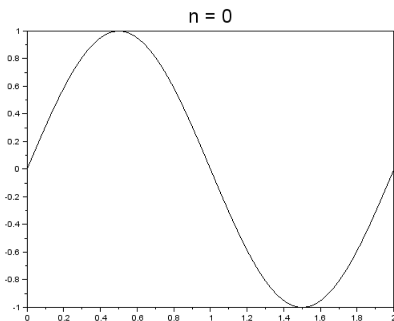


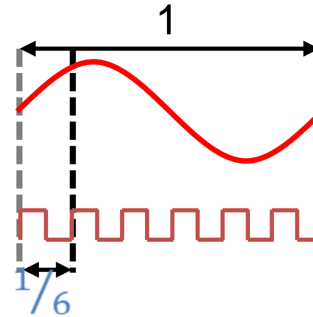
Toothless waveform appears

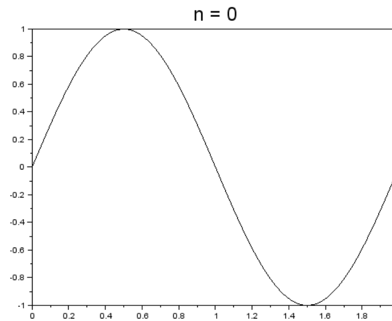
Waveform Missing Conditions

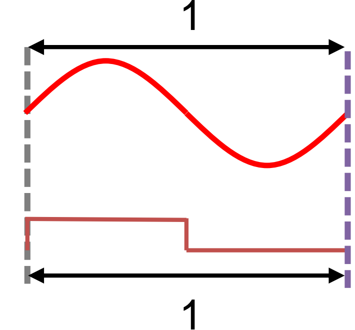
$f_{CLK} \gg f_{sin}$ $\quad$ $f_{CLK} \approx \frac{1}{\alpha} f_{sin} \left(\alpha = 1, \frac{1}{2}, \frac{1}{3}, \frac{2}{3}, \cdots, \frac{1}{6}, \cdots \right)$ $\quad$ $f_{CLK} \approx f_{sin}$

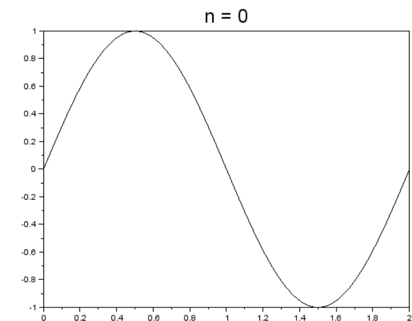






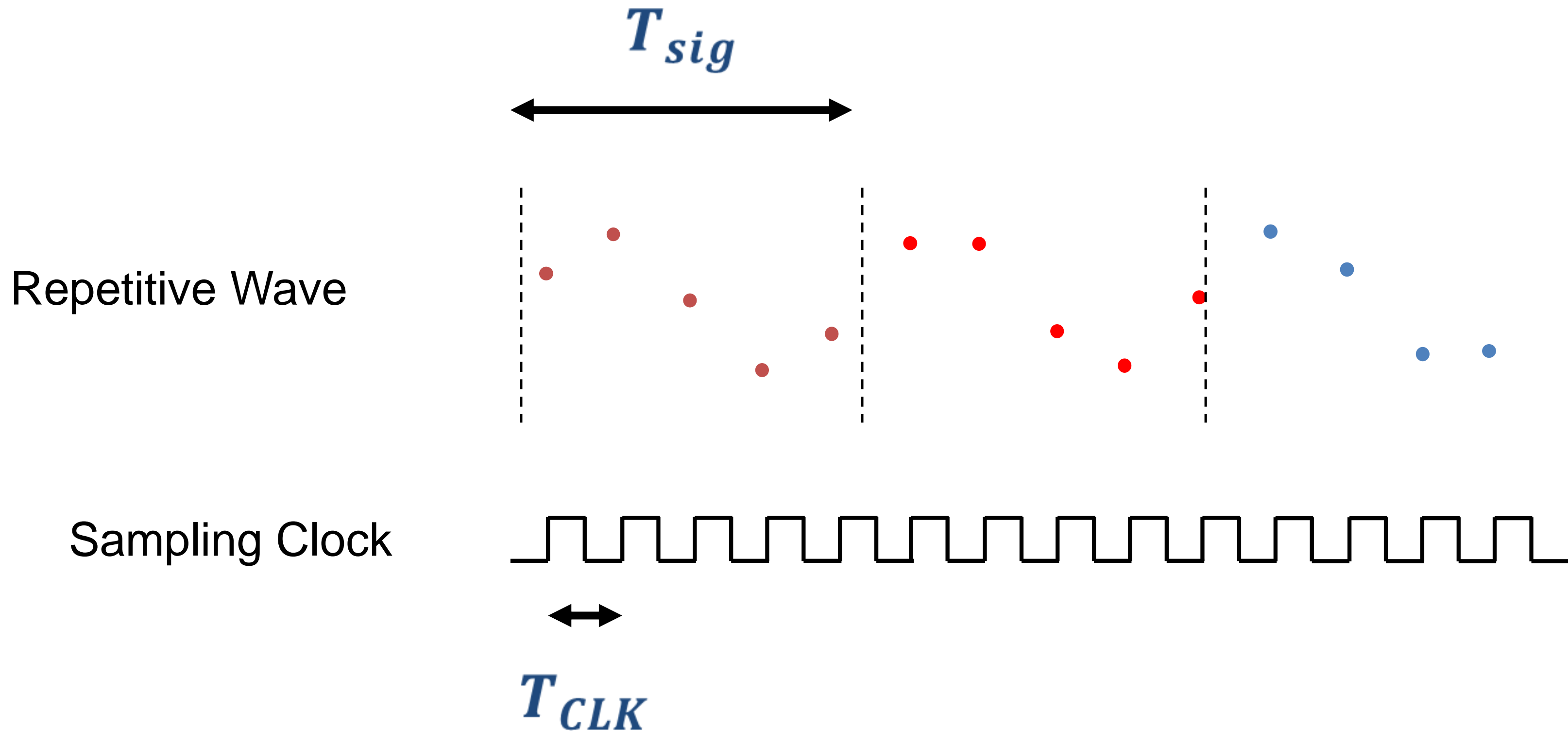






Sampling points move little ➡ Requires long time

Waveform Sampling Condition



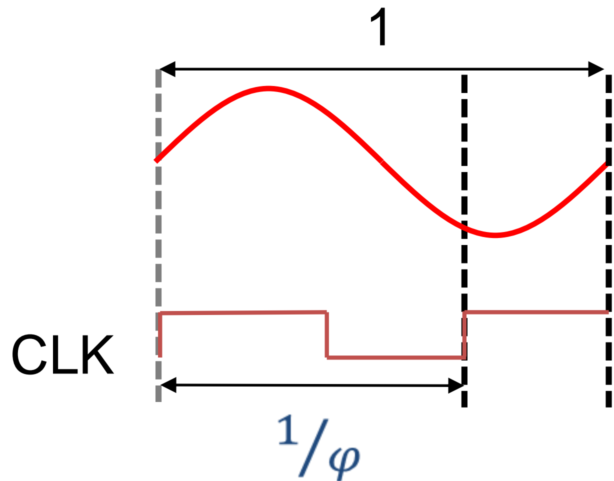
$$T_{CLK} = \ ? \ \times T_{sig}$$

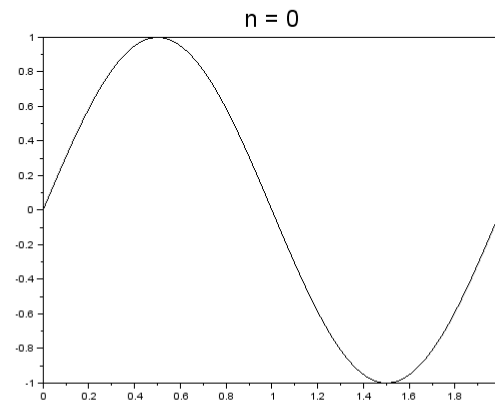
[18] Y. Sasaki, Y. Zhao, A. Kuwana, H. Kobayashi,
"Highly Efficient Waveform Acquisition Condition in Equivalent-Time Sampling System"
27th IEEE Asian Test Symposium, Hefei, Anhui, China (Oct. 2018)

Proposed Golden Ratio Sampling

$$f_{CLK} = \varphi \times f_{sig}$$

φ : Golden ratio (= 1.6180339887…)

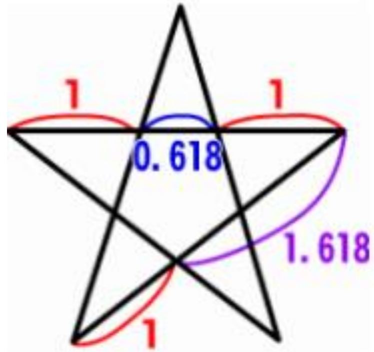


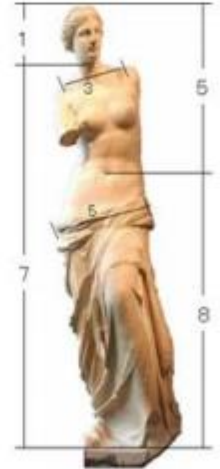


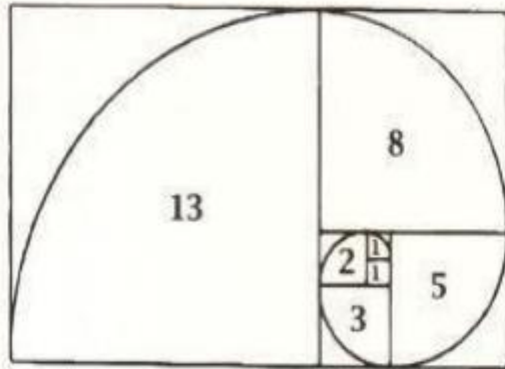
Sampling points disperse uniformly through measurement

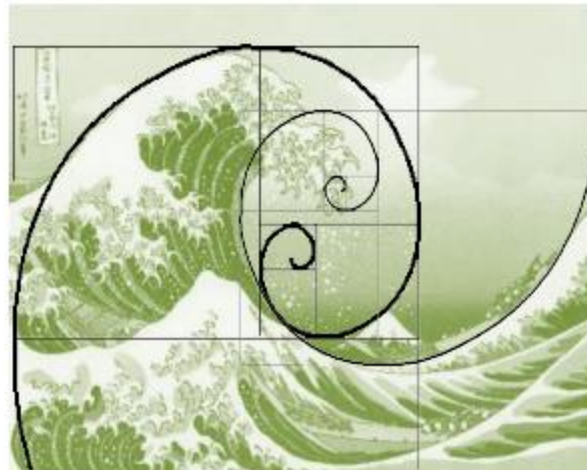
Golden Ratio is Everywhere !

The most beautiful ratio









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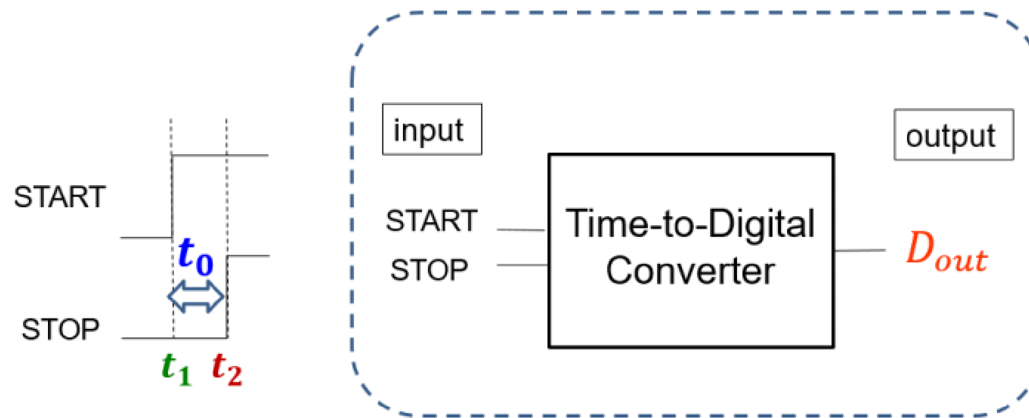
Time-to-Digital Converter (TDC)



CLK1
T
T
CLK2
CLK
Command
READ
DQS
Data

High-speed I/O interface signal timing testing

CLK1
τ τ τ τ τ τ τ
MUX
select
3
CLK2
D Q
SAR Logic
3
D_{out}

SAR TDC

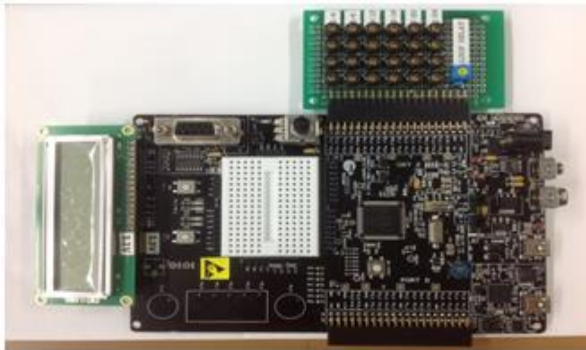
- ✓ **Small circuit**
- ✓ **Full digital**
- ✓ **High linearity**
- ✓ **High resolution**

[19] Y. Ozawa, H. Kobayashi, et. al.,
"SAR TDC Architecture with Self-Calibration Employing Trigger Circuit,"
The 26th IEEE Asian Test Symposium, Taipei, Taiwan (Nov. 2017)

TDC BOSTs for Timing Signal Testing

Single-bit ΔΣ TDC with analog FPGA

Multi-bit ΔΣ TDC with analog FPGA



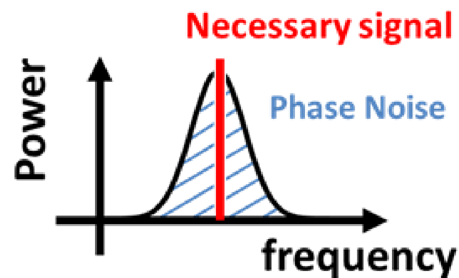
Flash-type TDC with analog FPGA

Flash-type TDC with digital FPGA

BOST: Built-Out Self-Test

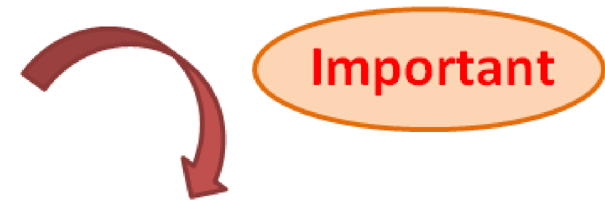
[20] T. Chujo, H. Kobayashi, et. al., ″Timing Measurement BOST With Multi-bit Delta-Sigma TDC”, 20th IEEE International Mixed-Signal Testing Workshop, Paris, France (June, 2015).

Phase Noise Test with ΔΣ TDC



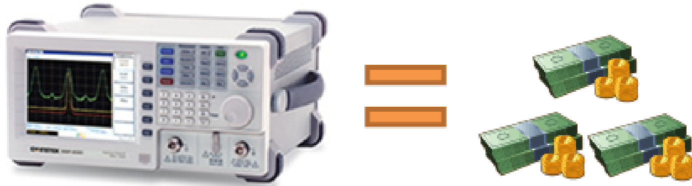
Malfunction of electronic systems

- RF circuit & system
- ADC



Phase noise test at low cost, in short time

Conventional



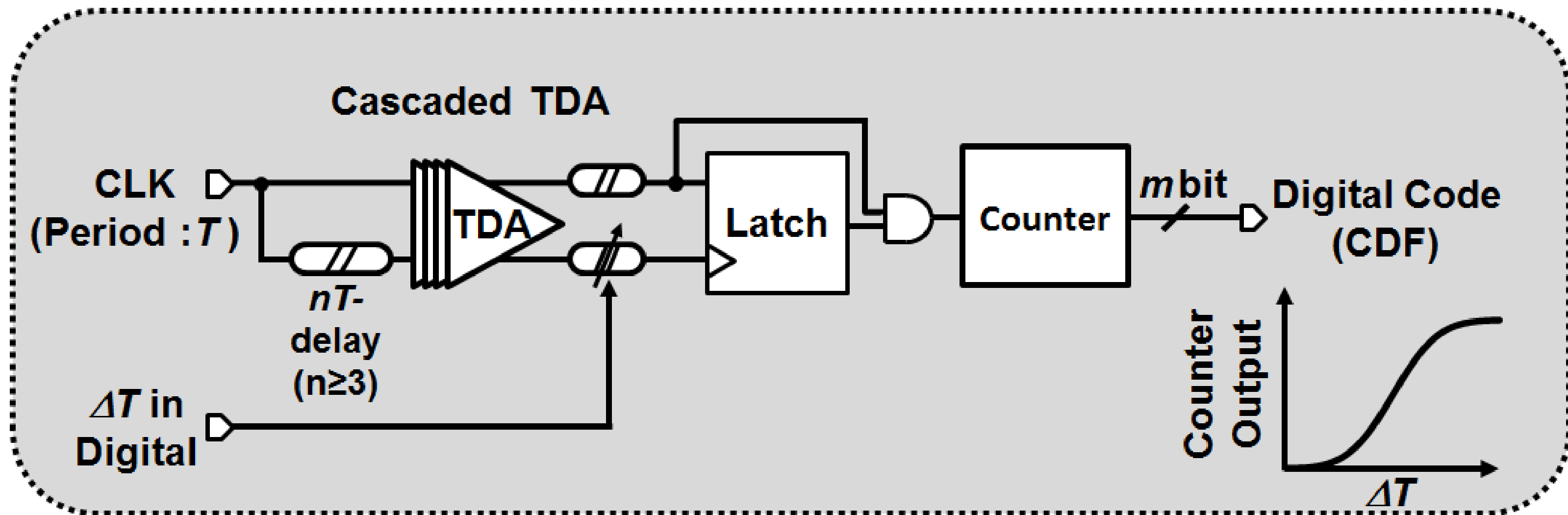
- Expensive : Spectrum analyzer
- Long : test time (~10seconds)

Proposed

ΔΣ Time-to-Digital Converter

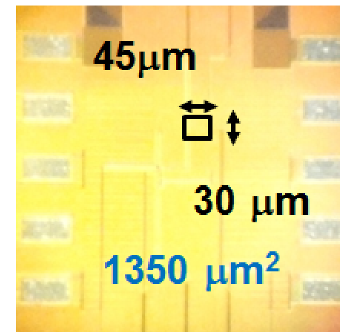
[21] Y. Osawa, D. Hirabayashi, N. Harigai , H. Kobayashi, K. Niitsu, O. Kobayashi, "Phase Noise Measurement Techniques Using Delta-Sigma TDC", IEEE International Mixed-Signals, Sensors and Systems Test Workshop, Porto Alegre, Brazil (Sept. 2014).

On-Chip Jitter Measurement Circuit



Experiments show that 1.67 ps RMS timing jitter can be measured

Process : 65 nm CMOS
Supply Voltage : 1.2 V



[22] K. Niitsu, M. Sakurai, N. Harigai, T. Yamaguchi, H. Kobayashi, "CMOS Circuits to Measure Timing Jitter Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier with Duty-Cycle Compensation," IEEE Journal of Solid-State Circuits, (Nov. 2012)

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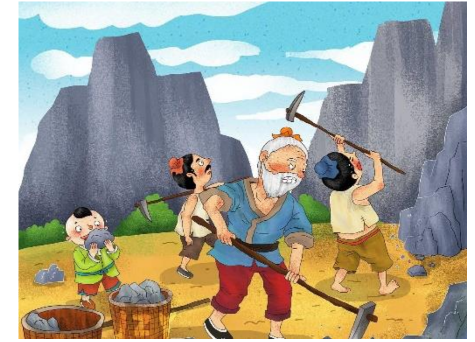
Challenges of Analog Testing



愚公移山

- Analog part testing is important for mixed-signal SOC cost reduction.
- Cost is the most important criterion.
- Its research is not easy.
- Analog BIST technique progress may be slow but it is steady.
- Solve the problems one by one. No general or systematic method
- Should be practical.
- Use engineering sense, as well as science.

Future Perspective

Aristotelēs

「学問無王道」

- Use all aspects of technologies
  - Circuit technique
  - Cooperation among BIST, BOST & ATE as well as software & network
  - Signal processing algorithm
  - Use resources in SOC such as μP core, memory, ADC/DAC

There is no science without measurement.

There is no production without test

No royal road to analog testing

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presented here