Analog/Mixed-Signal Circuit Testing Technologies in IoT Era

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Contents

● Research Background
● Analog/Mixed-Signal Circuit Testing
● Operational Amplifier Testing
● ADC Linearity Testing
● Analog Signal Generation with AWG
● Waveform Sampling Technique
● Timing Testing
● Challenges and Conclusion
Contents

- Research Background
  - Analog/Mixed-Signal Circuit Testing
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  - Timing Testing
  - Challenges and Conclusion
Hot Applications in IC Industry

- Automotive application
  ppm (parts per million) → ppb (parts per billion)
  low quality → out of business

- IoT systems
  A lot of sensors, interface analog circuits
  High reliability, Low cost system

High quality, low cost testing of LSI is important!
Test and Measurement are different

- **Production Test**: Decision of “Go” or “No Go”
  - LSI testing → manufacturing engineering.

- **Measurement / Characterization**: Accurate performance evaluation of circuit
IC Testing Technologies

● Analog/mixed-signal portions continue to be difficult part of SoC test.

→ most troublesome parts

● LSI testing technology reduces cost and improves quality simultaneously.

● Additional benefits of testing:
  Improvement of
  - Yield
  - Reliability
  - Security
  - Diagnosis
Management Strategy

- **Strategy 1:**
  Use low cost ATE and develop analog BIST/BOST to make testing cost lower.

- **Strategy 2:**
  Use high-end mixed-signal ATE as well as its associated services & know how. Fast time-to-market & no BIST can make profits much more than testing cost.

**Save or Earn**

- **ATE:** Automatic Test Equipment
- **BIST:** Built-In Self-Test, **BOST:** Built-Out Self-Test
Low Cost Testing

● Low cost ATE

Digital ATE
- No analog option such as
  Arbitrary Waveform Generator: AWG
- Input/output are mainly digital.

● Short testing time
● Multi-site testing
● Minimum or no chip area penalty for BIST
● Extensive usage of BIST

A penny saved is a penny earned.
Sine Wave Generation with Digital ATE

3rd harmonics suppression

Phase parameters

\[ \varphi_1 = \frac{2\pi r_1}{T} \]

3 rectangular add/subtract

Harmonics are cancelled

Phase shift parameter

\[ r_1 = \pm \frac{T}{6k} \]

Phase shift parameter is simple

High resolution is not needed

Digital phase shift

Digital ATE outputs

Hot Topics in Analog/Mixed-Signal Circuit Testing

- Analog fault model
- Analog fault simulation
- Analog test coverage
- Defect-based analog test

Very difficult, but automotive industry strongly demands
Analog BIST

- BIST for digital: Successful
- BIST for analog: Not very successful
  - Challenging research

- Digital test: Functionality Easy
- Analog test: Functionality & Quality Hard

Analog: parametric fault as well as fatal fault.

Prof. A. Chatterjee
Specification-based Test ↔ Alternative Test ↔ Defect-based Test

- In many cases
  - Analog BIST depends on circuit.
  - No general method like scan path in digital.
  - One BIST, for one parameter testing
Cooperation of Analog BIST and ATE

Output signals from SoC can be repetitive by controlling all inputs to SOC with ATE
→ No need for T/H circuit in front of SAR ADC
→ Wideband signal testing is possible

RF / High-Speed IO / Power Circuit Testing

- RF / HSIO / Power circuit testing is different from each other as well as analog testing technology.
- These are also challenging areas.
- Power supply circuit test example:
  - Power supply circuit stability test without breaking the loop

Robust design makes its testing difficult.

- Feedback suppresses parameter variation effects.
- **Self-calibration** and redundancy hide defects in DUT.
- **Secure** IC is difficult to test.

Redundancy SAR ADC Design Example

Reliable circuit ↔ Test difficulty

Based on Principle of Balance

Fibonacci sequence weight
(1, 2, 3, 5, 8, 13, 21, ...)


ATE for Mixed-Signal IC Testing

- Analog part of ATE is costly for development.
- Analog BIST is also beneficial for mixed-signal ATE manufacturer.
- ATE must be designed with today’s technology for tomorrow’s higher performance chip testing.

Interleaved ADC used in ATE to realize very high sampling rate with today’s ADCs.

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IoT System and OP amp

- OP amp with smaller than μV-order offset is a key component of IoT system

Its guarantee at production test
μV-order Voltage Measurement

- μV-order OP amp offset voltage testing in short time at low cost.
- DC-AC conversion
  - No influence by DC noise, drift, thermal effects
- Applicable to multi-site testing

OP amp test with Null Method

Low-cost, high-quality testing of operation amplifier

Goal

Null Method → Apply for mass production testing

Null Method

Measurement time: Long

Mass production testing: Difficult

1 second test time for 1 US dollar chip

Good capacitor value selection → Fast, stable operation
Null Method Circuit

Switches (S1,.., S6)

- Offset
- Bias Current
- DC gain
- AC gain
- DC CMRR
- DC PSRR
- AC CMRR
- AC PSRR etc.

can be measured accurately

Operational Amplifier Measurement Circuit using the Null Method

Source: Analog Dialogue Vol 45 Apr. 2011 Analog Devices

Accurate but slow!
Experiment & Simulation Verification

- Optimization of phase compensation constants
  \[ C_1 = 1\text{nF}, \quad C_2 = 0.1\mu\text{F} \]
  Null Circuit → Fast and Stable

- Null Circuit: Change of signal application point depending on the measurement item

- Switching \( C_1 \) and \( C_2 \) depending on the measurement item
  Settling time reduction → \( \approx 1/10 \)

Null method → Production testing

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ADC Testing (DC Linearity)

- DC linearity test is the most important in many cases of ADC under test.
  - Precise ramp generation is challenging.
  - High resolution ADC long testing time

- DC testing time is proportional to number of codes / sampling frequency
  - large
  - slow
ADC Testing (AC Performance)

- ADC AC performance testing
  - Sampling clock jitter
  - High frequency input signal
- We have to build low clock jitter system and apply high frequency input signal.

No alternative method so far.
ΔΣADC INL Test

Target

Product: 24bit 6.8sps Delta-Sigma ADC
Test Item: INL
Final Product:
- Air Flow Sensor
- Temperature Sensor
- Pressure Sensor
- Strain Gauge

Problems of direct method

INL: Integral Non-Linearity

All Code Testing

Analog Input

Step Ramp

DUT

Delta-Sigma Modulator
Decimation Filter

6.8sps

Digital Output

24bit 6.8sps Digital Data

INL Computation

Digital Code

Analog Input

TestTime = $2^{24} \times \frac{1}{6.8} \times n = 685[h] \times n$

$n = \frac{Samples}{Code}$

Test Time will be 685[h]. Is it acceptable?
Proposed ΔΣADC INL Test Method

[Image of a block diagram showing the flow from Analog Input to Digital Output through DUT (Device Under Test), Delta-Sigma Modulator, Decimation Filter, and SCAN Test.]

FFT based INL Prediction

Power[db] vs Frequency[Hz]

FFT Result
\( (P_1, P_2, P_3, P_4, \ldots) \)

Prediction
\( (a_0, a_1, a_2, a_3, \ldots) \)

Polynomial
\[ y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + \ldots \]

Test Time Estimation

Conventional \( TestTime = 685[h] \)

Proposed \( TestTime = 34[sec](2^{20} \text{point}) \)

DFT for SAR ADC Linearity

A high-resolution, low-sampling rate ADC requires a long test time for its linearity.

Shorten SAR ADC linearity test time.

For a 12-bit SAR ADC, its linearity test time → 1/4

DFT: Design for Testability

In mixed-signal SoCs, ...

- Accurate ADC linearity evaluation “around the middle of its input range” is required
- Single sine wave is unsuitable

This Work

- Middle range of histogram increases
ADC Histogram Test with Multi-tone

Input waveform

Proposed

\[ V_n = \frac{\cos((2n-1)\omega t)}{(2n-1)^2} \]

\[ n = 1, 2, \cdots \]

\[ V_{in} = \frac{4}{\pi} \left( V_1 + 2.6 \cdot V_2 + 1.8 \cdot V_3 + 1.4 \cdot V_6 + 1.2 \cdot V_7 \right) \]

Linearity test time reduction

Architecture for Generating Proposed Test Signal

- DSP program: Multi-tone sine wave
- Analog filter: Harmonics removal

As a result...

- Histogram for the middle of ADC input range can be high.

ADC linearity test time → 1/2
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Signal Generation for Analog Circuit Test

Problem with Conventional Method

\[ Z = b_1 Y + b_3 Y^3 \]

ADC test signal

\[ Y = a_1 D_{in} + a_3 D_{in}^3 \]

Test signal Generation

ADC

Test result

fundamental

HD3

Freq.

\[ f_{in} \quad 3f_{in} \]

AWG HD3 + ADC HD3

ADC HD3 cannot be measured accurately.

Low quality test

AWG: Arbitrary Waveform Generator
Low-Distortion Sine Wave Generation

- Low-distortion sine-wave generation using Arbitrary Waveform Generator (AWG)
- Compensation of AWG nonlinearity by digital pre-distortion
- ADC test signal

Phase switching method

\[
X_0 = 1.15A \cdot \cos(2\pi f_{in} n T_s - \pi/6) \\
X_1 = 1.15A \cdot \cos(2\pi f_{in} n T_s + \pi/6)
\]

\[
A_{out} = a_1 D_{in} + a_2 D_{in}^3
\]

Low IMD3 2-Tone Signal Generation with AWG for Communication Application ADC Testing

IMD: Intermodulation Distortion

Conventional
\[ X(n) = A\cos(2\pi f_1 n T_s) + A\cos(2\pi f_2 n T_s) \]

Proposed phase switching
\[ X_0(n) = B\cos(2\pi f_1 n T_s + \pi/6) + B\cos(2\pi f_2 n T_s - \pi/6) \]
\[ X_1(n) = B\cos(2\pi f_1 n T_s - \pi/6) + B\cos(2\pi f_2 n T_s + \pi/6) \]

Measurement Results (AWG 2-tone output)

Two-tone Curve Fitting Algorithm for Communication Application ADC Testing

Complex Multi-Bandpass ΔΣ Modulator for I-Q Signal Generation

- Generation of high quality analog I-Q signals
- Testing of communication application ICs
- Digital rich
  (Suitable to the realization with nano CMOS → Low cost)

[16] M. Murakami, H. Kobayashi, et. al.,
“I-Q Signal Generation Techniques for Communication IC Testing and ATE Systems”,
IEEE International Test Conference, Fort Worth, TX (Nov. 2016).
Contents

- Research Background
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Waveform Sampling Technology

- Waveform sampling is important for analog signal test.
- Many issues for high performance sampling circuit
  - Noise, Distortion
  - Bandwidth
  - Jitter, Aperture time
  - Sampling clock rate
  - Power

Open-loop S/H circuit:
Switch and Capacitor

![Waveform Diagram](image)
Residue Sampling Circuit

- Proactive usage of aliasing by waveform sampling
- Multiple low-rate sampling circuits
  \[ \rightarrow \text{High-frequency waveform sampling} \]

Equivalent-Time Sampling in Testing

- **Production Test**: Input signal is controllable

- **Measurement**: Input signal is unknown

Waveform reconstruction of repetitive signal

Asynchronous sampling clock with input waveform

Pre-Trigger

Sampling oscilloscope
Waveform Missing Phenomena

Repetitive Wave

Sampling Clock

Reconstructed Waveform

Toothless waveform appears
Waveform Missing Conditions

\[ f_{\text{CLK}} \gg f_{\text{sin}} \]

\[ f_{\text{CLK}} \approx \frac{1}{\alpha} f_{\text{sin}} \left( \alpha = \frac{1}{2}, \frac{1}{3}, \frac{2}{3}, \ldots, \frac{1}{6}, \ldots \right) \]

\[ f_{\text{CLK}} \approx f_{\text{sin}} \]

Sampling points move little  →  Requires long time
Waveform Sampling Condition

\[ T_{\text{sig}} \]

Repetitive Wave

\[ T_{\text{CLK}} = ? \times T_{\text{sig}} \]

Proposed Golden Ratio Sampling

\[ f_{CLK} = \varphi \times f_{sig} \]

\( \varphi \) : Golden ratio (\( = 1.6180339887\ldots \) )

Sampling points disperse uniformly through measurement
Golden Ratio is Everywhere!

The most beautiful ratio
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Time-to-Digital Converter (TDC)

TDC BOSTs for Timing Signal Testing

Single-bit ΔΣ TDC with analog FPGA

Multi-bit ΔΣ TDC with analog FPGA

Flash-type TDC with analog FPGA

Flash-type TDC with digital FPGA

BOST: Built-Out Self-Test

Phase Noise Test with $\Delta \Sigma$ TDC

Phase noise in oscillator

Malfunction of electronic systems
- RF circuit & system
- ADC

Important

Phase noise test at low cost, in short time

Conventional

- Expensive: Spectrum analyzer
- Long: test time (~10 seconds)

Proposed

Simple circuit

$\Delta \Sigma$ Time-to-Digital Converter

Low cost, high quality Phase noise test

On-Chip Jitter Measurement Circuit

Experiment show that 1.67 ps RMS timing jitter can be measured

Process: 65 nm CMOS
Supply Voltage: 1.2 V

Challenges of Analog Testing

- Analog part testing is important for mixed-signal SOC cost reduction.
- Cost is the most important criterion.
- Its research is not easy.
- Analog BIST technique progress may be slow but it is steady.
- Solve the problems one by one.
  - No general or systematic method
- Should be practical.
- Use engineering sense, as well as science.
Future Perspective

- Use all aspects of technologies
  - Circuit technique
  - Cooperation among BIST, BOST & ATE as well as software & network
  - Signal processing algorithm
  - Use resources in SOC such as μP core, memory, ADC/DAC

There is no science without measurement.

There is no production without test

No royal road to analog testing
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