ICSICT-2016 Participation Report

群馬大学大学院 理工学府
理工学専攻 電子情報・数理教育プログラム
修士 1 年 アデイカリ　ゴパール

China, Hangzhou

White Horse, Jianguo Hotel

Conference: 2016 IEEE 13th International Conference on SICT

Location: White Horse Jianguo Hotel, Hangzhou, China

Date: 2016/10/24~2016/10/29

Presentation Title:

Study of Gray Code Input DAC Using MOSFETs for Glitch Reduction

Gopal Adhikari, Richen Jiang, Haruo Kobayashi

2016 IEEE 13th International Conference on SICT, White Horse Hotel, Hangzhou, China(Oct.26-28)

❖ Schedule

10/24 (Monday): Haneda Airport departure, arrival at the hotel
10/25 (Tuesday): Tour to West Lake, Lingyin Temple
10/26 (Wednesday): Hangzhou Conference (My presentation, 16:30, Meeting Room 3B)
10/27 (Thursday): Hangzhou Conference
10/28 (Friday): Hangzhou Conference, Banquet
10/29 (Saturday): Shanghai Airport departure, Haneda Airport arrival

❖ Purpose of International Conference

To present my research in front of international delegates and other researchers
To learn the research results of different researchers and students
To learn the presentation skills of students of different countries
To learn about the Chinese culture, environment and arts
To visit different places and taste different foods

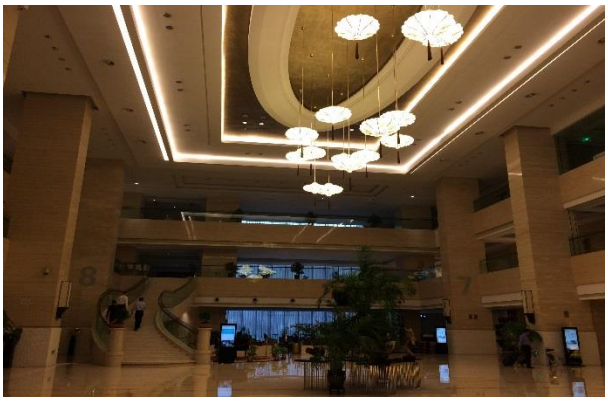
10/24 (Monday): Haneda Airport departure, arrival at the hotel

Everyone met at the Haneda International Airport at around 12 pm, ready to take off and excited for the upcoming international event. Some pictures at the Haneda Airport before departure and some during train transfers are inserted below.

At Haneda Airport

Waiting for Bullet Train Transfer at Shanghai

Mr. Wang JianLong helping all the way



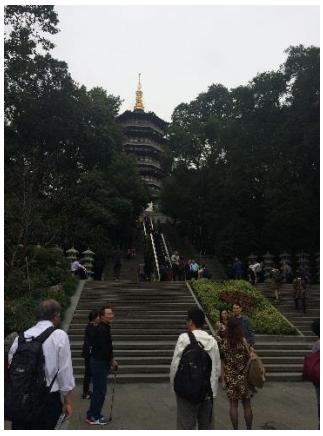
Jianguo Hotel Lobby, Beautiful !!

10/25 (Tuesday): Tour to Leifing Pagoda, West Lake, Lingyin Temple

The second day at China was exciting as well as tiresome. Visited the Leifing Pagoda, West Lake and Lingyin Temple. Language was the major problem during the visit. If Mr. Wang was not with us, we would have a lot of problem. It was very hard to communicate with the locals. Besides difficulties of language barrier, we also learnt to make Chinese Tea and taste it. Below are some pictures taken during the trip.

Exploring the Leifing Pagoda

A temple in the West Lake



The Leifing pagoda

Linyin Temple and statue of Lord Buddha

After a long trip at the locations around the west lake, everyone was tired. So we took a short rest and some great tea.

Taking a short rest after a long walk uphill

Learning to make Chinese Tea

10/26 ~28 (Wednesday~Friday): Presentation

This was the first day of presentation. I attended several presentations. I got interested in the keynote presentation by John A. Rogers titled Soft Electronics for the Human Body. After I attended several other presentations, it was time for my own. It was in meeting room 3B at 16:30. I was confident and gave a pretty nice presentation. It was a good opportunity to express my research. No questions were put forward, so I think that everyone understood my research. I attended several other presentations of our university too. During the presentations, I learnt that studying hard gives ideas for new inventions. Here are some presentations pictures of our laboratory members.

Presentation Photo Gallery

Gunma University professors and students during their presentation

10/29~10/30 Banquet and Departure

The final night of the ICSICT 2016 featured some exquisite cuisine of probably Chinese origin and some cultural session. All participants inside one big hall was a great experience. The cultural events were followed by prize distribution. Everyone of GU were happy as two of our presenters (Mr. Kojima and Mr. Tsukiji) were awarded for excellent student's paper award. Congratulations to these two heroes of the conference from GU. The moments during the Banquet were captured and depicted below

Finally, Early in the Saturday morning, we departed from the hotel and transferred trains to finally arrive at the Haneda Airport.

Finally

- Displayed my research with international delegates and researchers.
- Had a chance to listen and learn different innovations in Electronics
- Had a chance to see different cultural aspects, art and religion.
- Had a chance to taste different delicious food.
- Visited temples, pagodas and see environment.

平成 28 年 11 月 06 日

ICSICT-2016 参加報告書

群馬大学大学院　理工学府
理工学専攻　電子情報・数理領域
小林研究室　博士後期課程 2 年
王建龍

1. 参加学会名称

2016 IEEE 13th International Conference
on Solid-State and Integrated Circuit Technology (ICSICT-2016)

2. 開催場所

White Horse Lake Hotel, Hangzhou, China

3. 開催期間

2016/10/25(火)～10/28(金)　　(滞在期間は 2016/10/24(月)～10/29(土))

4. 発表論文

Analysis and Design of Operational Amplifier Stability
Based on Routh-Hurwitz Method

JianLong Wang, Gopal Adhikari, Haruo Kobayashi,
Nobukazu Tsukiji, Mayu Hirano, Keita Kurihara(Gunma University)
Akihito Nagahama, Ippei Noda, Kohji Yoshii (Ricoh Electronic Devices Co.)

5. 発表日

2016/10/16(水) Room 3B

私の発表の様子

Last week, I went to Hangzhou with Professor Kobayashi, Professor Kobori and many students from Kobayashi lab and Takai lab at Gunma University, to attend ICSICT (International Conference on Solid-State and Integrated Circuit Technology). Good time always passes quickly. So in order to remember significant and interesting time, and also to summarize important information and experience obtained from the conference, I write this report as follows:

CONFERENCE

This is my first time to take part in an international forum, and it left a deep impression to me. In my oral representation, I introduced own research to others (masters and researchers in the related field), told them my research using correct and appropriate English, and I need to let them understand what we want to say to them, and what we want to express in my representation. And then, during Q&A time, I need to understand the questions from the audience and answer them. Everyone speaks English in the forum, not only in oral representation but also in poster sessions. English is very important for our research, because we need to communicate with other researchers, and we need their suggestions; it is a precious property for our research. Sir Isaac Newton said: “If I have seen further, it is by standing on the shoulders of giants.” So, English and communication are very very important.

During my presentation, three people (one student, two professors) put forward their questions, and I could understand their questions by about 70%. After my presentation, I talked about my research with them, and continued to obtain helpful information.

In the course of the conference, other activities were provided, which were extensive opportunities for technical information exchange as well as stimulating environments for mutual communication among the participants. An exhibition of equipment and materials for solid-state and integrated-circuit technologies was held concurrently with the conference.

The conference provided a chance to meet new friends who are like-minded and have a common goal. We had an enjoyable discussion about our studies and lives.

SIGHTSEEING

Smartphone is a double-edged sword. I have always felt that we excessively rely on smartphone in our ordinary life. It has been influencing our life toward negative effects, more than positive effects. We can use it to communicate with friends in the APP, and play the internet games. It overmuch occupies our off-hours, and even our working hours. We do not have enough time to think. But…, during the time staying at Hangzhou, my telephone did not have card and the internet was not used, and the related APPs were also not used. So I cannot call a taxi and cannot consult its maps. It was unlucky. Smartphone is sometimes useful, but we should not be addicted to it.

The happiness passed away the time with friends. I think that this trip will be becoming my sweet memories when I recollect it. Hangzhou is a beautiful city which has historical background, and I always wanted to go. I am very happy that I can explore the charming city with my mentor and friends together.

As another harvest, my speaking Japanese level has been enhanced by talking with my Japanese friends.

Thanks to Professor Kobayashi and Professor Kobori. Thanks to Mr. Ishikawa. Thanks to all friends. Thanks to God. Thanks to everyone.

Let's look forward to next time.

Congratulations on Mr. Tsukiji and Mr. Kojima's Excellent Student Paper Awards

Participation Report

Gunma University
Graduate School of Science and Technology
Kobayashi Laboratory
The Second Year of Doctoral Program
Yifei Sun

Conference name: 2018 IEEE 14th International Conference on Solid-State and Integrated Circuit Technology (ICSICT-2018)

Host location: Huangdao Sheraton Hotel, Qingdao, China

Holding date: October 31-November 3, 2018

Schedule:

October 29: Take plane to Qingdao, China
October 30: Haier Group study tour
October 31: ISICT2018 Tutorial
November 1: ISICT2018 Opening & Keynote & Session
November 2: ISICT2018 Session
November 3: ISICT2018 Session & Banquet
November 4: Return to Japan

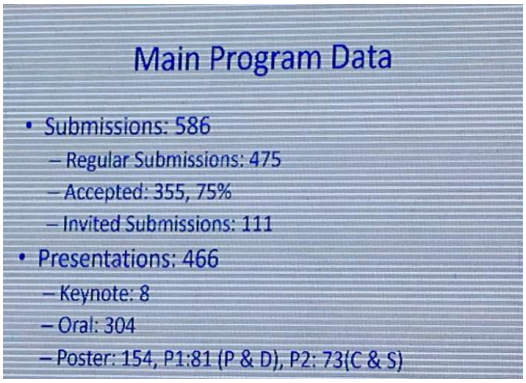
Home page: http://www.icsict.com/

Publish paper: Full Automatic Notch Generation in Noise Spectrum of Pulse Coding Controlled Switching Converter
Authors: Yi-Fei Sun, Yasunori Kobori, Haruo Kobayashi

1. Conference overview

The ICSICT-2018 conference is the 14th in the series aiming to provide an international forum for the presentation and discussion of recent advances in solid-state and integrated circuit technology. The conference sponsored by IEEE and co-sponsored by Peking University and Fudan University; they are among the top universities in China. All aspects of solid-state devices, circuits, processing technologies, materials and other related research are within the scope of the conference. It was held for the first time in 1986 and has been held once every two years. This is the fourteenth time to holding the conference. The three days of contributed and invited presentations on the latest developments in diverse fields given in oral and poster sessions, panel discussions on leading edge technology issues, and other activities were provided extensive opportunities for technical information exchange as well as a stimulating environment for mutual communication among participants.

In this conference, paper acceptance rate is about 75%; number of regular paper submissions are 475 and 355 papers were accepted. Moreover 111 papers were invited submissions. Invited talks by inviting prominent teachers and scholars from abroad. There are including two papers from Prof. Kobayashi and a paper from Prof. Yin.



ICSICT-2018 main program data


Host location: Huangdao Sheraton Hotel

2. Program

18 people from Gunma University participated in this conference. Including 5 professors and 13 students in Kobayashi Lab. There are 13 oral presentations. Invited paper takes 30 minutes: 25 minutes for talk and 5 minutes for question and answer. Regular paper takes15 minutes: 12 minutes for talk and 3 minutes for question and answer. Invited paper from Prof. Kobayashi and Prof. Yin on the second day. 9 papers on the second day and a paper on the third day from the Gunma University presentation of regular articles.

November 1: Registration Opening & Keynote session Oral presentation Poster session

8:30 Opening Ceremony
9:00 Keynote Speech 1: The Next Era of Hyper Scaling in Electronics
Suman Datta
University of Notre Dame, USA
9:45 Keynote Speech 2: Energy-Efficient Electronic Technologies for Internet of Things
Adrian M. Ionescu
Nanolab, Ecole Polytechnique Federale de Lausanne, Switzerland
10:45 Keynote Speech 3: All-solid-state battery - History, Current Status and Future Perspectives
Ryojikanno
Tokyo Institute of Technology, Japan
11:30 Keynote Speech 4: Emerging Terahertz Technologies for Security, Quality Control, Vision and Medical Applications
Thomas Skotnicki & Wojciech Knap
13:30-17:30 Oral presentation
17:45-18:45 Poster session


Opening Ceremony

Invited presentation by Prof. Kobayashi

November 2: Keynote session Oral presentation Poster session Panel discussion

8:30 Keynote speech 5: Silicon Technology Solutions for 5G millimeter-wave Applications
Alvin Joseph
Essex Junction, USA
9:15 Keynote speech 6: The Path to Saving Moore's Law
Sanjay Natarajan
Applied Materials, USA
10:15-17:30 Oral presentation
17:45-18:45 Poster Session
20:00 Panel discussion: Consolidation of the semiconductor industry: is it real? Is it a good thing?

Most people from our laboratory have presentation on this day. The title of my presentation was [Full Automatic Notch Generation in Noise Spectrum of Pulse Coding Controlled Switching Converter]. Publishing time was 12 minute, and question & answer time was 3 minute. During the presentation I was a little nervous. The most feared session should be the question session. This time I found that the understanding of the question was not in place. In the future, I think I need more exercise and improve the level of English listening and speaking in order to answer the question and in research region.

In poster session, there were many posters in solid state devices and circuits area. They mostly came from Chinese Universities. I also learned some other fields knowledge by talking with them.

State of my presentation

Excellent student paper certificate

November 3: Keynote Session Oral presentation Closing banquet

8:30 Keynote speech 7: Blurring the Lines Between Mind, Body and Prosthetics
Ralph Etienne-Cummings
Johns Hopkins University, USA
9:15 Keynote speech 8: System-on Chip in the Age of AI
Yong Lian
York University, UK
10:15-15:15 Oral presetation
19:00 Closing banquet

The excellent student paper award was announced on the closing banquet. Fortunately, my presentation paper was chosen as excellent student paper. I am very happy and want to thank Prof. Kobayashi and Prof. Kobori very much. I also want to thank those who helped me in my studies and life.

Prof. Kobayashi and myself

Prof. Kobori and myself


Banquet


Banquet

3. Study Tour in Haier Group at October 30 and Qingdao City

Haier Group is a home appliance maker based in Qingdao, Shandong Province, China; it is a global enterprise group. Main products are white goods such as refrigerators and washing machines, televisions, air conditioners, laptop personal computers and so on. They are producing and selling in more than 165 countries worldwide.

Study tour in Haier Group


Study tour in Qingdao City

4. Experience

In this conference and study tour I gained a lot of experience. The participation of this

conference is helpful to my future research and study. According to communication with students from top universities in China and listen to research presentation by top scholars from all over the world, I not only had a better understanding of my own research knowledge, but also known other scope knowledge. I also realized that English is very important, and I will improve English conversation ability and spoken English in the future. As an international student, it is a pleasure to go back to my home country to participate conference.

Qingdao is a very beautiful tourist port. In Qingdao I have eaten seafood that I have never eaten before and experienced different humanistic customs. The participation of this international conference was an unforgettable experience in life.

5. Acknowledgments

First of all, thank Prof. Kobayashi for giving me this rare opportunity. Thank you for your guidance and help. Thanks for Prof. Kobori who gives me a lot of guidance in my research and guidance in my slide and presentation. Also thanks for Prof. Matsuda, Prof. Yin and Prof. Kuwana who gave me guidance for accompanying. Thanks for my senior Jianlong Wang for taking care of us in Qingdao. Thanks for Mr. Ishikawa who gave us support for traveling. At last, thanks for students from Kobayashi laboratory, it was a very valuable experience for me.

Group photo

ICSICT-2018 Participation Report

EMI Reduction and Output Ripple Improvement of Switching DC-DC Converters with Linear Swept Frequency Modulation

Minh Tri Tran*, Natsuko Miki, Yifei Sun, Yasunori Kobori and Haruo Kobayashi

Gunma University, Japan
***Email: t182d002@gunma-u.ac.jp**

ACKNOWLEDGEMENT

I would like to thank Prof. H. Kobayashi, Dr. Kobori and Kobayashi Lab members who gave me a good chance to travel many beautiful places at Qingdao in China.


服 务 台
INFORMATION
안내대
サービス合
机 场 国 际 售 票 处
INTERNATIONAL TICKET OFFICE
出国随身WI-FI租赁


锦江之星
JINJIANG
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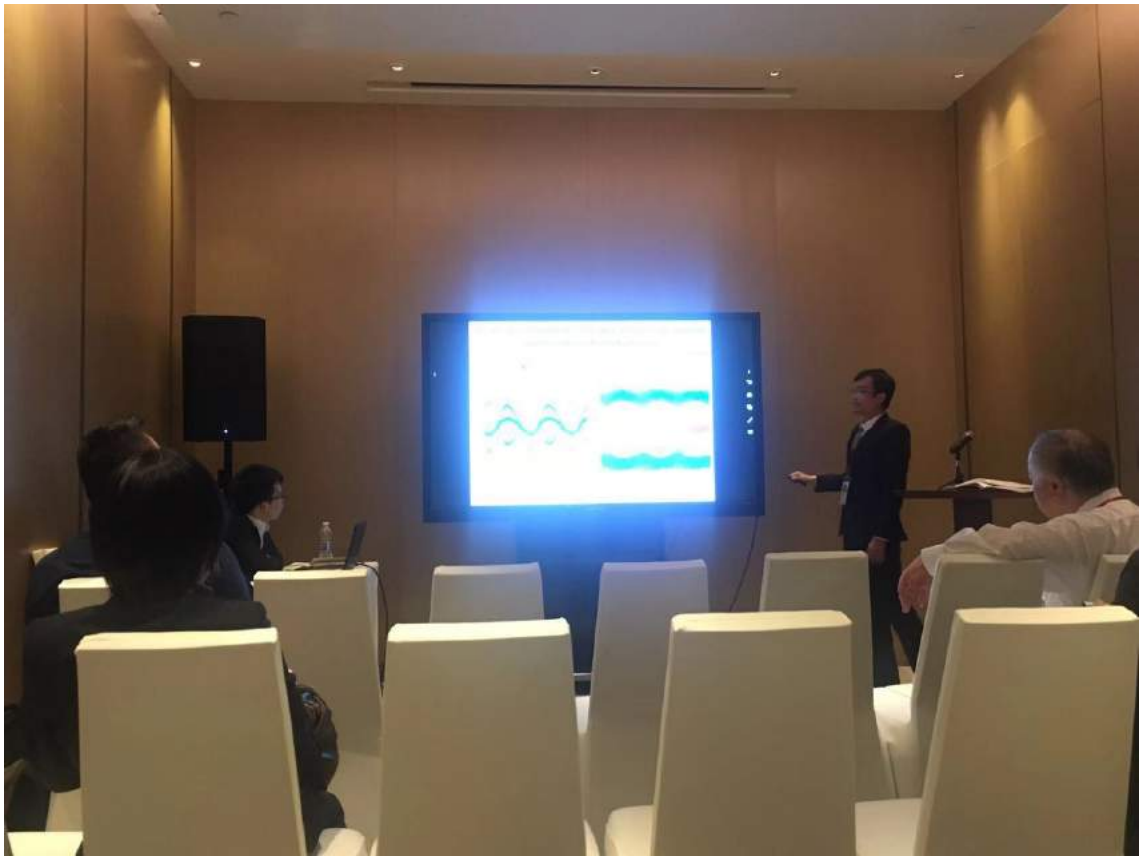
I would like to thank my lovely Prof. Kobayashi!



It was the first time I attended a large conference, therefore I was very nervous.

I would like to thank my lovely Dr. Kobori!

I would like to thank my lovely Dr. Mastuda!

I could see many scholars from all over the world.

I would like to thank Prof. Thomas Skotnicki!

https://www.semiwiki.com/forum/content/4830-thomas-skotnicki-fd-soi-26-years-making.html

In one particular instance, Thomas had a long fight over a key paper at IEEE Transactions on Electron Devices, where the editors didn't want to publish. Then a serendipitous change of editor opened the door to publication; the paper was given the Rappaport Award, as "best publication of the year" by the IEEE Electron Devices Society. As Mahatma Gandhi said: First they ignore you, then they laugh at you, then they fight you, then you win.

With these successes building momentum, the semiconductor community finally started to believe in the idea. One important believer was Carlos Mazure from SOITEC where they make wafer blanks. SOITEC was excited by the potential of these thin-box, short-channel devices, but at the time they could only make a box 145nm thick, not the 10-20nm that was required. Under Carlos' leadership, SOITEC was instrumental in launching the R&D program that successfully delivered thin box SOI wafers.

At this point LETI got involved. Although most of their work was on thick-box devices, they decided to collaborate with Thomas to actually fabricate his ideas into real silicon. LETI helped with both silicon-on-nothing and then with thin-box FD-SOI. Up until then it had all been equations. The whole idea gained speed once the project was transferred from the whiteboard to silicon.

Then, in 2011, Intel announced FinFET. Everyone already knew about FinFET and it was known to be really difficult technology. The complexity of FinFETs and the concerns about efficiently producing it led to raucous debate within the industry and within companies. Thomas sold the deal at ST when he showed that by turning a FinFET on its side you pretty much had silicon-on-nothing, FD-SOI with a thin box. It was the biggest day of Thomas' professional life when ST's top management, including CEO Carlo Bozotti, COO Jean-Marc Chery, and EVP of Front-End Manufacturing Joël Hartmann made the decision to take its Ultra-Thin Body and Box FD-SOI to manufacture. Thomas recounted that from initial conception and equations to industrial fabrication it took 26 years.

Industrialization of the manufacturing process went fast since the technology worked even better than the equations and FD-SOI is a much simpler technology than FinFET—it leverages the learnings of planar (bulk) silicon with fewer masks and processing steps, albeit with a slightly more expensive wafer.

Still, selling FD-SOI beyond ST took a bit more time, as initially ST was alone and customers require partners, second sources, alliances and not just a single manufacturer. Today, however, the technology is being deployed worldwide not just at ST but also at Samsung and GlobalFoundries.

As a marketing guy, I can't but help noticing a missed opportunity. "Silicon on nothing" is a much better name than FD-SOI.

I would like to thank Prof. Adrian Ionescu!

https://people.epfl.ch/cgi-bin/people?id=122431&lang=en&cvlang=en

EPFL › People@EPFL › Mihai Adrian Ionescu

français / English

MIHAI ADRIAN IONESCU

Contact | Biography & current work | Main publications | Teaching & PhD

Share:

Biography and current work

Mission

The Nanoelectronic Devices group (NANOLAB) is working on various subjects in the field of silicon micro/nano-electronics with special emphasis on the technology, design and modelling of nanoscale solid-state devices (including Silicon-On-Insulator devices, few-electron devices, hybrid SET/CMOS, single electron memory, nanowires and nanotubes), Radio Frequency MEMS devices for in- and above-IC and integrated optoelectronic devices.
The group is interested in exploring new materials, novel fabrication techniques, and novel device concepts for future nanoelectronic systems.

Biography

Adrian M. Ionescu is Full Professor at the Swiss Federal Institute of Technology, Lausanne, Switzerland. He received the B.S./M.S. and Ph.D. degrees from the Polytechnic Institute of Bucharest, Romania and the National Polytechnic Institute of Grenoble, France, in 1989 and 1997, respectively. He has held staff and/or visiting positions at LETI-CEA, Grenoble, France and INP Grenoble, France and Stanford University, USA, in 1998 and 1999.
Dr. Ionescu has published more than 400 articles in international journals and conferences. He received many Best Paper Awards in international conferences, the Annual Award of the Technical Section of the Romanian Academy of Sciences in 1994 and the Blondel Medal in 2009 for remarkable contributions to the progress in engineering sciences in the domain of electronics. He is the 2013 recipient of the IBM Faculty Award in Engineering. He served the IEDM and VLSI conference technical committees and was the Technical Program Committee (Co)Chair of ESSDERC in 2006 and 2013.
He is director of the Laboratory of Micro/Nanoelectronic Devices (NANOLAB). He is appointed as national representative of Switzerland for the European Nanoelectronics Initiative Advisory Council (ENIAC) and member of the Scientific Committee of CATRENE. Dr. Ionescu is the European Chapter Chair of the ITRS Emerging Research Devices Working Group.

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Nationality : Romanian

FIELDS OF EXPERTISE

Nanoelectronic devices
Silicon nanotechnology
Silicon On Insulator
Radio Frequency MEMS and NEMS
Small Swing Switches
Emerging Memories
Modeling and Simulation of Solid-State Electronic

I would like to thank Prof. Yeo Kiat Seng!

https://epd.sutd.edu.sg/people/faculty/yeo-kiat-seng

Yeo Kiat Seng

Associate Provost, Research & International Relations

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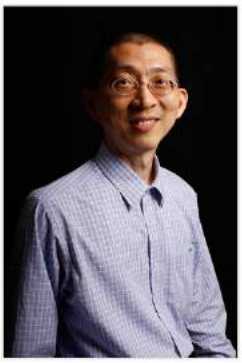
Research Areas:
Electrical Engineering

Pillar / Cluster: Engineering Product Development



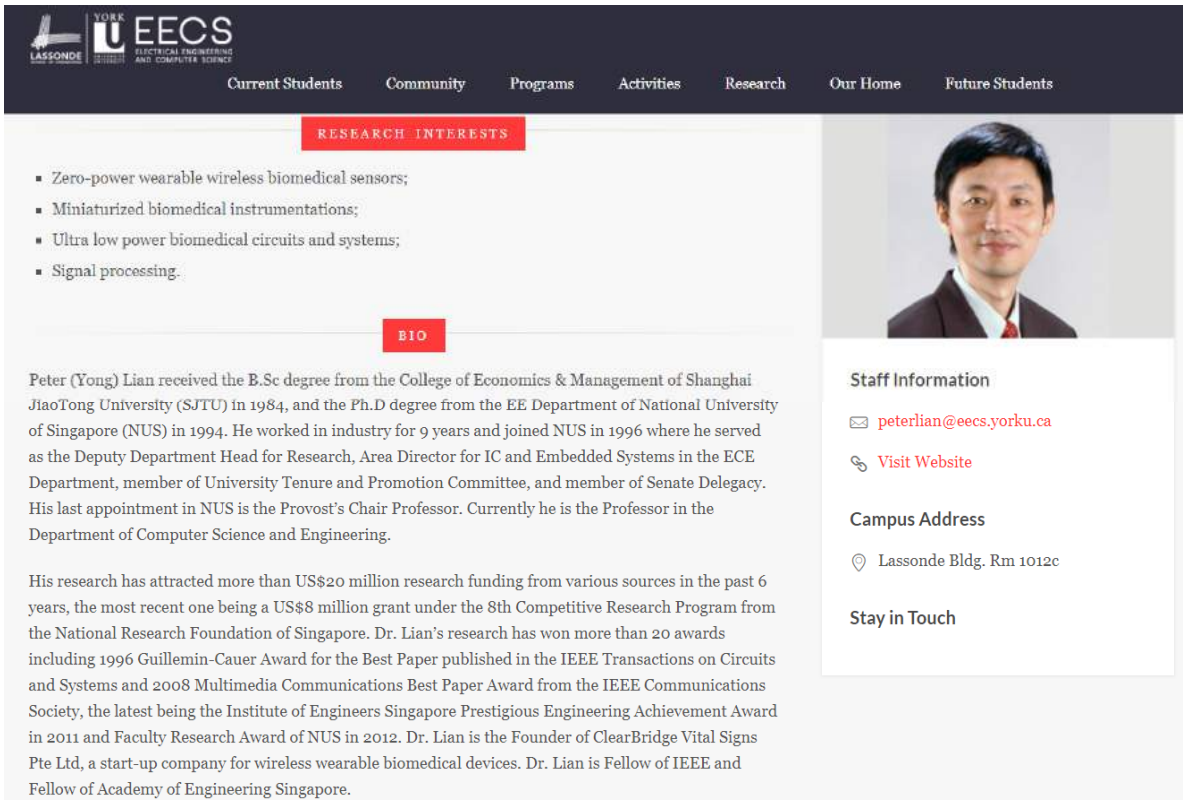
Biography

Associate Provost for International Relations and Graduate Studies, Professor Yeo Kiat-Seng joined Singapore University of Technology and Design (SUTD) on 2nd July 2014. He has over 25 years of experience in industry, academia and consultancy. Before his appointment at SUTD, he was Full Professor at Nanyang Technological University (NTU), Singapore, and spent 13 years in management positions as Associate Chair (Research), Head of Circuits and Systems and Sub-Dean (Student Affairs) in the School of Electrical and Electronic Engineering (EEE). As Associate Chair (Research), he developed EEE mega research centres into a top-notch hub to advance cutting-edge research innovations and unparalleled inventions. Prof. Yeo was also a Fellow of the Renaissance Engineering Programme (REP) and served as Senator and Advisory Board Member at NTU. Besides, he was the Founding Director of VIRTUS, a $50 million IC Design Centre of Excellence jointly set up by NTU and Singapore Economic Development Board. Since 1996, he has been providing consultancy services to statutory boards, local SMEs and multinational corporations in the areas of electronics and IC design.

Currently, Prof. Yeo is a Visiting Professor in the School of EEE at NTU, a Member of Board of Advisors of the Singapore Semiconductor Industry Association, a Council Member of the Assembly & Test WSQ Framework Industry Skills and Training of the Singapore Workforce Development Agency, a Member of the Engineering Science (ES) Advisory Committee of Ngee Ann Polytechnic and a Member of Hwa Chong Institutional IP Advisory Board.

I would like to thank Prof. Yong Lian!

http://eecs.lassonde.yorku.ca/faculty/peter-lian/



LASSONDE YORK U EECS ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

Current Students | Community | Programs | Activities | Research | Our Home | Future Students

RESEARCH INTERESTS

- Zero-power wearable wireless biomedical sensors;
- Miniaturized biomedical instrumentations;
- Ultra low power biomedical circuits and systems;
- Signal processing.

BIO

Peter (Yong) Lian received the B.Sc degree from the College of Economics & Management of Shanghai JiaoTong University (SJTU) in 1984, and the Ph.D degree from the EE Department of National University of Singapore (NUS) in 1994. He worked in industry for 9 years and joined NUS in 1996 where he served as the Deputy Department Head for Research, Area Director for IC and Embedded Systems in the ECE Department, member of University Tenure and Promotion Committee, and member of Senate Delegacy. His last appointment in NUS is the Provost's Chair Professor. Currently he is the Professor in the Department of Computer Science and Engineering.

His research has attracted more than US$20 million research funding from various sources in the past 6 years, the most recent one being a US$8 million grant under the 8th Competitive Research Program from the National Research Foundation of Singapore. Dr. Lian's research has won more than 20 awards including 1996 Guillemin-Cauer Award for the Best Paper published in the IEEE Transactions on Circuits and Systems and 2008 Multimedia Communications Best Paper Award from the IEEE Communications Society, the latest being the Institute of Engineers Singapore Prestigious Engineering Achievement Award in 2011 and Faculty Research Award of NUS in 2012. Dr. Lian is the Founder of ClearBridge Vital Signs Pte Ltd, a start-up company for wireless wearable biomedical devices. Dr. Lian is Fellow of IEEE and Fellow of Academy of Engineering Singapore.

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Visit Website

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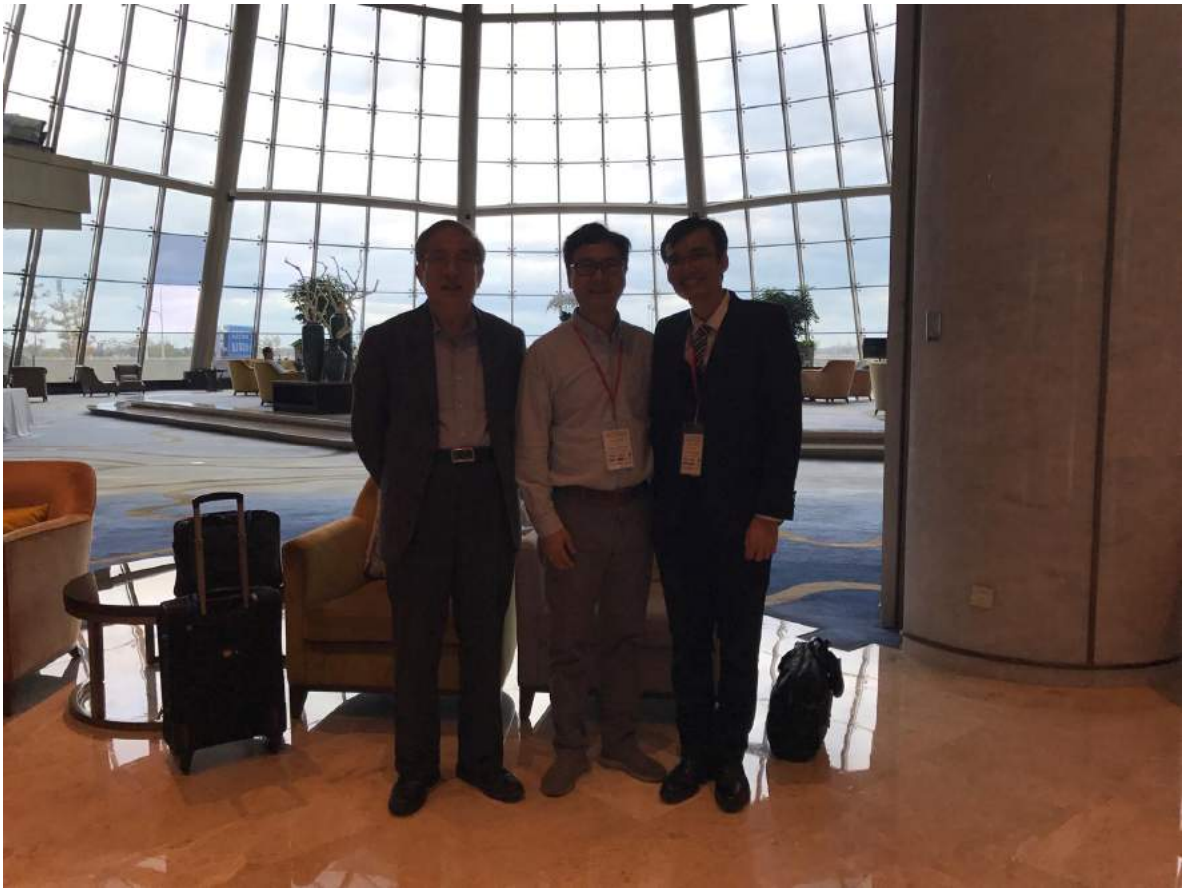
Stay in Touch



I would like to thank Prof. Cheng Yuhua!

http://eecs.pku.edu.cn/EN/People/Faculty/Detail/?ID=5954

Cheng, Yuhua

Professor

Research Interests: Advanced analog/mixed-signal/RF integrated circuits for system integration applications

Office Phone: 86-21-6109 1006-816

Email: chengyh@pku.edu.cn

Cheng, Yuhua received the BSEE, MSEE, and Ph.D. EE degrees in Shandong Polytechnic University (Now Shandong University), Tianjin University, and Tsinghua University, China in 1982, 1985 and 1989, respectively. In 1990, he joined in the Institute of Microelectronics (IME), Peking University, China. From 1992 to 1996, he was an associate professor in IME. He is now with Peking University, as a full professor.

Dr. Cheng has served on many Technical Program Committees and chaired numerous Sub-committees at international conferences, including the IEEE Custom Integrated Circuits Conference (CICC) (from 2002 to 2005) and Radio Frequency Integrated Circuits Symposium (since 2002). He organized and participated in numerous workshops and panels related to RFCMOS technology and SoC design. He has authored and co-authored over 160 research papers, two book chapters, two books "MOSFET Modeling & BSIM3 User's Guide" by Kluwer Academic Publishers (1999), and "Device modeling for analog/RF circuit design" by John Wiley and Sons (2002). He was a Guest Editor for IEEE Journal of Solid-State Circuits. He is an IEEE Fellow and a member of both Electronic Device Society (EDS) and Solid-state Circuit Society (SSCS). His research interests include smart power discrete semiconductor devices and advanced analog/mixed-signal/RF integrated circuits for system integration applications.

Dr.Cheng was the principal developer to BSIM3v3 (Yuhua Cheng, et al., BSIM3v3 User's Manual, UC Berkeley, UCB/ERL M97/2, 1997). Due to Dr. Cheng's efforts, the discontinuity problems, considered as a major shortcoming in BSIM models, were resolved in BSIM3v3, while many new physical effects were implemented. BSIM3v3 has been used worldwide by foundries and design companies for IC simulation. It was selected as the first MOSFET model for compact model standardization effort for IC simulation by Electronics Industry Association/Compact Model Council and given an R&D 100 Award in 1996.

Since 2006, Dr. Cheng has been conducting research on ESD for more than 10 years, which has made significant achievements, which resulted in more than 30 research papers. He shared with the IC industry his research results in international conferences and journals including IEEE Journal of Solid-state Circuits, IEEE Trans. On Electron Devices, and IEEE Electron Devices Letters.

I would like to respect, thank and acknowledge the ICSICT 2018 which gave me a chance to represent my research paper.

I would like to thank my new friend!

I would like to thank my new friend!

I would like to thank my new friend!

I would like to thank my new friend!

I would like to thank my new friends!

https://www.hisim.hiroshima-u.ac.jp/

HiSIM 研究センター

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HiSIM: Hiroshima-University STARC IGFET Model

The 2nd International Symposium on Device Circuit and Systems (ISDCS 2019)
を2019年3月6日～8日にかけ、広島大学 東広島キャンパスにて開催予定。
(ISDCSのウェブサイトへのリンクはこちらです。)

コンパクトトランジスタモデルHiSIMの概要

集積回路は膨大な数のトランジスタを組み合わせて様々な機能を作り出している。
この際に、トランジスタ特性を記述したトランジスタモデルを用いて、与えられた電圧に対するトランジスタ応答を計算して集積回路特性を予測しながら設計を進めていく。トランジスタ特性としては電圧に対する電流やトランジスタに蓄えられる電荷応答がある (図1参照。)

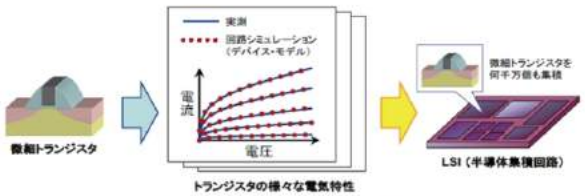

図1：トランジスタが回路特性を決定する原理。


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谢 谢

Don’t be sad my friend!

I hope that you will be able to come back Qingdao on someday in future!

Simple Reference Current Source Insensitive to Power Supply Voltage Variation - Improved Minoru Nagata Current Source

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Abstract - This paper describes design improvement of the constant current source (peaking current mirror), originally invented by Nagata Minoru in 1966. Our improved current mirror circuits with MOS and Bipolar are insensitive to wide range of power supply voltage variation; they are realized by addition of multiple current peaks. We show their circuit topologies, operations and simulation results. The proposed reference current circuits are simple, small yet well-insensitive to power supply voltage variations, and hence they can be widely used in analog ICs.

Keywords: Reference current source, Nagata current mirror, Peaking current mirror, Supply voltage variation

I. Introduction

In many analog IC applications, one reference current/voltage source is required; the other current sources can be generated from the reference current/voltage. The reference current/voltage source should be stable against the change of the environment in analog IC.

Representative example of the reference voltage source is a bandgap reference circuit. This circuit provides a stable voltage against temperature and supply voltage variations, but its design is complicated and it occupies relatively large chip area.

Another example is a peaking current mirror invented by Minoru Nagata in 1966 [1,2]; hereafter we call this circuit as Nagata current mirror. Its output current has a peak with respect to the input current change. When it is biased at the vicinity of the peak, its output current change with respect to the input current change is slight. When the input current is realized by a resistor whose one terminal is connected to a power supply voltage (V_{DD}), a constant output current is obtained over the supply voltage fluctuation. Even though this circuit does not take care of temperature variation, it is widely used such as in DC-DC converter ICs due to its simplicity.

In this paper, we propose an improved Nagata current mirror which provides constant current over much wider range of the power supply voltage fluctuation than the original Nagata current mirror, using multiple current mirror circuits with different current peaks. Its MOS and Bipolar circuit configuration, analysis and simulation results are described.

II. Nagata Current Mirror Circuit

Fig. 1 shows the original Minoru Nagata current mirror circuit, and its output current (I_{OUT}) with respect to the input current (I_{IN}) has a peak as shown in Fig. 2. When the input current (I_{IN}) increases from a small value, the output current (I_{OUT}) follows and increases. For further input current increase, a voltage drop (RI_{IN}) between nodes *a* and *b* is caused: then the gate-source voltage of M_2 becomes smaller than that of M_1, and the drain current of M_2 decreases.

We see from Fig. 2 that the output current has a peak, and the input current source can be realized with a resistor whose one terminal is connected to the power supply. Then at the vicinity of the peak, the output current is almost constant with respect to the power supply change, but the peak vicinity is narrow. In the following sections, we will describe its improved circuit whose output current is constant over the wide range of the input current.

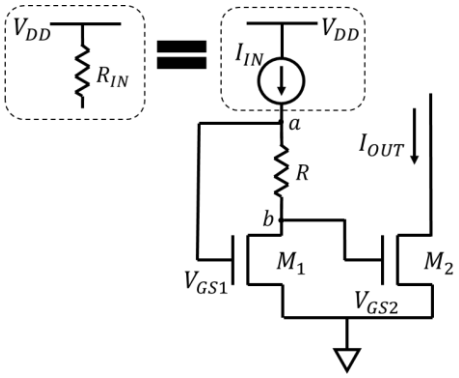

Fig. 1. Nagata current mirror

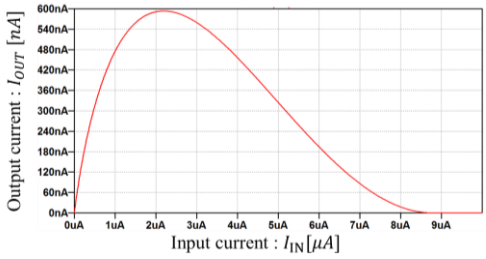

Fig. 2. I_{IN} - I_{OUT} characteristics of Nagata current mirror (SPICE simulation result)

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III. Proposed MOS Reference Current Source

3.1 Proposed Circuit Configuration and Operation

Fig. 3 shows the proposed reference current source, which is an improved MOS Nagata current mirror. It uses multiples of Nagata current mirror circuits with different peaks, and its output current is their total current. As a result, the output current is constant over the wide range of the power supply voltage (or input current) as shown in Fig. 4.

Now we will explain the operation principle of the circuit in Fig. 3. It follows from Kirchhoff Voltage Law (KVL) that

$$V_{GSn} = V_{GS1} - R^{total}{}_{n-1} I_{IN} \qquad (1)$$

$$(n = 2,3,4,5) \quad (R^{total}{}_{n-1} = R_1 + R_2 + \ldots + R_{n-1}).$$

Currents (I_{IN} , I_{OUTn}) flowing into M1 – M5 can be expressed by eqs. (2), (3), using the MOSFET current formula in the saturation region.

$$I_{IN} = K_1 (V_{GS1} - V_{TH})^2 (1 + \lambda V_{DS1}) \qquad (2)$$

$$I_{OUTn} = K_n (V_{GSn} - V_{TH})^2 (1 + \lambda V_{DSn}) \qquad (3)$$

$$\text{where} \quad K_n = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L} \right)_n$$

V_{GS1} and V_{GSn} can be obtained from eqs. (2), (3).

$$V_{GS1} = \sqrt{\frac{I_{IN}}{K_1 (1 + \lambda V_{DS1})}} + V_{TH} \qquad (4)$$

$$V_{GSn} = \sqrt{\frac{I_{OUTn}}{K_n (1 + \lambda V_{DSn})}} + V_{TH} \qquad (5)$$

Eqs. (1) and (2) are substituted into (3), and the output current I_{OUTn} is obtained as:

$$I_{OUTn} = K_n (V_{GS1} - R^{total}{}_{n-1} I_{IN} - V_{TH})^2 (1 + \lambda V_{DSn})$$

$$= K_n I_{IN} R^{total}{}_{n-1}{}^2 \times$$

$$\left(\sqrt{I_{IN}} - \frac{1}{R^{total}{}_{n-1} \sqrt{K_1 (1 + \lambda V_{DS1})}} \right)^2 (1 + \lambda V_{DSn}) \qquad (6)$$

We will find the extreme value of input-output characteristics of the circuit in Fig. 3. Differentiate I_{outn} in eq. (6) with respect to I_{IN} and then we have:

$$\frac{dI_{OUTn}}{dI_{IN}} = K_n R^{total}{}_{n-1}{}^2 (1 + \lambda V_{DSn}) \left(\sqrt{I_{IN}} - \frac{1}{R^{total}{}_{n-1} \sqrt{K_1 (1 + \lambda V_{DS1})}} \right)$$

$$\times \left(2\sqrt{I_{IN}} - \frac{1}{R^{total}{}_{n-1} \sqrt{K_1 (1 + \lambda V_{DS1})}} \right) \qquad (7)$$

For $\frac{dI_{OUTn}}{dI_{IN}} = 0$, we have the following:

$$I_{IN} = \frac{1}{4 R^{total}{}_{n-1}{}^2 K_1 (1 + \lambda V_{DS1})} \qquad (8)$$

Eq. (8) is substituted into (6), and the peak output current is given by

$$I_{OUTn} = \frac{(W/L)_n}{4(W/L)_1} \bullet \frac{1}{4 R^{total}{}_{n-1}{}^2 K_1} \bullet \frac{(1 + \lambda V_{DSn})}{(1 + \lambda V_{DS1})} \qquad (9)$$

We see from eqs. (8), (9) that the input current value at which the output current has the peak, and the amount of the peak output current can be changed by changing resistor values and MOSFET sizes. Fig. 4 shows SPICE simulated characteristics of the proposed reference current source circuit in Fig. 3, where TSMC 0.18μm parameters are used. We see that the total output current (I_{OUT_total}) is almost constant over wide range of the input current I_{IN}.

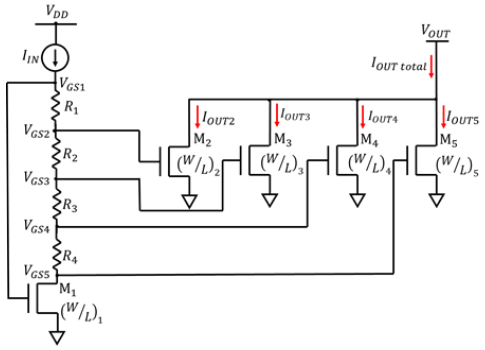

Fig. 3. Proposed MOS reference current source.

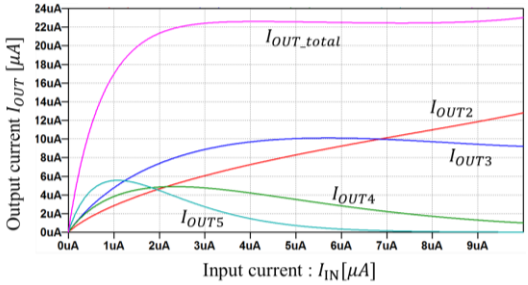

Fig. 4. I_{IN} - I_{OUTn} characteristics of the proposed MOS refence current source.

Note that our simulation circuit has used 4 peaks, however, the number of peaks is not restricted to 4.

3.2 Influence of Resistor Values and MOS Characteristics Variation

In order to investigate the effect of the resistor value variation to the output current, we have performed SICE simulation: all resistance values are uniformly shifted by ±10%. In addition, MOS fast and slow models are used. We see from Figs. 5, 6 that when MOS models and resistor values are varied, the total output current keeps constant, but its magnitude is varied.

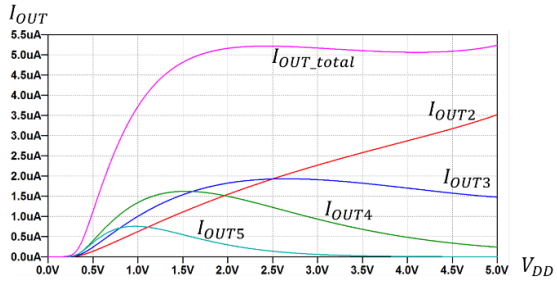

Fig. 5. Simulation results of the proposed circuit in Fig. 3 in case that all resistor values decrease by 10%.

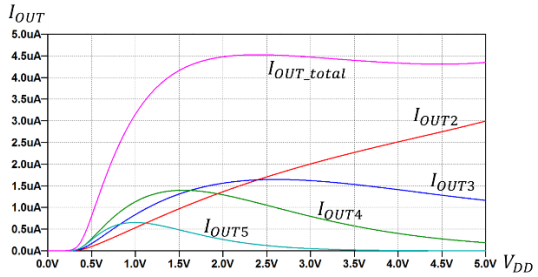

Fig. 6. Simulation results with SLOW NMOS model, of the proposed circuit in Fig. 4.

IV. Proposed Bipolar Reference Current Source

Fig. 7 shows the proposed Bipolar reference current source using multiple Nagata current sources with different peaks. Fig. 8 shows its SPICE simulation result and we see that its output current is constant over the wide range of the supply voltage variation.

Now we will analyze the circuit in Fig. 7. Using KVL, we have the following:

$$V_{BEn} = V_{BE1} - R^{total}{}_{n-1} I_{IN} \qquad (10)$$

$(n = 2,3,4,5)$ $(R^{total}{}_{n-1} = R_1 + R_2 + \ldots R_{n-1})$.

Note that

$$V_{BE1} = V_T \ln\left(\frac{I_{IN}}{I_{s1}}\right) \qquad (11)$$

$$V_{BEn} = V_T \ln\left(\frac{I_{OUTn}}{I_{sn}}\right) \qquad (12)$$

Here a thermal voltage $V_T = kT/q$.

It follows from eqs. (10), (11) and (12) that

$$V_T \ln\left(\frac{I_{IN}}{I_{s1}}\right) - V_T \ln\left(\frac{I_{OUTn}}{I_{sn}}\right) = R^{total}{}_{n-1} I_{IN} \qquad (13)$$

Suppose that all saturation currents (I*sk*, k=1, 2, .. 5) are the same. Then the output current (I_{OUTn}) of each Bipolar transistor is given by

$$I_{OUTn} = I_{IN} \exp\left(-\frac{I_{IN} R^{total}{}_{n-1}}{V_T}\right) \qquad (14)$$

Now differentiate I_{OUTn} with respect to I_{IN}:

$$\frac{dI_{OUTn}}{dI_{IN}} = \exp\left(-\frac{I_{IN} R^{total}{}_{n-1}}{V_T}\right)\left(1 - \frac{R^{total}{}_{n-1}}{V_T}\right) \qquad (15)$$

Then we have the following for $\frac{dI_{OUTn}}{dI_{IN}} = 0$.

$$I_{IN} = \frac{V_T}{R^{total}{}_{n-1}} \qquad (16)$$

Then we have the peak output current:

$$I_{OUTn} = \frac{V_T}{R^{total}{}_{n-1}} \cdot \frac{1}{e} \qquad (17)$$

We see from eqs. (16), (17) that the input current value for the peak output current, and the peak output current value can be changed by the resistor values.

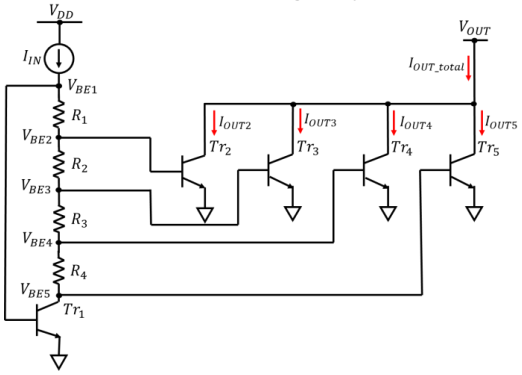

Fig. 7. Proposed Bipolar reference current source.

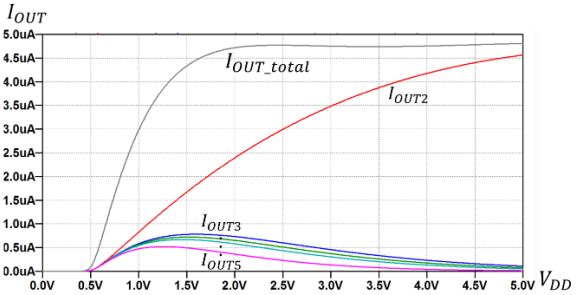

Fig. 8. Simulation results of the circuit in Fig. 7.

V. Conclusion

We have described simple MOS and Bipolar constant current sources, insensitive to wide range of power supply voltage variation; they are realized by addition of multiple current peaks. Their circuit topologies, analyses, and SPICE simulation results are presented.

Authors would like to thank Dr. M. Nagata, Prof. H. Tanimoto, Dr. T. Miki for valuable comments.

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[1] Inventor M. Nagata, Japanese Patent, Showa 46-16463 (Dec. 12, 1966)

[2] P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th edition, John Wiley & Sons Inc. (2009).