Phase-Locked Loop Circuit Design
— From Basics to State-of-The-Art and Industrial Practices —

Atsushi Motozawa
(email: atsushi.motozawa.kx@renesas.com )

Renesas Electronics Corporation
Outline

- What is a PLL?
- Applications
- Building blocks & Design tips
- Advanced architecture
- Summary
- Operation frequency getting higher year by year
- Quadruples every decade
- Clocks of a few giga Hz are needed for SoCs
What is a PLL?

- Frequency multiplication
- Phase difference reduction

CLKin → PLL → CLKout

CLKin

CLKout

CLKin

CLKout

x N
How to distribute high frequency clock

- IC without PLL
- IC with PLL

CPU 1.5GHz
Logic 500MHz

CPU 1.5GHz
PLL X 75
Logic 500MHz
PLL X 25

✓ Crosstalk and reflection can occur
✓ Extra space in PCB
✓ Many pins are needed

✓ Low input frequency
✓ w/o crosstalk or reflection
✓ Several identical PLLs with different divisors in one IC
Outline

- What is a PLL?
- Applications
- Building blocks & Design tips
- Advanced architecture
- Summary
Clock skew due to clock distribution
- With skew, it’s difficult to make synchronous systems
- Skew is dependent on power supply voltage and temperature
Clock buffers are put into deskew PLL

- PLL reduces the phase difference between CLK1 and CLK2
- PLL can work even if supply voltage and temperature change.
An LSI operates at 1GHz. The LSI emits EMI noise.

It can interfere with other LSIs and signals on PCBs.
Spread Spectrum Clock (SSC)

Fin=10MHz → PFD/CP → Filter → VCO → Fout

DIV 1/N

N=100

N=99

1%

1/fmod

iosismodated divider to generate SSC

ΔΣ noise is filtered by PLL

Output frequency

1GHz

0.99GHz

10MHz (1% of 1GHz)

PSD

EMI reduction

Conventional

AME

SSC

Freq.

0.99 GHz

1 GHz

D. Motozawa
CDR (Clock and Data Recovery)

- Incoming data without accompanying clock
- CDR extracts a clock to sample incoming data
Outline

- What is a PLL?
- Applications
- Building blocks & Design tips
- Advanced architecture
- Summary
PLL Diagram

How do we design a PLL?

IN → DQ → R → UP → Icp → OUT

DRQ → DN

Cpl, gm, R, Cz, Rdeg

Q, D

A. Motozawa
Block diagram and Domains

PLL’s building blocks
- PFD: Phase-Frequency Detector
- CP: Charge Pump
- Loop filter
- GM (Voltage-current converter)
- CCO: Current-controlled Oscillator
- Divider

<table>
<thead>
<tr>
<th>Line</th>
<th>Domain</th>
</tr>
</thead>
<tbody>
<tr>
<td>rad</td>
<td>[rad]</td>
</tr>
<tr>
<td>A</td>
<td>[A]</td>
</tr>
<tr>
<td>V</td>
<td>[V]</td>
</tr>
</tbody>
</table>
PLL Diagram

PFD
(Phase-frequency detector)

IN

D Q
R

DRQ

UP

DN

OUT

Icp

Cpl

R

Cz

gm

R_{deg}

D Q

I_{cp}

A. Motozawa
PFD (Phase-frequency detector)

Case 1 (CLKfb is behind)
- CLKin
- CLKfb
- RST
- RSTd
- UP
- DN

Case 2 (CLKfb is ahead)
- CLKin
- CLKfb
- RST
- RSTd
- UP
- DN

- CLKfb is behind CLKin
  → UP is wider
- CLKfb is ahead of CLKin
  → DN is wider
- RST is delayed to avoid dead zone
PLL Diagram

CP
(Charge pump)
Output is pulse-shaped current that is dependent on the width of the phase difference.

CP gain is \( \frac{I_{CP}}{2\pi} \) [A/rad]
Modeling of PFD and CP set

- PFD becomes summing block.
- CP becomes gain block
PLL Diagram

Loop filter (Lead-lag filter)
Loop Filter

- Converts the domain: current → voltage
- Cz is much larger than Cpl → Cz+Cpl ≈ Cz
- Lead-lag compensation
PLL Diagram

GM
(Transconductor)
Voltage-current converter
R\text{deg} reduces the transconductance but the linear range becomes wider.

\[ g_{m_{\text{eq}}} = \frac{g_m}{g_m R_{\text{deg}} + 1} \]
Modeling of loop filter and GM set

- Loop filter converts the domain from current to voltage
- GM becomes gain block and converts the domain from voltage to current
PLL Diagram

CCO
(Current-controlled oscillator)

IN

OUT

DCO (Current-controlled oscillator)
CCO (Current-Controlled Oscillator)

- The number of stages is commonly 3—5.
- \( F_{cco} = \frac{1}{2 \cdot T_d \cdot N} \) [Hz]
- In this talk, [rad/s/A] is used for \( K_{cco} \). NOT [Hz/A]

\[ K_{cco} [\frac{rad/s}{A}] \]
\[ \omega_{cco} [rad/s] \]
\[ I_{cco} [A] \]
\[ \frac{\partial}{\partial I_{cco}} \]

The number of stages is commonly 3—5.

\( F_{cco} = \frac{1}{2 \cdot T_d \cdot N} \) [Hz]

In this talk, [rad/s/A] is used for \( K_{cco} \). NOT [Hz/A]

\( N \): the number of stages for CCO
Phase is the time integral of frequency

\[
\begin{align*}
\text{Frequency} & \quad \omega [\text{rad/s}] \\
\text{Phase} & \quad \theta [\text{rad}] \\
\end{align*}
\]

\[
\theta = \int \omega \, dt
\]
Modeling of CCO

- Domain change: A → rad/s → rad
- -90° phase shift at DC
- \( K_{cc0} \) is dependent on the operation frequency
PLL Diagram

Divider
**Divider**

- **Divide-by-2 and 4 divider**

  ![Divider Circuit Diagram]

  - D1
  - Q1(Divide-by-2)
  - D2
  - Q2(Divide-by-4)
  - CLK
  - Q1
  - D1
  - Q2
  - D2

- **Divide-by-3 divider**

  ![Divider Circuit Diagram]

  - D1
  - Q2(Divide-by-3)
  - D2
  - Q1
  - D1
  - Q2
  - D2

**A. Motozawa**
Modeling of Divider

Divide-by-N divider

Frequency Domain

\[ \omega_{out} = \frac{1}{N} \omega_{in} \]  [rad/s]

Phase Domain

\[ \phi_{out} = \frac{1}{N} \phi_{in} \]  [rad]
Modeling of Single-Path PLL

\[ \Phi_{fb}[\text{rad}] \]

\[ \Phi_{in}[\text{rad}] \quad \text{I}_{out}[\text{A}] \]

\[ \text{I}_{cp} \]

\[ \text{I}_{cp} \]

\[ \text{V}_{c}[\text{V}] \]

\[ \text{I}_{cco}[\text{A}] \]

\[ \omega_{cco} \quad [\text{rad/s}] \]

\[ \Phi_{out}[\text{rad}] \]

\[ \frac{1}{N} \]

\[ \frac{1}{s} \]
PLL transfer function and Bode Plot

\[ H_{op} = \frac{K_{CCO}I_{cp}}{2\pi N} \cdot \frac{1}{s^2} \cdot \frac{g_{m_{eq}}}{C_z} \cdot \frac{sRC_z + 1}{sRC_{pl} + 1} \]

Poles [Hz]
0, 0, \frac{1}{2\pi RC_{pl}}

Zero [Hz]
\frac{1}{2\pi RC_z}

Crossover freq. [Hz]
\approx \frac{K_{CCO}I_{cp}g_{m_{eq}}R}{(2\pi)^2 N}

Open loop Transfer function
PLL open loop line on Nichols Chart

The X-axis: Open loop Phase
The Y-axis: Open loop Gain

Dashed circles: Closed loop Gain

■ If the open loop line passes by the right side of the red cross(-180deg, 0dB), the system is stable.

■ System is stable as long as the open loop gain is large enough
Dual-Path PLL

Integral Path

Proportional Path

Open loop transfer function

\[ H_{op} = \frac{K_{CCO} I_{CPI}}{2\pi N} \cdot \frac{1}{s^2} \cdot \frac{g_{m\_eq}}{C_z} \cdot \frac{s \cdot \frac{C_z}{g_{m\_eq}} \cdot \frac{I_{CPP}}{I_{CPI}} + 1}{s R_C p + 1} \]

Poles [Hz]

\[ 0, \quad 0, \quad \frac{1}{2\pi R_C p} \]

Zero [Hz]

\[ \frac{1}{2\pi} \frac{g_{m\_eq}}{C_z} \frac{I_{CPP}}{I_{CPI}} \]

Crossover freq. [Hz]

\[ \approx \frac{K_{CCO} I_{CPP}}{(2\pi)^2 N} \]

- Zero can be controlled by the ratio of \( I_{CPP} \) and \( I_{CPI} \). That leads to smaller \( C_z \)
- Single-path PLL: \( C_z \sim 100\text{pF} \)
- Dual-path PLL: \( C_z \sim 20\text{pF} \)
Hybrid PLL

“A 0.7-to-3.5 GHz 0.6-to-2.8 mW Highly Digital Phase-Locked Loop With Bandwidth Tracking”
Wenjing Yin, et al., IEEE JSSC, VOL. 46, NO. 8, pp1870—1880, AUG. 2011

- Analog-Digital Hybrid
  ✓ Small & programmable
  ✓ Analog proportional path to reduce quantization error
- !!PD instead of TDC
  ✓ Simple, Small, and Low power
  ✓ Intrinsically nonlinear → Jitter makes it linear

<table>
<thead>
<tr>
<th>Technology</th>
<th>90nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1V</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>0.7GHz-3.5GHz</td>
</tr>
<tr>
<td>Random jitter @ 2.5GHz</td>
<td>1.6ps r.m.s</td>
</tr>
<tr>
<td>Jitter from integrated phase noise</td>
<td>0.9ps r.m.s</td>
</tr>
<tr>
<td>Peak-to-peak jitter @ 2.5GHz</td>
<td>11.6ps</td>
</tr>
<tr>
<td>Reference spur</td>
<td>-50.1dBc</td>
</tr>
<tr>
<td>Deterministic jitter from reference spur</td>
<td>0.83ps</td>
</tr>
<tr>
<td>Loop bandwidth @ 2.5GHz</td>
<td>16MHz</td>
</tr>
<tr>
<td>Power @ 2.5GHz</td>
<td>1.6mW</td>
</tr>
<tr>
<td>Die area</td>
<td>0.36mm²</td>
</tr>
</tbody>
</table>
Outline

- What is a PLL?
- Applications
- Building blocks & Design tips
- Advanced architecture
- Summary
Summary

- PLLs are utilized in many ICs
  - One IC contains several identical PLLs to provide different frequency clocks while reducing I/O pins and avoiding the reflection

- Many PLL applications
  - Not only frequency multiplication
  - SSC to reduce EMI noise
  - CDR system to generate from incoming data
  - Deskew PLL to decrease phase error among clocks

- Building blocks and transfer functions are discussed
  - Several domains in PLL loop
  - Dual-path PLL is used to reduce capacitor

- Analog-digital hybrid PLL with !!PD is introduced
  - The keywords, digital-rich and !!PD, are important for an advanced PLL design