



# **Phase-Locked Loop Circuit Design**

**— From Basics to State-of-The-Art and Industrial Practices —**

**Atsushi Motozawa**

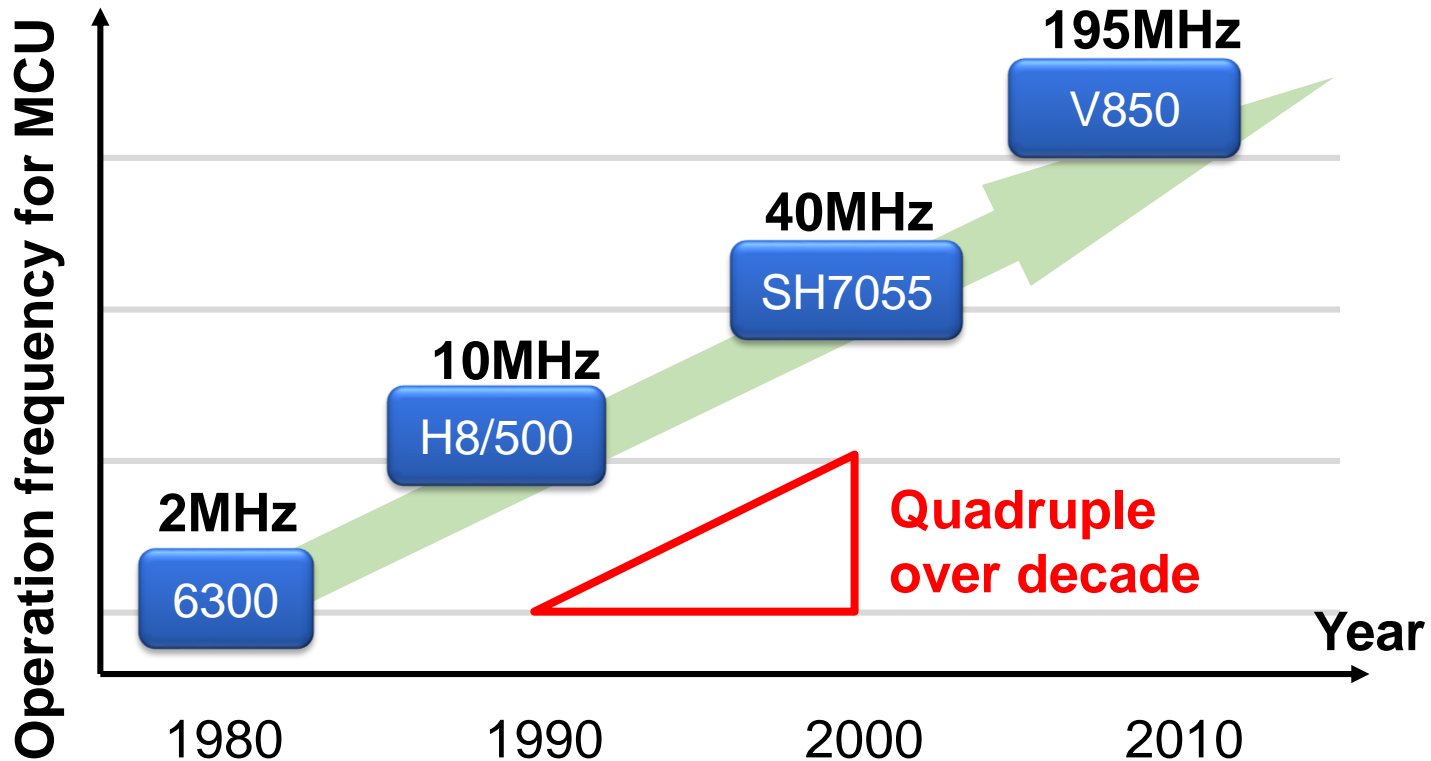
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Renesas Electronics Corporation



- What is a PLL?
- Applications
- Building blocks & Design tips
- Advanced architecture
- Summary

# MCU Operation Frequency

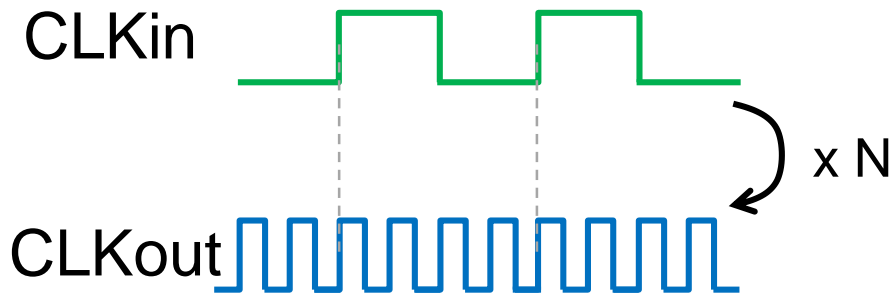


- Operation frequency getting higher year by year
- Quadruples every decade
- Clocks of a few giga Hz are needed for SoCs

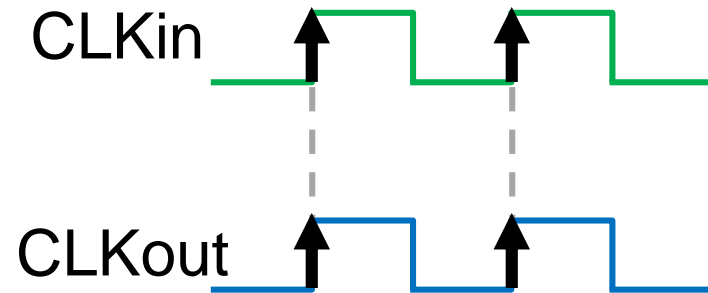
# What is a PLL?



## ■ Frequency multiplication



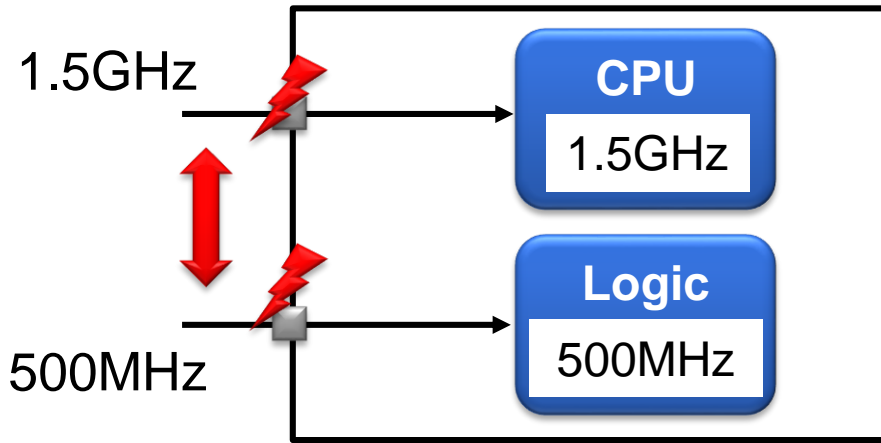
## ■ Phase difference reduction



# How to distribute high frequency clock

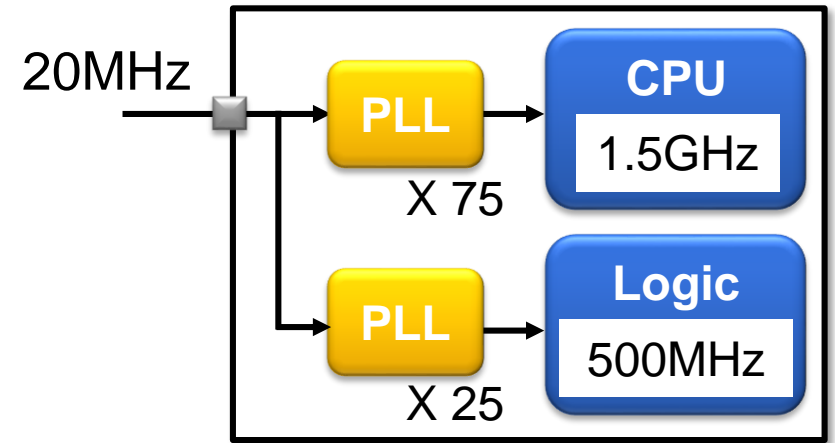


## ■ IC without PLL



- ✓ Crosstalk and reflection can occur
- ✓ Extra space in PCB
- ✓ Many pins are needed

## ■ IC with PLL



- ✓ Low input frequency
- ✓ w/o crosstalk or reflection
- ✓ Several identical PLLs with different divisors in one IC



- What is a PLL?



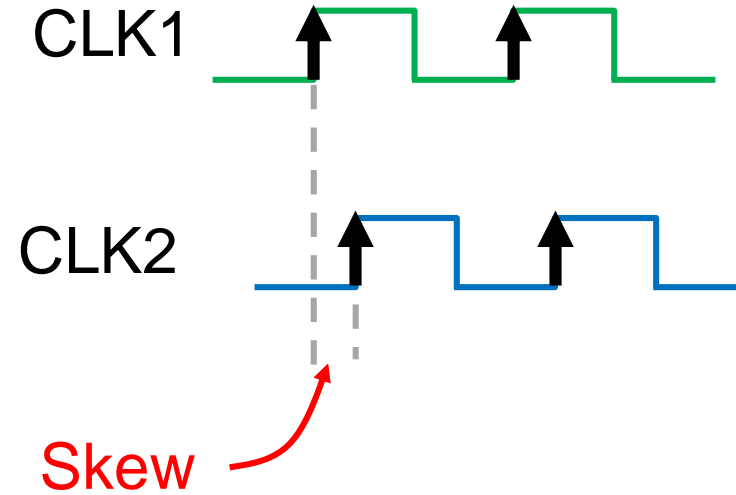
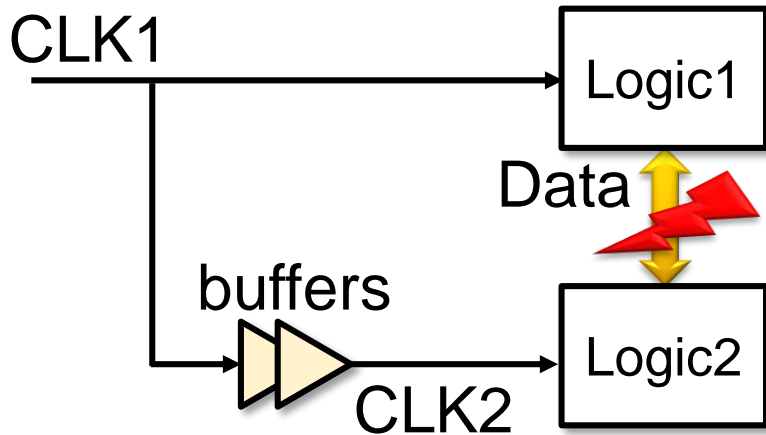
- Applications

- Building blocks & Design tips

- Advanced architecture

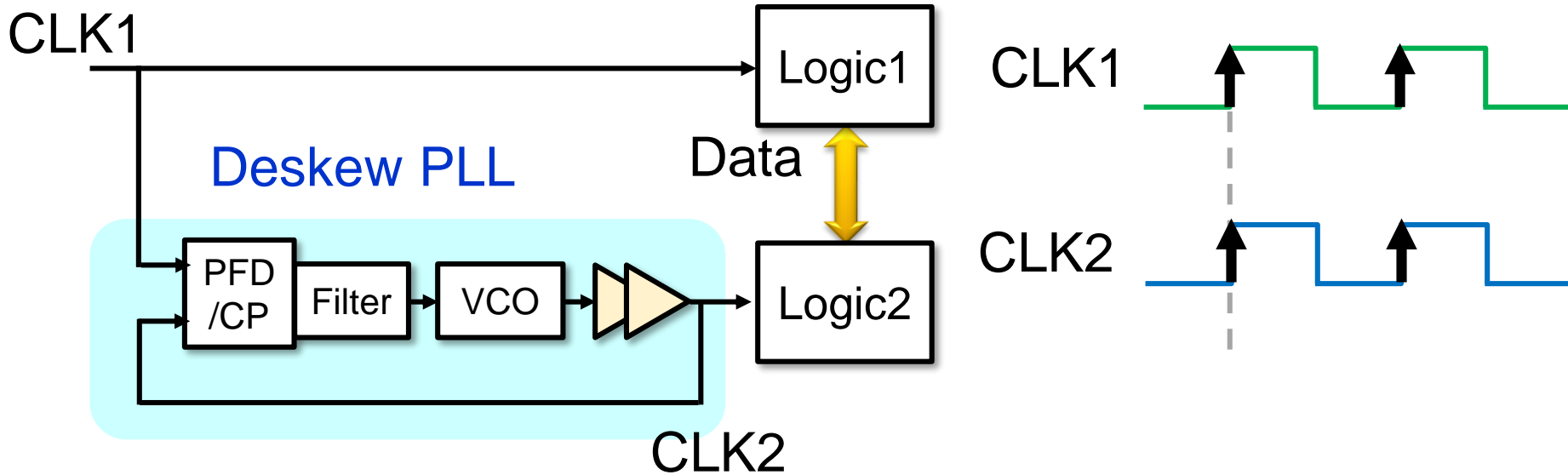
- Summary

# Clock Deskewing



- Clock skew due to clock distribution
- With skew, It's difficult to make synchronous systems
- Skew is dependent on power supply voltage and temperature

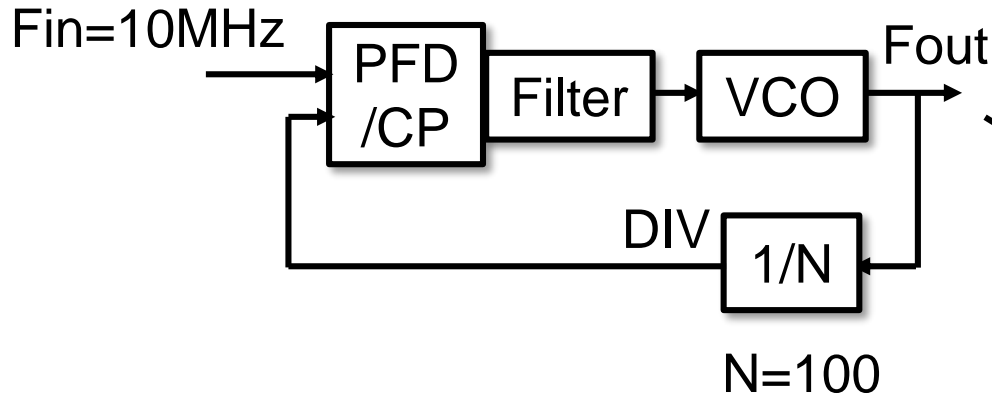
# Clock Deskewing



- Clock buffers are put into deskew PLL
- PLL reduces the phase difference between CLK1 and CLK2
- PLL can work even if supply voltage and temperature change.

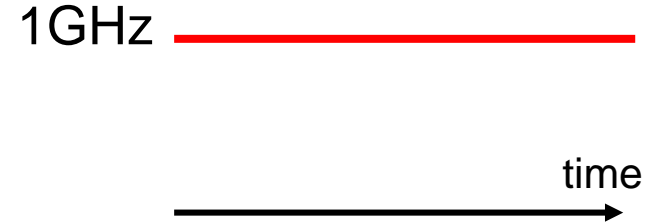


# Spread Spectrum Clock (SSC)

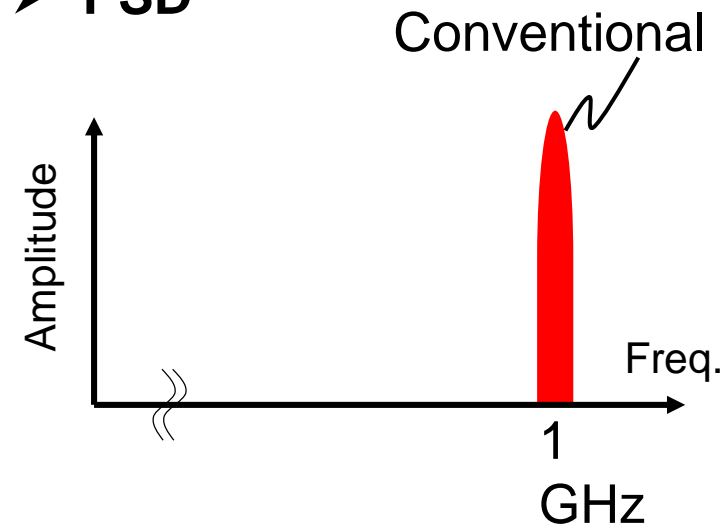


- An LSI operates at 1GHz. The LSI emits EMI noise.
- It can interfere with other LSIs and signals on PCBs.

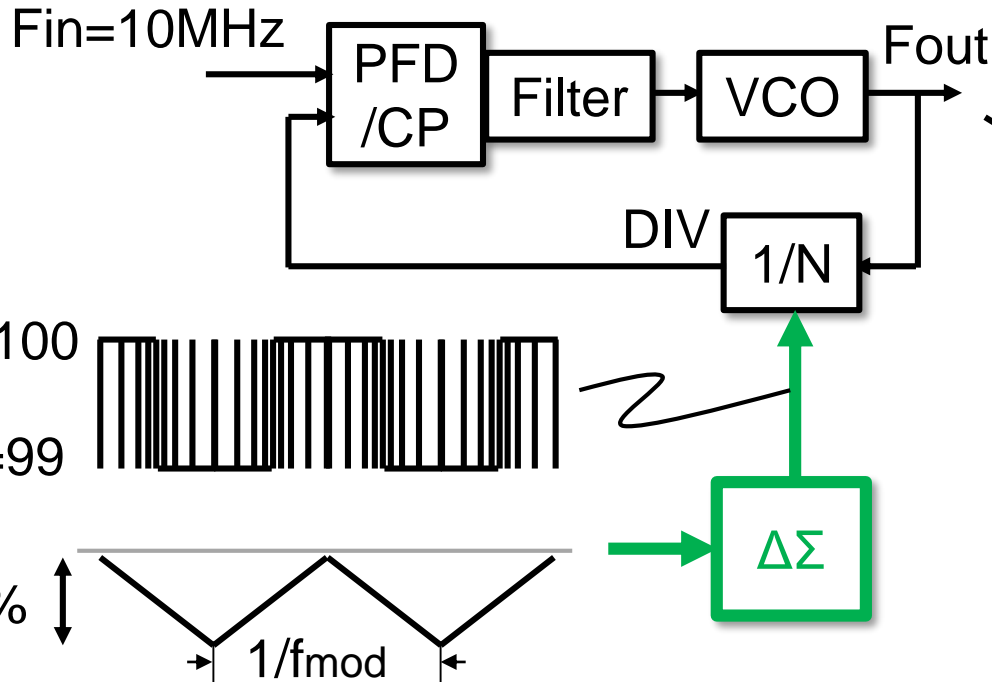
## ➤ Output frequency



## ➤ PSD

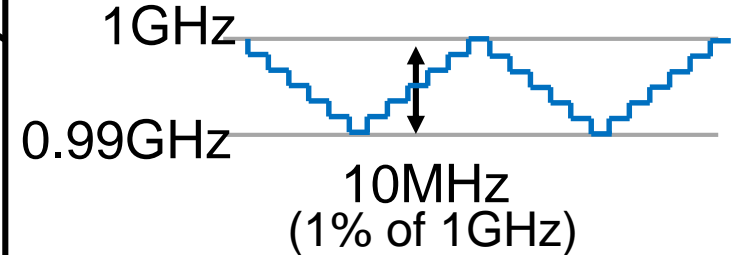


# Spread Spectrum Clock (SSC)

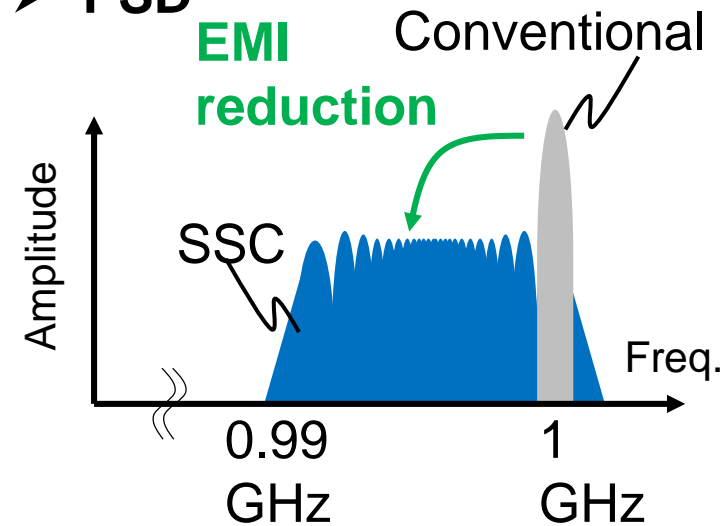


- $\Delta\Sigma$  modulated divider to generate SSC
- $\Delta\Sigma$  noise is filtered by PLL

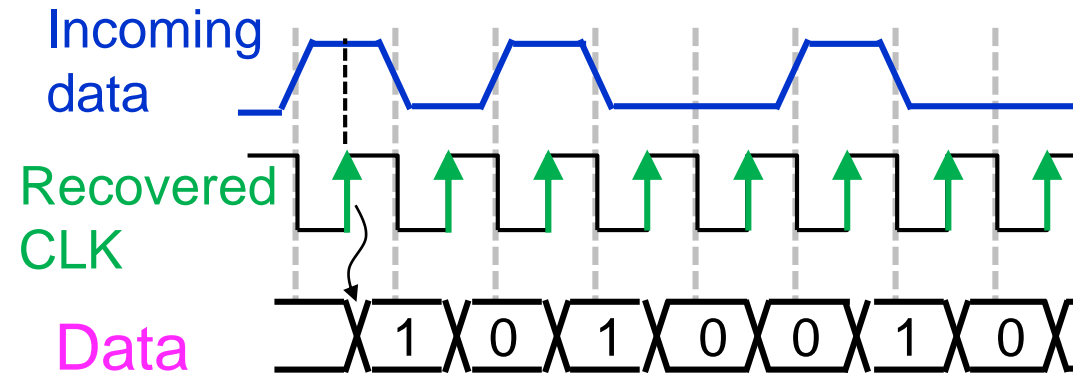
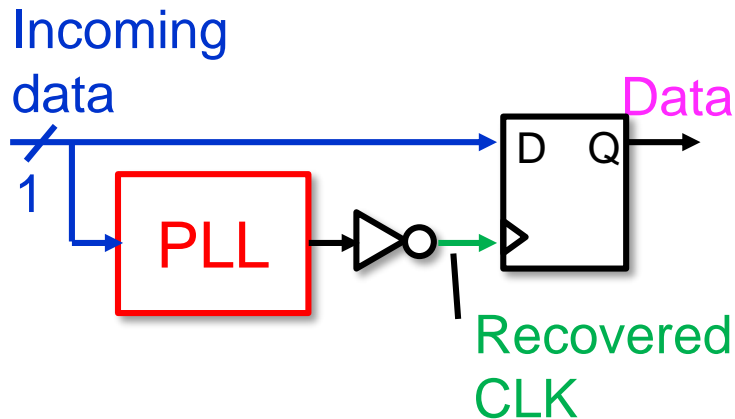
## ➤ Output frequency



## ➤ PSD



# CDR(Clock and Data recovery)



- Incoming data without accompanying clock
- CDR extracts a clock to sample incoming data

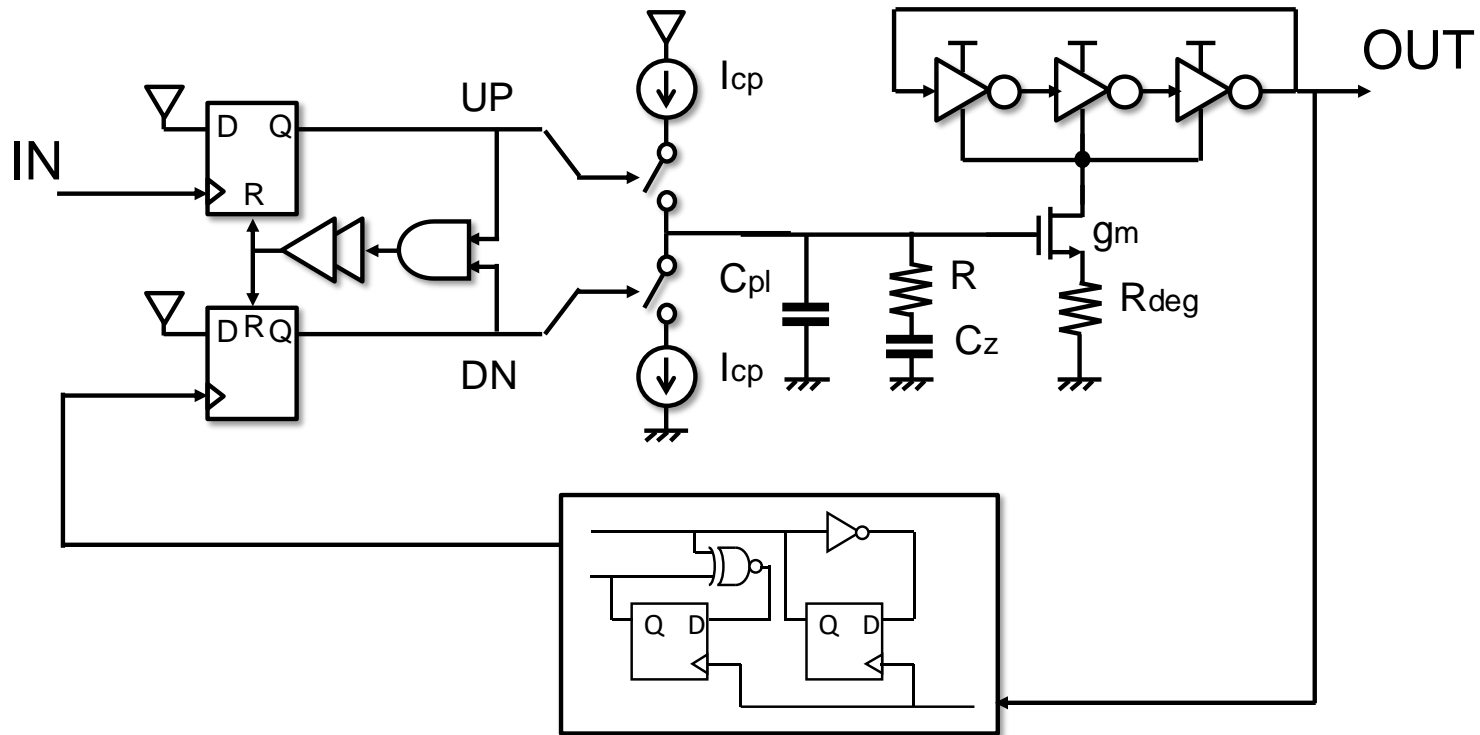


- What is a PLL?
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- ➔ ■ Building blocks & Design tips
- Advanced architecture
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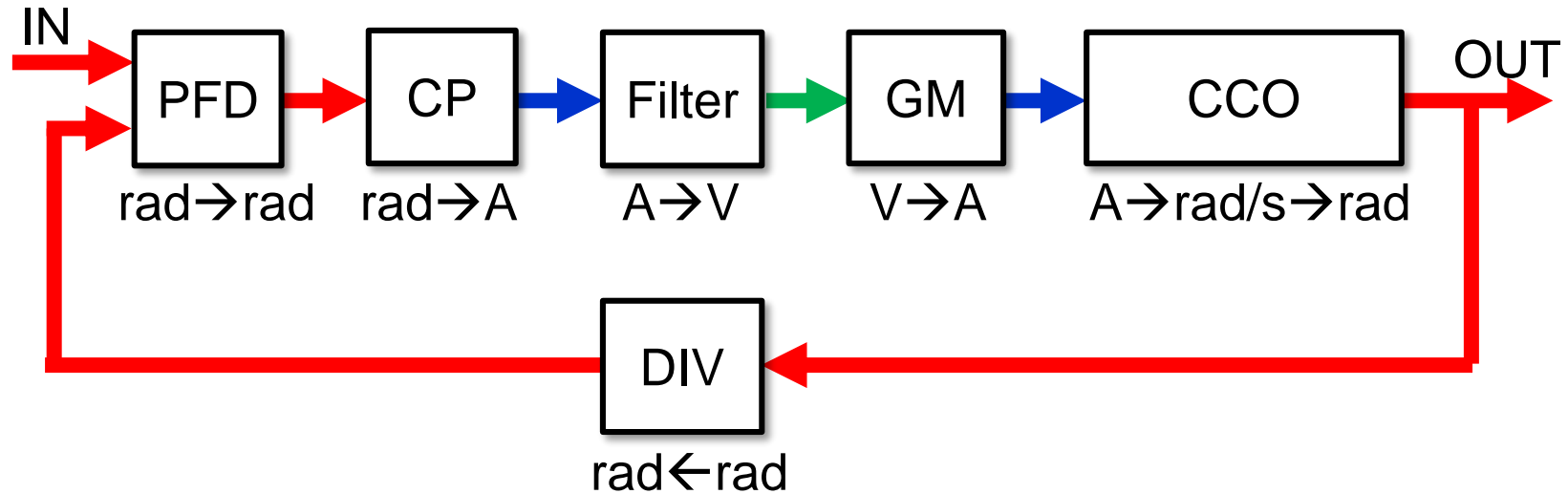
# PLL Diagram



How do we design a PLL?






# Block diagram and Domains



## PLL's building blocks

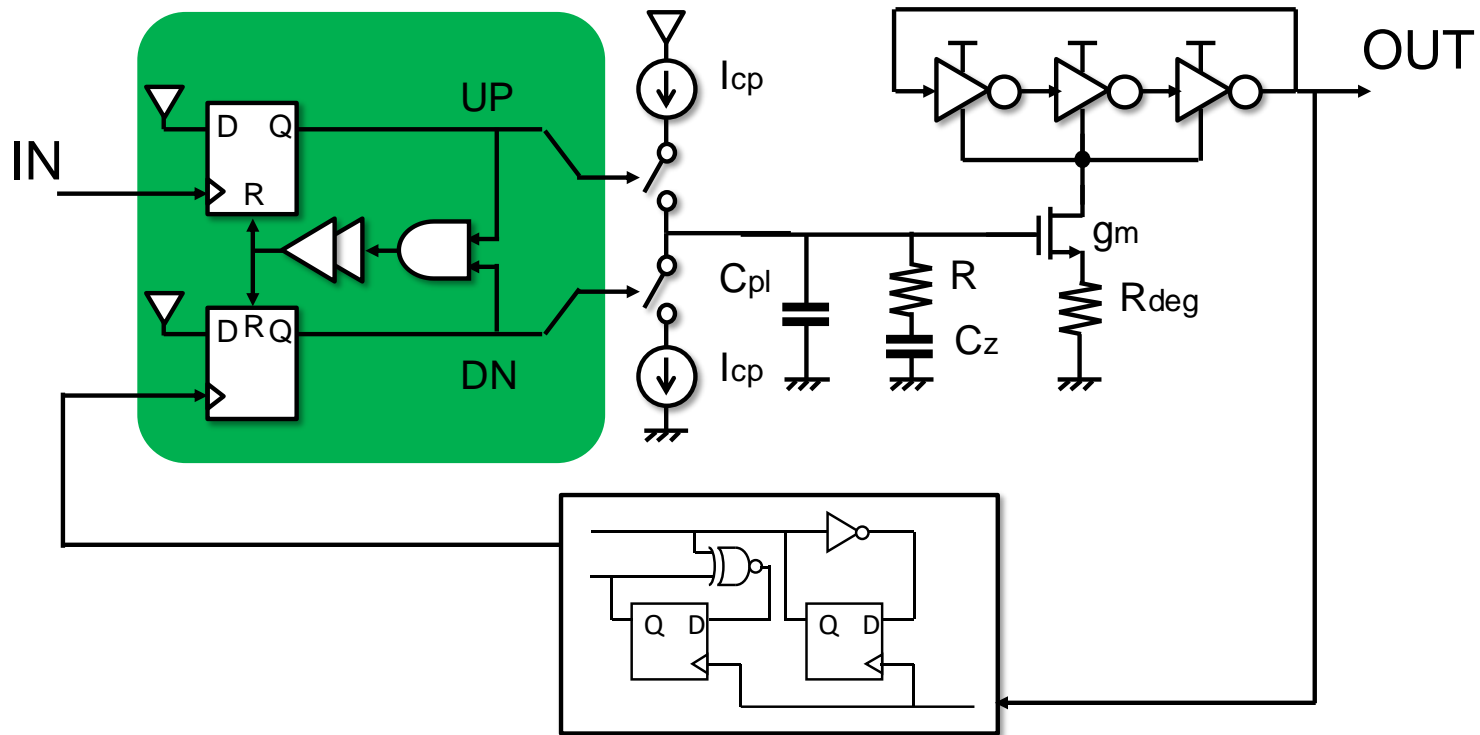
- PFD: Phase-Frequency Detector
- CP: Charge Pump
- Loop filter
- GM (Voltage-current converter)
- CCO: Current-controlled Oscillator
- Divider

Line	Domain
	[rad]
	[A]
	[V]

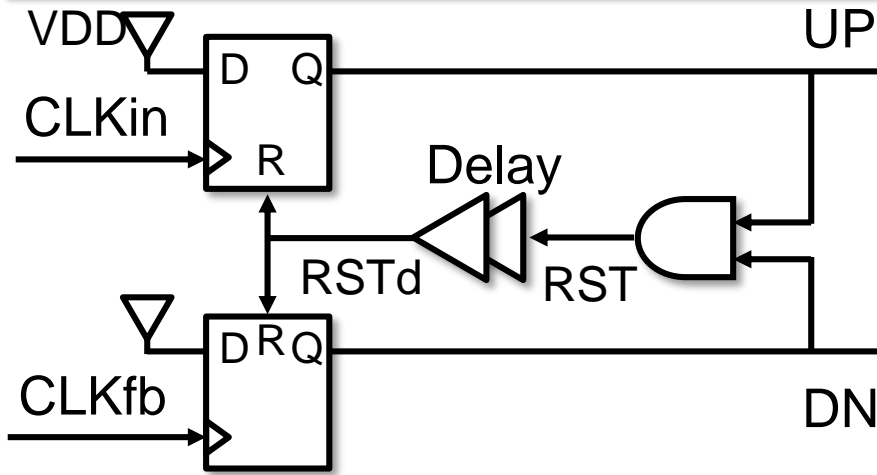
# PLL Diagram



## PFD (Phase-frequency detector)

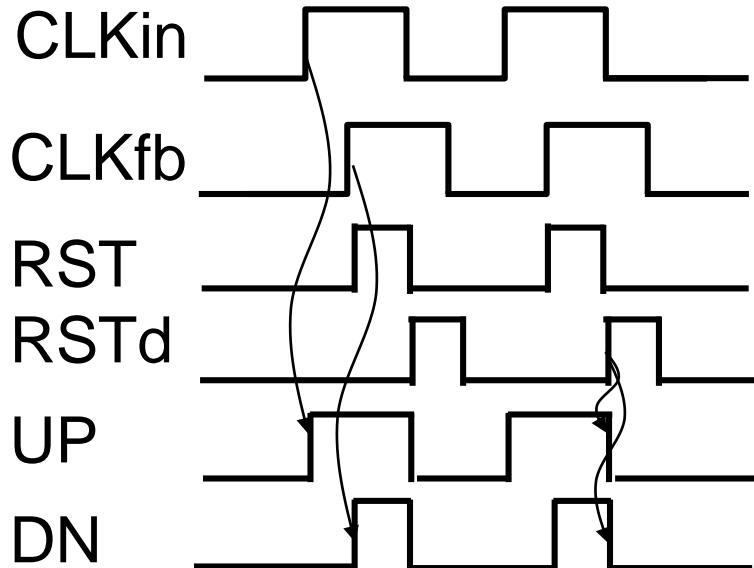


# PFD(Phase-frequency detector)

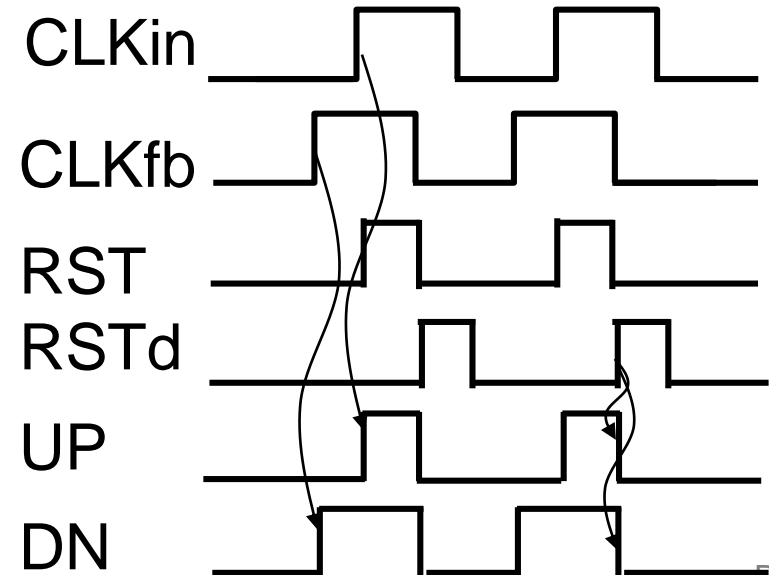


- CLKfb is behind CLKin  
→ UP is wider
- CLKfb is ahead of CLKin  
→ DN is wider
- RST is delayed  
to avoid dead zone

## Case1 (CLKfb is behind)



## Case2 (CLKfb is ahead)

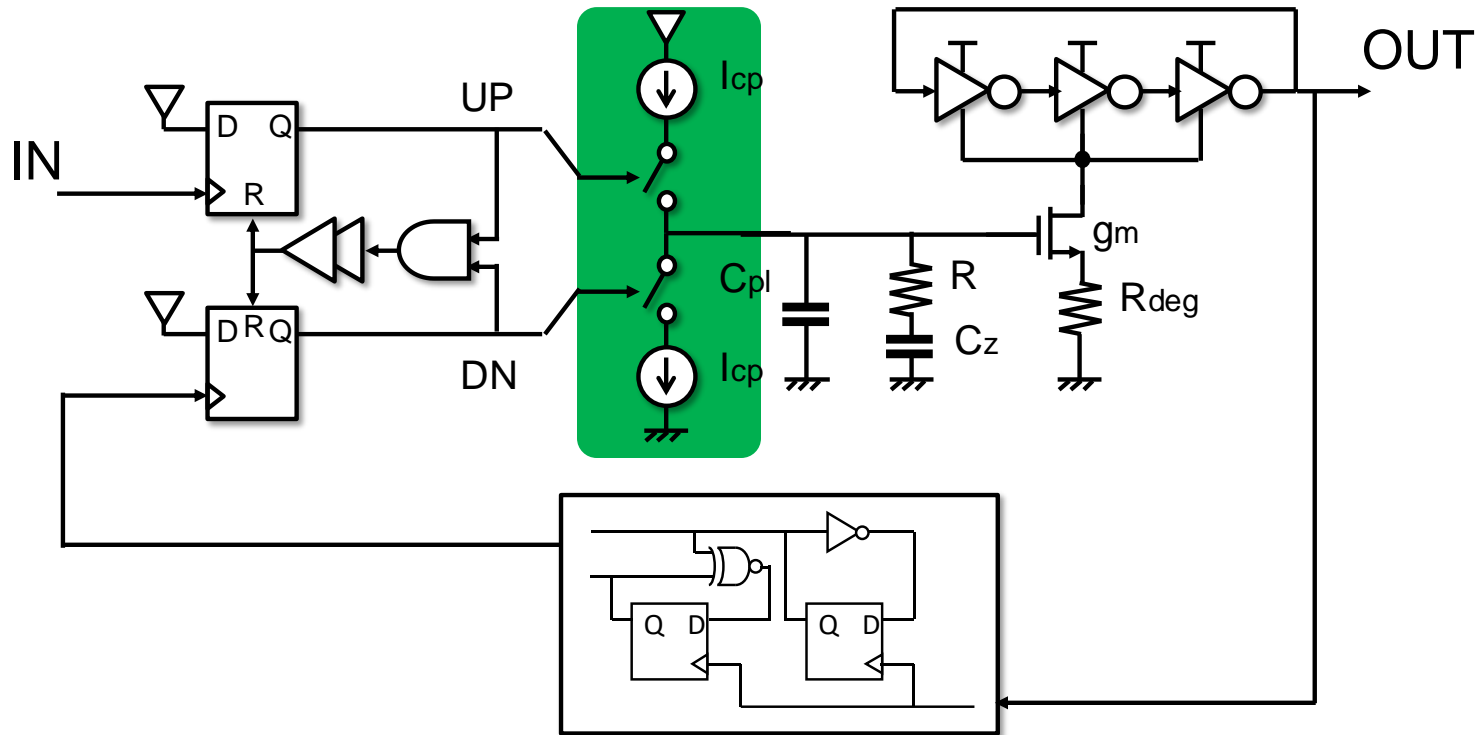




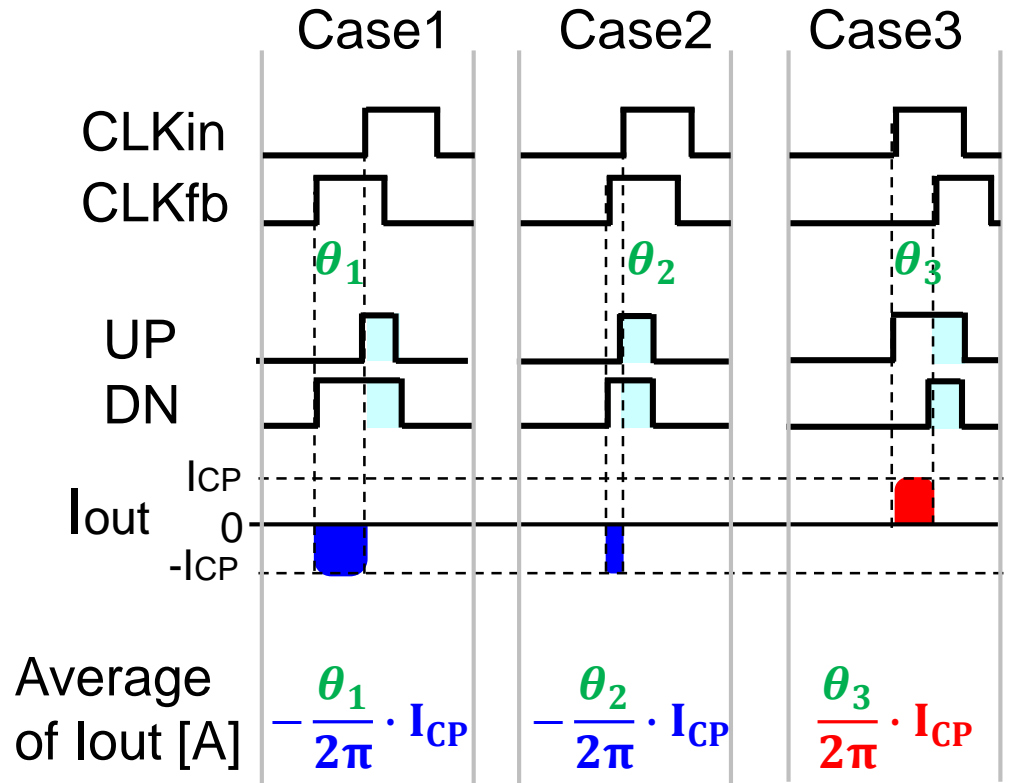
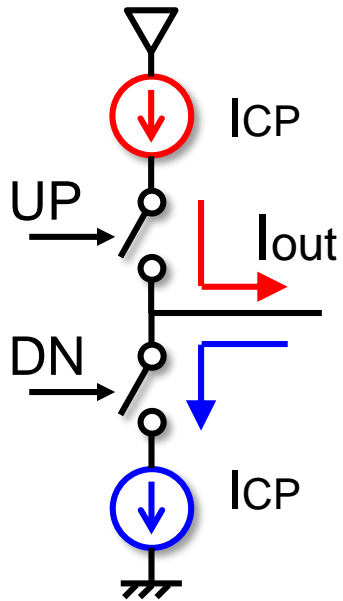
# PLL Diagram



## CP (Charge pump)

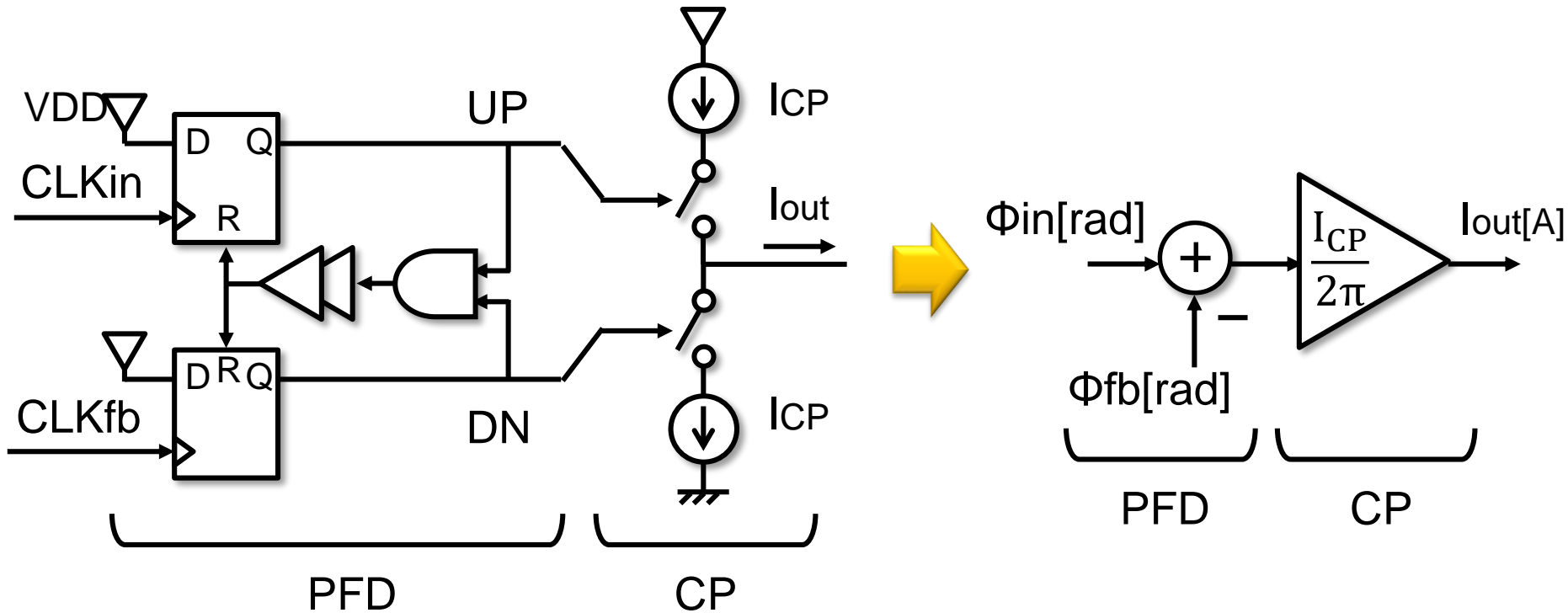


# CP (Charge Pump)



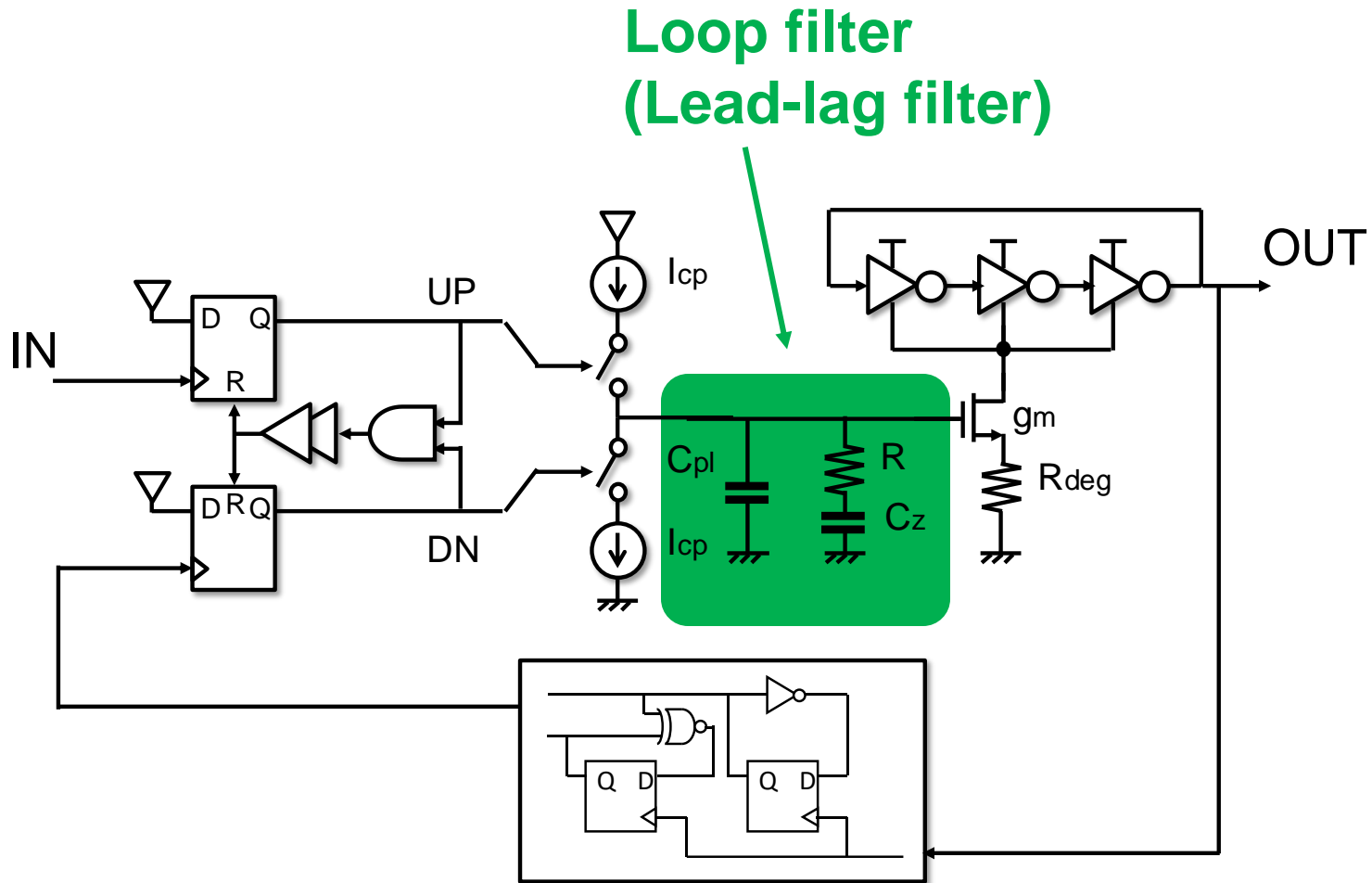
- Output is pulse-shaped current that is dependent on the width of the phase difference
- CP gain is  $I_{cp}/(2*\pi)$  [A/rad]

# Modeling of PFD and CP set

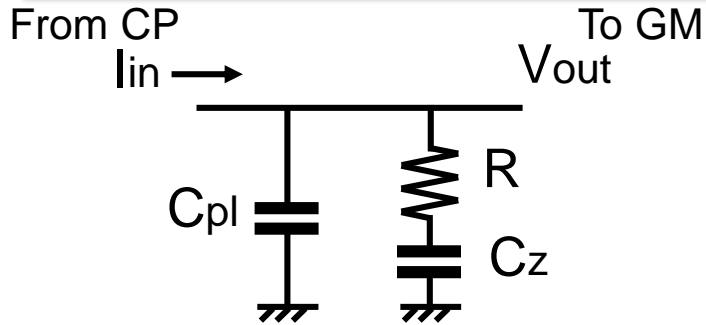


- PFD becomes summing block.
- CP becomes gain block

# PLL Diagram

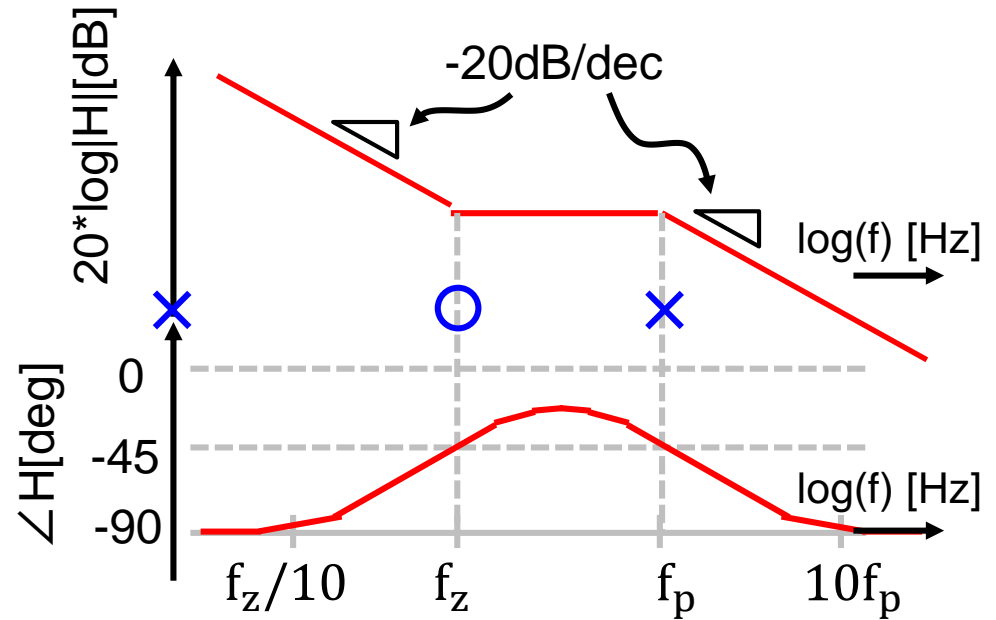


# Loop Filter



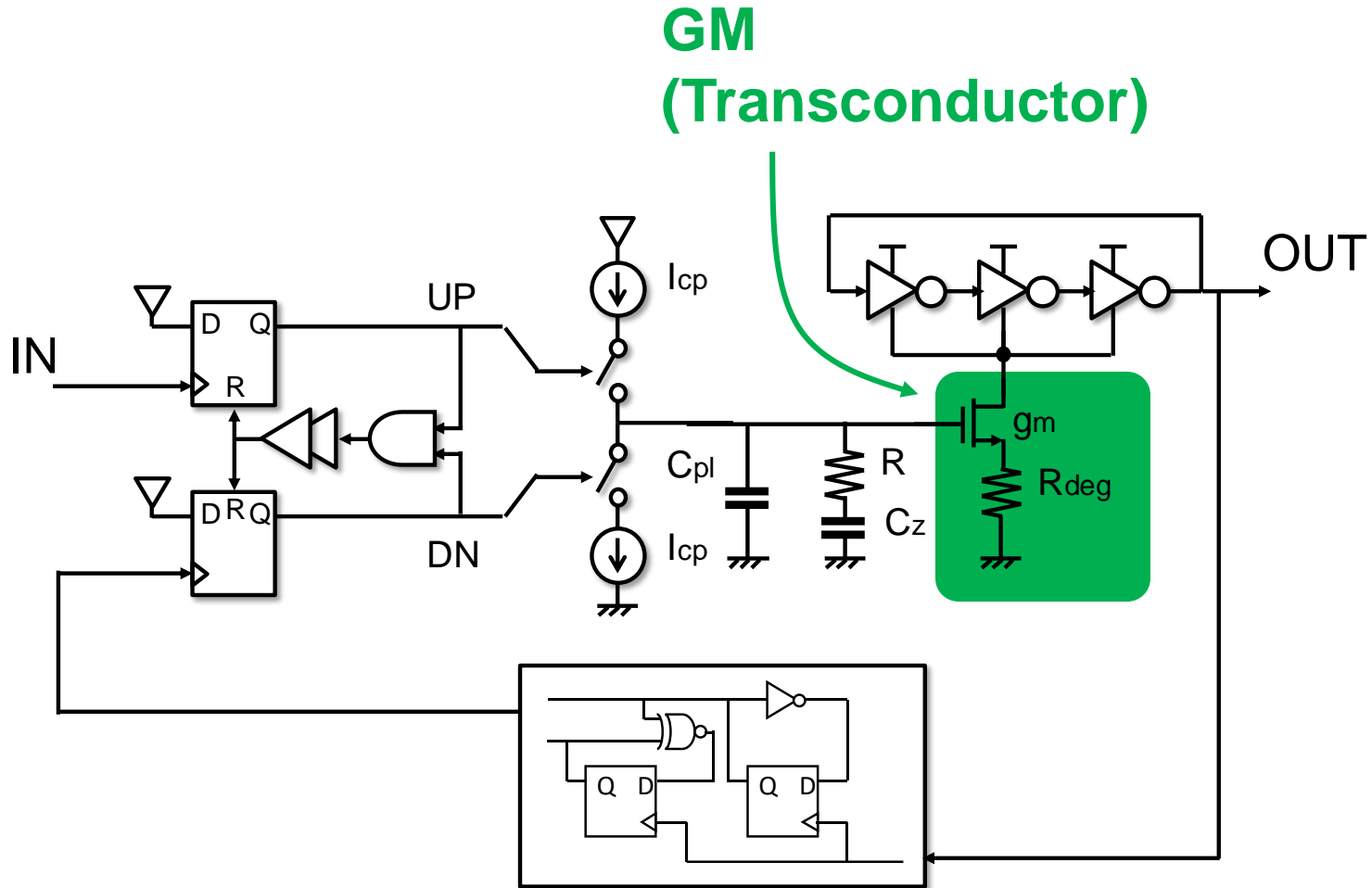
$$H(s) = \frac{V_{out}}{I_{in}} = \frac{1}{sC_z} \cdot \frac{sRC_z + 1}{sRC_{pl} + 1}$$

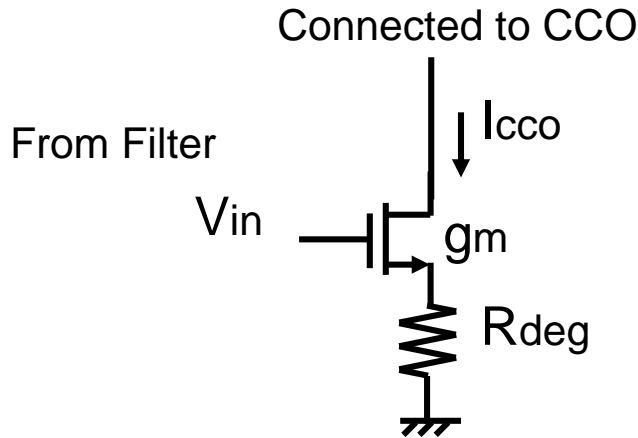
**Zero**  $f_z = \frac{1}{2\pi RC_z}$  [Hz]      **2<sup>nd</sup> pole**  $f_p = \frac{1}{2\pi RC_{pl}}$  [Hz]



- Converts the domain: current → voltage
- $C_z$  is much larger than  $C_{pl}$  →  $C_z + C_{pl} \approx C_z$
- Lead-lag compensation

# PLL Diagram

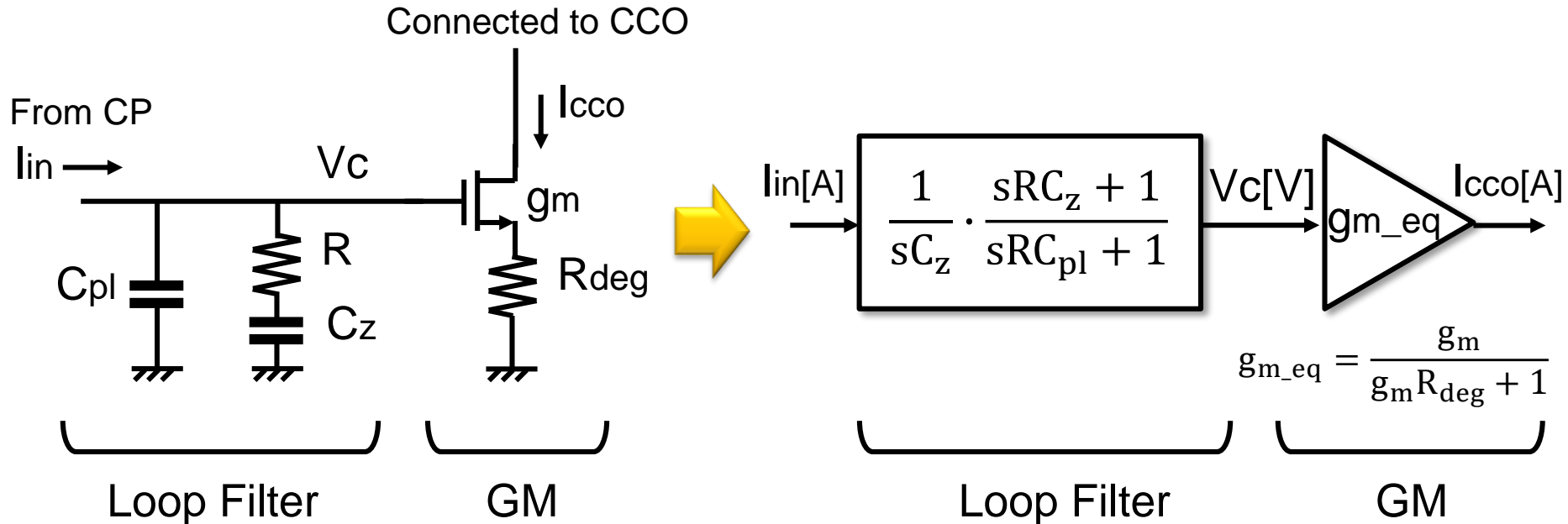




$$g_{m\_eq} = \frac{g_m}{g_m R_{deg} + 1}$$

- Voltage-current converter
- $R_{deg}$  reduces the transconductance but the linear range becomes wider.

# Modeling of loop filter and GM set



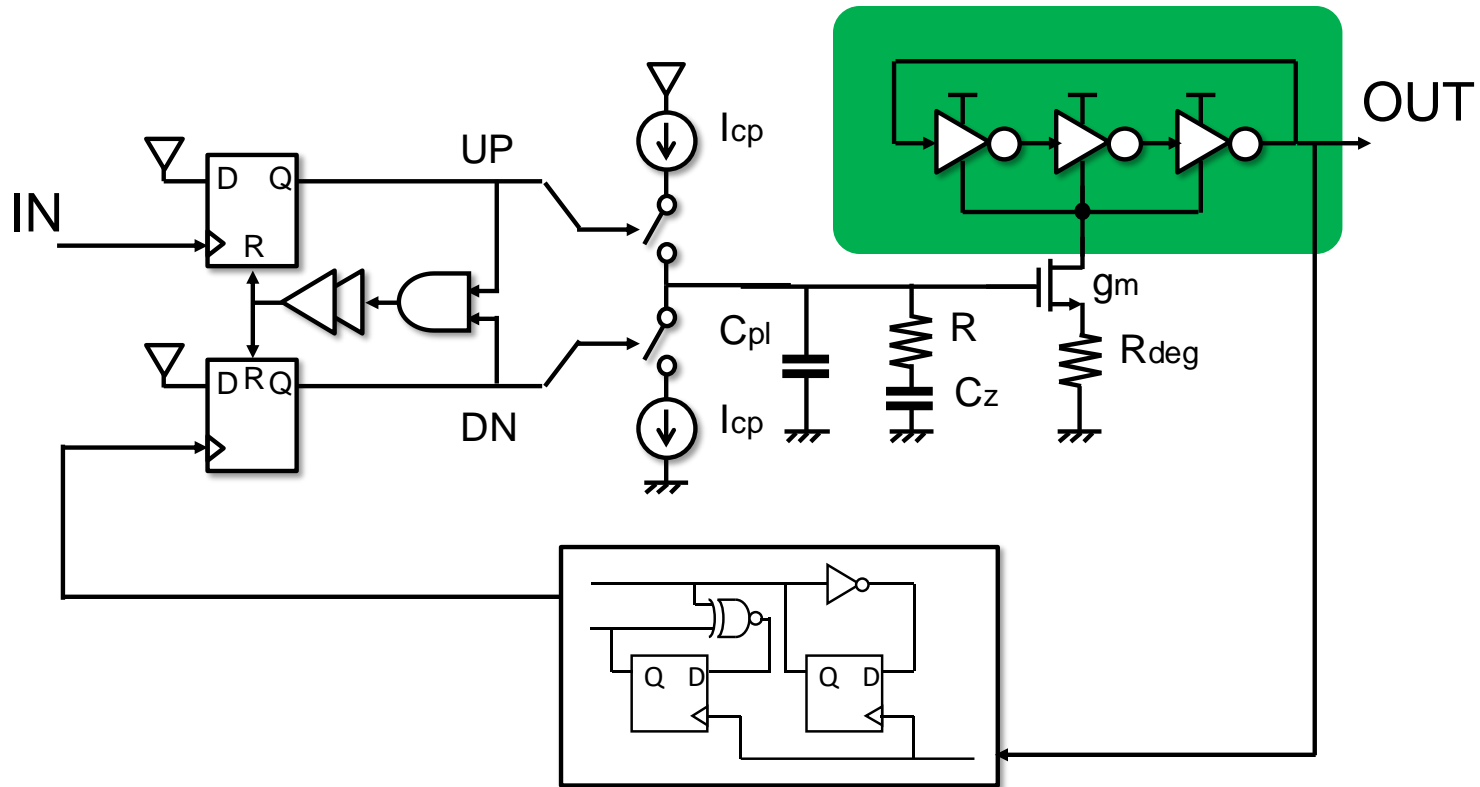
- Loop filter converts the domain from current to voltage
- GM becomes gain block and converts the domain from voltage to current



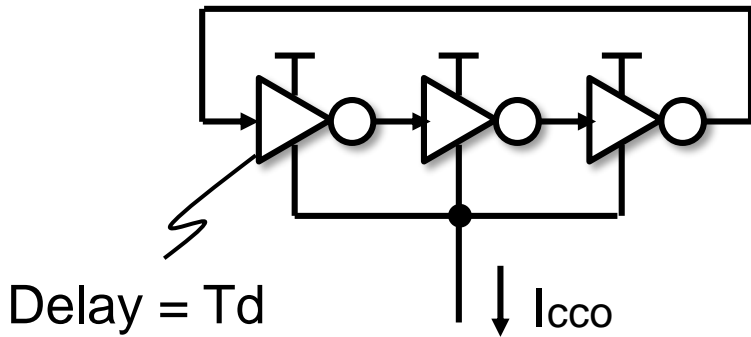
# PLL Diagram



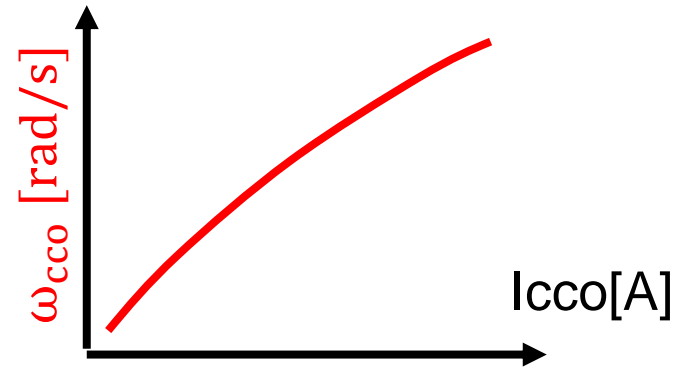
## CCO (Current-controlled oscillator)



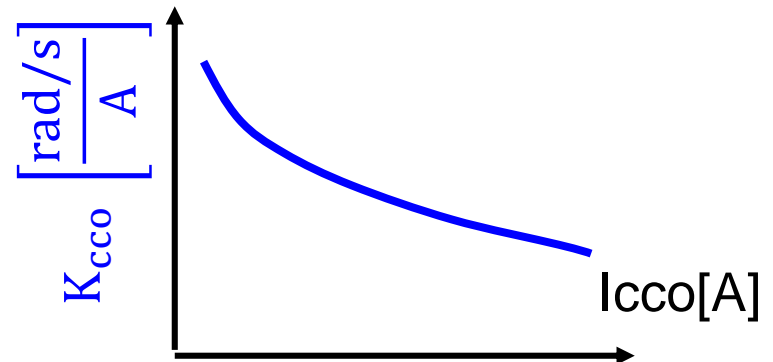
# CCO (Current-Controlled Oscillator)



- The number of stages is commonly 3—5.
- $F_{cco} = 1/(2 * T_d * N)$  [Hz]
- In this talk, [rad/s/A] is used for  $K_{cco}$ . NOT [Hz/A]



$$\frac{\partial}{\partial I_{cco}}$$

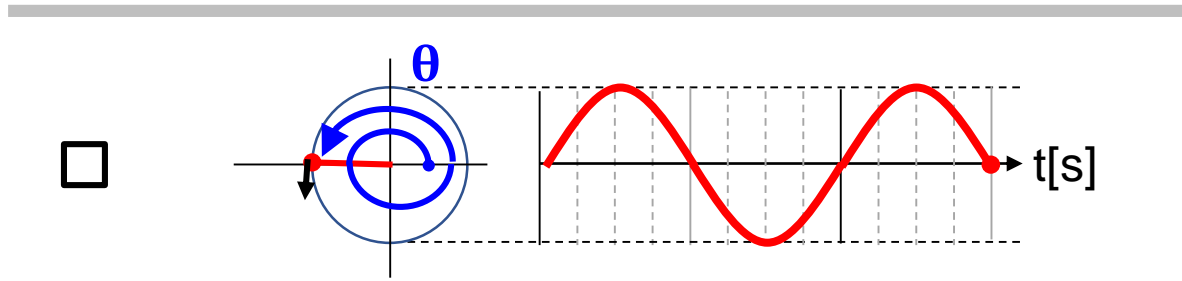
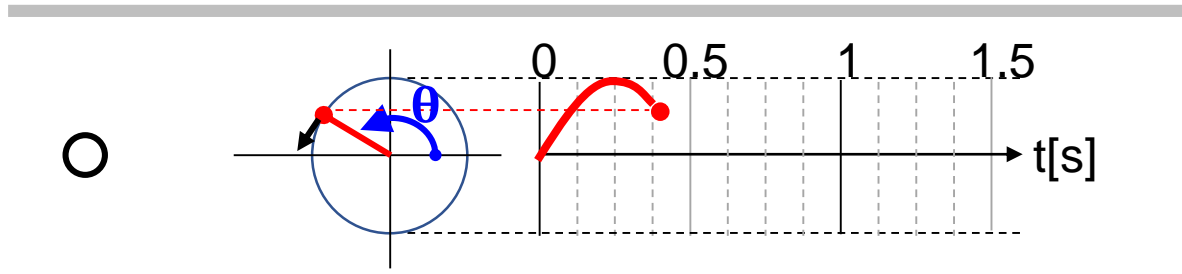
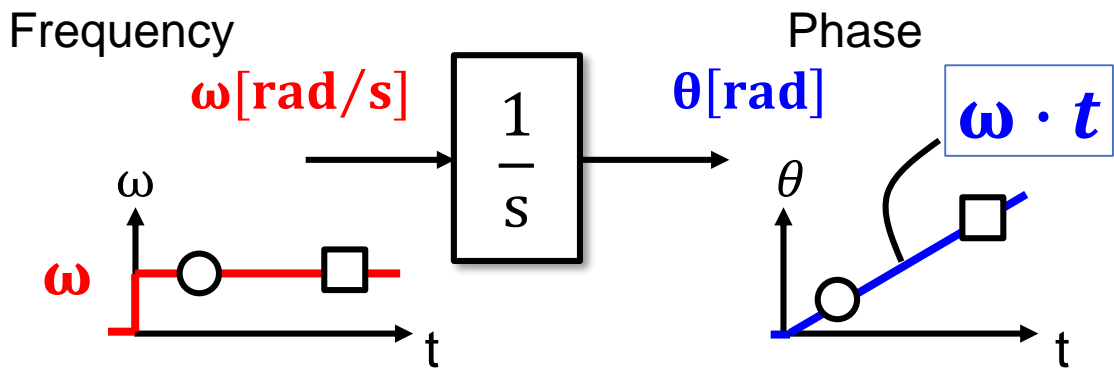


N: the number of stages for CCO

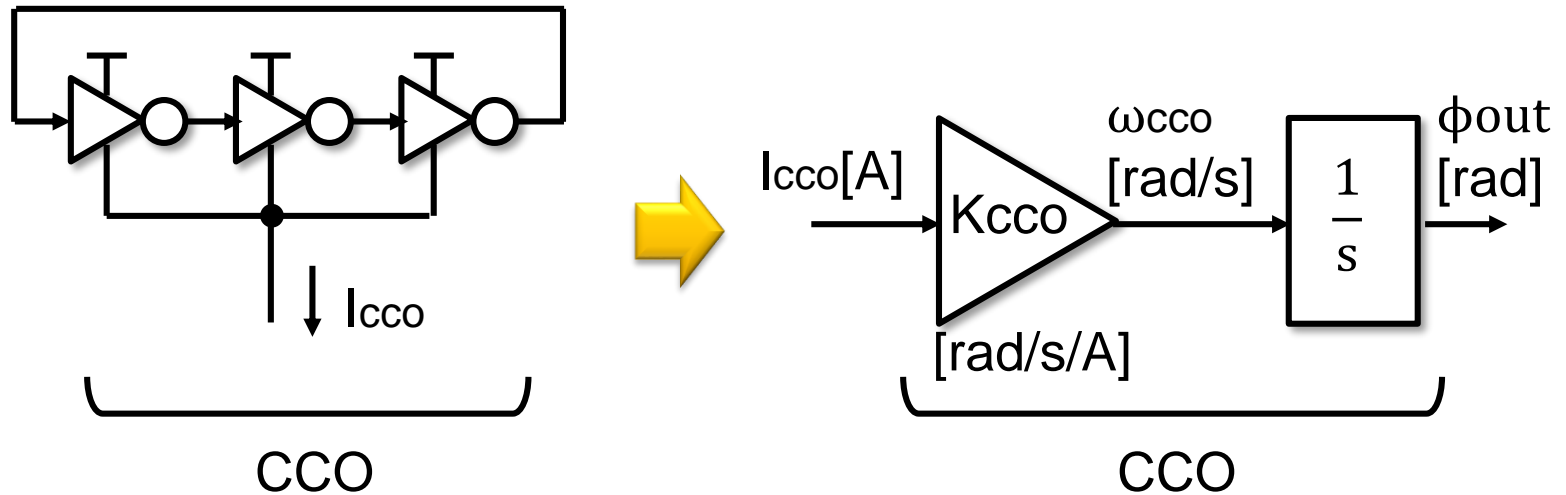
# Relationship Between Frequency and Phase



- Phase is the time integral of frequency

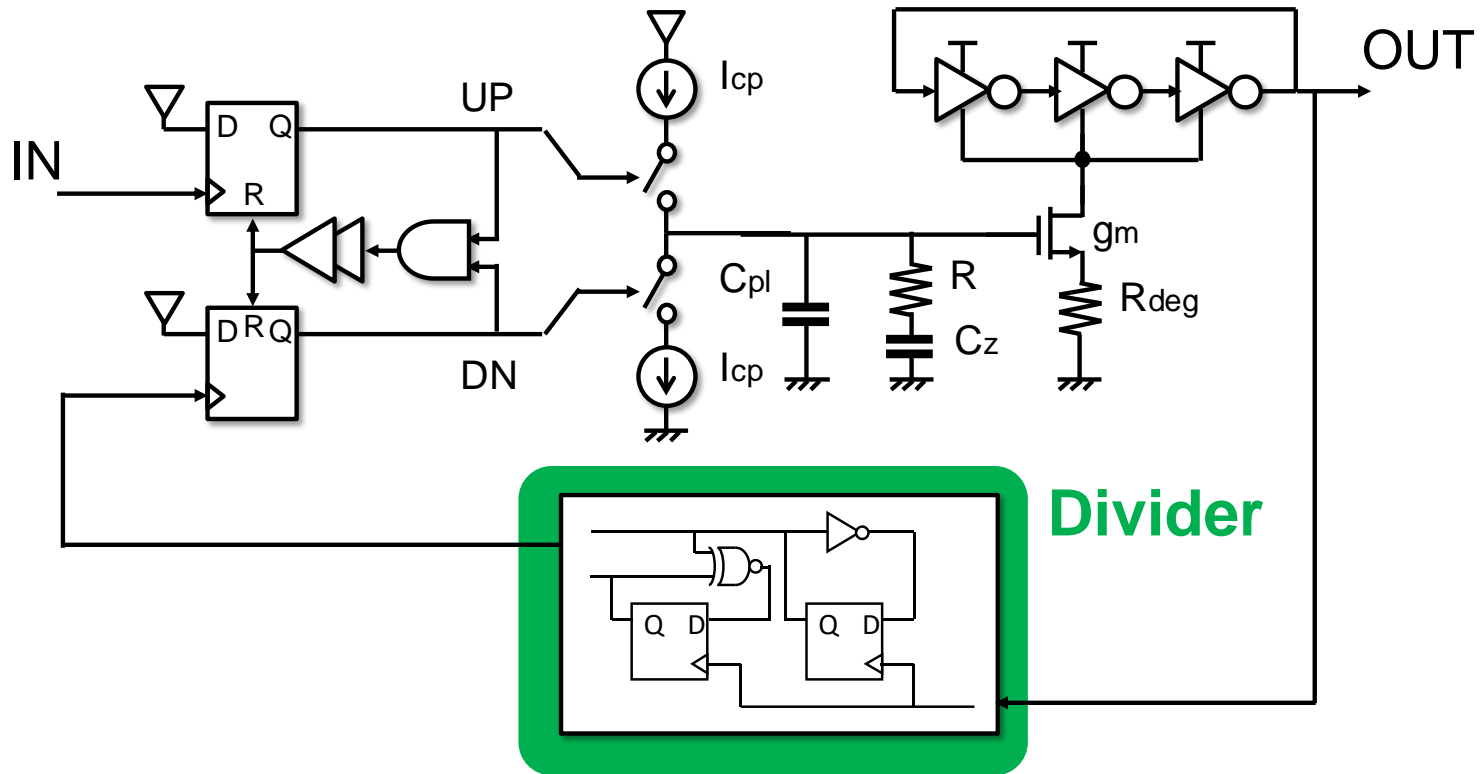


# Modeling of CCO



- Domain change:  $A \rightarrow \text{rad/s} \rightarrow \text{rad}$
- $-90^\circ$  phase shift at DC
- $K_{cco}$  is dependent on the operation frequency

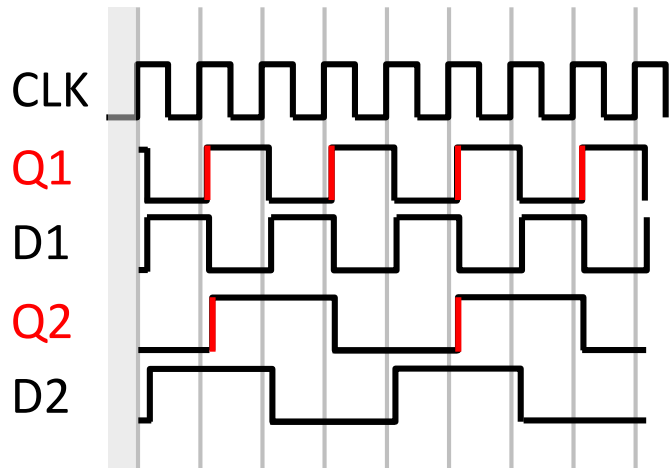
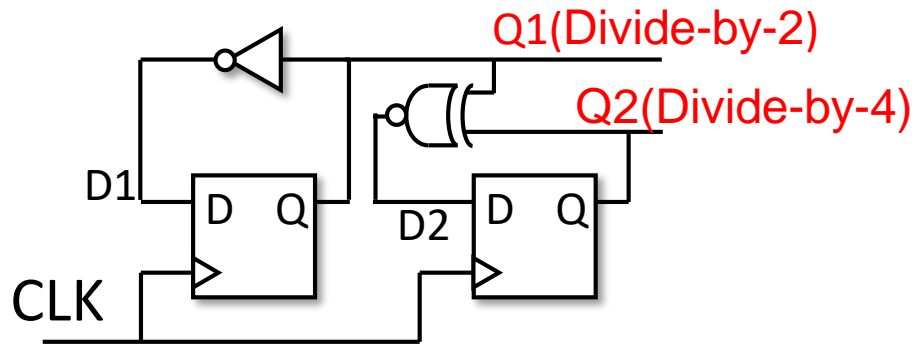
# PLL Diagram



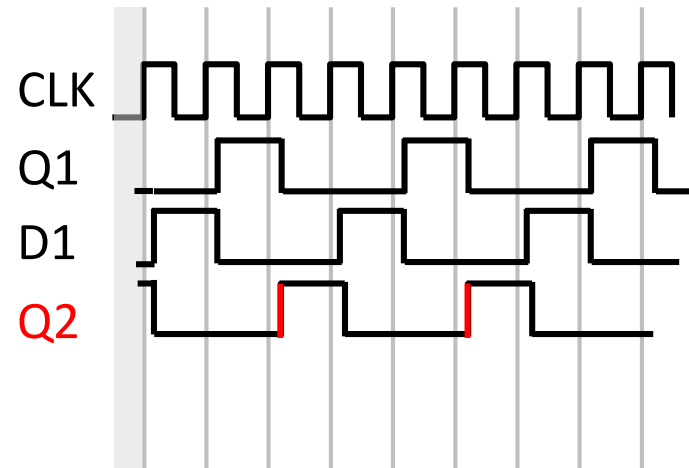
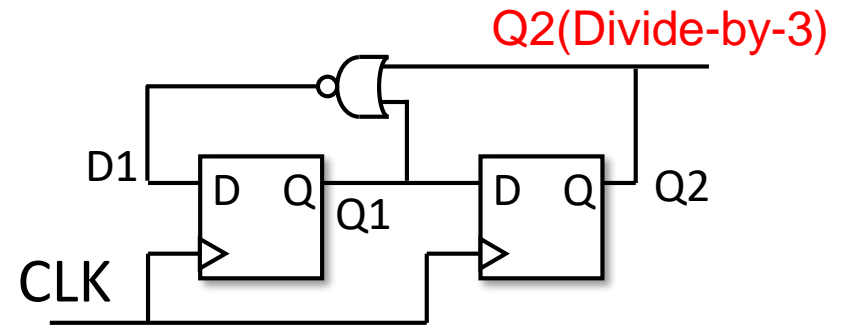
# Divider



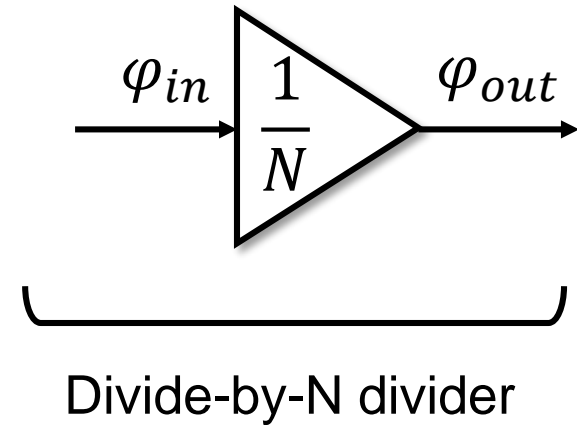
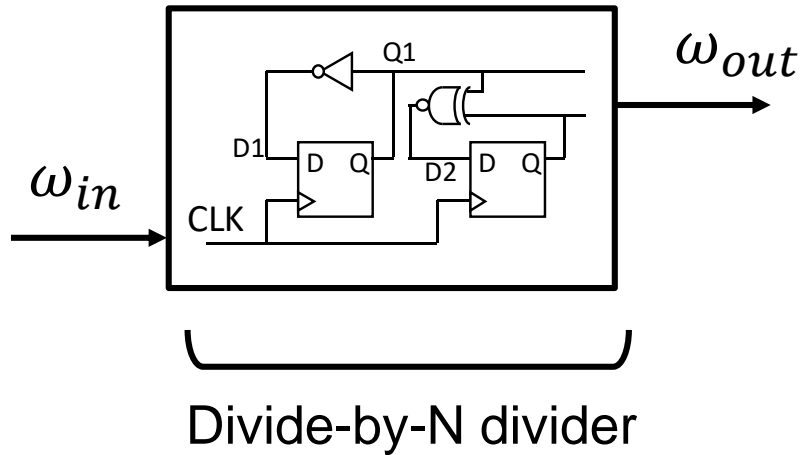
- Divide-by-2 and 4 divider



- Divide-by-3 divider



# Modeling of Divider



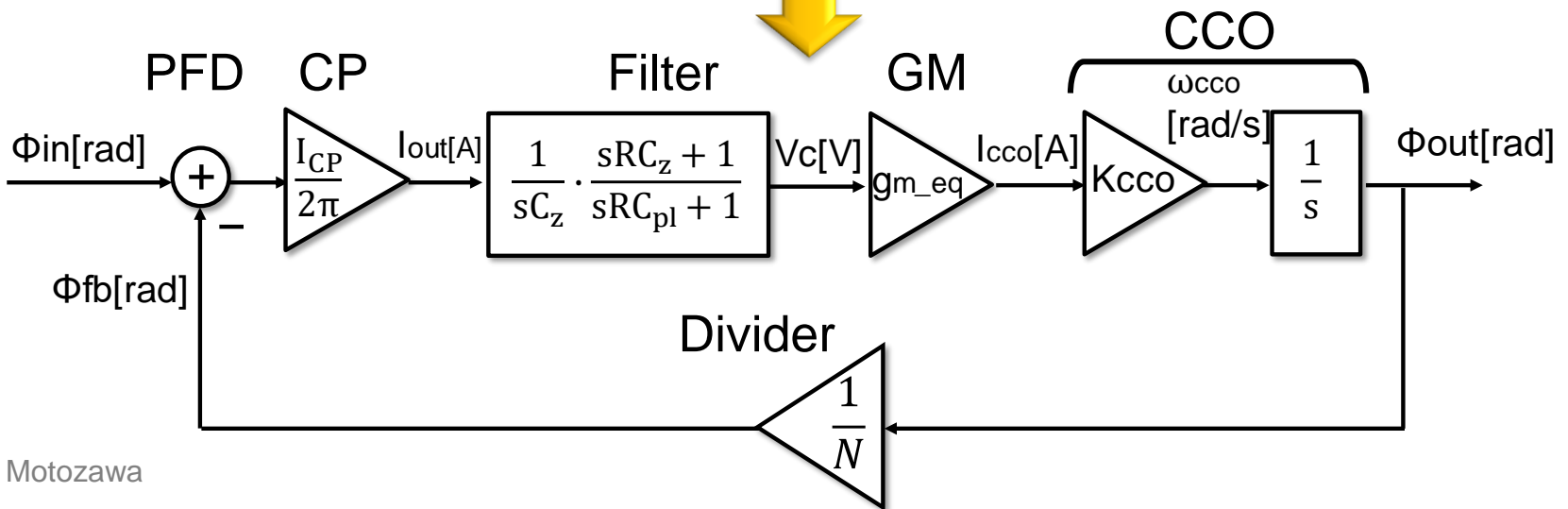
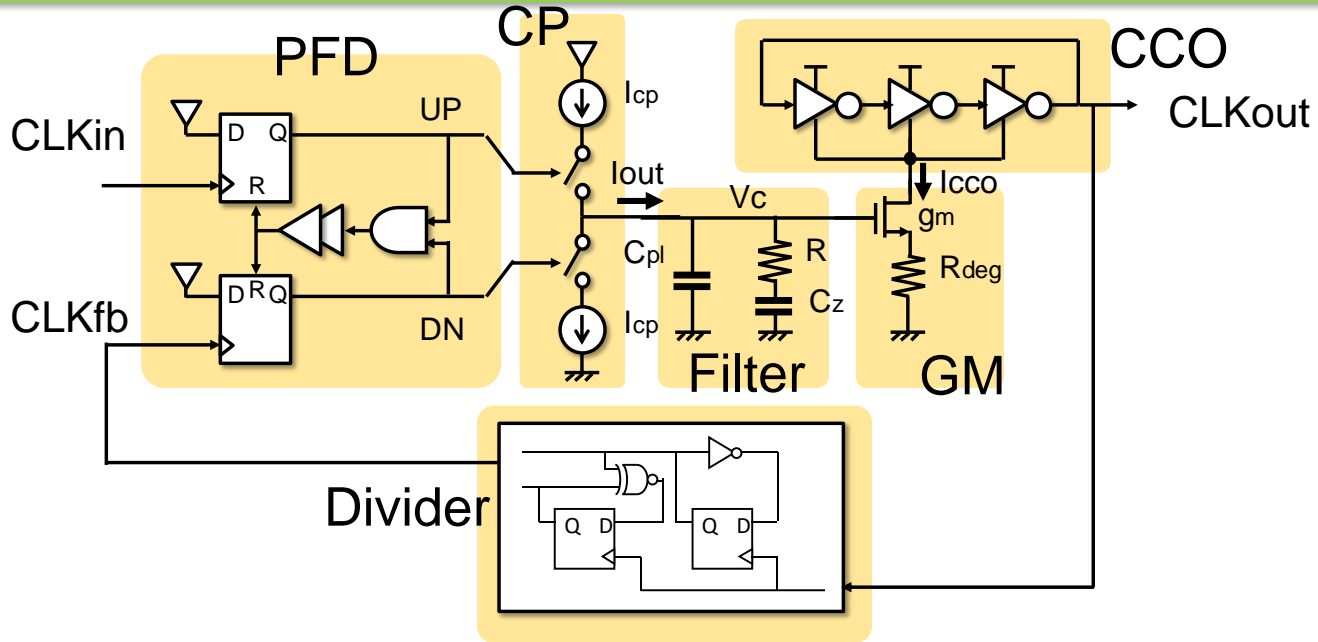
Frequency Domain

$$\omega_{out} = \frac{1}{N} \omega_{in} \quad [\text{rad/s}]$$

Phase Domain

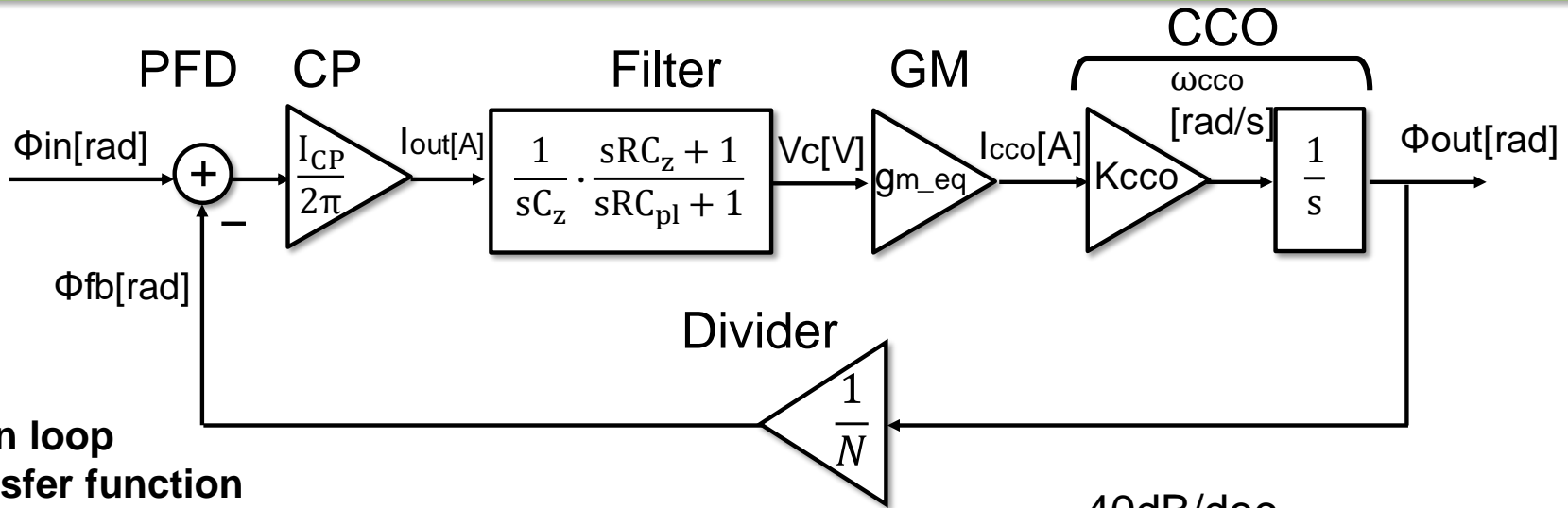
$$\phi_{out} = \frac{1}{N} \phi_{in} \quad [\text{rad}]$$

# Modeling of Single-Path PLL





# PLL transfer function and Bode Plot



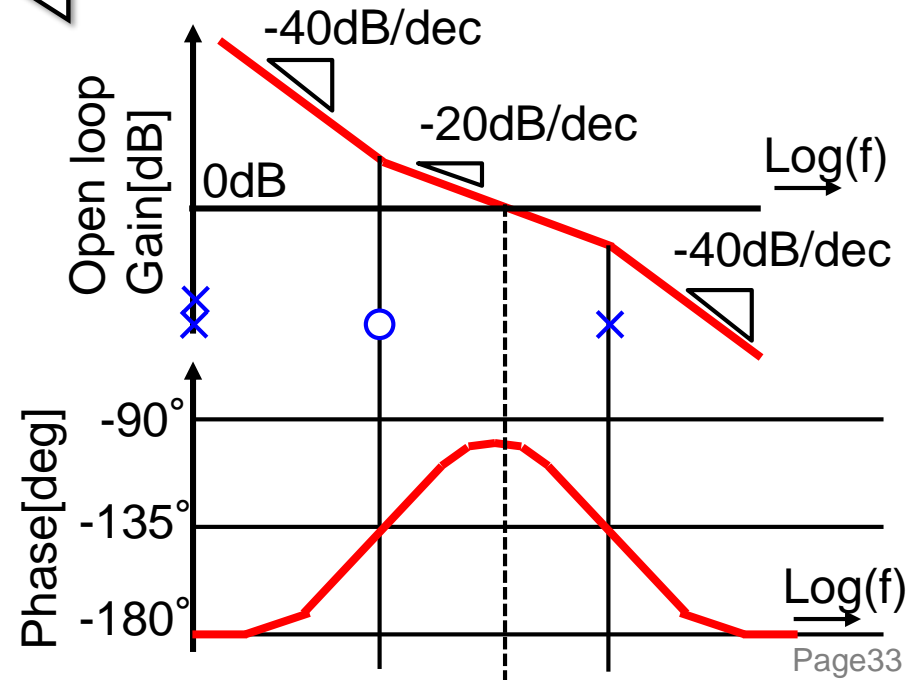
Open loop  
Transfer function

$$H_{op} = \frac{K_{CCO} I_{cp}}{2\pi N} \cdot \frac{1}{s^2} \cdot \frac{g_{m\_eq}}{C_z} \cdot \frac{sRC_z + 1}{sRC_{pl} + 1}$$

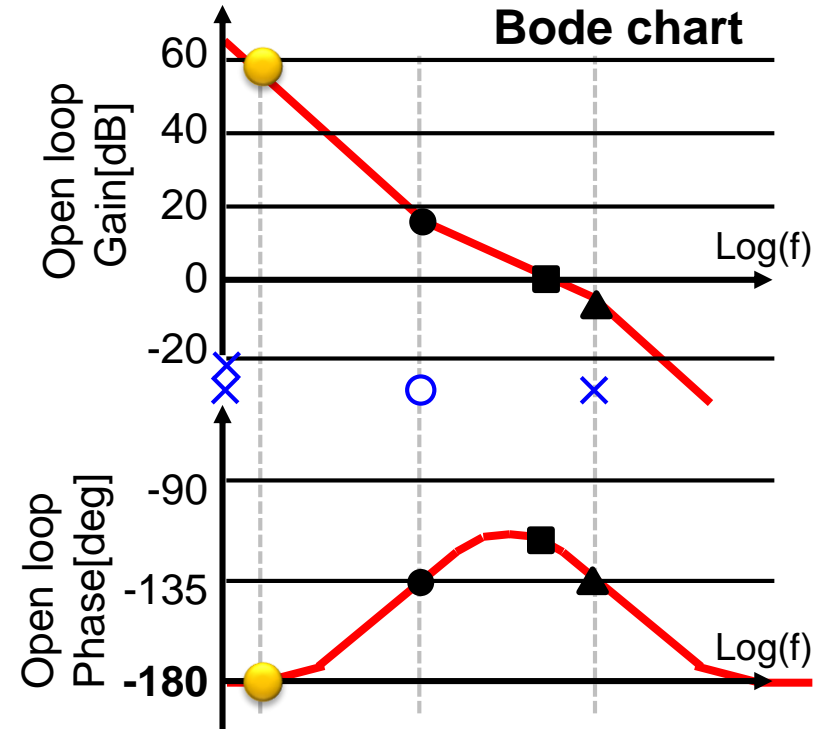
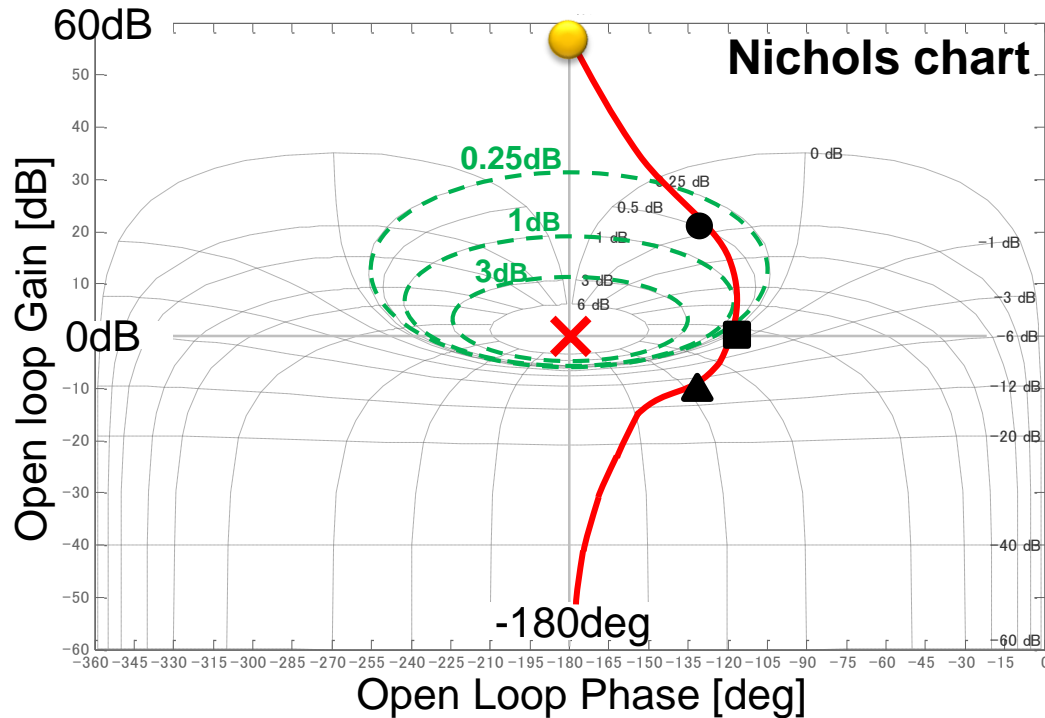
**Poles[Hz]**  $0, 0, \frac{1}{2\pi RC_{pl}}$

**Zero[Hz]**  $\frac{1}{2\pi RC_z}$

**Crossover freq.[Hz]**  $\approx \frac{K_{CCO} I_{cp} g_{m\_eq} R}{(2\pi)^2 N}$

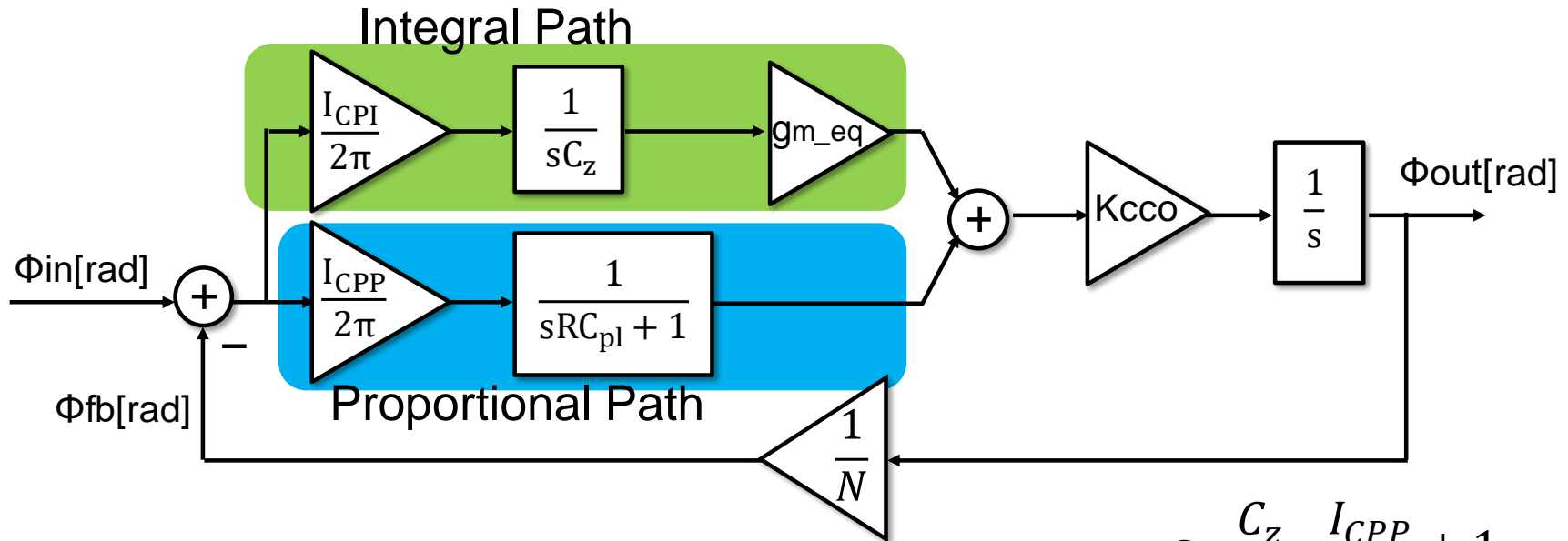


# PLL open loop line on Nichols Chart



- The X-axis: Open loop Phase  
The Y-axis: Open loop Gain  
**Dashed circles: Closed loop Gain**
- If the open loop line passes by the right side of the red cross(-180deg, 0dB), the system is stable.
- System is stable as long as the open loop gain is large enough

# Dual-Path PLL



Open loop

Transfer function

$$H_{op} = \frac{K_{CCO} I_{CPI}}{2\pi N} \cdot \frac{1}{s^2} \cdot \frac{g_{m\_eq}}{C_z} \cdot \frac{s \frac{C_z}{g_{m\_eq}} \frac{I_{CPP}}{I_{CPI}} + 1}{sRC_{pl} + 1}$$

**Poles[Hz]**  $0, 0, \frac{1}{2\pi RC_{pl}}$

**Crossover freq.[Hz]**  $\approx \frac{K_{CCO} I_{CPP}}{(2\pi)^2 N}$

**Zero[Hz]**  $\frac{1}{2\pi} \frac{g_{m\_eq} I_{CPI}}{C_z I_{CPP}}$

- Zero can be controlled by the ratio of I<sub>CPP</sub> and I<sub>CPI</sub>. That leads to smaller C<sub>z</sub>
- Single-path PLL: C<sub>z</sub>~100pF  
**Dual-path PLL : C<sub>z</sub>~20pF**



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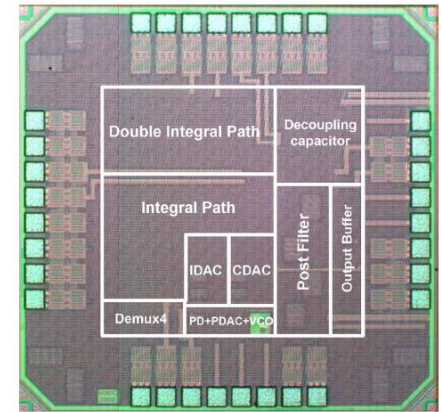
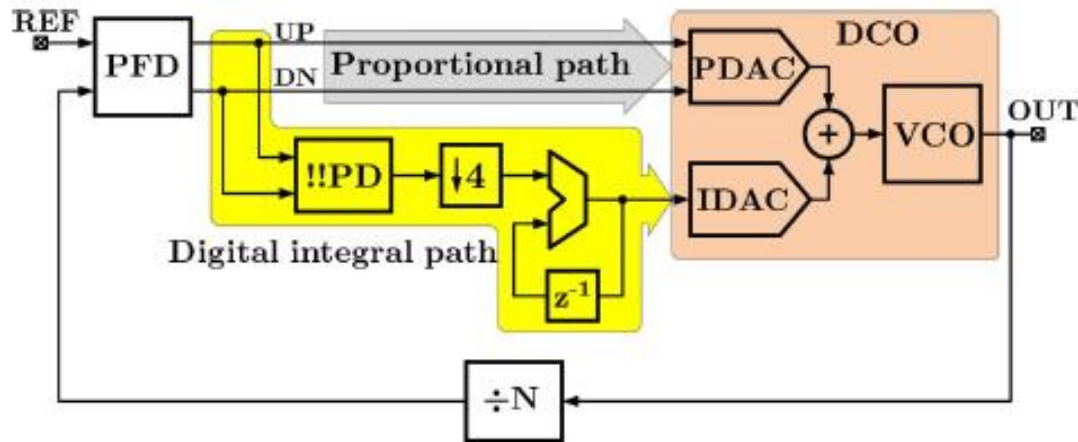
# Hybrid PLL



“A 0.7-to-3.5 GHz 0.6-to-2.8 mW

Highly Digital Phase-Locked Loop With Bandwidth Tracking”

Wenjing Yin, *et al.*, IEEE JSSC, VOL. 46, NO. 8, pp1870—1880, AUG. 2011



DPLL PERFORMANCE SUMMARY

Technology	90nm CMOS
Supply voltage	1V
Operating frequency	0.7GHz-3.5GHz
Random jitter @ 2.5GHz	1.6ps r.m.s
Jitter from integrated phase noise	0.9ps r.m.s
Peak-to-peak jitter @ 2.5GHz	11.6ps
Reference spur	-50.1dBc
Deterministic jitter from reference spur	0.83ps
Loop bandwidth @ 2.5GHz	16MHz
Power @ 2.5GHz	1.6mW
Die area	0.36mm <sup>2</sup>

- Analog-Digital Hybrid
  - ✓ Small & programmable
  - ✓ Analog proportional path to reduce quantization error
- !!PD instead of TDC
  - ✓ Simple, Small, and Low power
  - ✓ Intrinsically nonlinear → Jitter makes it linear



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- PLLs are utilized in many ICs
  - ✓ One IC contains several identical PLLs to provide different frequency clocks while reducing I/O pins and avoiding the reflection
- Many PLL applications
  - ✓ Not only frequency multiplication
  - ✓ SSC to reduce EMI noise
  - ✓ CDR system to generate from incoming data
  - ✓ Deskew PLL to decrease phase error among clocks
- Building blocks and transfer functions are discussed
  - ✓ Several domains in PLL loop
  - ✓ Dual-path PLL is used to reduce capacitor
- Analog-digital hybrid PLL with !!PD is introduced
  - ✓ The keywords, digital-rich and !!PD , are important for an advanced PLL design