1st IEEE International Workshop on Automotive Reliability & Test
ART Workshop

Redundant SAR ADC Algorithms for Reliability Based on Number Theory

Y. Kobayashi, T. Arafune , S. Shibuya
H. Kobayashi, H. Arai

Kobayashi Laboratory

Gunma University

群馬大学
GUNMA UNIVERSITY

Nov. 17-18, 2016

Outline

- Objective
- SAR ADC
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Fibonacci Sequence and Golden Ratio
  - Fibonacci Weighted SAR ADC
  - DAC Settling Time
- Realization of Fibonacci DAC
- Conclusion

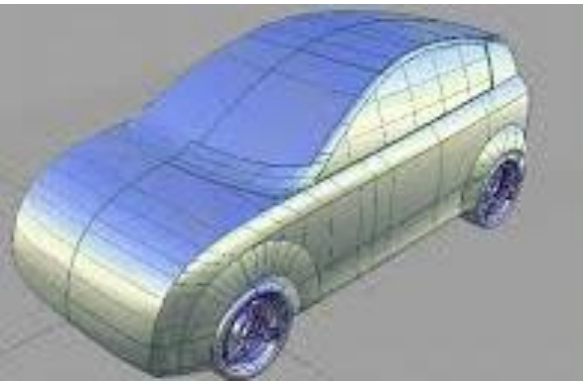
Outline

- Objective
- SAR ADC
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Fibonacci Sequence and Golden Ratio
  - Fibonacci Weighted SAR ADC
  - DAC Settling Time
- Realization of Fibonacci DAC
- Conclusion

Presentation Objective

We show here
redundancy design example for reliability.

We hope that this stimulates
automotive reliability & test engineers



Research Objective

Objective

- **Development of**
  Reliable & High-speed SAR ADC

Our Approach

- **Redundancy search algorithm design with Number Theory**

Golden ratio ← Today's talk

Silver ratio

SAR ADC : Successive Approximation Register ADC

Outline

- Objective
- SAR ADC
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Fibonacci Sequence and Golden Ratio
  - Fibonacci Weighted SAR ADC
  - DAC Settling Time
- Realization of Fibonacci DAC
- Conclusion

Research Background

Automotive Electronics are in spotlight

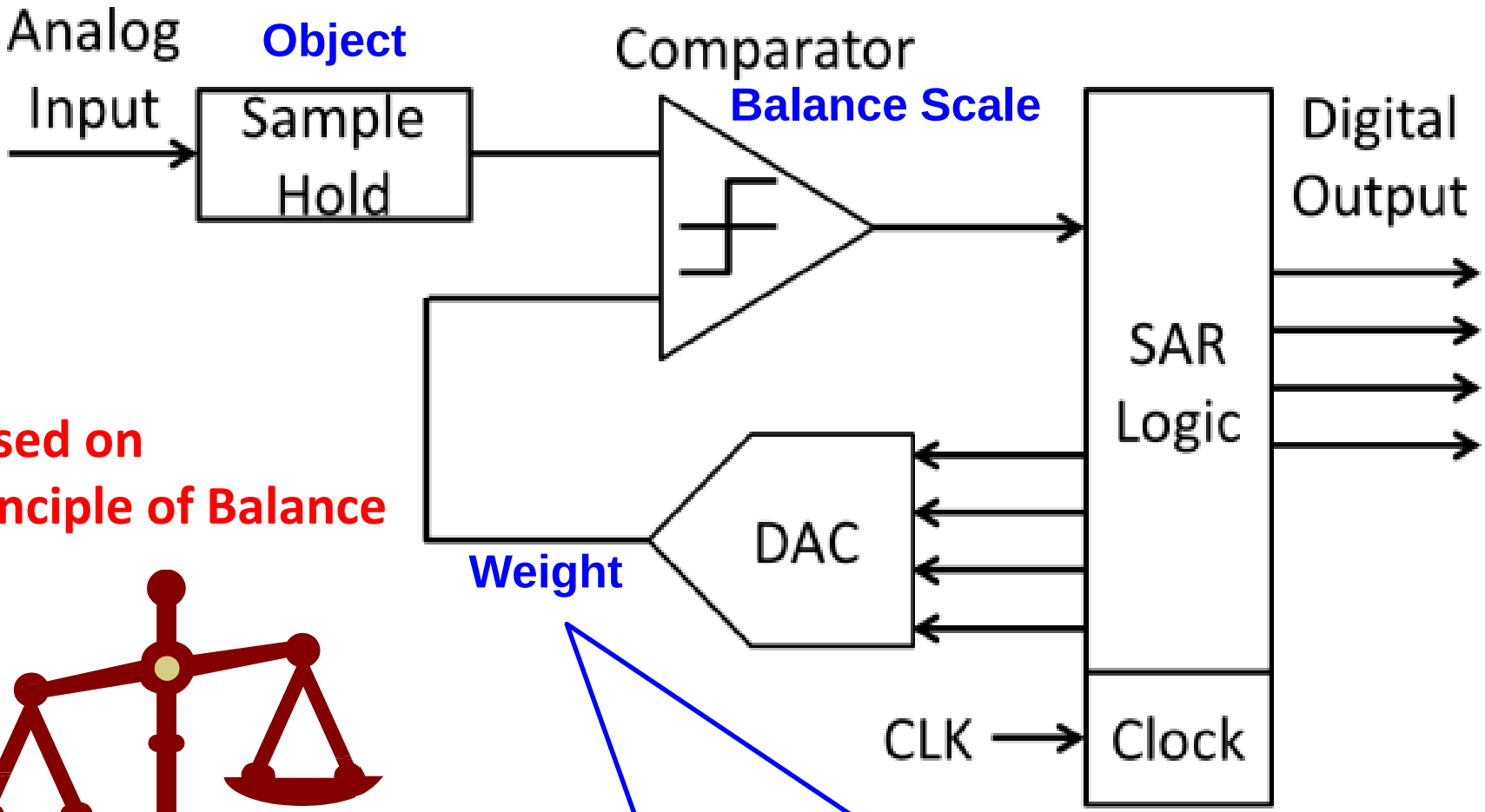
High-speed, Reliable

“SAR ADC” in microcontroller is needed

Redundancy design for error correction

Design issues

SAR ADC Configuration



Based on Principle of Balance

Generally use binary weight

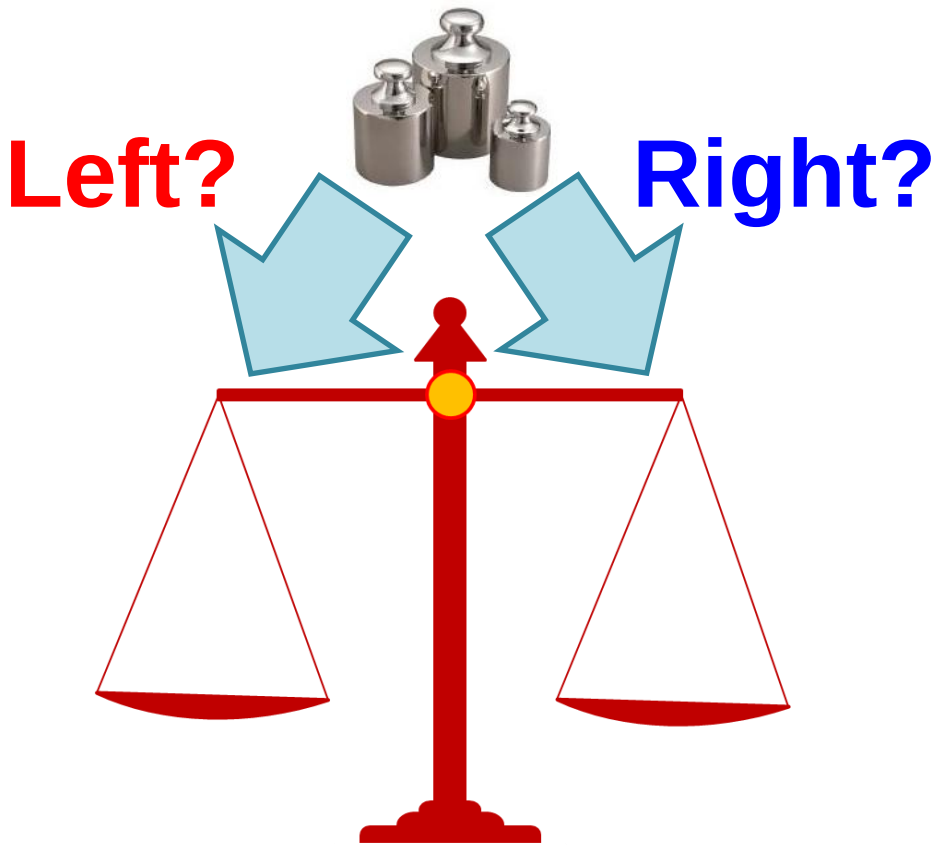
(1 , 2 , 4 , 8 , 16 , 32, 64 …)

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input : 7.3 V
- Binary weight :

16, 8, 4, 2, 1



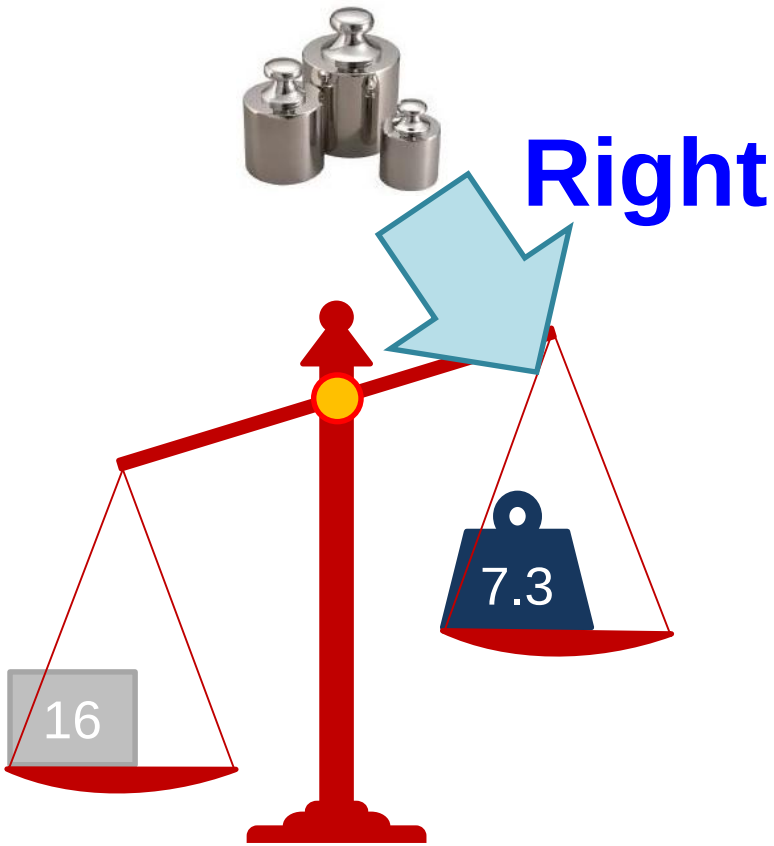
Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
Level	31						31
	30						30
	29						29
	28						28
	27						27
	26						26
	25						25
	24						24
	23						23
	22						22
	21						21
	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input : 7.3 V
- Binary weight :

8, 4, 2, 1



Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
Level	31						31
	30						30
	29						29
	28						28
	27						27
	26						26
	25						25
	24						24
	23						23
	22						22
	21						21
	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

Down!

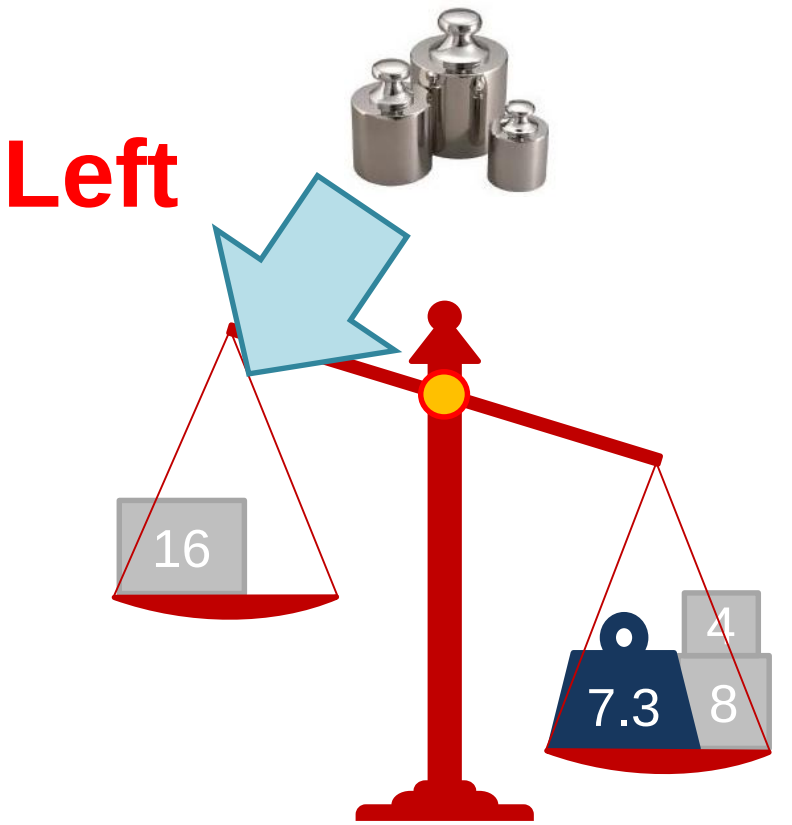
0

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input : 7.3 V
- Binary weight :

2, 1



Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
Level	31						31
	30						30
	29						29
	28						28
	27						27
	26						26
	25						25
	24						24
	23						23
	22						22
	21						21
	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

UP!

0 0 1

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input : 7.3 V
- Binary weight :

7.3⇒00111⇒7

$16 - 8 - 4 + 2 + 1 + 0.5 - 0.5 = 7$

Step	1st	2nd	3rd	4th	5th	output
Weight p(k)	16	8	4	2	1	
Level 31						31
30						30
29						29
28						28
27						27
26						26
25						25
24						24
23						23
22						22
21						21
20						20
19						19
18						18
17						17
16						16
15						15
14						14
13						13
12						12
11						11
10						10
9						9
8						8
7						7
6						6
5						5
4						4
3	0	0	1	1	1	3
2						2
1						1
0						0

Outline

- Objective
- SAR ADC
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Fibonacci Sequence and Golden Ratio
  - Fibonacci Weighted SAR ADC
  - DAC Settling Time
- Realization of Fibonacci DAC
- Conclusion

SAR ADC Redundancy Design

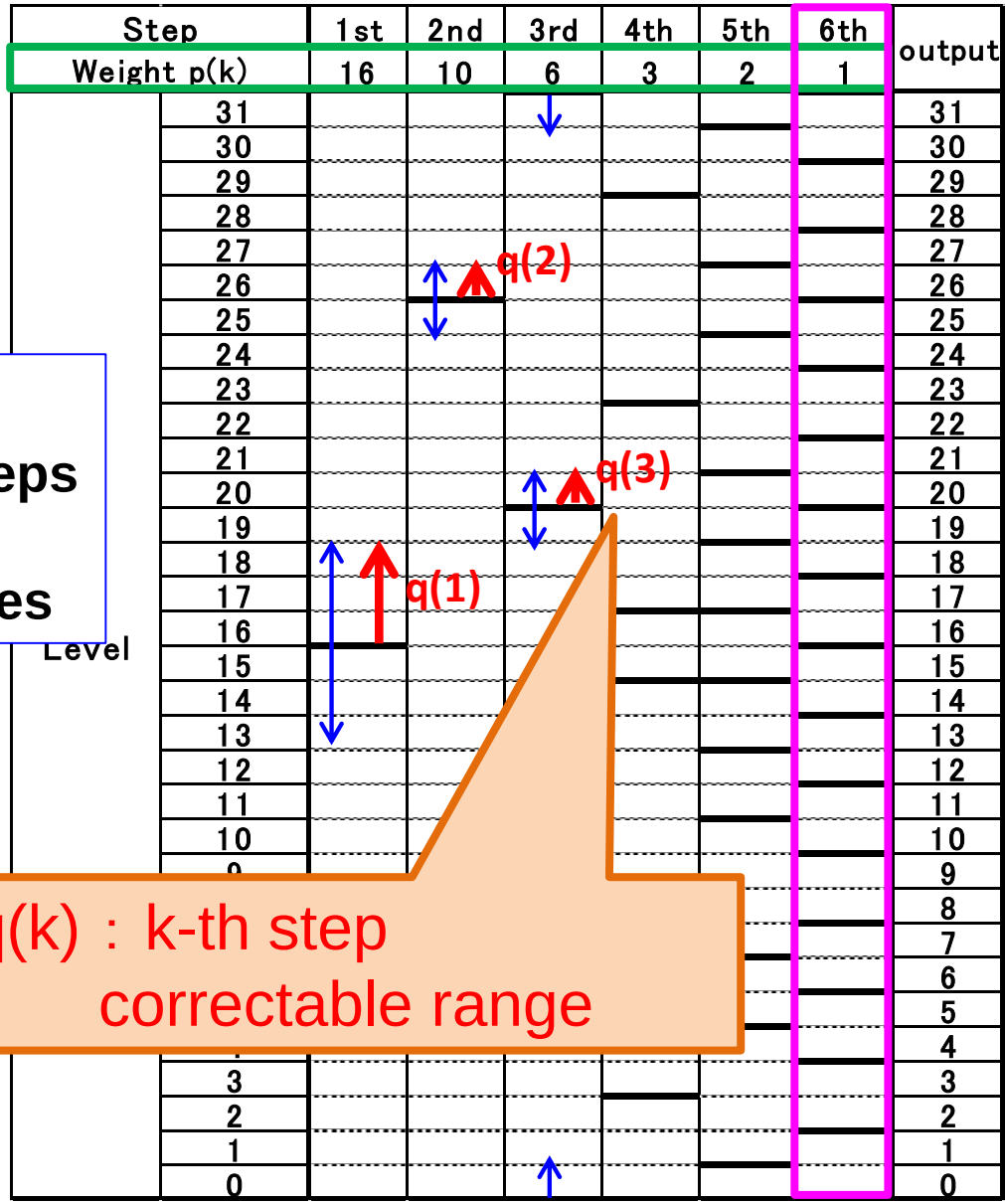
Redundancy

- Surplus, Extra

Using time redundancy

- Increase Extra comparison steps
- Change reference to Non-binary voltages

Enable digital error correction!



Redundancy Design Operation(No Error)

5bit-6step SAR ADC

- Analog input : 6.3
- Redundant weight :

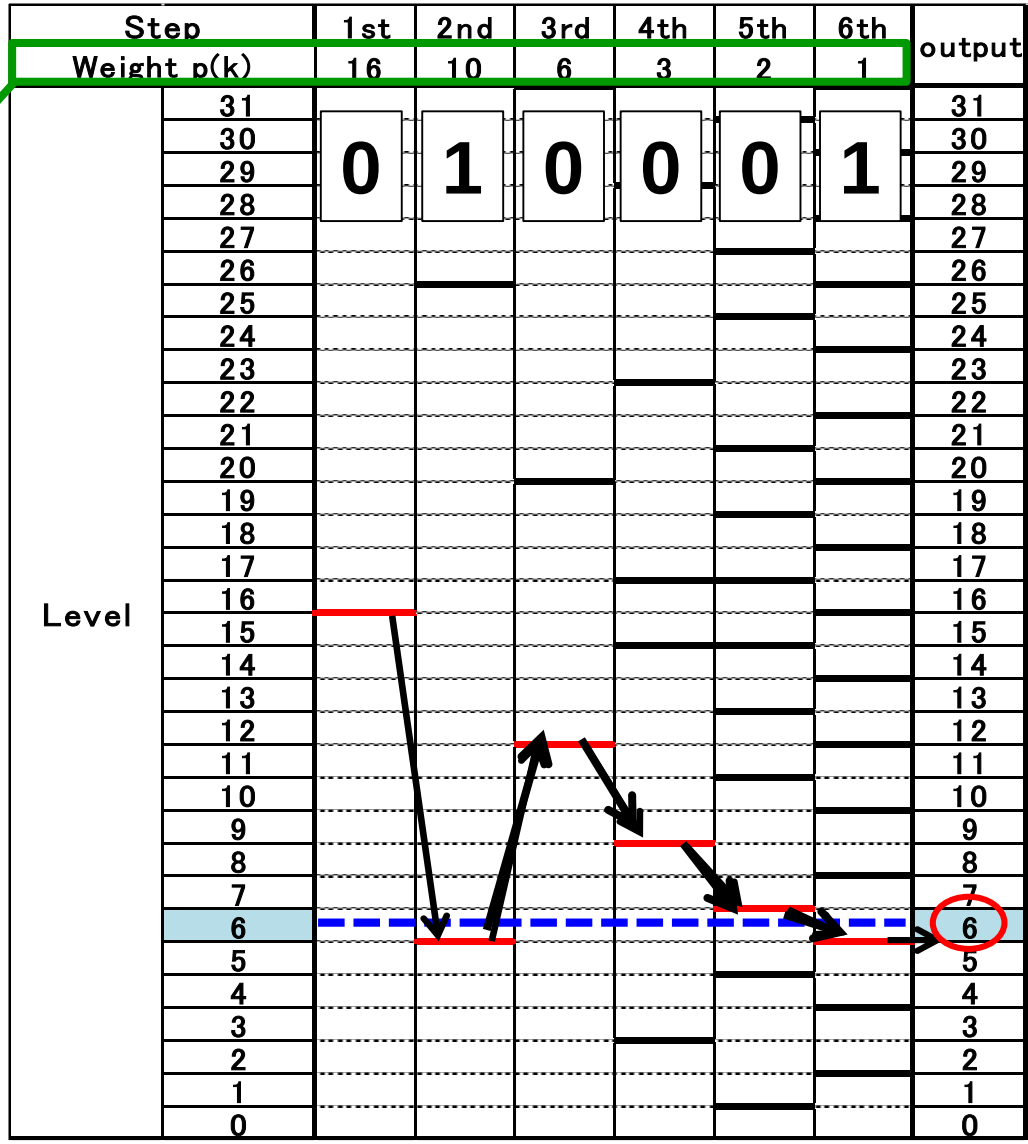
  16, 10, 6, 3, 2, 1

Correctable expression

6.3⇒010001⇒6

$$16 - 10 + 6 - 3 - 2 - 1 + 0.5 - 0.5$$

=6



Redundancy Design Operation(One Error)

5bit-6step SAR ADC

- Analog input : 6.3
- Redundant weight :
  16, 10, 6, 3, 2, 1

One expression

6.3⇒010001⇒6

Another expression

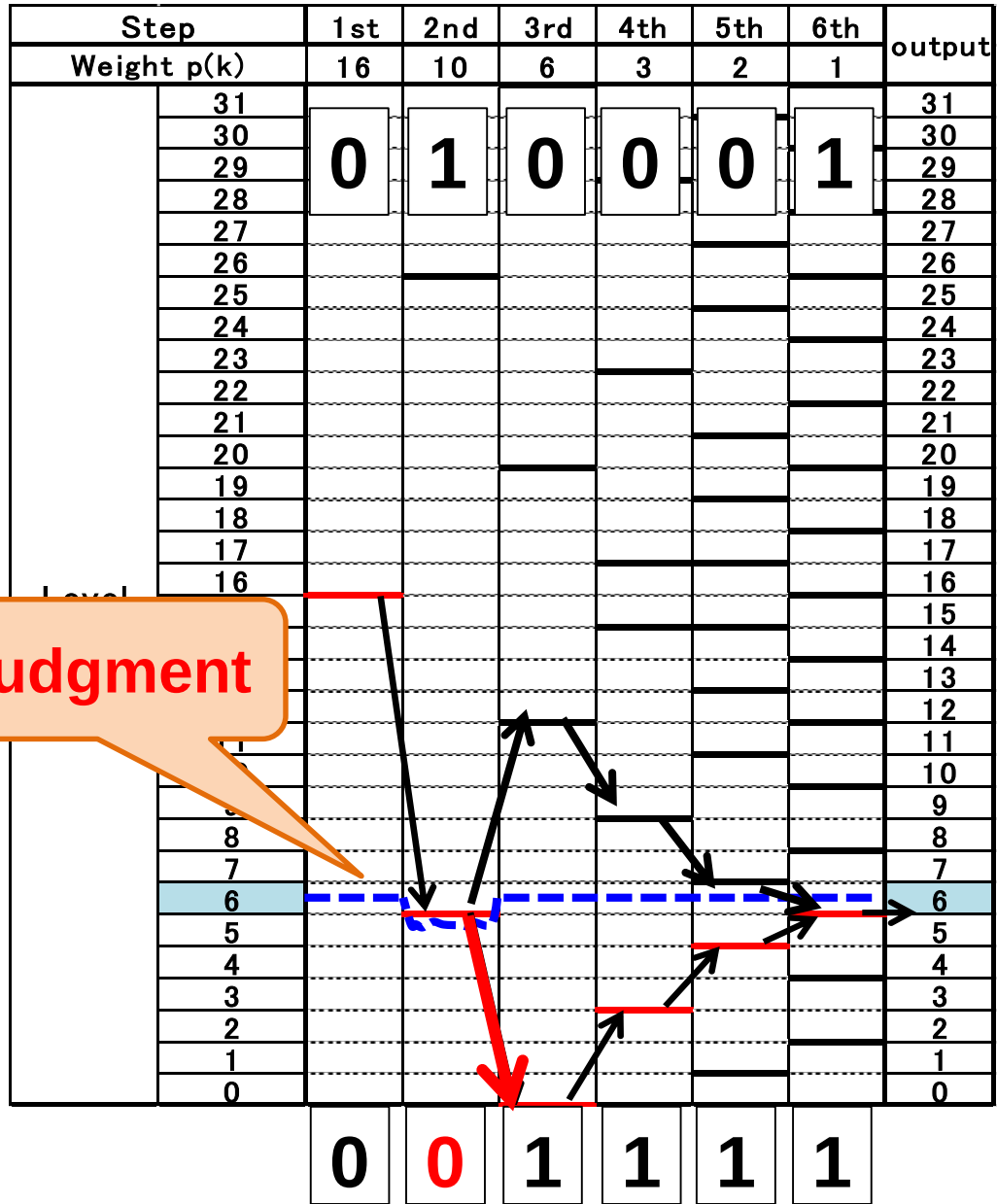
6.3⇒001111⇒6

$16 - 10 - 6 + 3 + 2 + 1 + 0.5 - 0.5$

$= 6$

Error correction

High-Reliability



Issues of Conventional Method

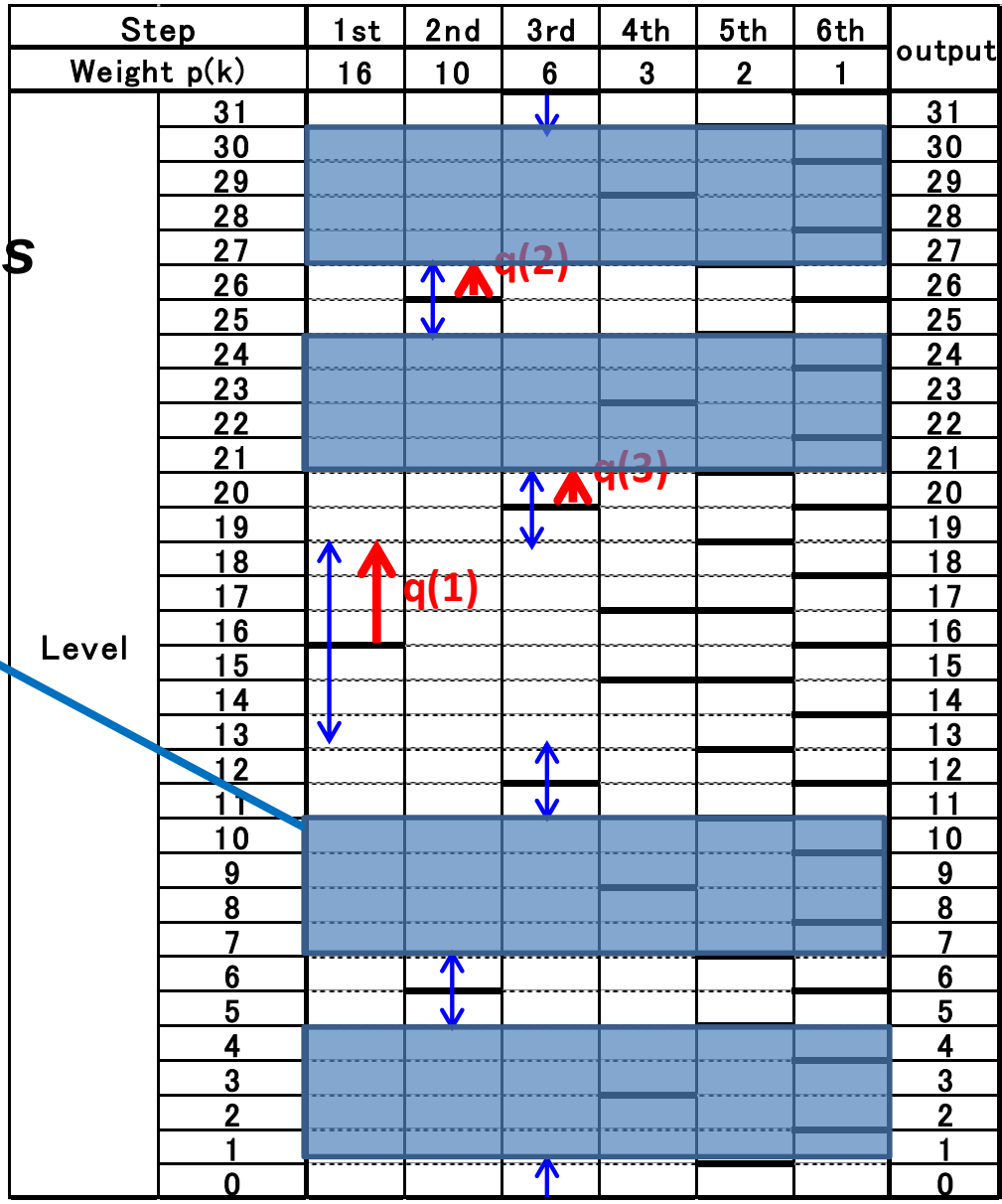
Reference Voltage Selection

1. ***Difficult to select proper reference voltages***
2. ***q(k) must be fraction***

Uncorrectable Range

Not effective redundancy design

Good radix selection method is needed !



Outline

- Objective
- SAR ADC
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - ➢Fibonacci Sequence and Golden Ratio
  - ➢Fibonacci Weighted SAR ADC
  - ➢DAC Settling Time
- Realization of Fibonacci DAC
- Conclusion

Outline

- Objective
- SAR ADC
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - ➢ Fibonacci Sequence and Golden Ratio
  - ➢ Fibonacci Weighted SAR ADC
  - ➢ DAC Settling Time
- Realization of Fibonacci DAC
- Conclusion

Fibonacci Sequence

Fibonacci Definition

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1} \qquad \text{(n=0,1,2…)}$$

Example of Fibonacci number

$$0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55 \ldots$$

Leonardo Fibonacci
(Italy:1170-1250)

Property

The closest terms ratio : ***"Golden Ratio"***

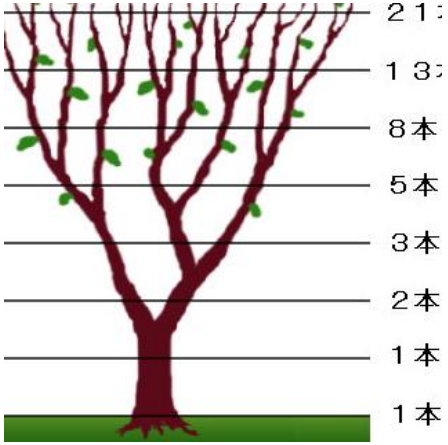
(about 1.62)

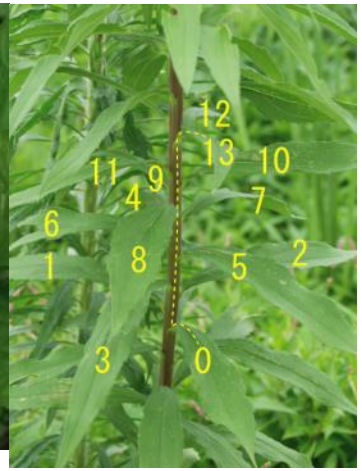
$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895$$

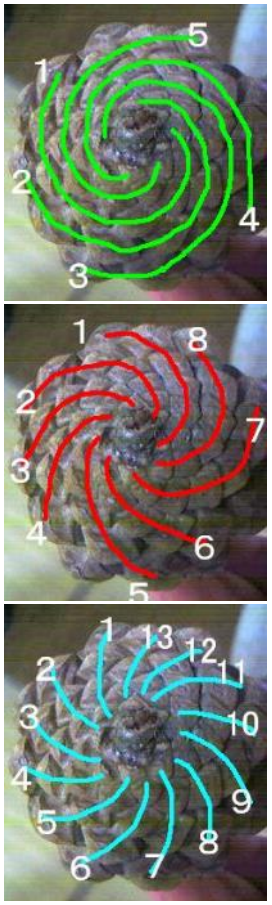
Fibonacci Numbers

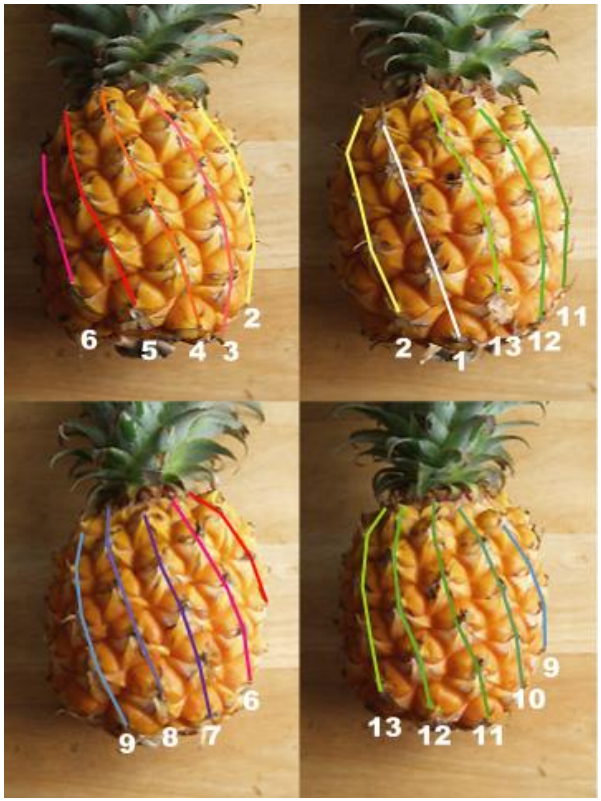
0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144…

We can see Fibonacci numbers in nature, especially in plants.





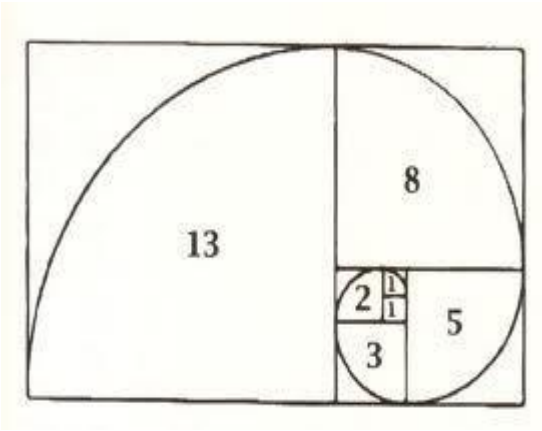


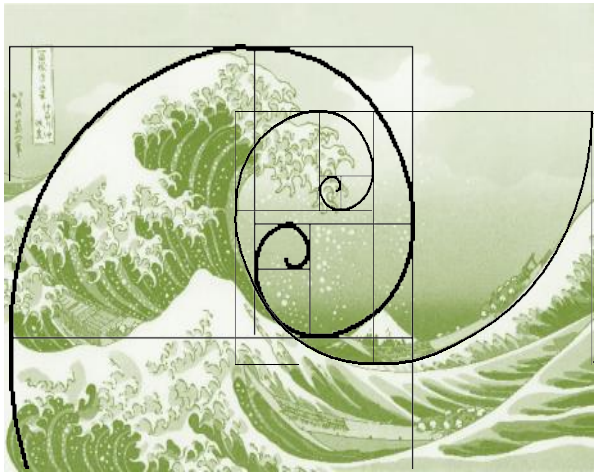


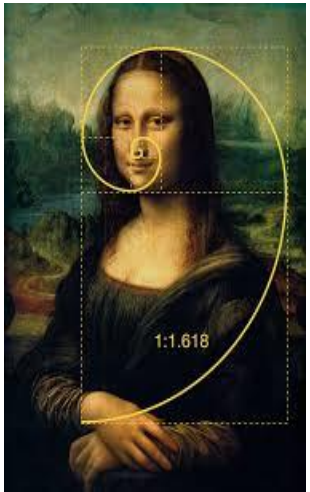
Golden Ratio

Golden Ratio : $\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.618033988749895 = \varphi$

The most beautiful ratio





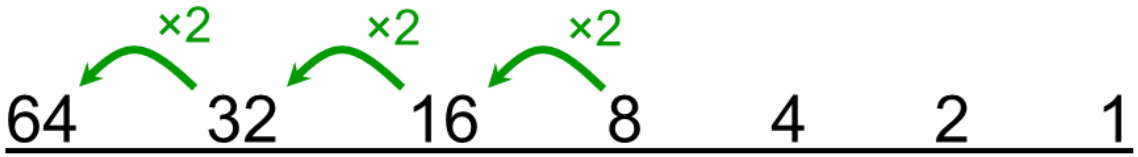


Outline

- Objective
- SAR ADC
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Fibonacci Sequence and Golden Ratio
  - Fibonacci Weighted SAR ADC
  - DAC Settling Time
- Realization of Fibonacci DAC
- Conclusion

Use of Fibonacci Sequence

Use of **Binary**

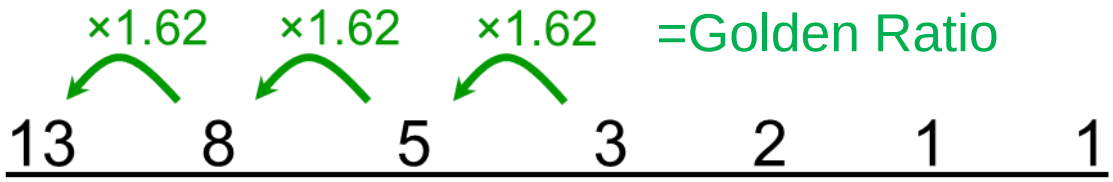


Binary Weighted (Radix=2)

Radix：Decision weighted number

Change weighted

Use of **Fibonacci**



Fibonacci Weighted (Radix=1.62)

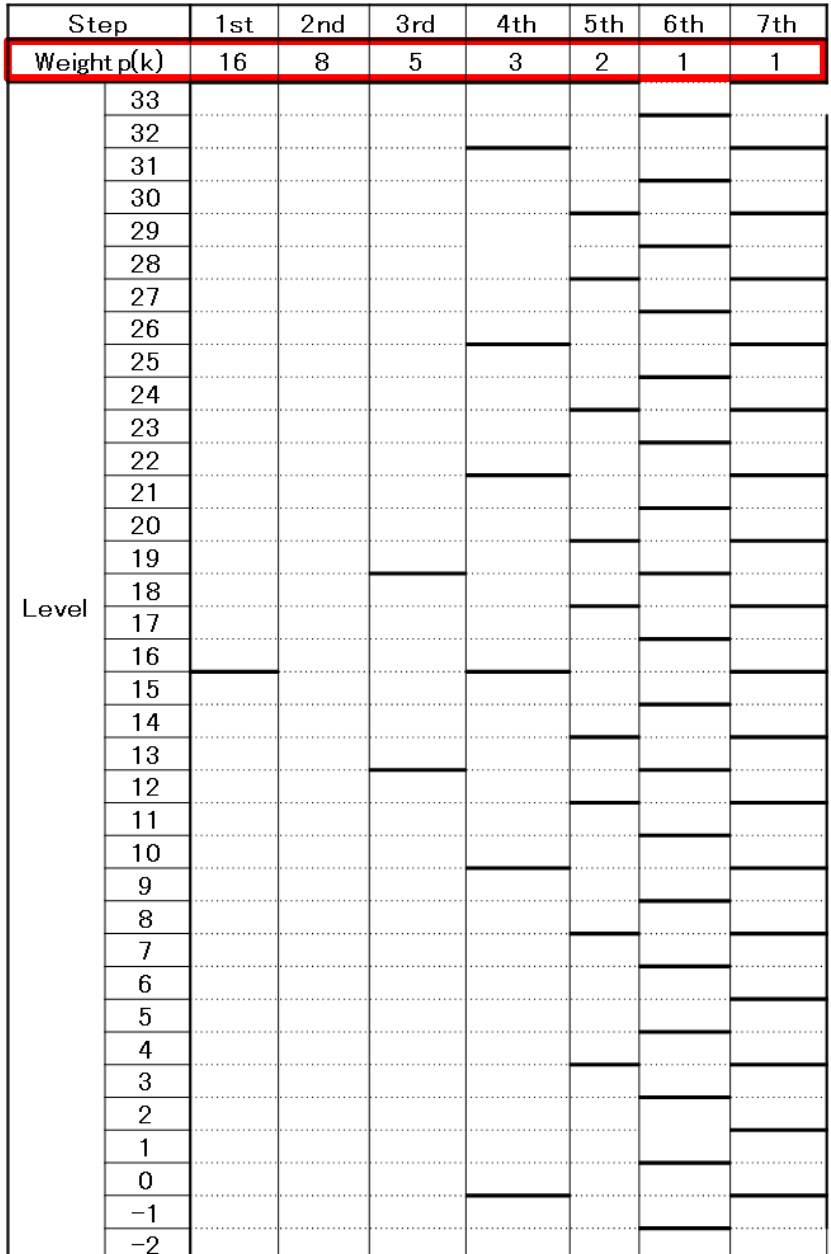
Realize 1.62 weighted by using only integer

Correction of Fibonacci Redundancy Design

Fibonacci sequence SAR ADC

Found out properties of two points !

1. ***Correctable range q(k) is always Fibonacci number*** F_{M-k-1}.
2. ***q(k) is exactly in contact q(k+1) without overlap.***

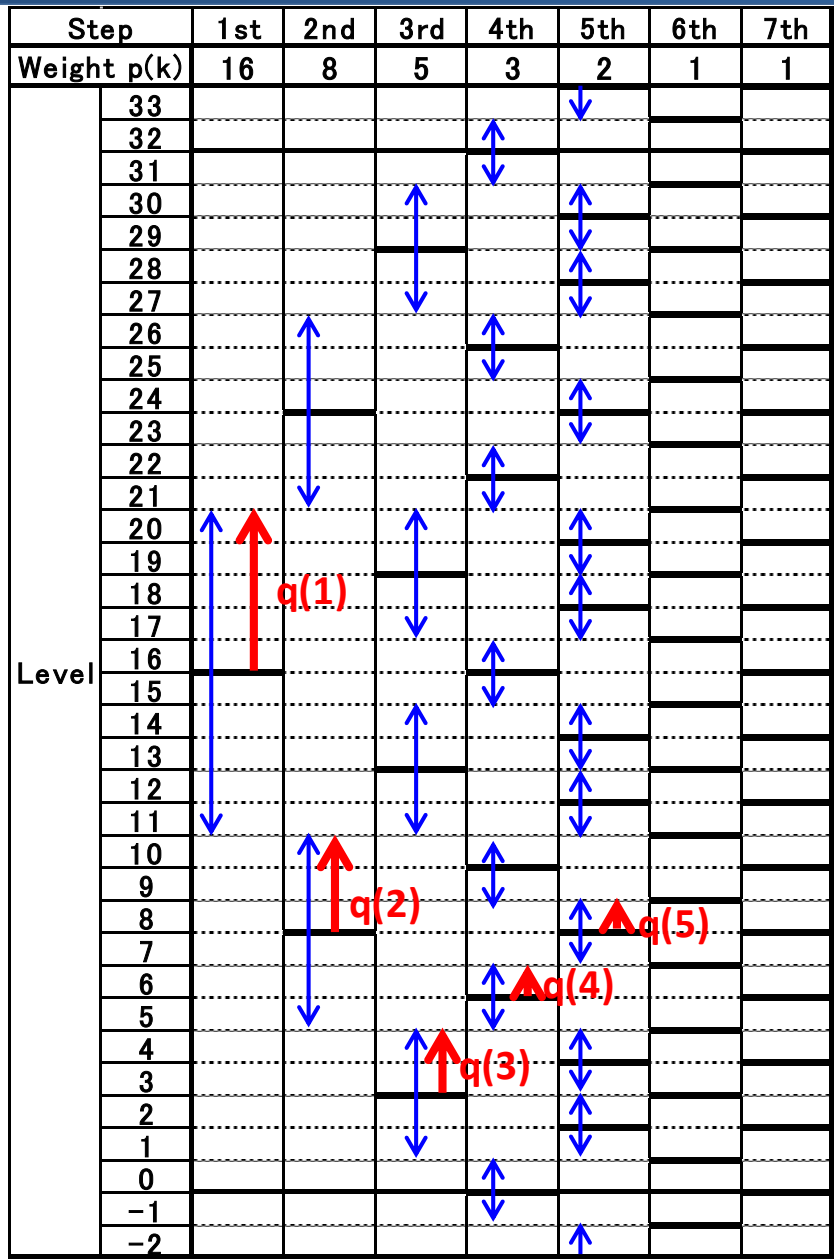


Correction of Fibonacci Redundancy Design

Fibonacci sequence SAR ADC

Found out properties of two points !

1. ***Correctable range q(k) is always Fibonacci number*** F_{M-k-1}.
2. *q(k) is exactly in contact q(k+1) without overlap.*

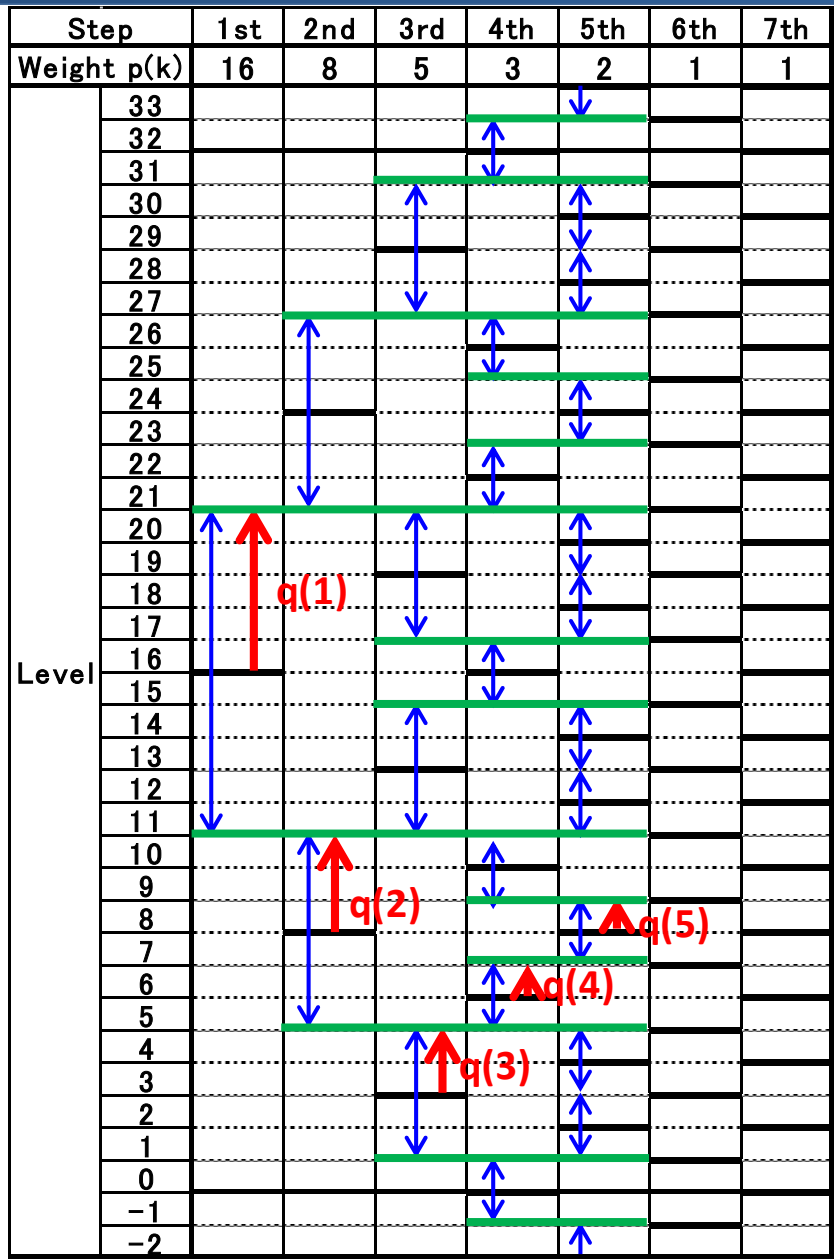


Correction of Fibonacci Redundancy Design

Fibonacci sequence SAR ADC

Found out properties of two points !

1. *Correctable range q(k) is always Fibonacci number* F_{M-k-1}.
2. ***q(k) is exactly in contact q(k+1) without overlap.***



Correction of Fibonacci Redundancy Design

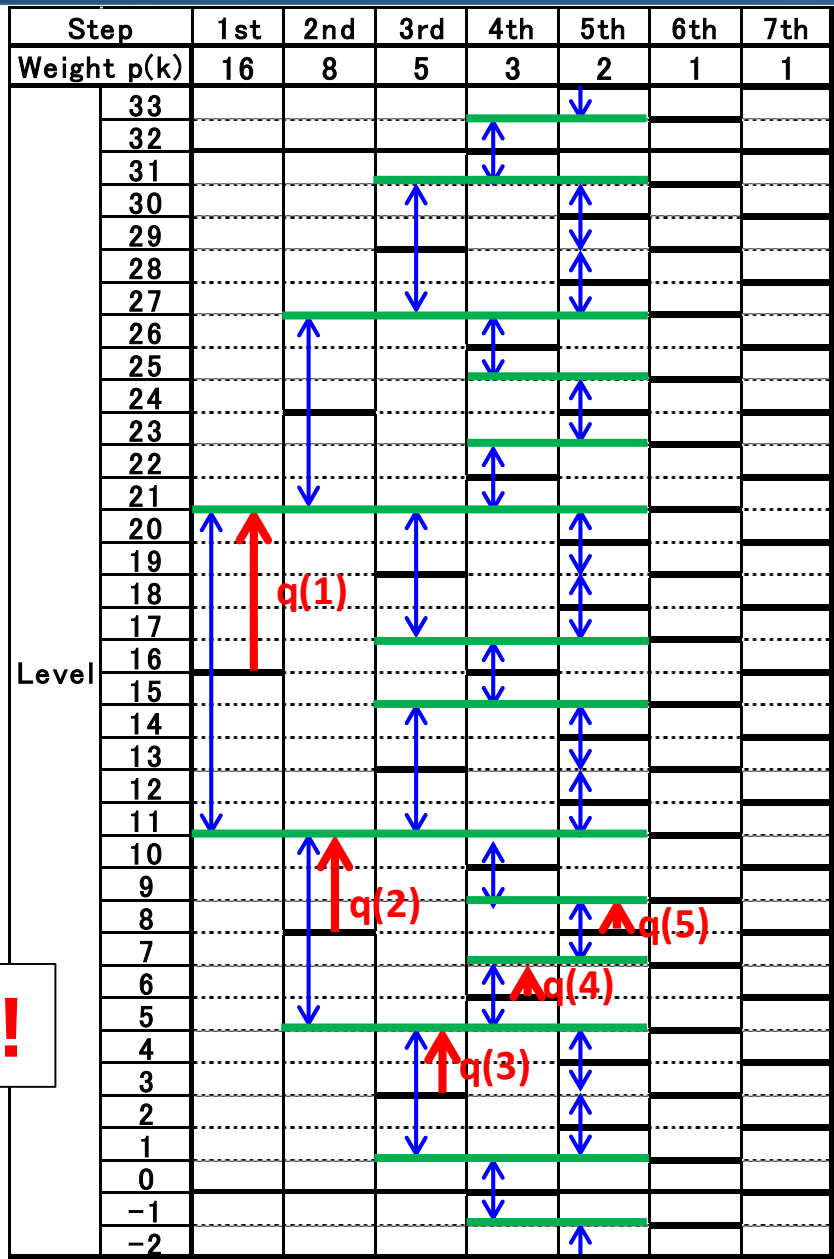
Fibonacci sequence SAR ADC

Found out properties of two points !

1. ***Correctable range q(k) is always Fibonacci number*** F_{M-k-1}.
2. ***q(k) is exactly in contact q(k+1) without overlap.***

Golden ratio covers wide input range by minimum extra comparison steps.

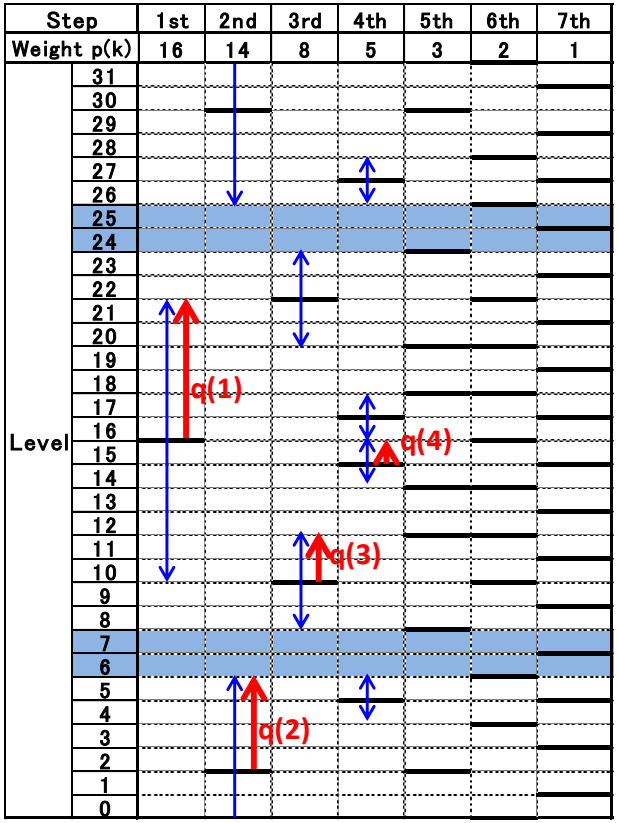
The most efficient design !

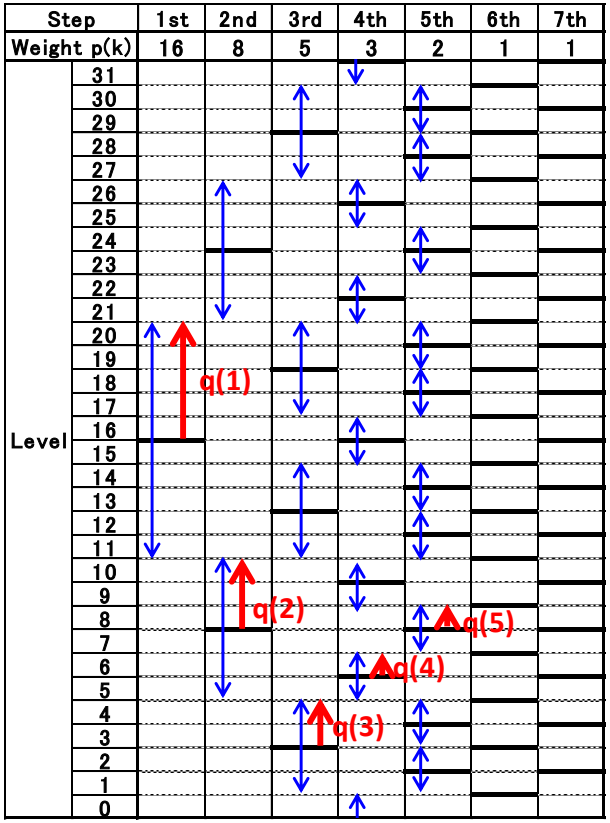


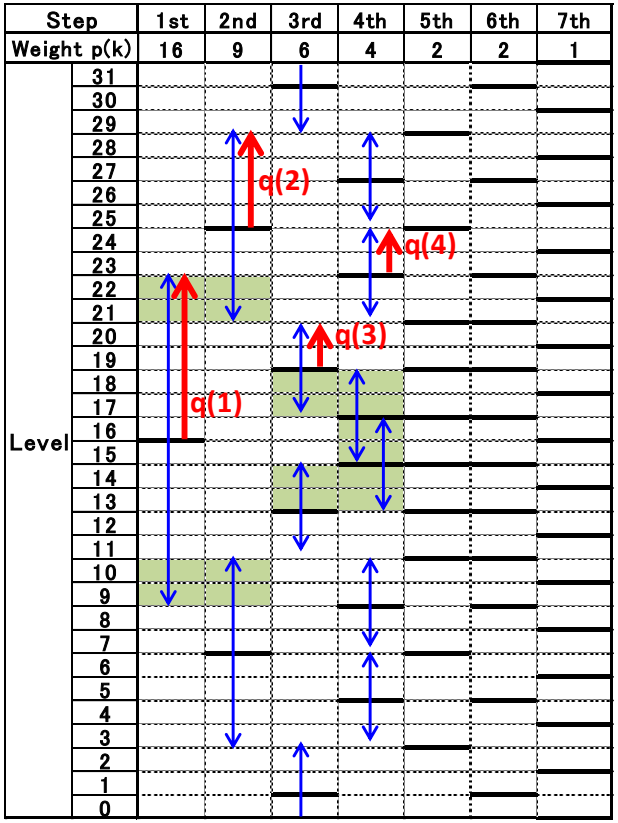
Comparison with Other Radix Methods

5bit SAR ADC

Conventional method	Proposed method	Conventional method
Radix=**1.7**	**1.62**	**1.55**
Radix is **bigger** than 1.62	**Standard !**	Radix is **smaller** than 1.62
⇨ **separated**		⇨ **overlapped**







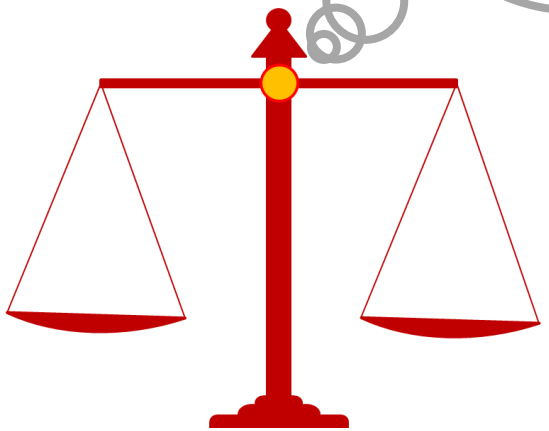
Outline

- Objective
- SAR ADC
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Fibonacci Sequence and Golden Ratio
  - Fibonacci Weighted SAR ADC
  - DAC Settling Time
- Realization of Fibonacci DAC
- Conclusion

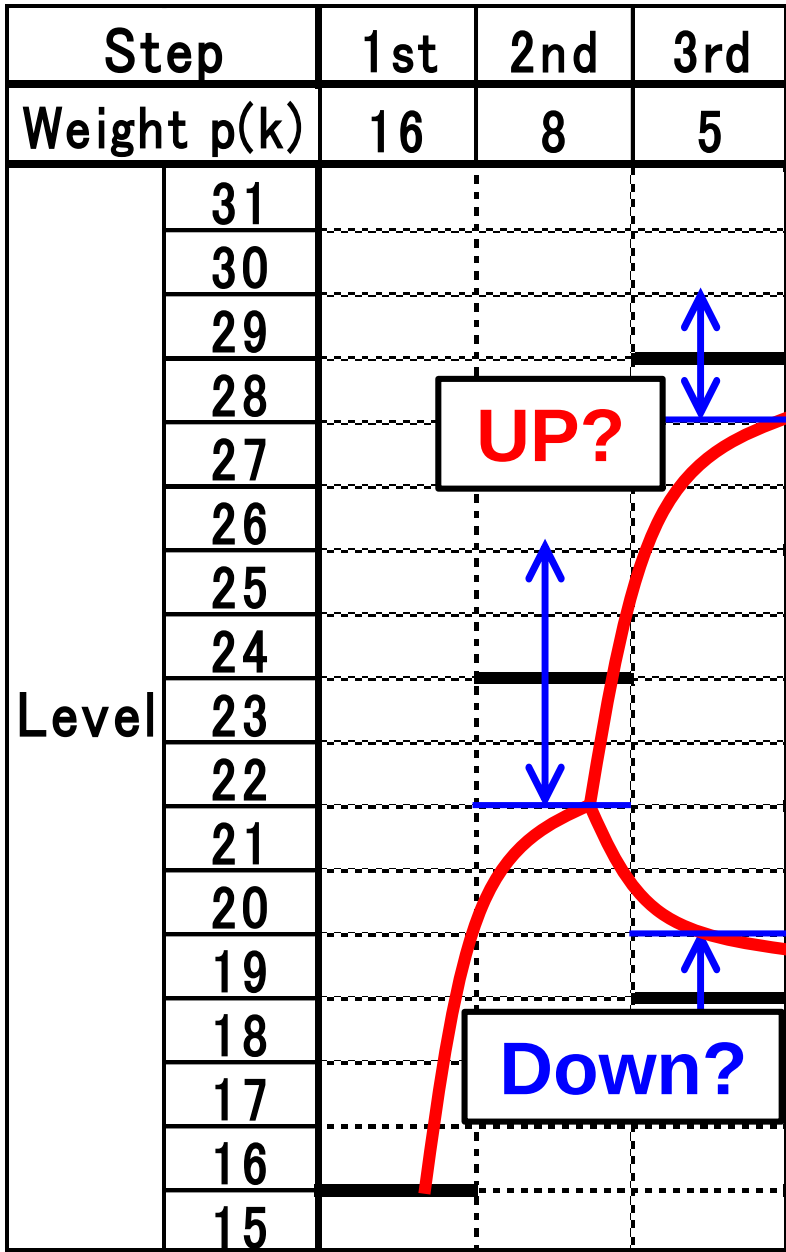
Internal DAC Output Settling Time

Settling Time

Transition time from k-th step voltage to next step voltage

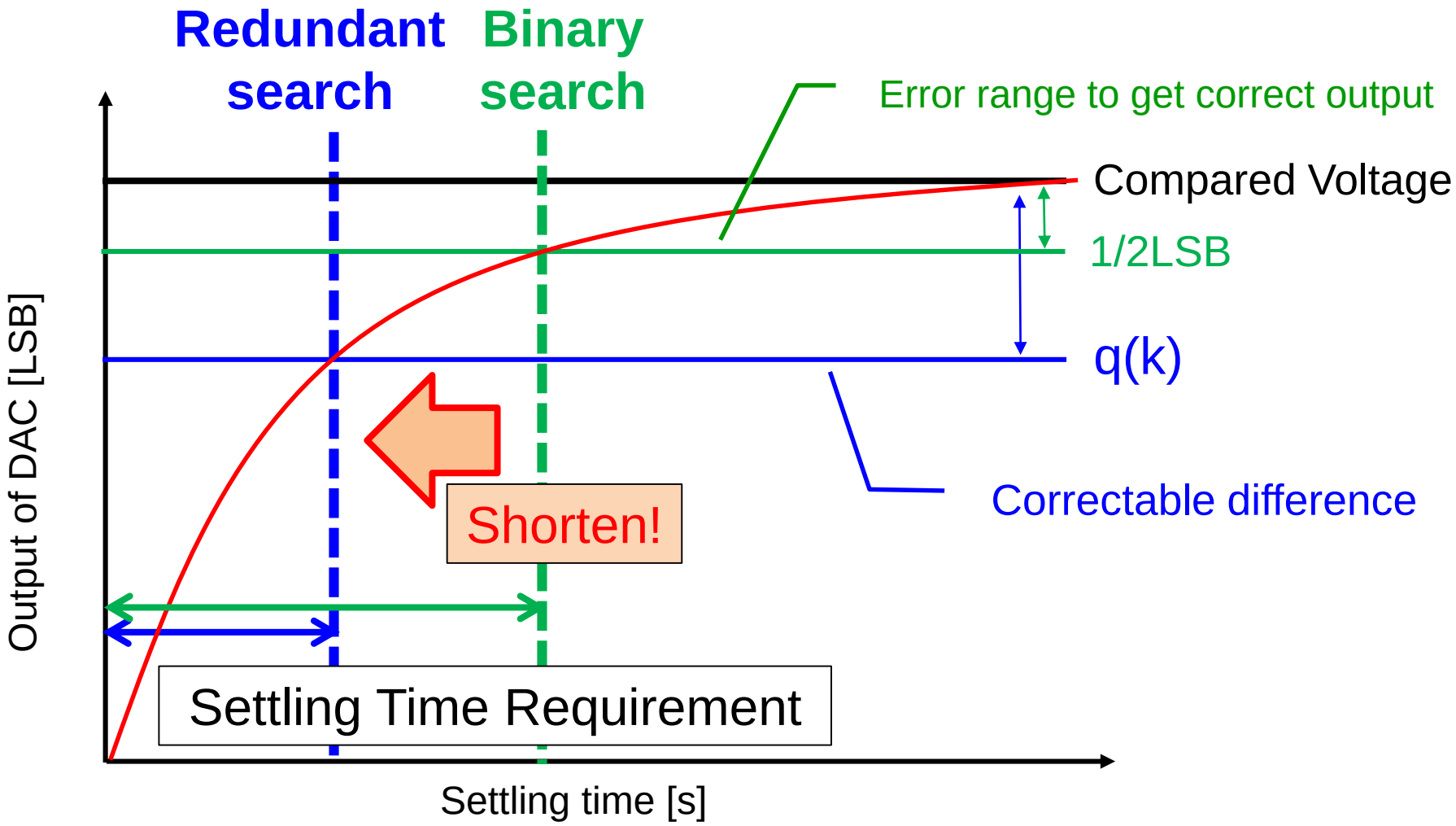


Comparator Thinking!!



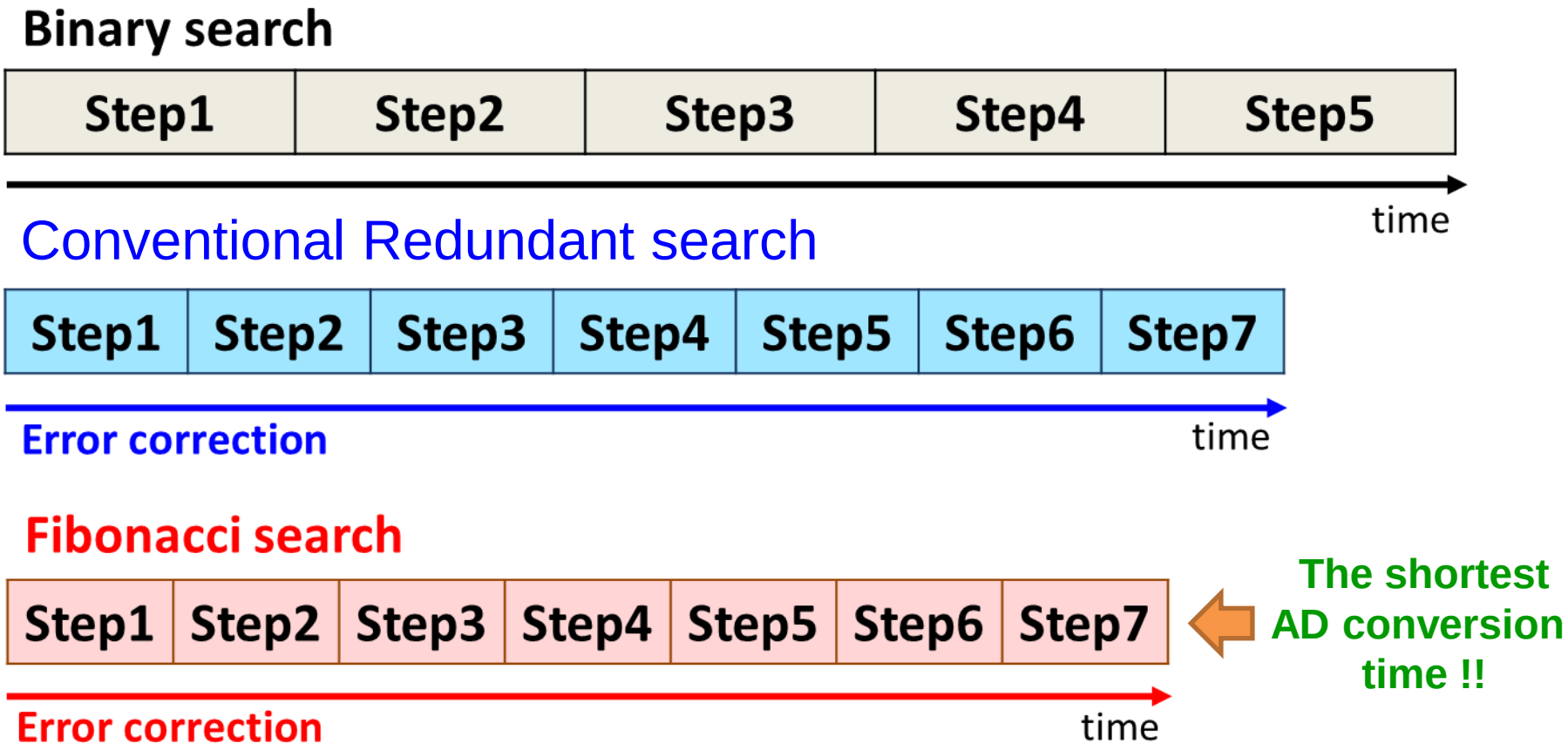
Internal DAC Incomplete Settling

Shorten AD Conversion time

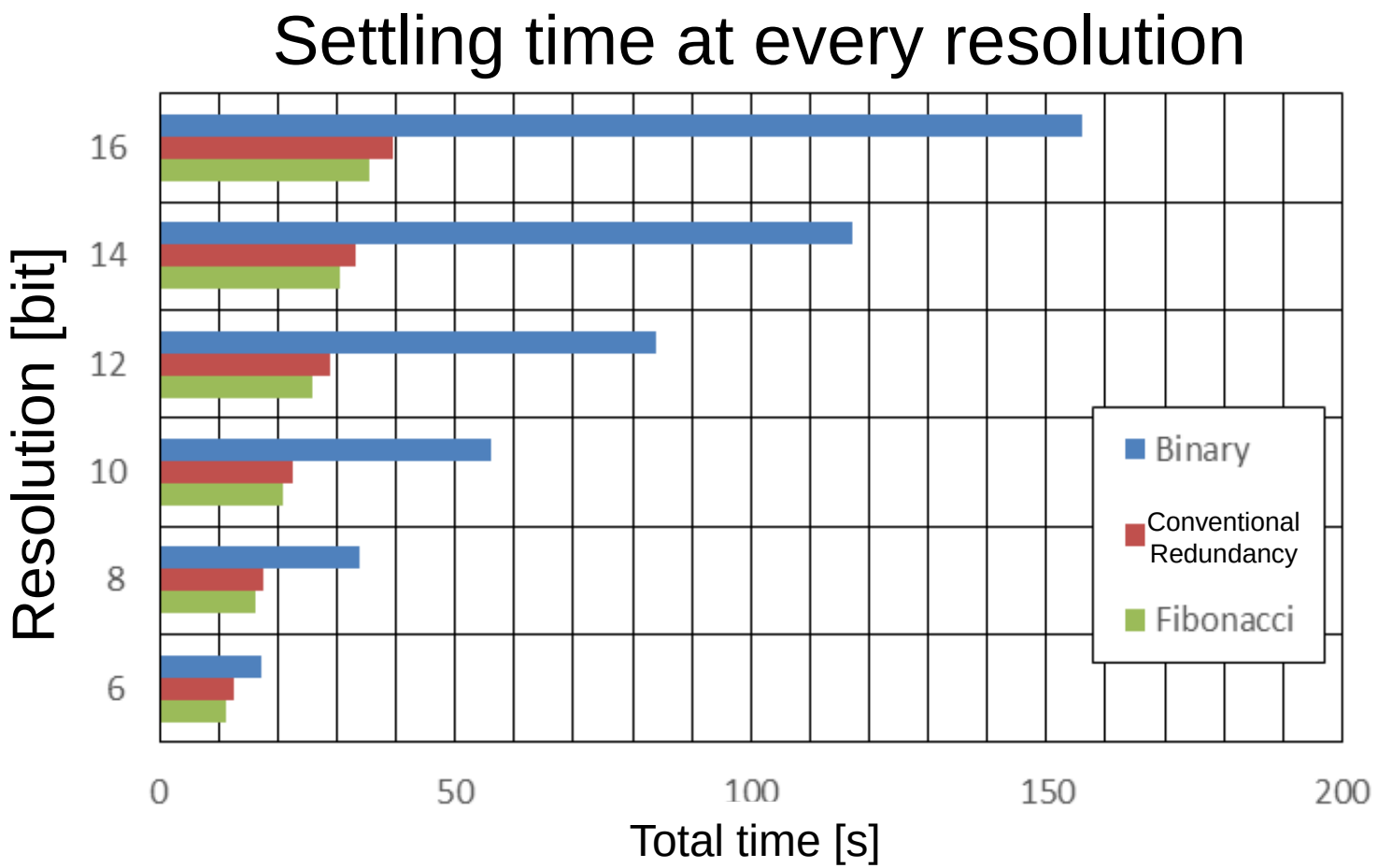


Reduction of AD Conversion Time

5bit SAR ADC



Comparison of SAR AD Conversion Time



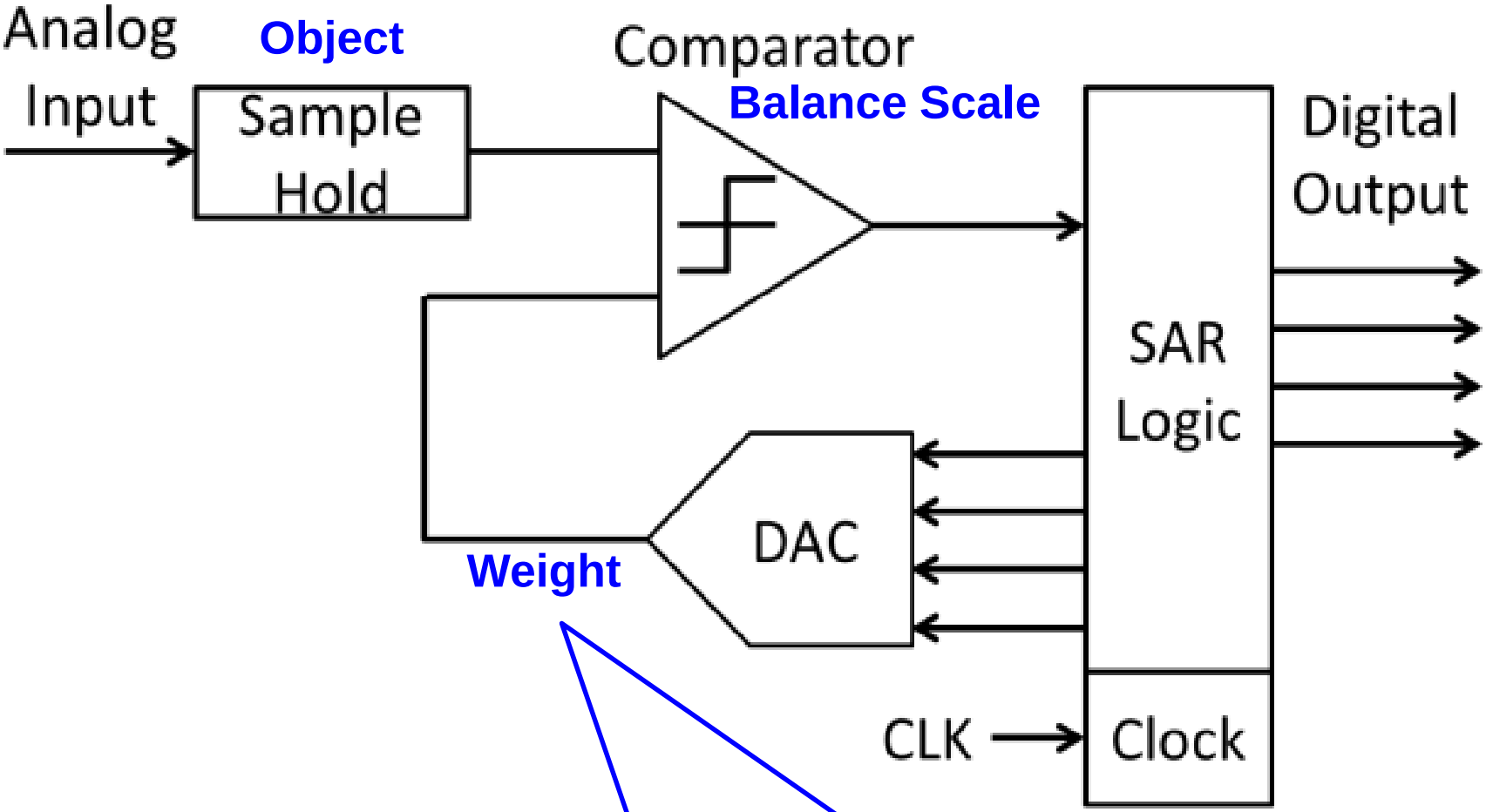
At fixed clock,

Fibonacci ⇨ the shortest AD conversion time !!

Outline

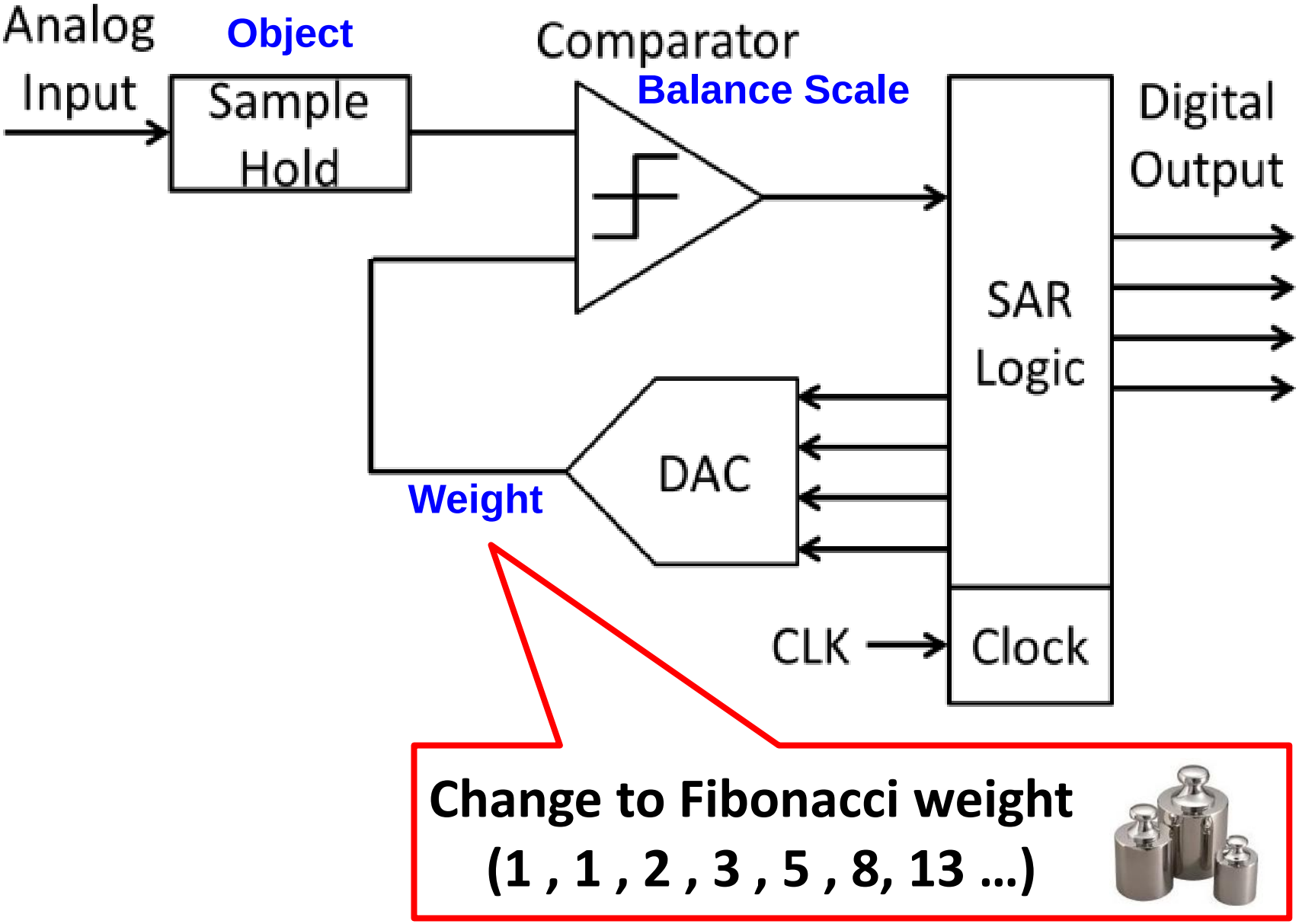
- Objective
- SAR ADC
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Fibonacci Sequence and Golden Ratio
  - Fibonacci Weighted SAR ADC
  - DAC Settling Time
- Realization of Fibonacci DAC
- Conclusion

Binary SAR ADC Configuration

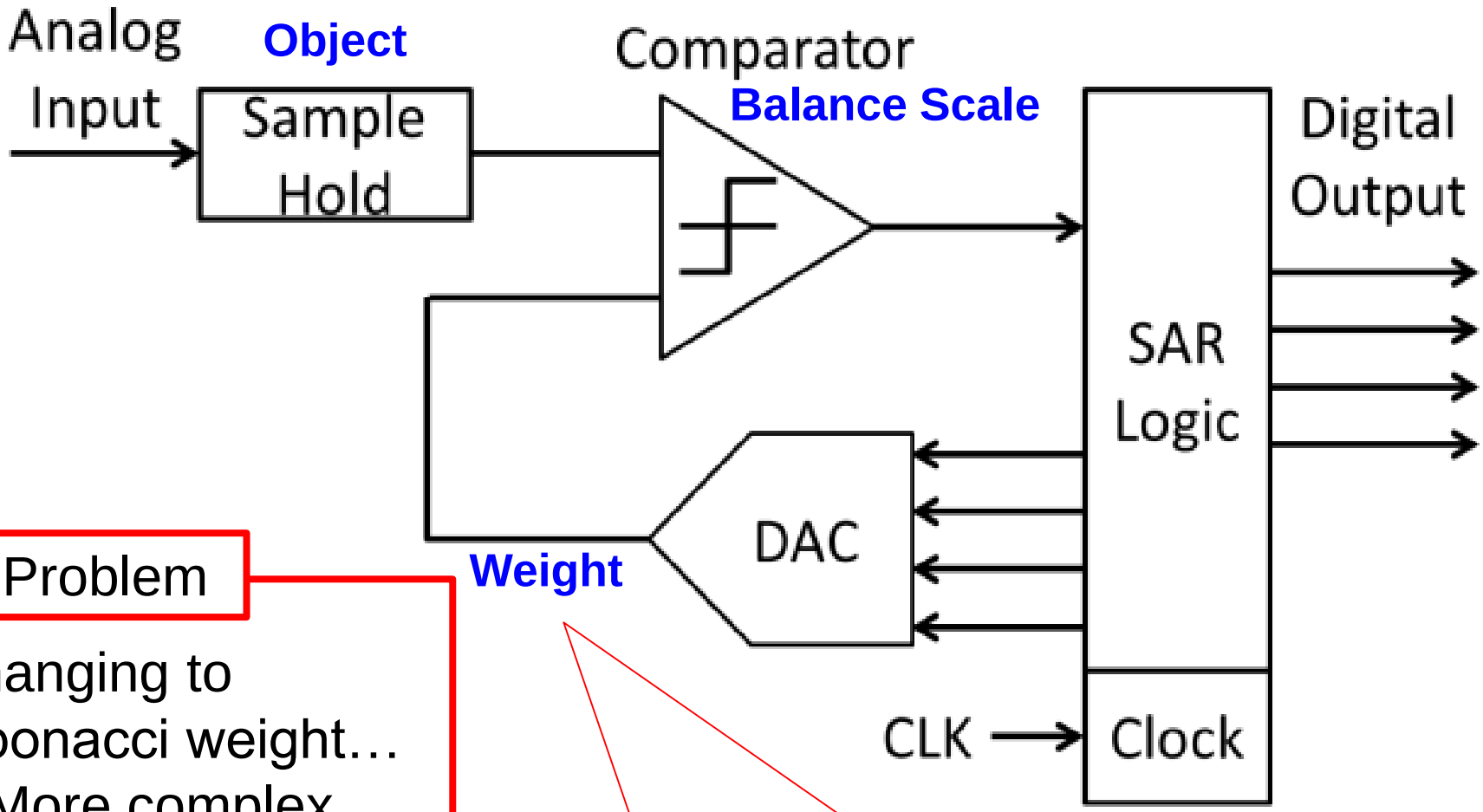


Generally use binary weight
(1 , 2 , 4 , 8 , 16 , 32, 64 …)

Fibonacci SAR ADC Configuration



Fibonacci SAR ADC Configuration



Problem

Changing to Fibonacci weight…

- More complex
- More large-scale

than conventional.

Change to Fibonacci weight

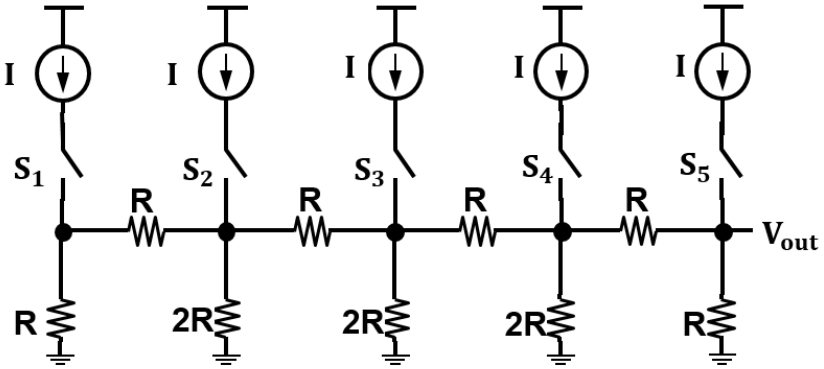
(1 , 1 , 2 , 3 , 5 , 8, 13 …)

Binary and Fibonacci DACs

Binary

R-2R resistor ladder

⇒Generate **binary** voltage



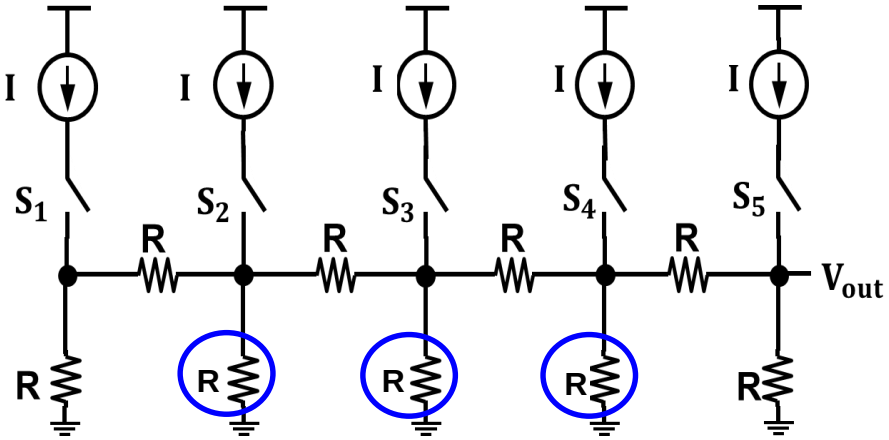
R-2R resistor ladder

Change all resistors to R

Proposal

R-R resistor ladder

⇒Generate **Fibonacci** voltage

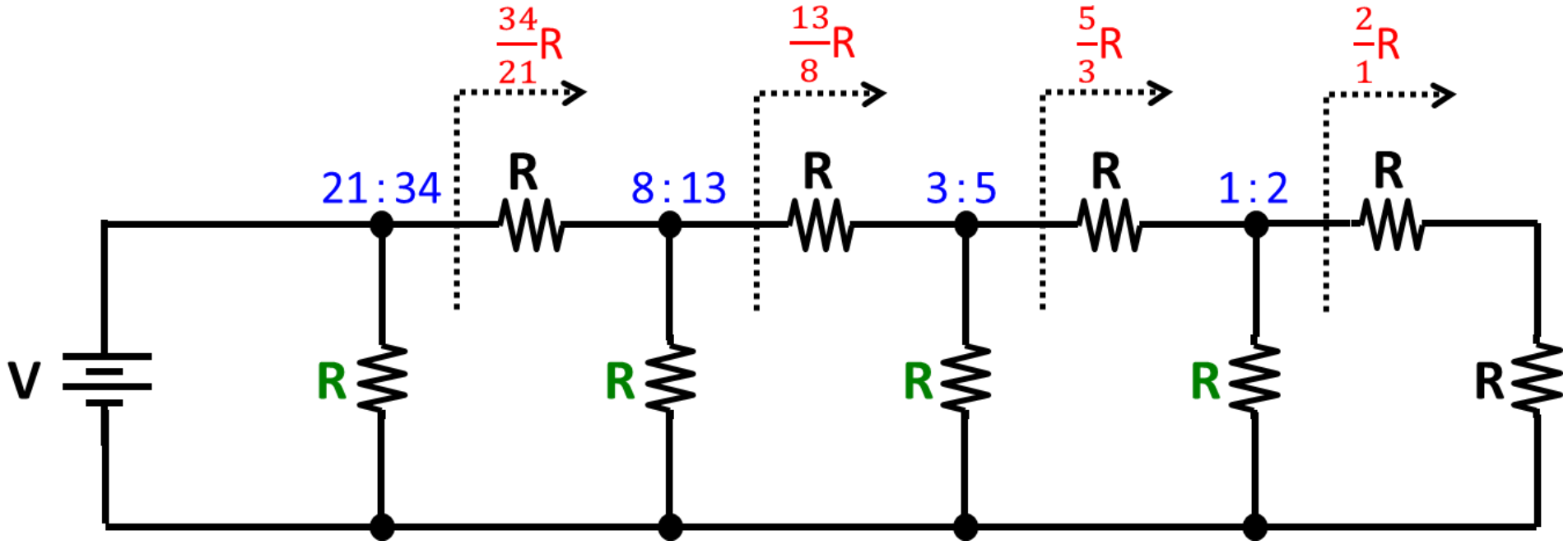


R-R resistor ladder

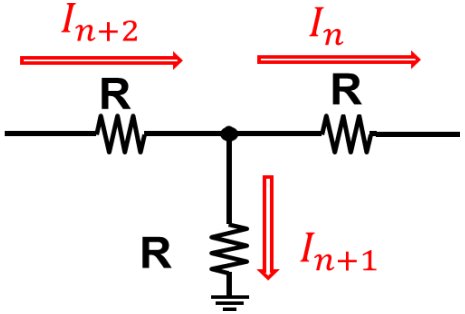
Realize Fibonacci DAC
by using simple circuit !

Principle of Fibonacci Voltage Generation

Divides current into **Fibonacci ratio** in each node



Principle



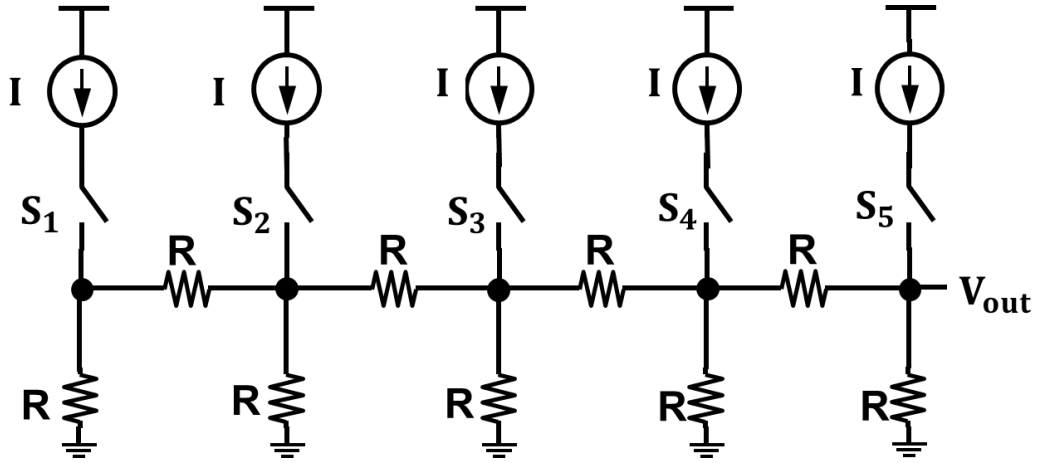
$$I_{n+2} = I_{n+1} + I_n$$

$$F_{n+2} = F_{n+1} + F_n$$

Proposal of R//R Fibonacci DAC

R-R resistor ladder

Generate
Fibonacci voltage
of **odd** term

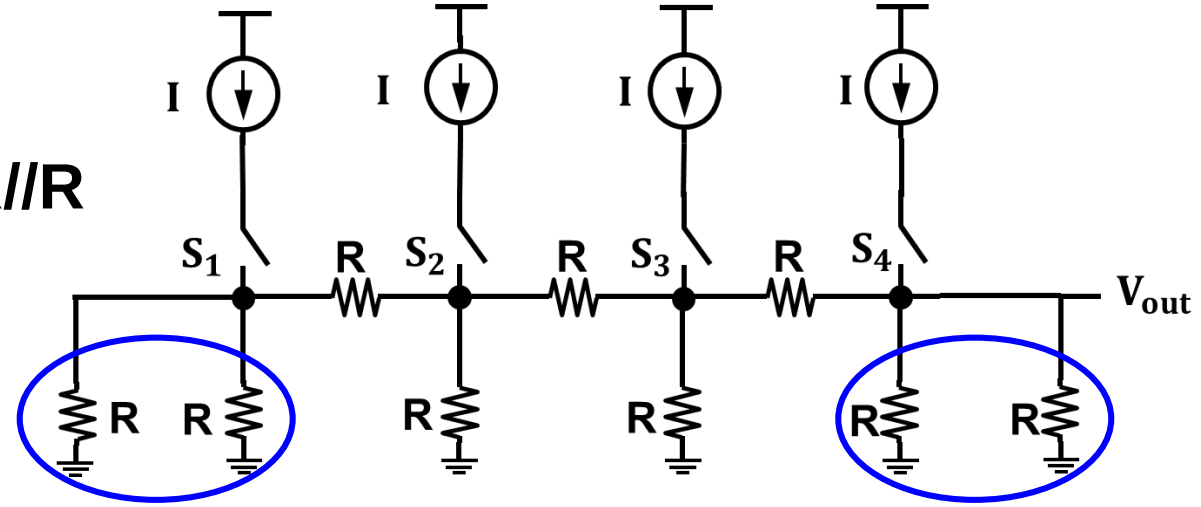


Change terminal resistors to
parallel resistors

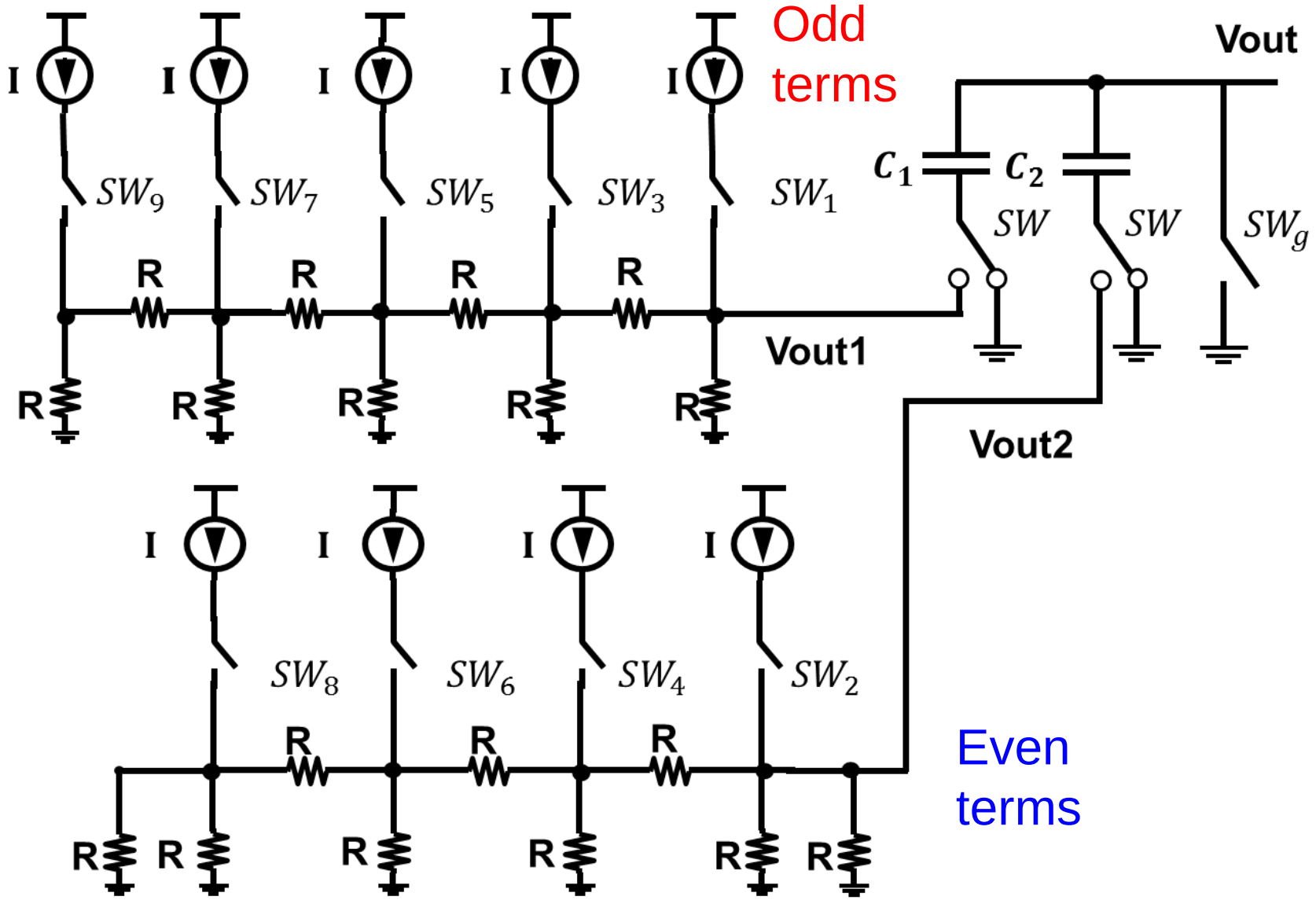
Proposal

R-R resistor ladder
with terminations of R//R

Generate
Fibonacci voltage
of **even** term



Fibonacci DAC Architecture



Outline

- Objective
- SAR ADC
- SAR ADC Redundancy Design
- Proposed SAR Algorithm Using Fibonacci Sequence
  - Fibonacci Sequence and Golden Ratio
  - Fibonacci Weighted SAR ADC
  - DAC Settling Time
- Realization of Fibonacci DAC
- Conclusion

Conclusion

- Propose redundant SAR ADC design methods

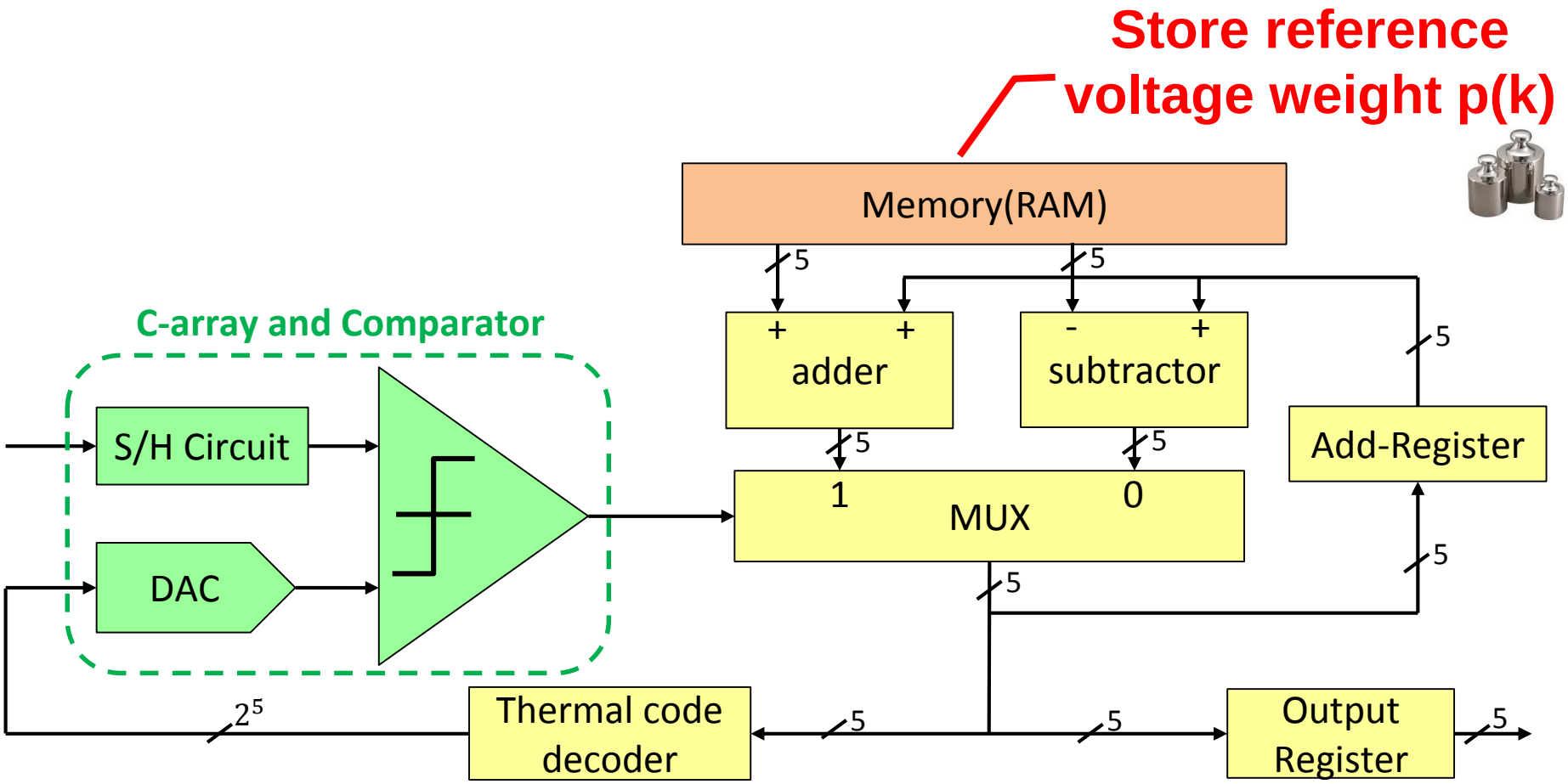
- Get important properties by using Fibonacci sequence
  - **Reliable**
    Correctable difference covers wide input range
  - **Shortest SAR AD Conversion**
    Conversion time is the shortest in a fixed clock
  - **Radix-Standard**
    Golden ratio φ establish radix standard

- Propose beautiful DAC structures
  which generate Fibonacci voltages.

Hope that these will contribute to automotive applications !

Appendix

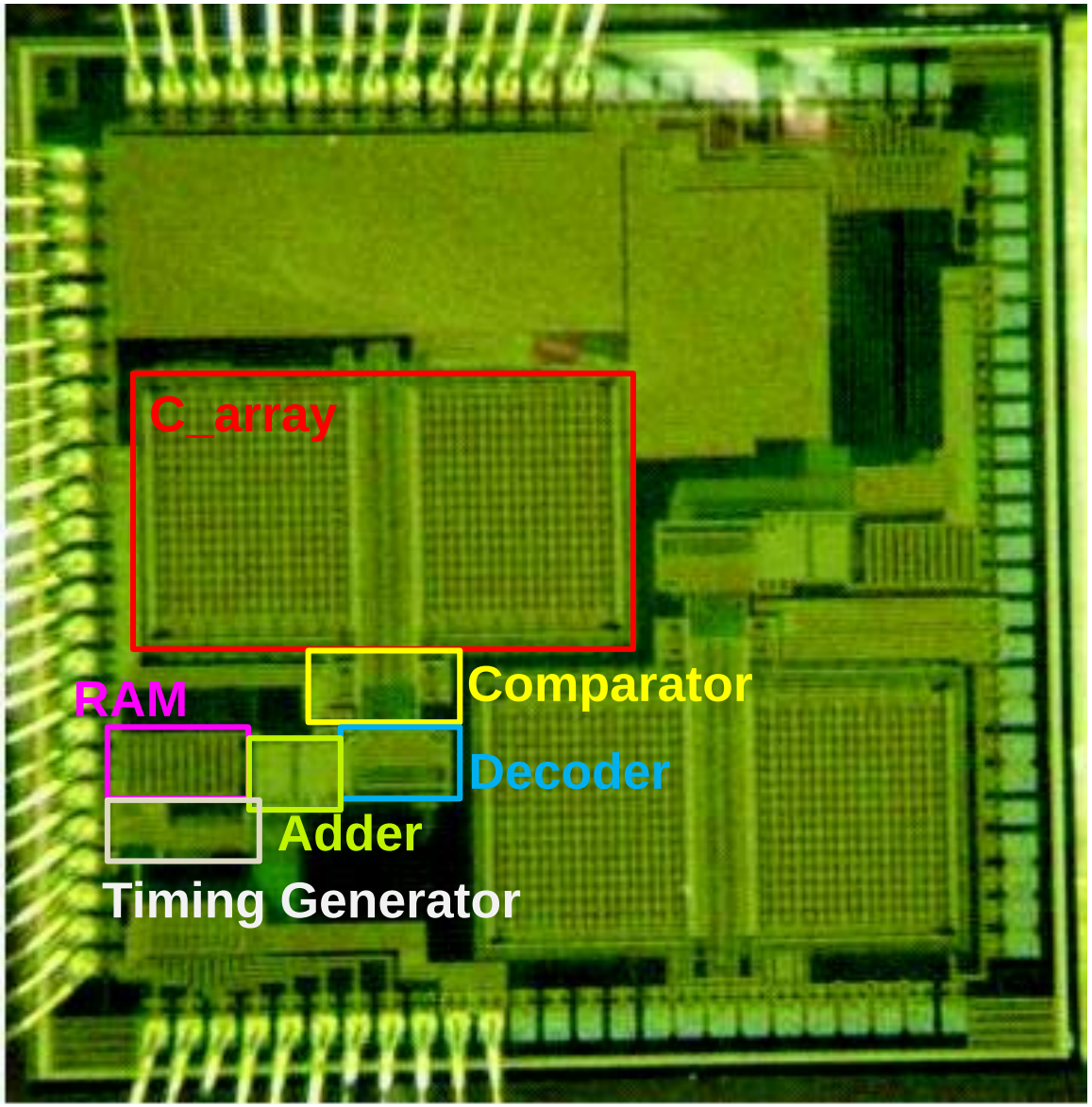
Configuration of Redundancy SAR ADC



SAR ADC circuits consist of mostly digital circuit.

Chip of Redundancy SAR ADC

(0.18um CMOS 2.5mm x 2.5mm)



Additional circuits

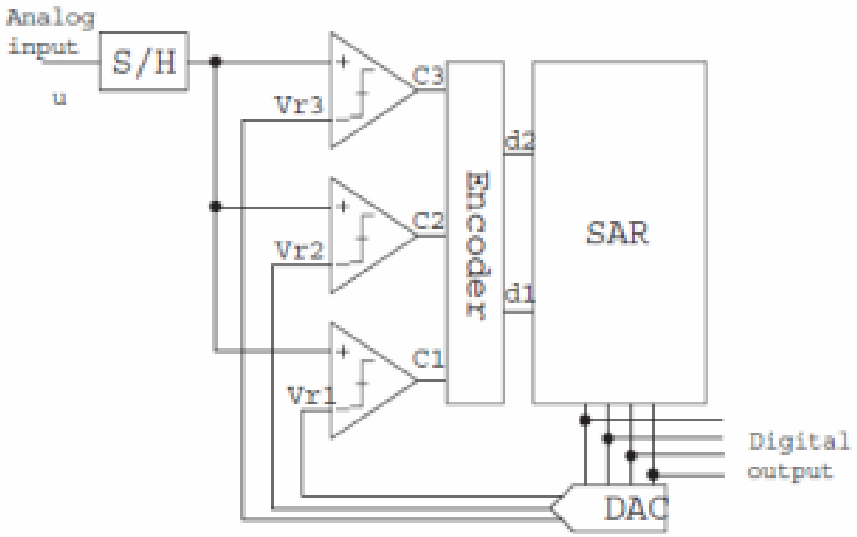
are very small !!

Temporal vs Spatial Redundancy

- Temporal redundancy
- Spatial redundancy

  SAR ADC

  with 3 comparators [1]



- I have a feeling

  temporal redundancy is more effective.

[1] M. Hotta, M. Kawakami, H. Kobayashi, et. al.,
"SAR ADC Architecture with Digital Error Correction",
IEEJ Trans. Electrical and Electronic Eng. (Nov. 2010).

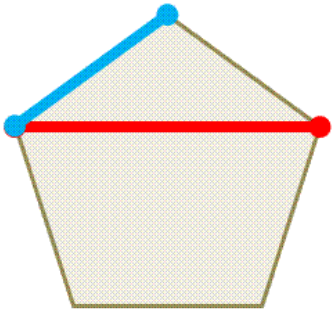
Redundancy vs Testing

- Robust design makes its testing difficult.
- Redundancy hides defects in DUT.

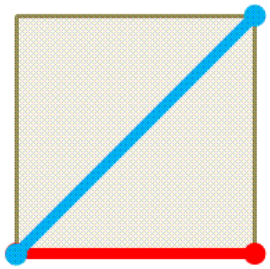
Testing of redundant systems is a challenge.

Silver Ratio

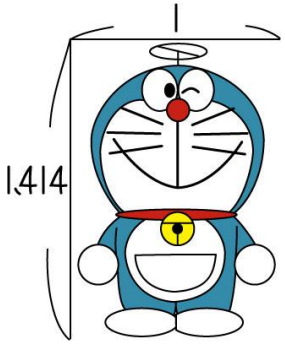
Silver Ratio : $\frac{\sqrt{2}}{1} = 1.414\ldots$



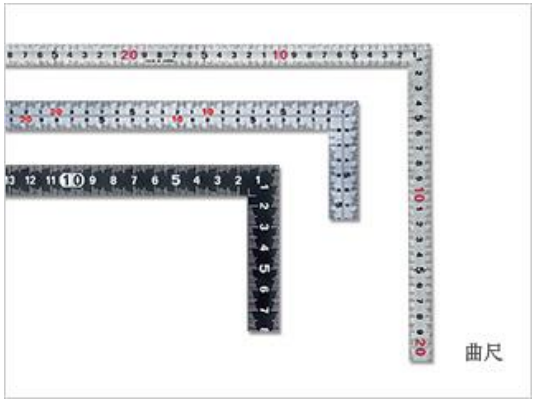
Golden ratio
1 : 0.618

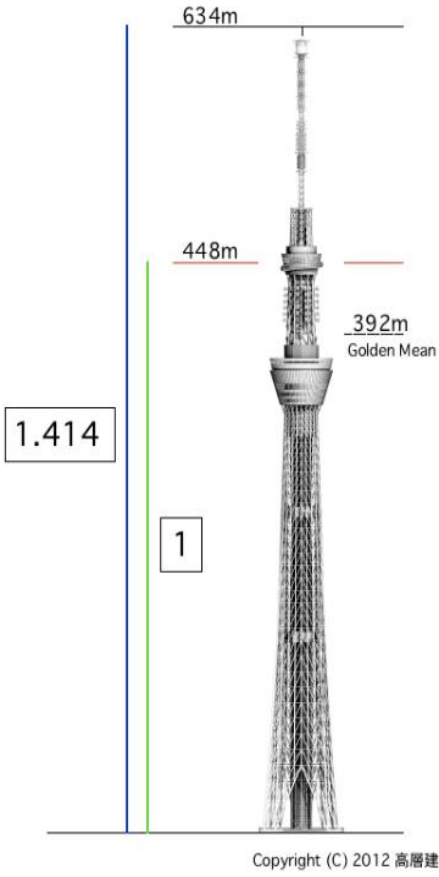


Silver ratio
1 : 1.414



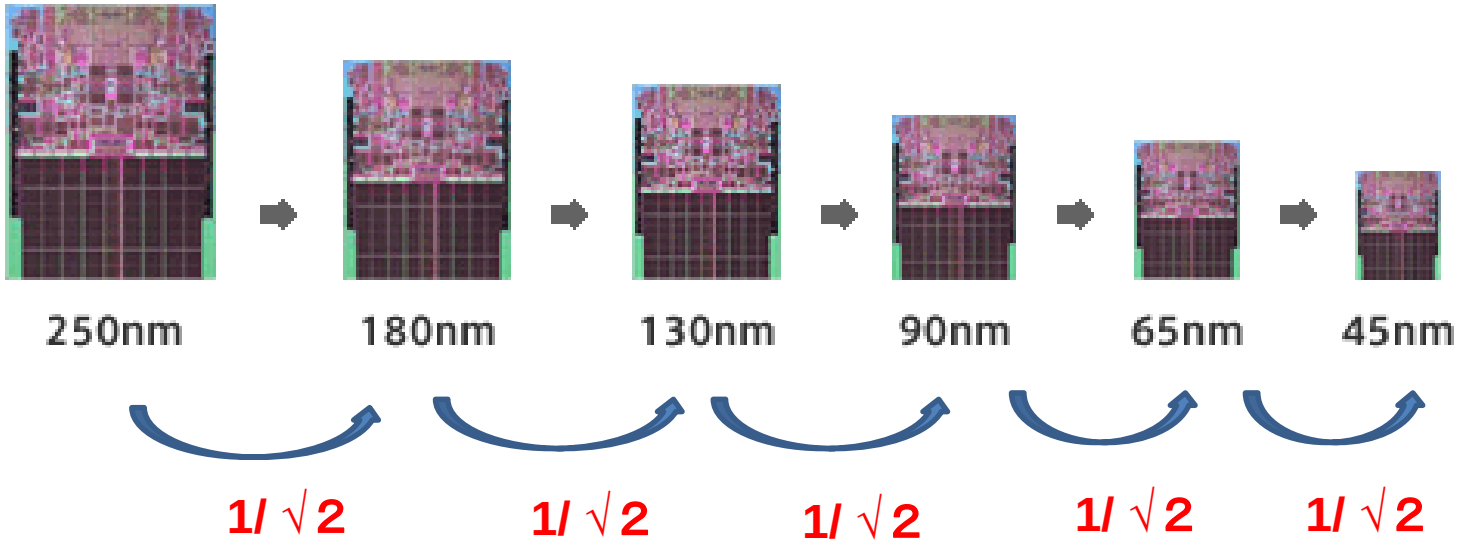
1 : 1.414





LSI Scaling vs. Silver Ratio

LSI Scaling Rule



Silver Ratio Weight

N bit M step SAR ADC

Weights p(k)

p(M)	=1		
p(M-1)	=1	×1	×$\sqrt{2}$
p(M-2)	=1	×2	×$\sqrt{2}$
p(M-3)	=2	×1	×$\sqrt{2}$
p(M-4)	=2	×2	×$\sqrt{2}$
p(M-5)	=4	×1	×$\sqrt{2}$
p(M-6)	=4	×2	×$\sqrt{2}$
p(M-7)	=8		
p(M-8)	=8		
p(M-9)	=16		
p(M-10)	=16		

For 2 steps, 2 times ($r^2 = 2$)

II

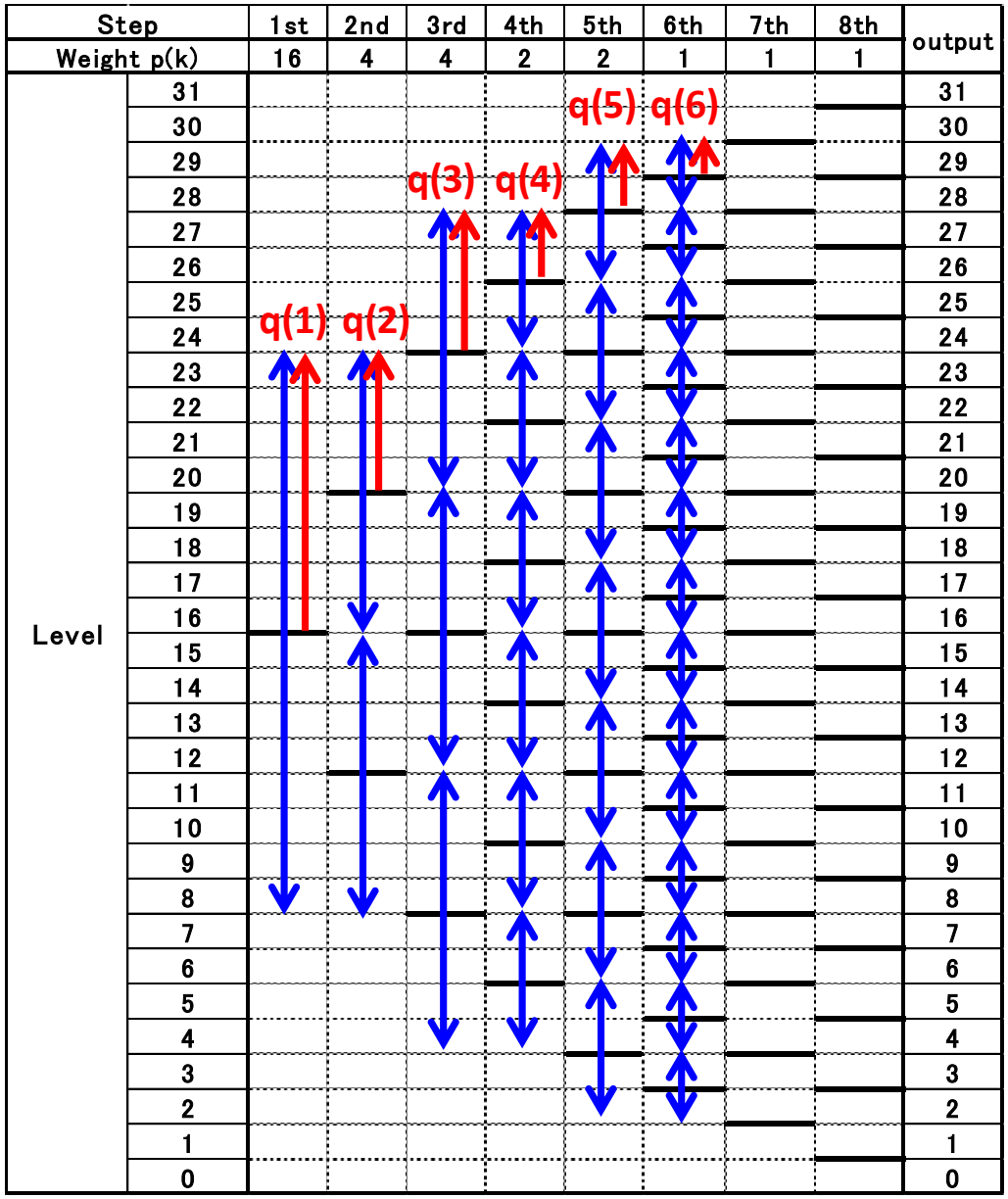
For 1 step, $\sqrt{2}$ times ($r = \sqrt{2}$)

Peudo radix $\sqrt{2}$ weight

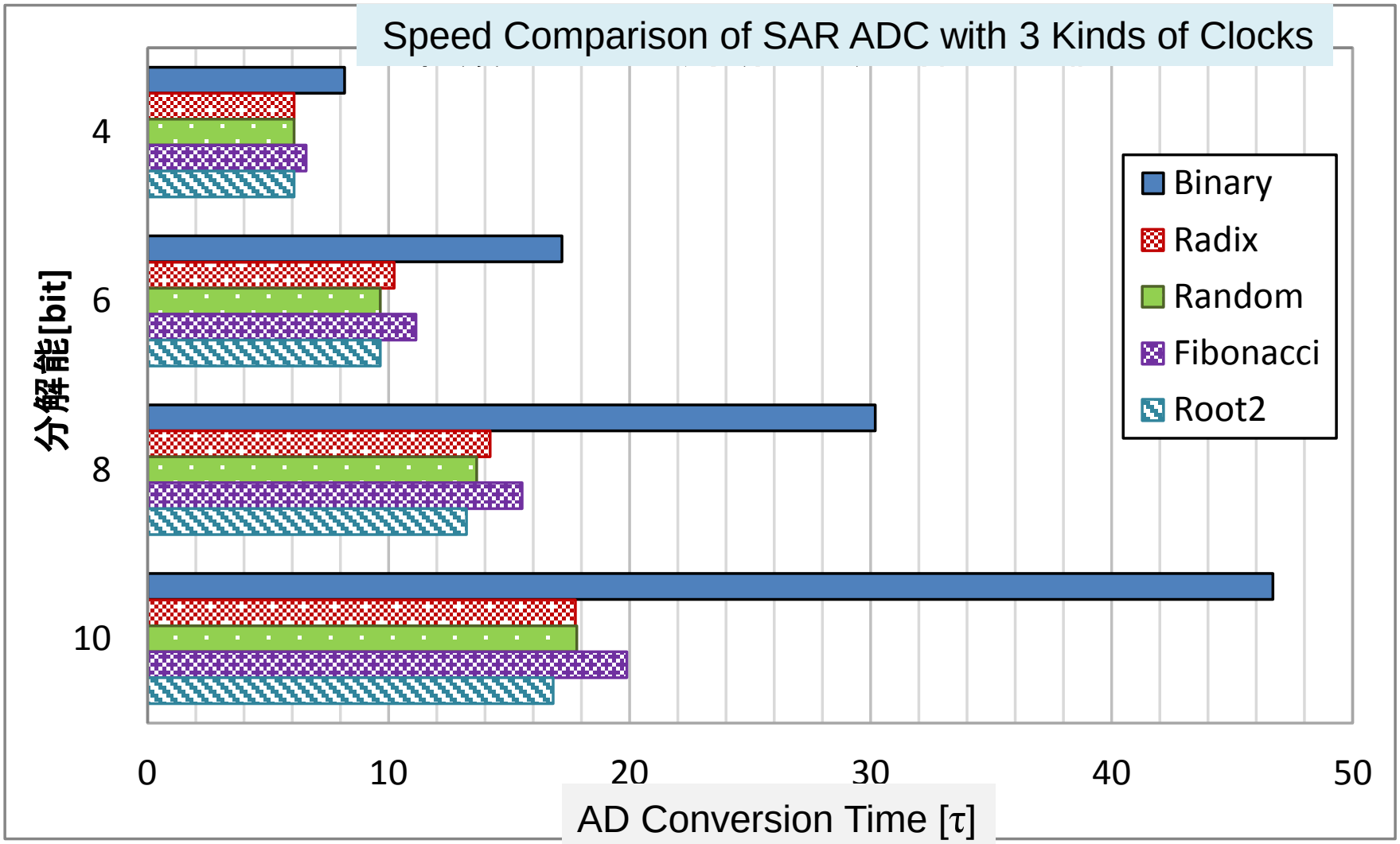
"Silver ratio"

Silver Ratio Weight SAR ADC

5bit 8step　SAR ADC



SAR ADC Speed Comparison



For 3 kinds of clocks, the silver ratio SAR ADC is the fastest !

Number theory for Engineering

Carolus Fridericus Gauss
(1777-1855)

"Number theory is the queen of mathematics"

Carolus Fridericus Gauss

Past Number theory

Beautiful and Mysterious
was NEVER practical

Current Number theory

used information communication processing

➡ good match to digital technology

Number theory application for ADC/DAC is a frontier.
There are great chances for new discovering !

Kobayashi
Laboratory

Redundant SAR ADC Algorithms for Reliability Based on Number Theory

Yutaro Kobayashi, Takuya Arafune, Shohei Shibuya, Haruo Kobayashi, Hirotaka Arai
Division of Electronics and Informatics, Gunma University, Kiryu, Gunma 376-8515 Japan

***Abstract*—** This paper describes SAR ADC algorithms to ensure reliability with possible targets for automotive applications. The SAR ADC has beneficial characteristics of low power and small chip area, and hence it is widely used, especially in automotive applications together with micro-controllers. There, digital error correction method using redundant comparison is an effective method to improve its reliability and conversion speed because it realizes correction of misjudgment at a comparator and incomplete settling of an internal DAC. Then this paper describes two effective redundancy design algorithms based on number theory: (i) The first one uses Fibonacci sequence and its property called Golden ratio Especially, several interesting properties are clarified that contribute to solve SAR ADC design problems, such as radix standard and shortening required settling time. (ii) The second one uses pseudo silver ratio (square root of 2) for the SAR ADC, which leads to simple SAR logic design and fast conversion speed in case of multiple clock period usage.

***Keywords*—**SAR ADC, Reliability, Redundancy, Error Correction, Fibonacci Sequence, Golden Ratio, Silver Ratio

I. Introduction

SUCCESSIVE approximation resistor A-D converters (SAR ADCs) are gathering attention thanks to their useful characteristics for automotive applications. Its performance improvement of conversion reliability and speed is demanded to match with high technology, and we study here about redundancy design of SAR ADCs for their realization.

Redundancy design enables digital error correction to improve SAR ADC performance [1-7]. One redundancy design method is to use a non-binary search algorithm instead of a binary search algorithm. There, extra comparison steps and a non-binary weighted DAC are needed for a redundant SAR ADC and we have to determine its non-binary weighted values. Generally, their values are determined using a non-binary radix method or selected flexibly by the SAR ADC designer. However the efficient and systematic redundant SAR ADC algorithm design method has not been studied well yet.

In this paper, we discuss two methods to design redundant SAR algorithms based on number theory, i.e., (i) Fibonacci sequence (or golden ratio) and (ii) Pseudo silver ratio methods. Then we obtain well-balanced non-binary weight values.

This paper is organized as follows: Section II overviews SAR ADCs, and Section III outlines their redundancy design. Section IV presents our first method of redundancy design using Fibonacci sequence and Section V shows the incomplete settling problem of an internal DAC inside the SAR ADC. Section VI shows our second method of redundancy design using pseudo-silver-ratio for the SAR ADC using multiple clock periods. Section VII provides conclusion.

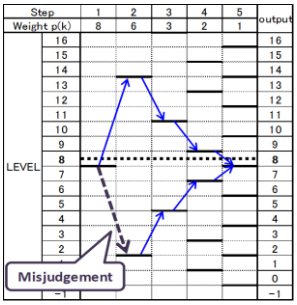


Fig. 3 Operation of a 4-bit 5-step SAR ADC in case of correct and incorrect judgments.

II. Overview of SAR ADC

The SAR ADC consists of a sample-and-hold circuit, a comparator, a DAC, an SAR logic and a timing generator as shown in Fig. 1. Conversion of the SAR ADC is based on principle of balance and generally it uses the binary search algorithm. Firstly, the sample-and-hold circuit samples analog input voltage regularly. Secondly, the comparator compares the sampled voltage and the reference voltage which is generated by the DAC and decides 1-bit digital output. Thirdly, SAR logic provides digital code for the DAC input based on the comparator output. The sampled input voltage and the updated DAC output voltage are compared by the comparator. These operations are repeated and finally SAR ADC obtains the whole digital output.

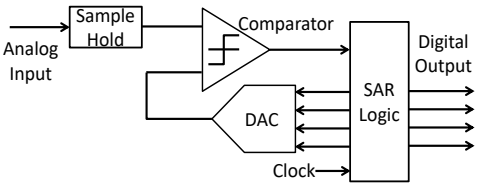


Fig. 1 Block diagram of an SAR ADC.

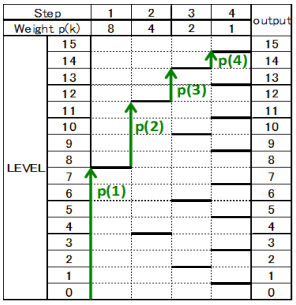


Fig. 2 Binary search algorithm of a 4-bit 4-step SAR ADC.

Fig. 2 shows the binary search algorithm of a 4-bit SAR ADC. The bold line in Fig. 2 indicates the reference voltage value to compare with the sampled input voltage at each step. Their

values are calculated by either sum or difference between the last step reference voltage and the weighted voltage p(k) of each step as shown in Fig. 2. The comparator outputs 1 if the input voltage is larger than the reference voltage; otherwise it outputs 0. Then we obtain the digital output at each step.

Usually, p(k) which is defined as a reference voltage weight of the DAC is a binary weighted value because the binary search algorithm is efficient. However, in reality, there is possibility of comparator misjudgment due to DAC incomplete settling and sample-and-hold circuit incomplete settling as well as noise. In the binary weighted SAR ADC, one misjudgment of the comparator leads to incorrect output and low reliability. Hence this paper investigates redundancy design of the SAR ADC to enable digital error correction for misjudgment of the comparator.

III. Redundancy Design of SAR ADC

Redundancy design is a technique to improve circuit and system performance. In the SAR ADC, redundancy design method adding extra comparison is often utilized [1-7]. This method changes binary weights to non-binary weights for the DAC that makes reference voltage and realizes digital error correction with redundancy property.

Fig. 3 shows an example of two redundant search operations of a 4-bit 5-step SAR ADC. There, the input voltage is 8.6-LSBs and the reference voltage weights p(k) are 1, 2, 3, 6 and 8. The one operation (solid arrows) assumes that the comparison is correct, whereas the other (dotted arrows) assumes that it is incorrect. However both obtain the correct digital output of 8 by digital error correction. In the 4-bit 5-step SAR ADC as shown in Fig. 3, there are 2^5 comparison patterns against 2^4 output patterns. In other words, a given output level can be expressed by multiple comparison patterns. Therefore even if comparator decision is wrong at some steps, the correct ADC output may be obtained. This is the basic principle of the digital error correction. In addition, even if the number of the comparison steps is increased, the digital error correction enables high-speed AD conversion as a whole, because the digital error correction can take care of the DAC incomplete settling [1-7]; thus redundancy design has potential for reliable and high-speed SAR AD conversion.

A. Generalization of redundant SAR ADC design

We generalize SAR ADC redundancy design from using some equations [3]. If we realize an N-bit resolution SAR ADC by M-step comparison ($M \geq N$), the reference voltage $V_{ref}(k)$ at k-th step and ADC output D_{out} are defined by (1) and (2), respectively. Here k = 1, 2, 3, 4, … , M and p(k) is the reference voltage weight value for addition to (or subtraction from) the DAC input in the previous step. Moreover, each d(k) is decided by the comparator output. If the comparator digital output at k-th step is 1, then d(k) = 1, and if the comparator digital output at k-th step is 0, then d(k) = -1. Furthermore d(0) = 1.

$$V_{ref}(k) = \sum_{i=1}^{k} d(i-1) \cdot p(i). \quad (1)$$

We can also define "the redundancy at k-th step q(k)" as (2).

$$q(k) = -p(k+1) + 1 + \sum_{i=k+2}^{M} p(i). \quad (2)$$

Here q(k) indicates correctable difference between the input voltage and the reference voltage at k-th step[3]. Even if the comparator result is wrong in the k-th step, we can obtain the correct output as long as (3) is satisfied.

$$q(k) > |Vin - Vref(k)|. \quad (3)$$

Fig. 4 shows q(k) as an example of Fig. 3. In Fig. 4, one-way arrows indicate q(k), while two-way arrows show correctable input ranges which means that these input ranges have multiple expressions. As shown in Fig. 4, since the input voltage 8.6-LSBs satisfies (3), the SAR ADC can obtain the correct output in Fig. 3. Therefore q(k) expresses the digital error correction capability. Moreover q(k) is defined by only the reference voltage weight p(k) in (2), and thus p(k) is an important parameter in the redundant SAR ADC algorithm design.

B. Conventional method to decide reference voltage weight

Only reference voltage weight p(k) decides correction capability of the redundant SAR ADC; if the design of the reference voltage weight p(k) is not appropriate, the SAR ADC cannot have the maximum compensation ability. The ratio of the reference voltage weights p(k+1)/p(k) must be between 1 (unary) and 2 (binary). In conventional methods, we can obtain the k-th step reference voltage weight p(k) based on the radix r in (4). Here, N is the ADC resolution, and M is the number of the whole steps.

$$p(k) = r^{M-k}. \quad (4)$$

Here $1 < r < 2$ and $p(1) = 2^{N-1}$**.** We set p(1) to 2^{N-1} which is half of the full scale range, to make the SAR algorithm efficient. Additionally, the total number of steps M has to satisfy (5) to enable all output level expression.

$$2^{N-1} - 1 \leq \sum_{i=0}^{M-2} p(M-i). \quad (5)$$

We can systematically decide conditions for redundancy design

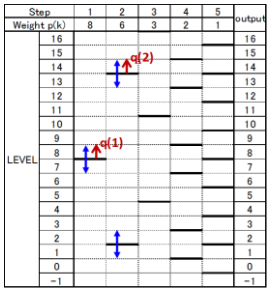


Fig. 4 4-bit 5-step SAR ADC algorithm and definition of correctable difference q(k).

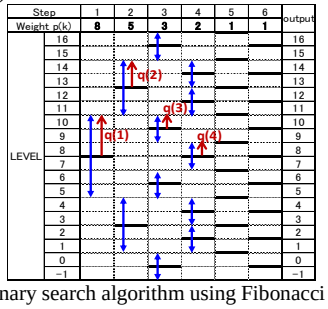


Fig. 5 Non-binary search algorithm using Fibonacci sequence of a 4-bit 6-step SAR ADC.

based on the above equations.

C. Problems of Conventional methods

Conventional methods may have some issues. First, the reference voltage weight p(k) in (5) is not an integer which is not suitable for the circuit design. Since the reference voltage weights p(k) must be integers for conversion accuracy, its rounding to an integer is needed to determine p(k). However rounding causes change of the radix and variability of the correction capability q(k), which may disturb performance improvement.

In addition, there is difficulty of an appropriate radix choice. Fig. 3 shows an example in case of radix 1.80 and rounding. However in Fig. 4, two-way arrows indicate that correctable input range cannot cover all input range, which means that there are some ranges that cannot be corrected. In Fig. 4, if the ADC input is not within the range of 1~3, 7~9, 13~15 LSBs, redundancy design becomes meaningless because these input ranges cannot be expressed in multiple. Thus the inappropriate selection of a radix loses redundancy design effectiveness. On the other hand, the selection of a small radix for larger values of q(k) induces an increase in the number of SAR ADC comparison steps and hence conversion time. In this way, there is a trade-off between correction capability and conversion speed, and the SAR ADC designer is forced to search a radix that is the most suitable for SAR ADC; these are causes of design difficulty.

D. Time redundancy and circuit redundancy

In this paper, we consider the time redundancy or step redundancy for the SAR ADC. Also circuit redundancy may be possible. For example, we previously investigated to use three comparators in the SAR ADC and there digital error correction was incorporated for high reliability and fast conversion [8]. However, we consider from our experiences that the time redundancy would be more effective, especially for low power.

IV. Redundancy design Using Fibonacci Sequence

Here, we propose a redundancy design method using *Fibonacci sequence*.

A. Fibonacci sequence

Fibonacci sequence is defined with a recurrence formula as shown in (6), where *n* in (6) is an integer greater than or equal to 0. It was presented in 1202 by Leonardo Fibonacci [9].

$$F_{n+2} = F_n + F_{n+1}. \tag{6}$$

Here, $F_0 = 0$ and $F_1 = 1$. Fibonacci numbers are expressed as the following by calculating (6) :

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, 610, … .

In short, the sum of neighboring two terms is next term. In addition, the closest terms ratio of Fibonacci sequence converges to about 1.62 as shown in (7).

$$\lim_{n\to\infty} F_n / F_{n-1} = 1.6180339887 \ \ldots = \varphi. \tag{7}$$

This ratio is called "Golden ratio", and widely recognized as the most beautiful ratio. We can find Fibonacci sequence and Golden ratio in various places such as nature and human societies, and they have many interesting properties [9].

B. Fibonacci sequence application to SAR ADC design

Equation (6) indicates that Fibonacci sequence numbers are integers, and (7) indicates that the closest term ratio of Fibonacci number converges to about 1.62 called Golden ratio. In other words, Fibonacci sequence can generate a number string at radix 1.62 with only integer terms. In general, multiplication result of an integer and a decimal fraction is a decimal fraction, nevertheless multiplication result of an integer and a decimal fraction (1.62..) is an integer in Fibonacci sequence. Therefore we can apply Fibonacci sequence to the redundancy algorithm design of the SAR ADC using effective properties of the fixed rate and integer terms.

We select the reference voltage weight p(k) by using Fibonacci sequence as shown in (8).

$$p(k) = F_{M-k+1}. \tag{8}$$

Here, $p(1) = 2^{N-1}$. In short, we set p(k) to Fibonacci number in ascending order. Since p(k) follows the property of Fibonacci sequence, the proposed method can realize radix 1.62 by using only integers. Here the total number of steps M satisfies (5). Fig. 5 shows correctable difference in a redundant search of a 4-bit 6-step SAR ADC using Fibonacci sequence as shown in (8). One-way arrows indicate q(k) and two-way arrows show correctable input range just like in Fig. 4.

C. Discovered Properties and Effectiveness

We have discovered two interesting properties in Fig. 5 as follows:

Property 1: Correctable difference q(k) of k-th step is always Fibonacci number F_{M-k-1}.

$$q(k) = F_{M-k-1}. \tag{9}$$

Property 2: q(k) of k-th step is exactly in contact with q(k+1) of (k+1)-th step without overlap. In other words, the tips of two-way arrows of k-th step and (k+1)-th step points are exactly the same level.

The property 2 is important for design of redundant SAR ADC algorithm due to the following two reasons:

First, the property can be a standard for all redundancy designs in the viewpoints of the radix of Fibonacci sequence which is golden ratio 1.62…, and the boundary condition of q(k). Hence, we can confirm that q(k) becomes overlapped, separated or contact by using golden ratio. If the radix value is larger than the golden ratio, the redundancy is small and q(k) boundaries are separated as shown in Fig. 4. On the other hand, if the value of the radix is smaller than the golden ratio, the redundancy is large and q(k) boundaries are overlapped, which means that all input range have multiple expressions. Thus we can easily select the radix by considering the golden ratio as the standard.

Second, the redundancy design using Fibonacci sequence can be considered as the most efficient design. The property 2 indicates that q(k) covers all input range by minimum extra comparison steps. Therefore, we can realize the redundancy design without waste by only integer terms. Moreover even if we change the first step reference voltage, the property 2 holds because of (2), which means that the redundancy design using Fibonacci sequence is flexible.

V. DAC Incomplete Settling

A. Summary and Generalization of DAC incomplete settling

An SAR ADC contains a DAC that outputs a reference voltage by the comparison result at previous step. Since the DAC output must change from the previous reference voltage to next one, the DAC output takes some time to settle. In the binary search algorithm which does not have redundancy, the DAC must take time to settle between the output voltage of the DAC and next reference voltage within 0.5-LSB for accurate conversion. This DAC settling time often dominates the SAR ADC conversion time. Besides, this settling time is much longer for a high resolution SAR ADC due to requirement for very small settling error. On the other hand, in the non-binary search algorithm which has finite correctable difference q(k), the DAC can decrease required settling time, thanks to redundancy and digital error correction at the following steps as shown in Fig. 6.

Difference between the DAC output voltage and the next reference voltage can be smaller than q(k) to accurate conversion when conversion step has correctable difference q(k). We generalize SAR ADC incomplete settling by using a first-order system model as shown Fig. 6. Firstly, we can obtain the output voltage of the DAC as (10) from Fig. 6.

$$V_{DAC}(t) = V_{ref}(k) + \{V_{ref}(k-1) - V_{ref}(k)\}\exp(-t/\tau). \quad (10)$$

Here, τ is a time constant of the DAC output.

To satisfy correctable condition at the redundant SAR ADC, difference between the input voltage of the comparator and the reference voltage has to be smaller than q(k). Thus we can use comparison voltage $V_{com}(k)$, that has distance q(k) from the original reference voltage, to compare the input voltage. Consequently settling time $T_{settle}(k)$ which is the time to make the k-th step comparison voltage to change from the previous comparison voltage $V_{com}(k-1)$ to next comparison voltage $V_{com}(k)$. As we should consider the longest settling time to decide each step settling time, we obtain k-th step settling time $T_{settle}(k)$ as (11).

$$T_{settle}(k) = \tau \ln[\{p(k) + q(k-1)\}/q(k)]. \quad (11)$$

Note that if correctable difference q(k) is less than 1-LSB, we can regard q(k) as 0.5-LSB. Finally, a variable clock SAR ADC takes sum of T_{settle} as total settling time. However, for a fixed clock SAR ADC total settling time is equal to the longest span of T_{settle} multiplied by the number of steps of SAR ADC used.

B. Analysis of Fibonacci SAR ADC settling time

We consider the settling time of the redundant SAR ADC using Fibonacci sequence in theory. In the Fibonacci sequence SAR ADC, we can transform (11) to (12) by using (8) and (9).

$$T_{settle}(k) = \tau \ln\{(F_{M-k+1} + F_{M-k})/F_{M-k-1}\}. \quad (12)$$

Here we transform (13) using (6) as follows:

$$\begin{aligned} T_{settle}(k) &= \tau \ln[\{(F_{M-k} + F_{M-k-1}) + F_{M-k}\}/F_{M-k-1}] \\ &= \tau \ln\{(2F_{M-k}/F_{M-k-1}) + 1\}. \end{aligned} \quad (13)$$

Therefore we obtain the settling time of k-th step at the SAR ADC using Fibonacci sequence as shown (14) by using (7).

$$T_{settle}(k) = \tau \ln(2\varphi + 1) \approx 1.444\tau. \quad (14)$$

Equation (14) indicates that settling time is constant regardless of step number k or usage of variable clock. On the other hand, the conventional method using radix cannot realize constant settling time, because its reference voltage weight p(k) does not have relationship for correctable difference q(k).

C. Settling time comparison of each method

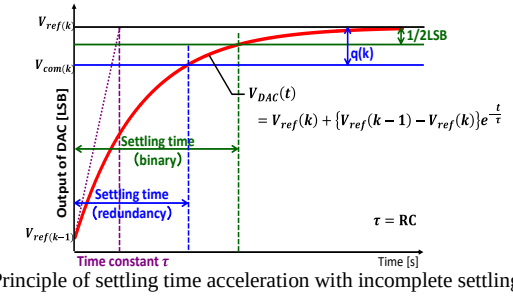


Fig. 6 Principle of settling time acceleration with incomplete settling of the internal DAC.

We have compared the Fibonacci sequence method and the radix one in terms of the redundant SAR ADC settling time. We have carried out comparison at 8-bit SAR ADC under the conditions of variable and fixed clocks, and obtained the results shown in Fig. 7 using (10). We found that total settling time using Fibonacci sequence is the shortest in fixed clock frequency for each ADC resolution.

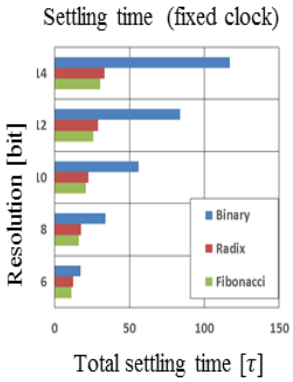


Fig. 7 the comparison of the settling time of ADC at each resolution.

VI. Redundant Algorithm using Pseudo-Silver-Ratio

Redundancy design has possibility for a great ADC, but we need further investigation of designing the redundant algorithm. Then, we derive pseudo-silver-ratio sequence by considering effective utilization of correctable input range, and we propose another redundancy design method using the sequence.

A. Derivation of reference voltage weight p(k) that can realize decrease of settling time

Here, we consider to reduce the settling time to shorten AD conversion time. If the reference voltage weight p(k) is equal to correction capability q(k), the redundant ADC can make the most of correction capability to decrease the settling time. Therefore we decide reference voltage p(k) values as shown in (15) while step number k satisfies $2 \le k \le M-2$.

$$p(k) = q(k) \quad (15)$$

From (2), we have to determine p(M) and p(M-1) to derive reference voltage weight p(k) by using (16). Then we decide p(M)=1 and p(M-1)=1. We can calculate reference voltage weight p(k) as follows:

$$p(M-2) = q(M-2) = -p(M-1) + 1 + \sum_{i=M}^{M} p(i) = 1$$

$$p(M-3) = q(M-3) = -p(M-2) + 1 + \sum_{i=M-1}^{M} p(i) = 2$$

$$p(M-4) = q(M-4) = -p(M-3) + 1 + \sum_{i=M-2}^{M} p(i) = 2$$

Then we obtain following numbers:
1, 1, 1, 2, 2, 4, 4, 8, 8, 16, 16, 32, 32, 64, 64, 128, 128 …
These numbers are used in order for the SAR ADC weights, p(k) as (16).

For 1< k < M, we have

$$p(k) = \sqrt{2}^{M-k-4}\left((1+\sqrt{2}) - (-1)^{M-k+1}(1-\sqrt{2})\right) \quad (16)$$

$$\text{Also,} \quad p(1) = 2^{N-1}, p(M) = 1$$

p(1) is determined by N, that is the ADC resolution. We assume the number of total step M is shown in Eq. (17) by using (5).

$$M = 2(N-1) \quad (17)$$

Fig. 8 shows a redundant search operation of a 4-bit SAR ADC using (17). We notice the correctable range is extended without space and the reference voltage weight p(k) satisfies (15).

B. *Silver ratio*

Term of a series derived by (16) doubles every two terms. It means that the terms are obtained by multiplication of a term and square root of 2 every one term. Therefore we call this weighted method as a pseudo-silver-ratio method.

Silver ratio (square root of 2) is a ratio between one side of a square and the diagonal line of the square. Silver ratio is recognized as one of the most beautiful ratio especially in Japan like Golden ratio in Western world, and Silver ratio has been used frequently for architectures, arts, and characters in Japan.

C. *Analysis settling time of Pseudo-Silver-ratio method*

Here, we calculate incomplete settling time by using (11). Incomplete settling time depends on step number k. When step number k satisfies $2 \le k \le M-2$, we can transform (11) using (15) as follows:

$$T_{settle}(k) = \tau \ln\left(p(k) + p(k-1)/p(k)\right)$$

By using (16), the closest term ratio(=p(k-1)/p(k)) are as follows:

$$p(k) + p(k-1)/p(k) = \begin{cases} 1 & (k = 2n+1) \\ 2 & (k = 2n) \end{cases}$$

Here, n = 1, 2, 3, … Then we obtain the following settling time:

$$T_{settle}(k) = \begin{cases} \tau \ln\{(p(k) + p(k))/p(k)\} \\ \tau \ln\{(p(k) + 2p(k))/p(k)\} \end{cases}$$

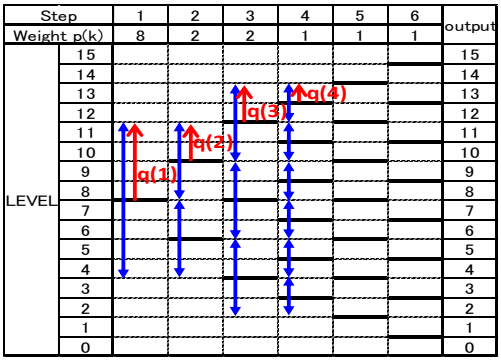


Fig. 8 Redundant search algorithm of a 4-bit 6-step SAR ADC using pseudo-silver-ratio weights.

$$= \begin{cases} \tau\ln 2 = 0.6931\tau & (k = 2n+1) \\ \tau\ln 3 = 1.0986\tau & (k = 2n) \end{cases}$$

Thus the SAR ADC takes two types of settling time alternately. As q(1) is equal to p(1)/2, when k = 1, the settling time is given as follows:

$$T_{settle}(1) = \tau\ln 2 = 0.6931\tau$$

If correctable difference q(k) is less that 1 LSB, we can regard q(k) as 0.5 LSB. Then when k =(M-1), the settling time is as follows:

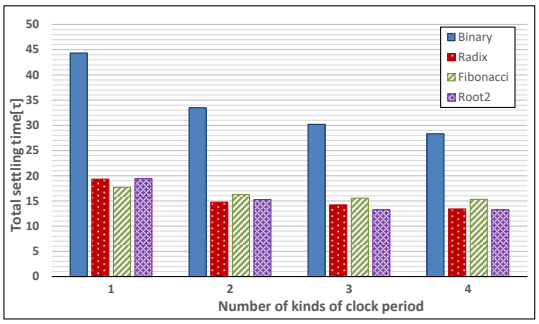


Fig. 9 Comparison of total settling time for each method in 3 types of clock periods.

$$T_{settle}(M-1) = \tau\ln 2^2 = 2 * 0.6931\tau = 1.3862\tau$$

Similarly, when k = M, the settling time is as follows:

$$T_{settle}(M) = \tau\ln 3 = 1.0986\tau$$

These results indicate that the SAR ADC using pseudo-silver-ratio needs only 3 types of settling time. Besides, the settling time at (M-1)-step which is 1.3862τ , is realized by doubling of 0.6931τ. Therefore, if the ADC has a clock period doubling circuit, only two types of clock period to realize incomplete settling is needed. As the incomplete settling time depends on the clock period, this method realized with only two types of clock period has superiority for simplification of circuit.

D. *Comparison of total settling time*

We calculate total settling time of the DAC by using (11) and compare each method. Here we examine the radix method, random method, Fibonacci method, and pseudo-silver-ratio method. We substitute the random method for the round robin algorithm because the round robin algorithm needs to examine a huge number of combinations for reference voltage weight. The random method tries 10,000 times and selects combination realizing the shortest settling time.

We also investigate how much total settling time depends on the number of clock periods. For example, if the ADC can use only one clock period, the total settling time is equal to the longest span of settling time multiplied by the number of steps of the SAR ADC used. We calculate the case using 1~4 types of clock period.

Fig. 9 shows calculation results in case of 8-bit SAR ADCs. We see from this result that the pseudo-silver-ratio method realizes the fastest settling in case of using 3 types of clock period. In an 8-bit SAR ADC using 3 types of clock period, the pseudo-silver-ratio method can reduce settling time by 56.2% from the binary method and by 5.0% from the random method.

We obtain almost the same results in 4, 6, and 10-bit cases. Practically, since the settling time is realized by using only two types of clock period, this method is useful for reduction of the settling time. Besides, we have to note that any method cannot realize shorter settling time than pseudo-silver-ratio method in case using 3 types of settling time. It may indicate that the pseudo-silver-ratio method is the fastest method.

E. Advantages of using pseudo-silver-ratio method

There are two advantages of using the pseudo-silver-ratio method for SAR ADC implementation.

First, ADC needs only few types of clock period. Generally, ADC needs many types of clock periods that correspond to the settling time at each step. However the pseudo-silver-ratio method needs only two types of clock period and it helps to ease circuit design.

Second, the SAR logic circuit can be designed with ease. Table I shows input transitions of 4-bit DAC using the binary method and the pseudo-silver-ratio method. In Table I, the ADC input is 0 LSB and first reference voltage weight p(1)= 2^{N-1} in the pseudo-silver-ratio method is dealt as sum of two 2^{N-2}. As shown in Table I, both methods are controlled in the same way. Therefore pseudo-silver-ratio method can be realized by changing wiring of SAR logic circuit for the binary method. In addition, the pseudo-silver-ratio method eases design of encoder. Typically, a redundant SAR ADC needs large encoder and decoder. But the pseudo-silver-ratio method can use full adder to make encoder. Because reference voltage weight p(k) values are made by putting two binary weights in order, we can encode digital code by addition as shown in Fig. 10. We see from Table I and Fig. 10 that we can realize a redundant SAR ADC using the pseudo-silver-ratio method in the same way as the binary SAR ADC by changing wiring and adding full adder for SAR logic circuit.

VII. CONCLUSIONS

We have described two redundant SAR ADC algorithms to ensure reliability for automotive applications together with micro-controllers. The first one uses Fibonacci sequence and its property called Golden ratio for the digital error correction. Especially, several interesting properties have been clarified that contribute to solve SAR ADC design problems. The second one uses pseudo silver-ratio (square root of 2) for the SAR ADC, which leads to simple SAR logic design and fast conversion speed in case of multiple clock period usage.

We conclude this paper by remarking that here we have demonstrated redundant SAR ADC algorithms to realize reliable electronic systems and also shown that the benefits of the reliability lead to high-speed operation. Our methods do not require special device/process or additional large circuit / major cricuit change; we have used only basic but beautiful mathematics (number theory).

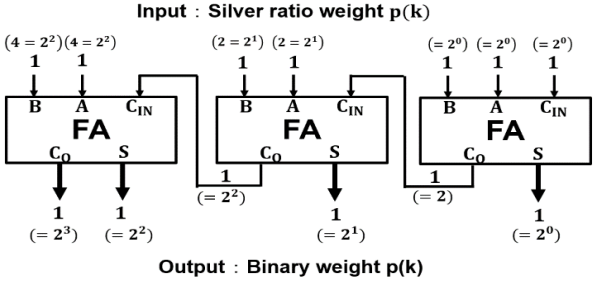


Fig. 10 4-bit encoder in case of using pseudo-silver-ratio weights.

ACKNOWLEDGEMENT

This work is supported in part by JSPS KAKENHI Grant Number 15K13965 as well as Semiconductor Technology Academic Research Center (STARC).

REFERENCES

[1] F. Kuttner. A 1.2V 10b 20MSample/s Non-Binary Successive Approximation ADC in 0.13μm CMOS. Tech. Digest of International Solid-State Circuits Conference, San Francisco. 2002, Feb.

[2] M. Hesener, T. Eichler, A. Hanneberg, D. Herbison, F. Kuttner, H. Wenske: "A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13μm CMOS", Tech. Digest of International Solid-State Circuits Conference, San Francisco (Feb. 2007).

[3] T. Ogawa, H. Kobayashi, Y. Takahashi, N. Takai, M. Hotta, H. San, T. Matsuura, A. Abe, K. Yagi and T. Mori. SAR ADC Algorithm with Redundancy and Digital Error Correction. IEICE Trans. Fundamentals, vol.E93-A, no.2, pp.415- 423. 2010, Feb.

[4] Y. Kobayashi, S. Shibuya, T. Arafune, S. Sasaki, H. Kobayashi : "SAR ADC Design Using Golden Ratio Weight Algorithm", The 15th International Symposium on Communications and Information Technologies 2015, Nara, Japan (Oct. 2015).

[5] H. Nakane, R. Ujiie, T. Oshima, T. Yamamoto, K. Kimura, Y. Okuda, K. Tsuiji, T. Matsuura, "A Fully Integrated SAR ADC Using Digital Correction Technique for Triple-Mode Mobile Transceiver", IEEE J. of Solid-State Circuits, vol. 49, no. 11, pp.2500-2514 (Nov. 2014).

[6] W. Liu, P. Huang, Y. Chiu, "A 12b 22.5/45MS/s 3.0mW 0.059mm^2 CMOS SAR ADC Achieving Over 90dB SFDR", Tech. Digest of International Solid-State Circuits Conference, San Francisco (Feb. 2010).

[7] T. Ogawa, T. Matsuura, H. Kobayashi, T. Takai, M. Hotta, H. San, A. Abe, K. Yagi and T. Mori. Non-binary SAR ADC with Digital Compensation for Comparator Offset Effects. IEICE Trans. vol. J94-C, no.2, pp.68-78. 2010, Mar.

[8] M. Hotta, M. Kawakami, H. Kobayashi, H. San, N. Takai, T. Matsuura, A. Abe, K. Yagi, T. Mori, "SAR ADC Architecture with Digital Error Correction", IEEJ Trans. Electrical and Electronic Engineering, vol.5, no.6, pp.651-659. 2010, Nov.

[9] T. Koshy: Fibonacci and Lucas Numbers with Applications, John Wiley & Sons, Inc. (2001).

Table I. 4-bit DAC input in case of using binary weights and pseudo-silver-ratio weights.

Binary weight		Weight p(k)			
step	Vref(k)[LSB]	8	4	2	1
1	8	1	0	0	0
2	4	0	1	0	0
3	2	0	0	1	0
4	1	0	0	0	1

Silver ratio weight		Weight p(k)						
step	Vref(k)[LSB]	4	4	2	2	1	1	1
1	8	1	1	0	0	0	0	0
2	6	0	1	1	0	0	0	0
3	4	0	0	1	1	0	0	0
4	3	0	0	0	1	1	0	0
5	2	0	0	0	0	1	1	0
6	1	0	0	0	0	0	0	1

IEEE International Symposium on Intelligent Signal Processing and Communication Systems 2017
NOVEMBER 6-9, 2017, XIAMEN, CHINA

Nov. 9 NA-L2 9:00-12:00

Fibonacci Sequence Weighted SAR ADC as Golden Section Search

H. Arai, T. Arafune, S. Shibuya, Y. Kobayashi,
K. Asami, H. Kobayashi

Gunma University

Kobayashi Laboratory

群馬大学
GUNMA UNIVERSITY

OUT LINE

- Introduction
- SAR ADC & Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

OUT LINE

- Introduction
- SAR ADC & Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

Background

Automotive electronics are in spotlight

High-speed, Reliable

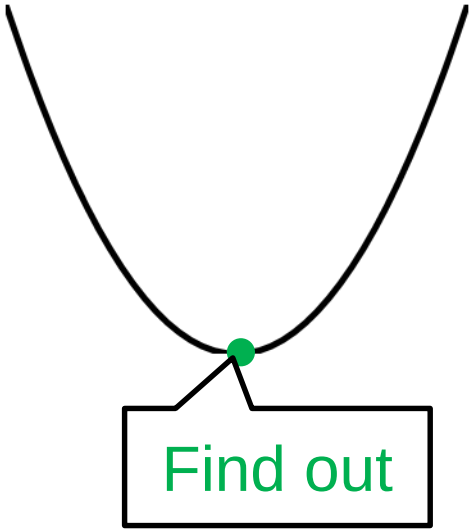
"SAR ADC" in microcontroller is needed.

In my laboratory

We have discovered various properties of SAR ADC using Fibonacci sequence.

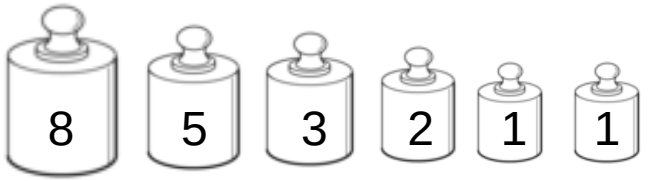
New Discovery

SAR ADC based on
golden section search
using unimodal function



equivalent

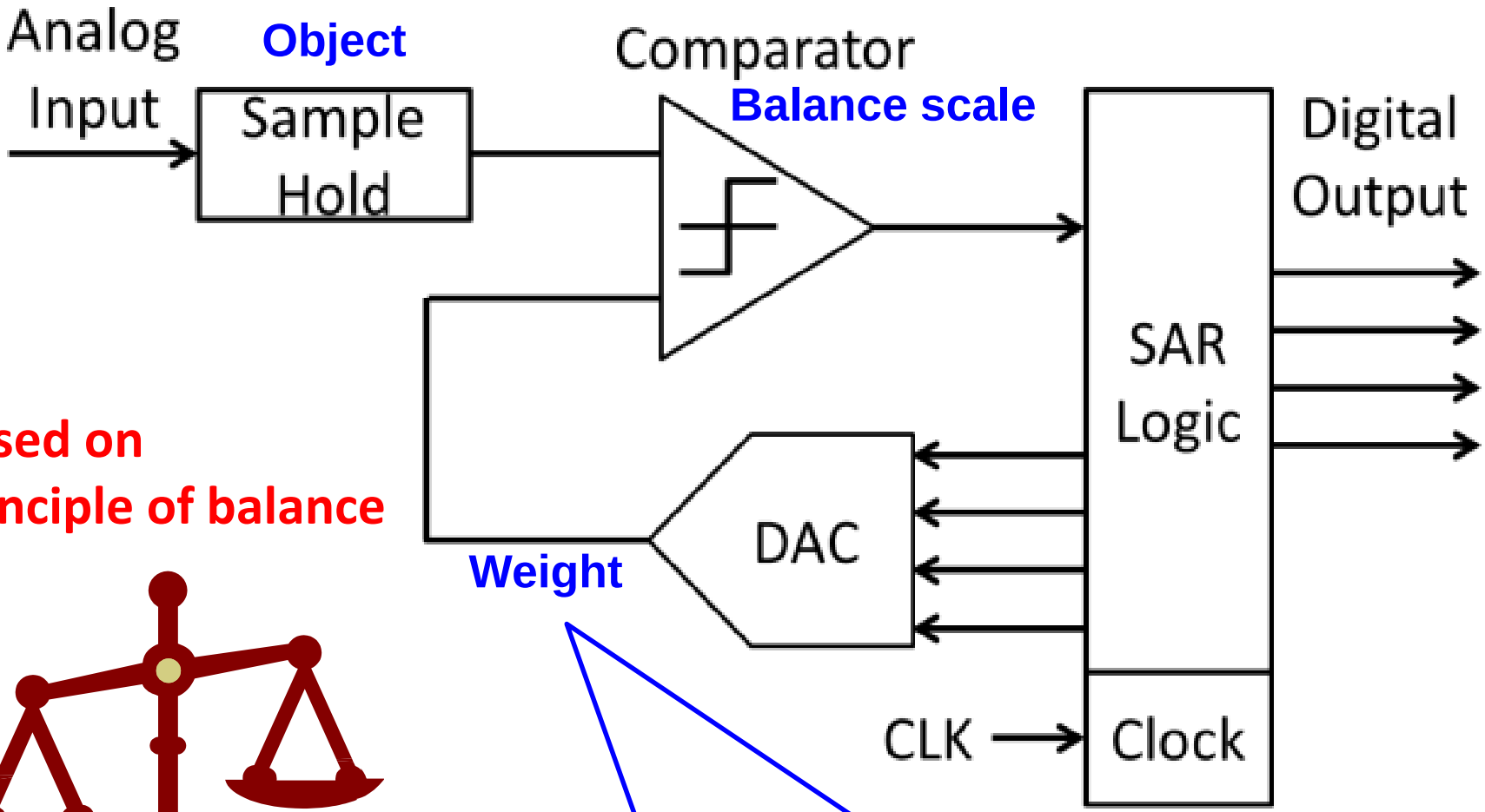
Fibonacci sequence weighted SAR ADC



OUT LINE

- Introduction
- SAR ADC & Redundancy Design
  - SAR ADC
  - SAR ADC Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

SAR ADC Configuration



Based on principle of balance

Generally use binary weight

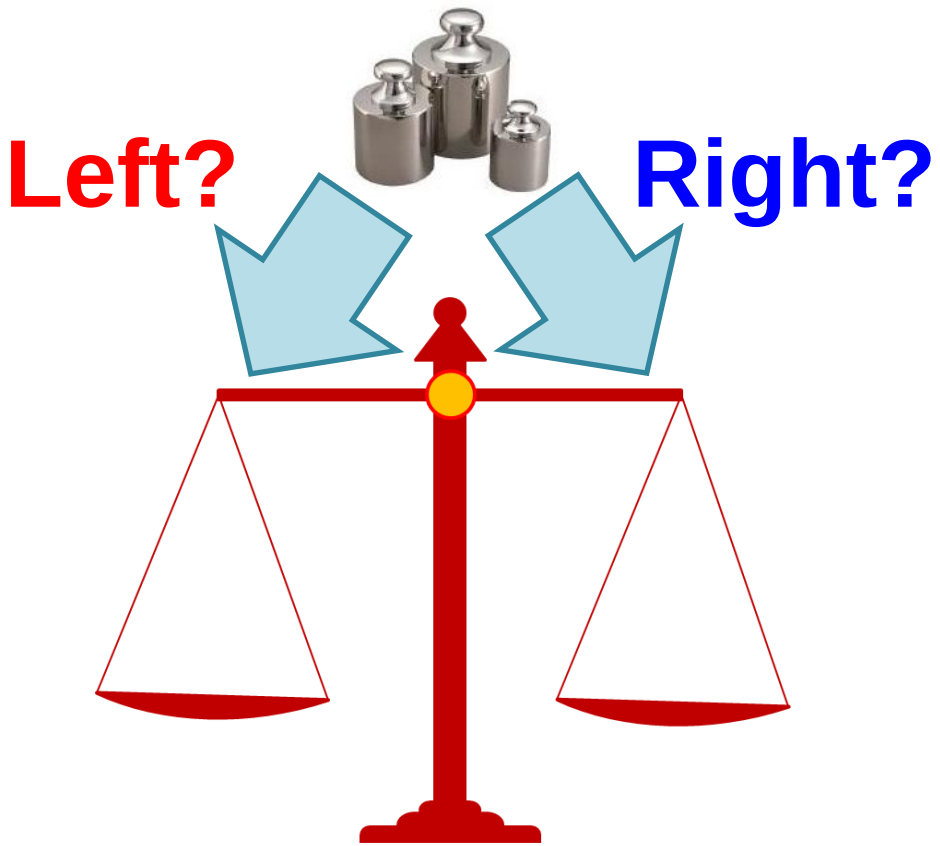
(1 , 2 , 4 , 8 , 16 , 32, 64 …)

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input：7.3 [V]
- Binary weight :

16, 8, 4, 2, 1



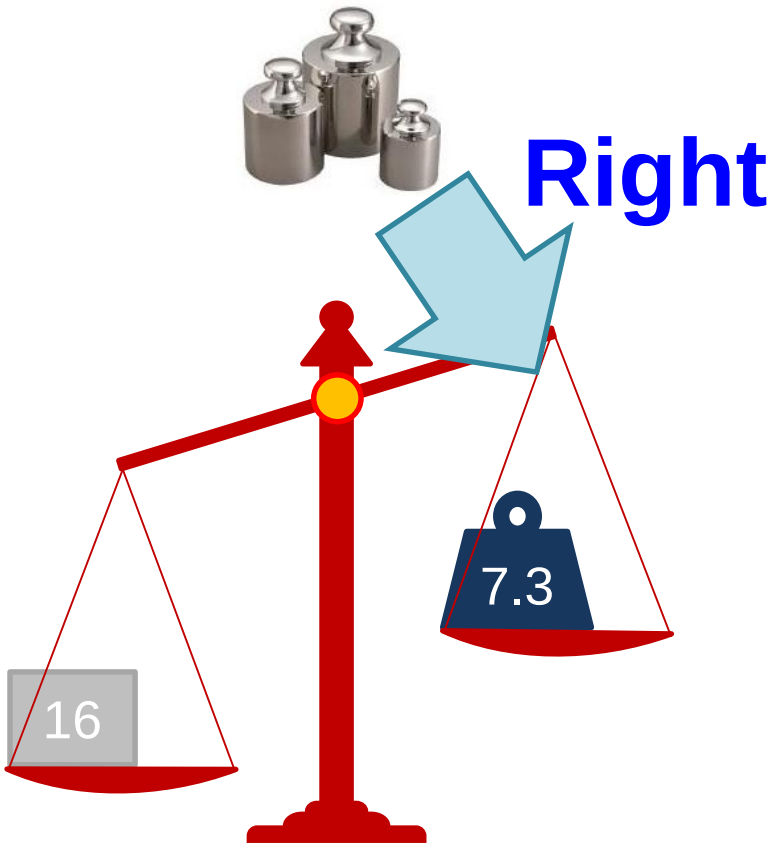
Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
Level	31						31
	30						30
	29						29
	28						28
	27						27
	26						26
	25						25
	24						24
	23						23
	22						22
	21						21
	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input：7.3 [V]
- Binary weight :

8, 4, 2, 1



Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
Level	31						31
	30						30
	29						29
	28						28
	27						27
	26						26
	25						25
	24						24
	23						23
	22						22
	21						21
	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1						1
	0						0

Down!

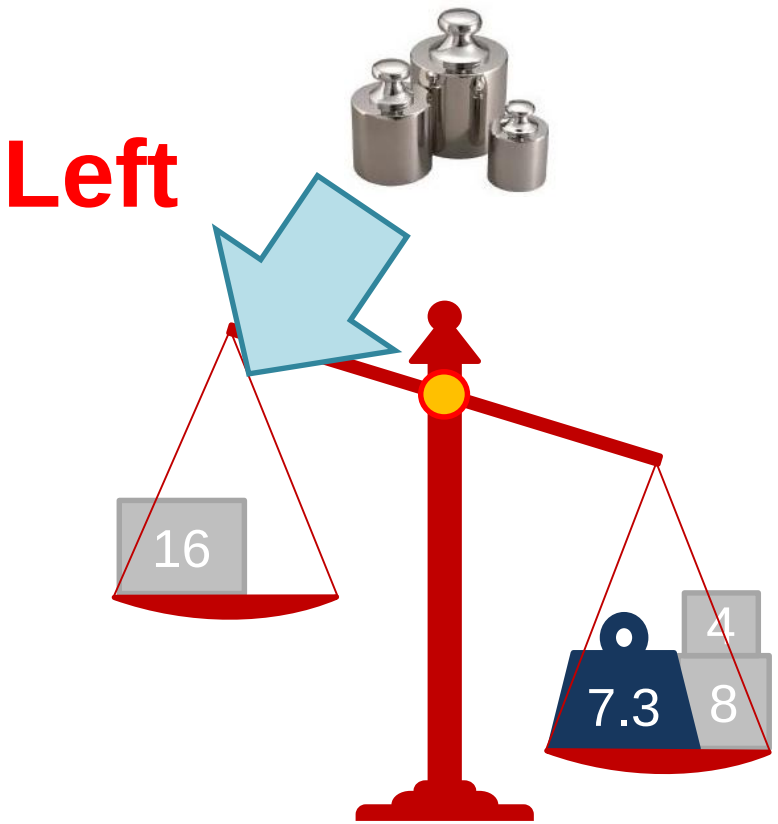
0

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input：7.3 [V]
- Binary weight :

2, 1



Step		1st	2nd	3rd	4th	5th	output
Weight p(k)		16	8	4	2	1	
Level	31						31
	30						30
	29						29
	28						28
	27						27
	26						26
	25						25
	24						24
	23						23
	22						22
	21						21
	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10			UP!			10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3	0	0	1			3
	2						2
	1						1
	0						0

Binary Search SAR ADC Operation

5bit-5step SAR ADC

- Analog Input：7.3 [V]
- Binary weight :

$$7.3 \Rightarrow 00111 \Rightarrow 7$$

$$16 - 8 - 4 + 2 + 1 + 0.5 - 0.5 = 7$$

Step	1st	2nd	3rd	4th	5th	output
Weight p(k)	16	8	4	2	1	
Level 31						31
30						30
29						29
28						28
27						27
26						26
25						25
24						24
23						23
22						22
21						21
20						20
19						19
18						18
17						17
16						16
15						15
14						14
13						13
12						12
11						11
10						10
9						9
8						8
7						7
6						6
5						5
4						4
3	0	0	1	1	1	3
2						2
1						1
0						0

OUT LINE

- Introduction
- SAR ADC & Redundancy Design
  - SAR ADC
  - SAR ADC Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

SAR ADC Redundancy Design

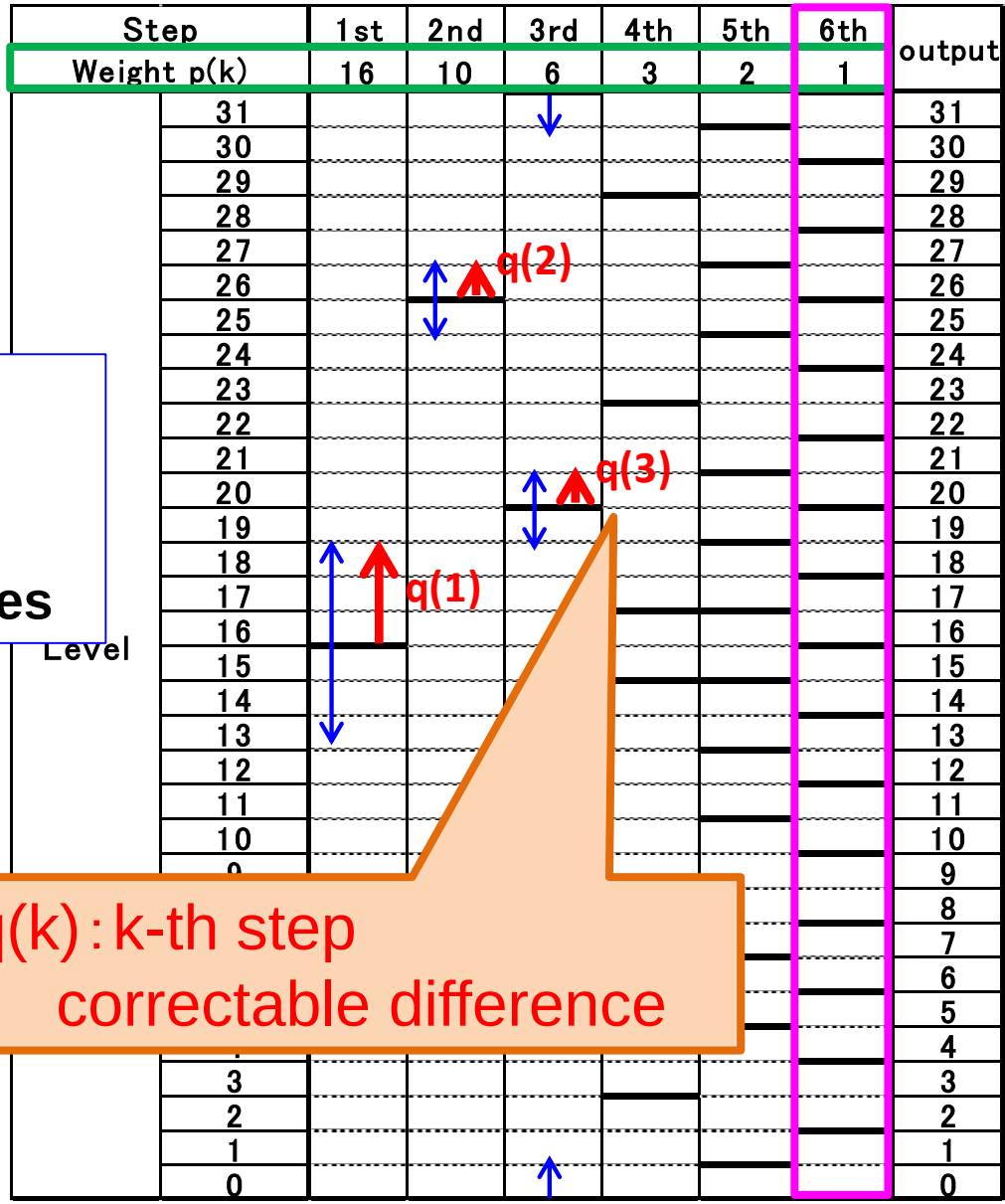
Redundancy

➡ Surplus, Extra

Using time redundancy

- **Extra comparison steps**
- **Change reference to Non-binary voltages**

Enable digital error correction!



Redundancy Design Operation(No Error)

4bit-5step SAR ADC

- Analog input : 6.3
- Redundant weight :

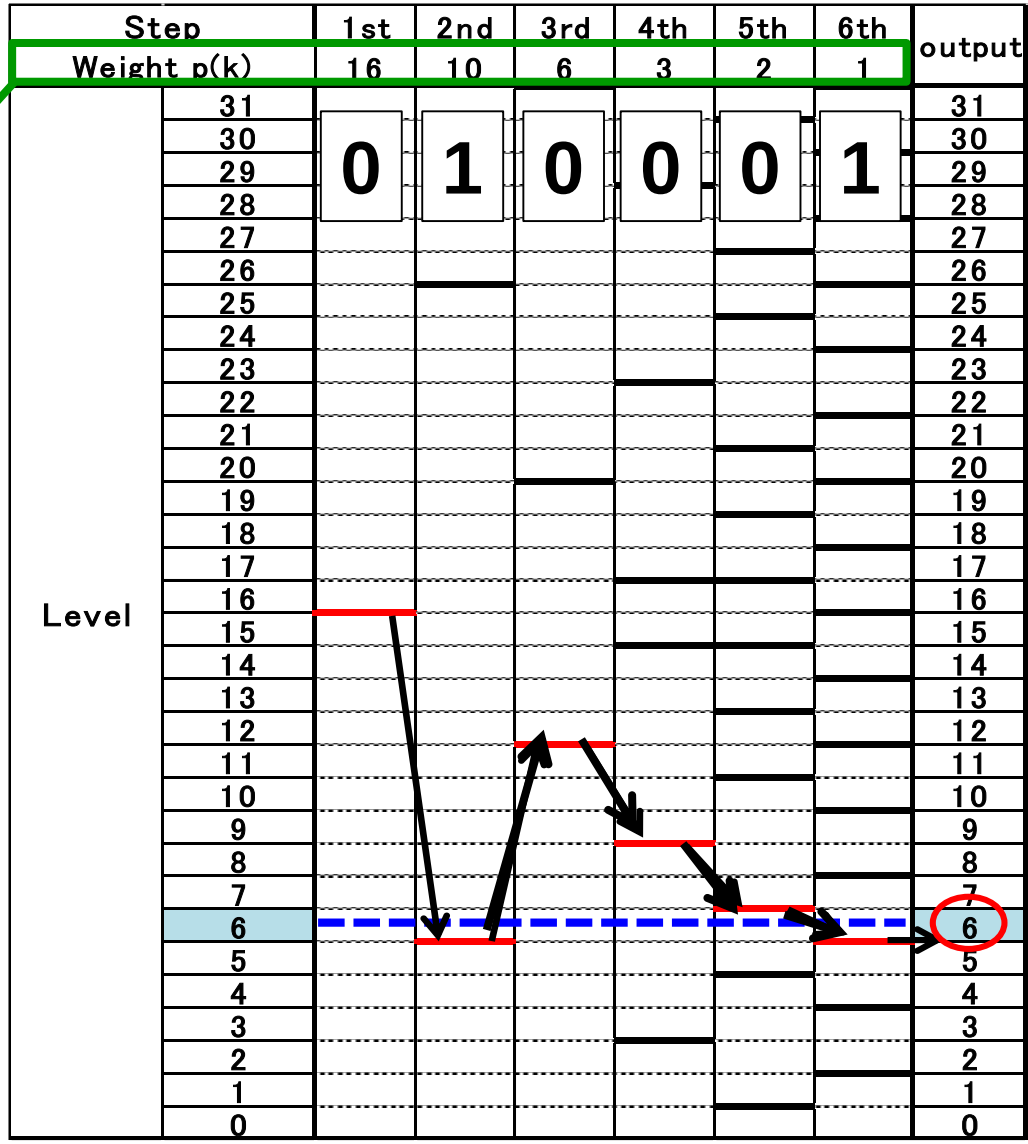
  16, 10, 6, 3, 2, 1

Correctable expression

6.3⇒010001⇒6

$$16 - 10 + 6 - 3 - 2 - 1 + 0.5 - 0.5$$

=6



Redundancy Design Operation(One Error)

4bit-5step SAR ADC

- Analog input：6.3
- Redundant weight :

  16, 10, 6, 3, 2, 1

Correctable expression

6.3⇒010001⇒6

Another expression

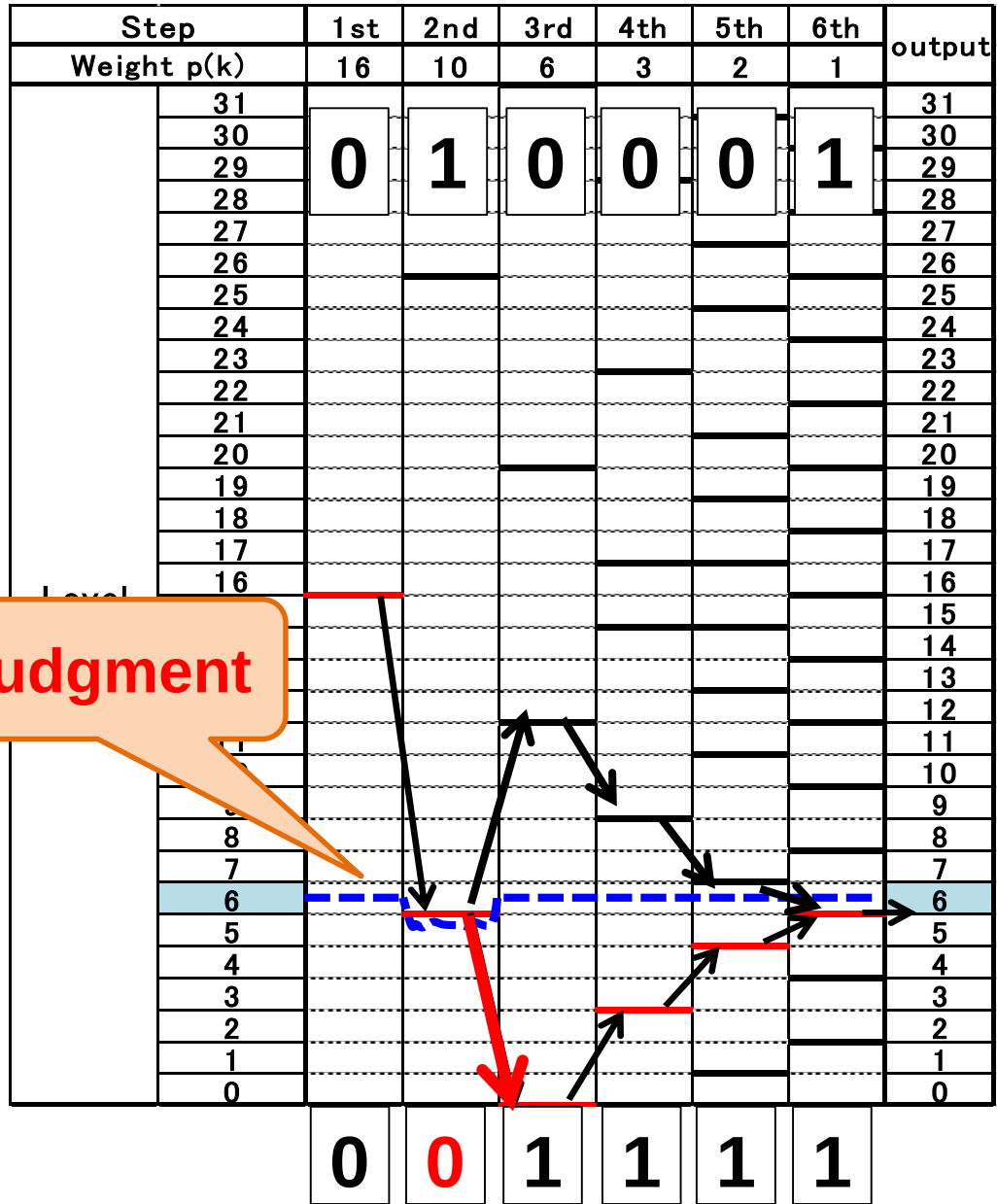
6.3⇒001111⇒6

$16 - 10 - 6 + 3 + 2 + 1 + 0.5 - 0.5$

$= 6$

Error correction

High-Reliability

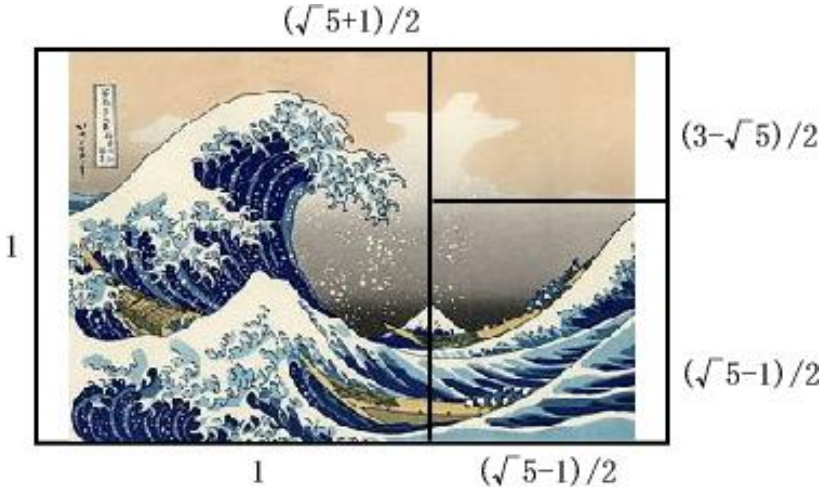


OUT LINE

- Introduction
- SAR ADC & Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

Golden Ratio

- Ratio satisfying $a : b = b : (a + b)$
- $\phi = \frac{b}{a} = \frac{1+\sqrt{5}}{2} = 1.618033988749895\cdots$
- The most beautiful ratio



Fibonacci Sequence

Definition (n=0,1,2,3…)

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1}$$

Fibonacci number

$$0, 1, 1, \mathbf{2}, 3, 5, \mathbf{8}, 13, 21, 34, \mathbf{55} \ldots$$

Property

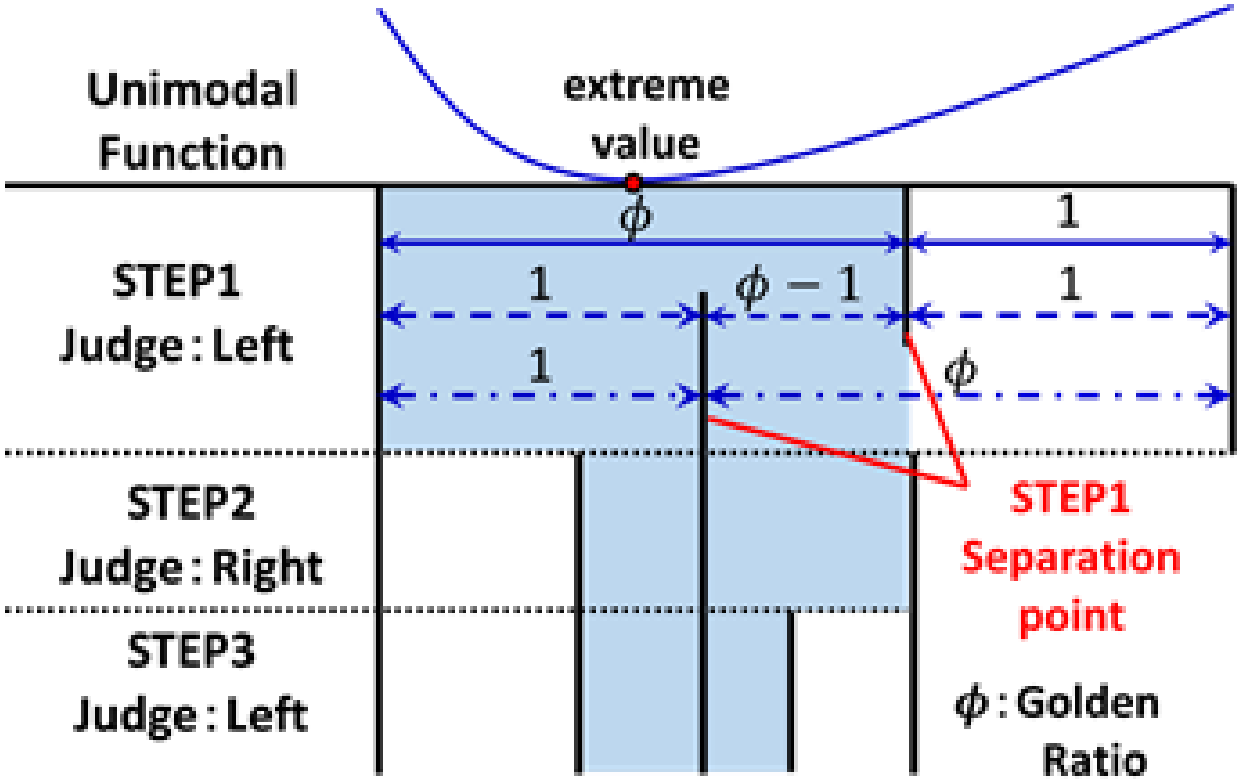
The closest terms ratio converges to *"Golden Ratio"* !

$$\lim_{n\to\infty} \frac{F_n}{F_{n-1}} = 1.6180339887 \ldots = \phi$$

Golden Section Search

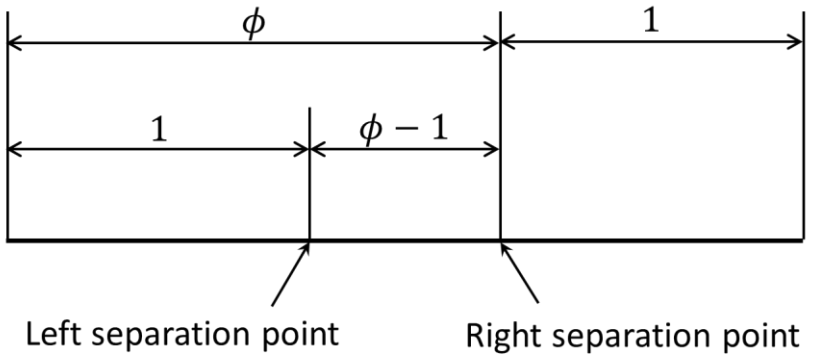
Finding of effectively extreme value of unimodal function

Division ratio = Golden ratio



Fibonacci Search

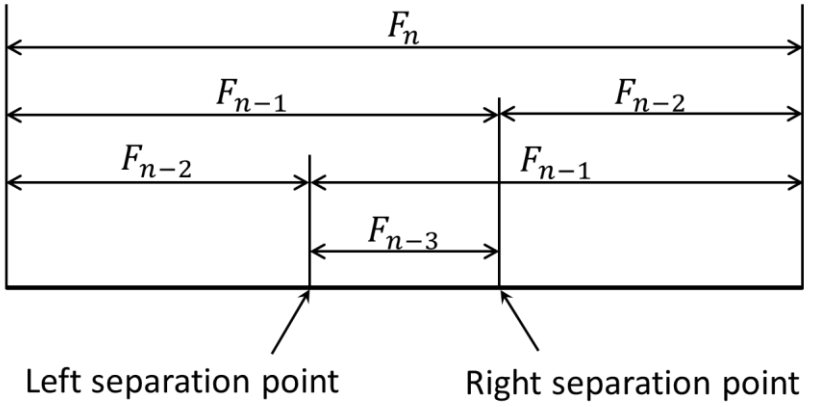
Golden Section Search
(ϕ:Golden ratio)



ADC treats only integers ⇒ **Difficult to realize**

Performing golden division with only integers

Fibonacci search
(F_x:Fibonacci number)



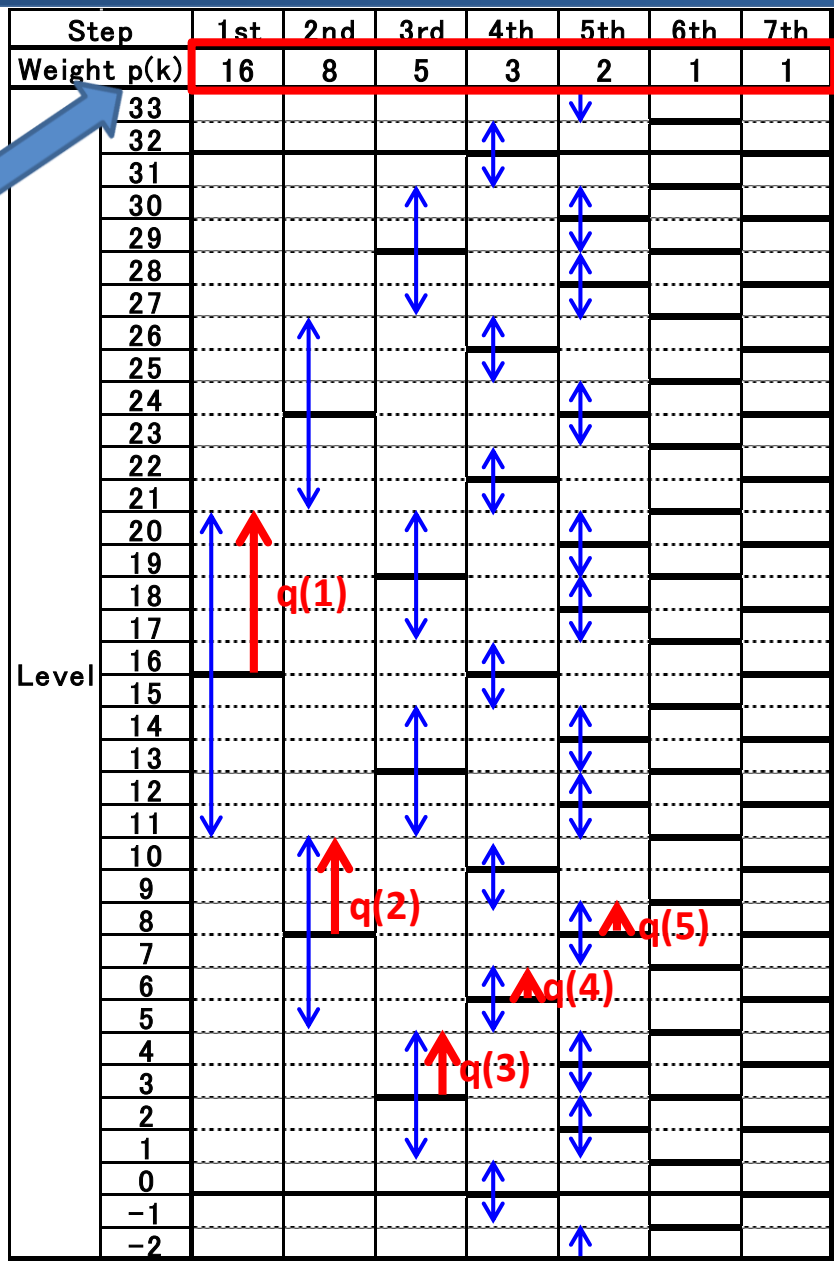
OUT LINE

- Introduction
- SAR ADC & Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

Fibonacci Sequence Weighted SAR ADC

Fibonacci sequence SAR ADC

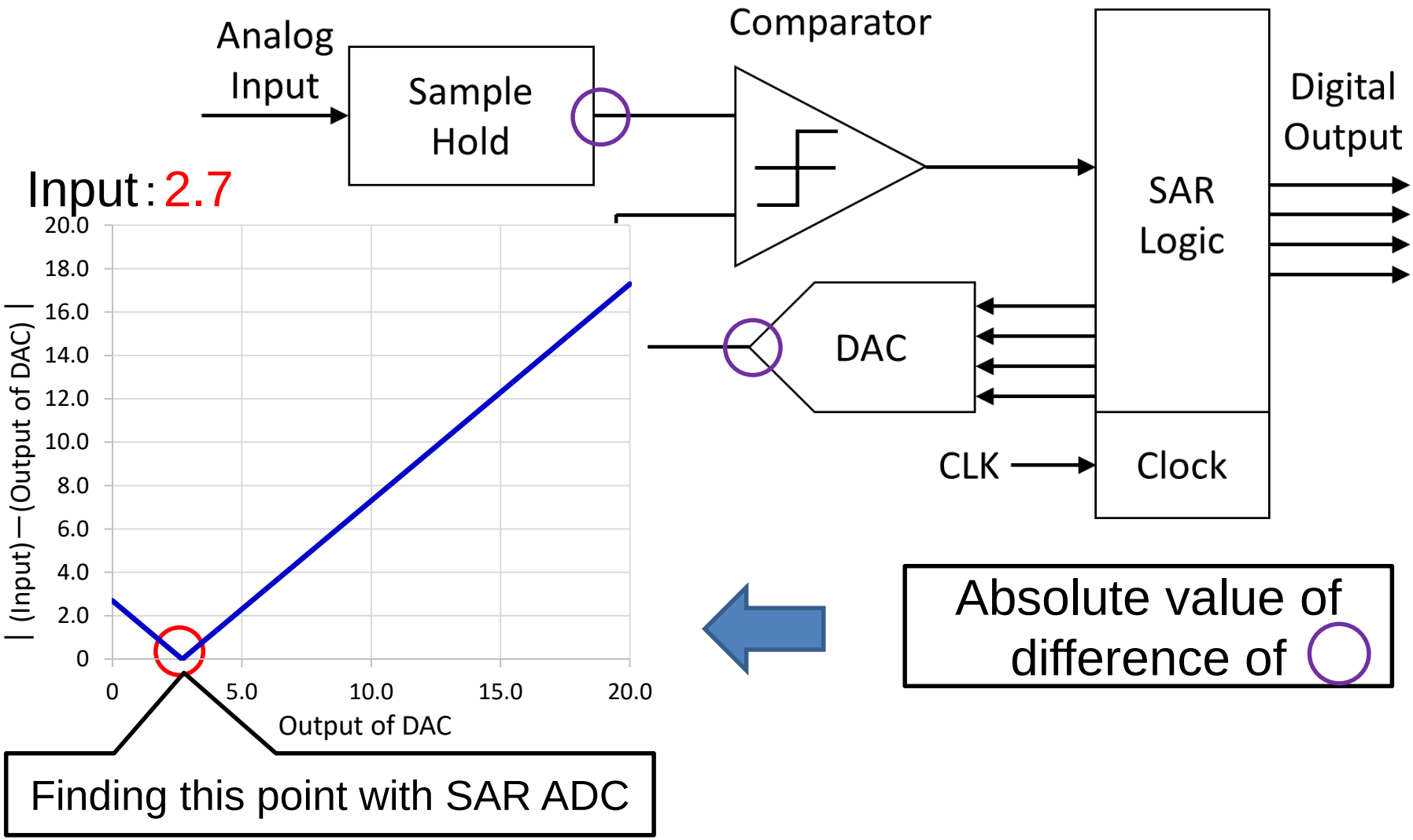
Weight is Fibonacci sequence



OUT LINE

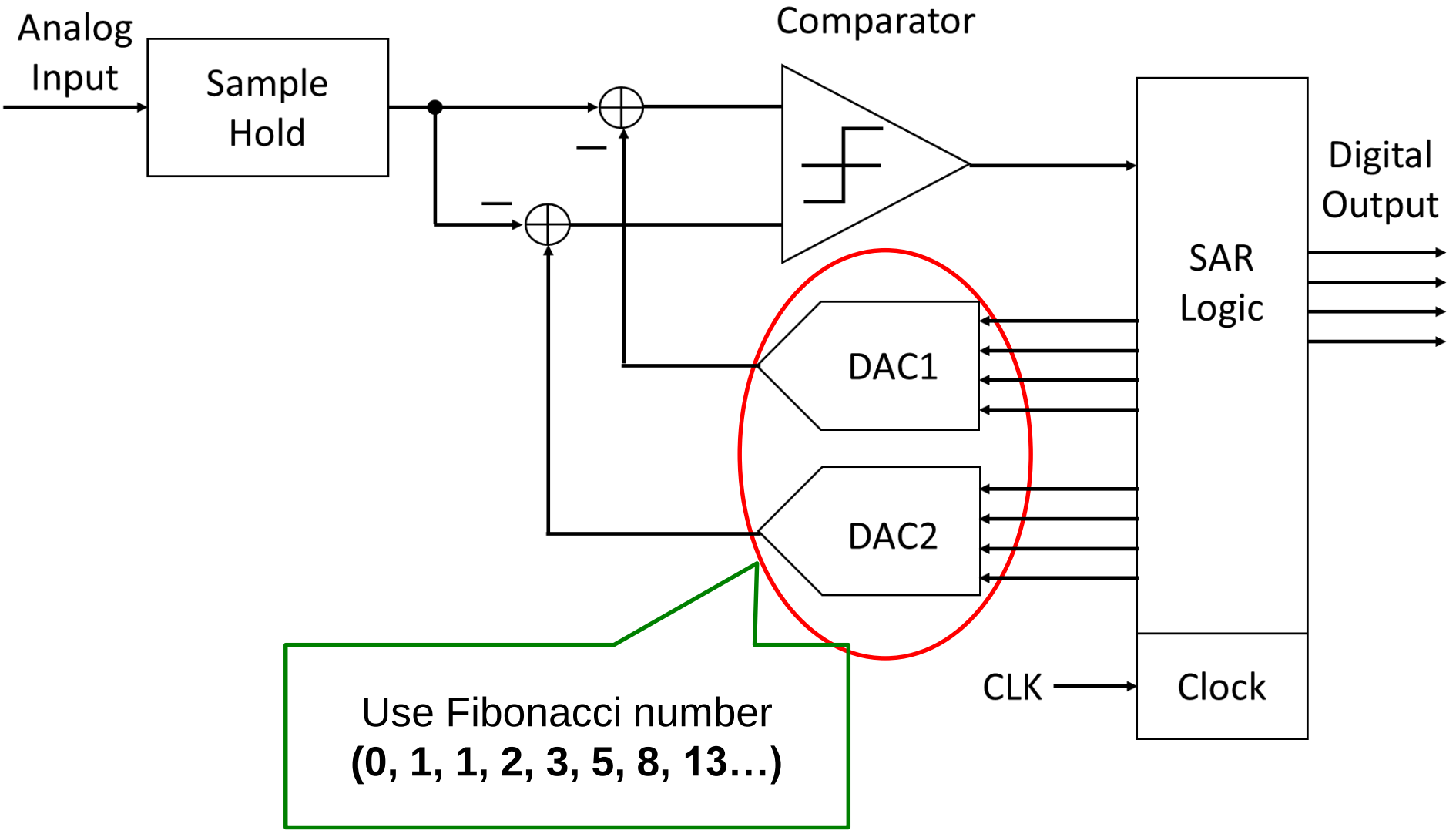
- Introduction
- SAR ADC & Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
  - SAR ADC Based on Fibonacci Search
  - Revised SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

SAR ADC Based on Fibonacci Search

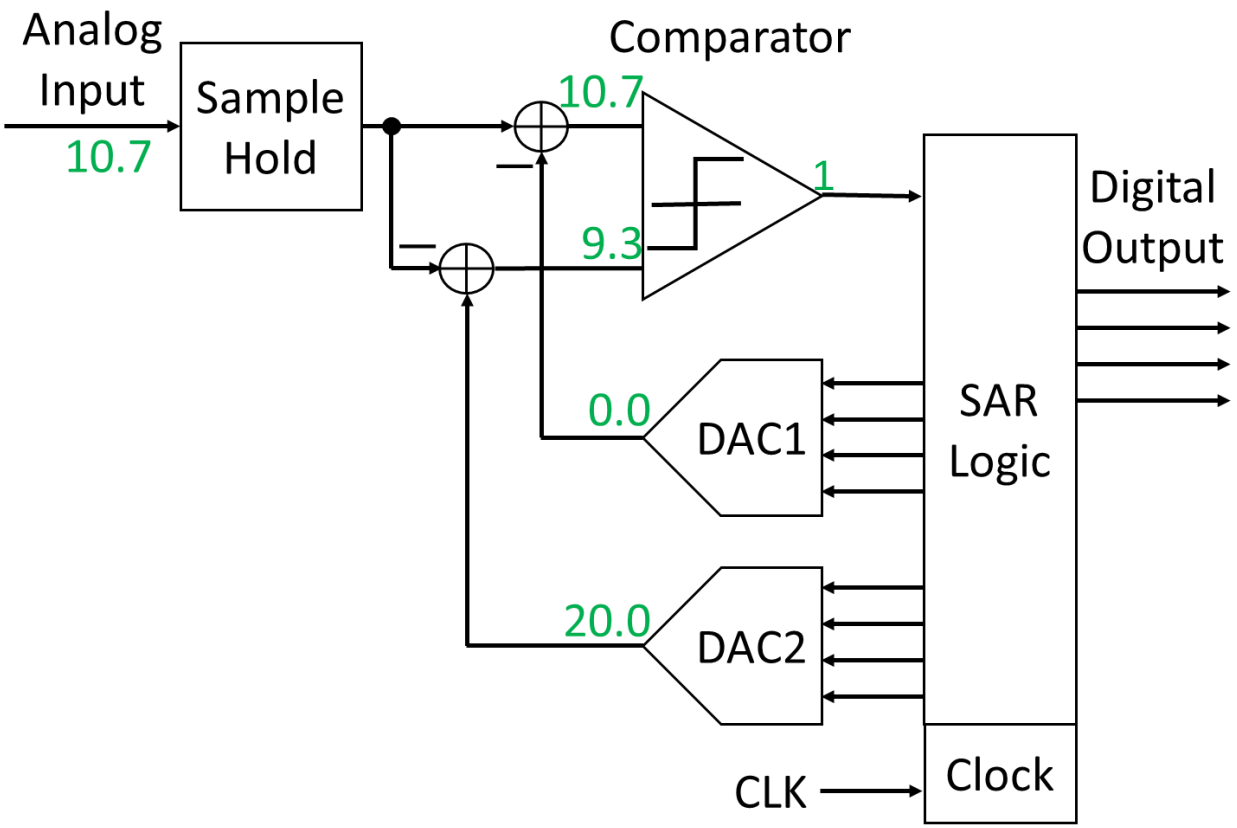


Unimodal function with local minimum → Use Fibonacci search

Block Diagram of SAR ADC Based on Fibonacci Search



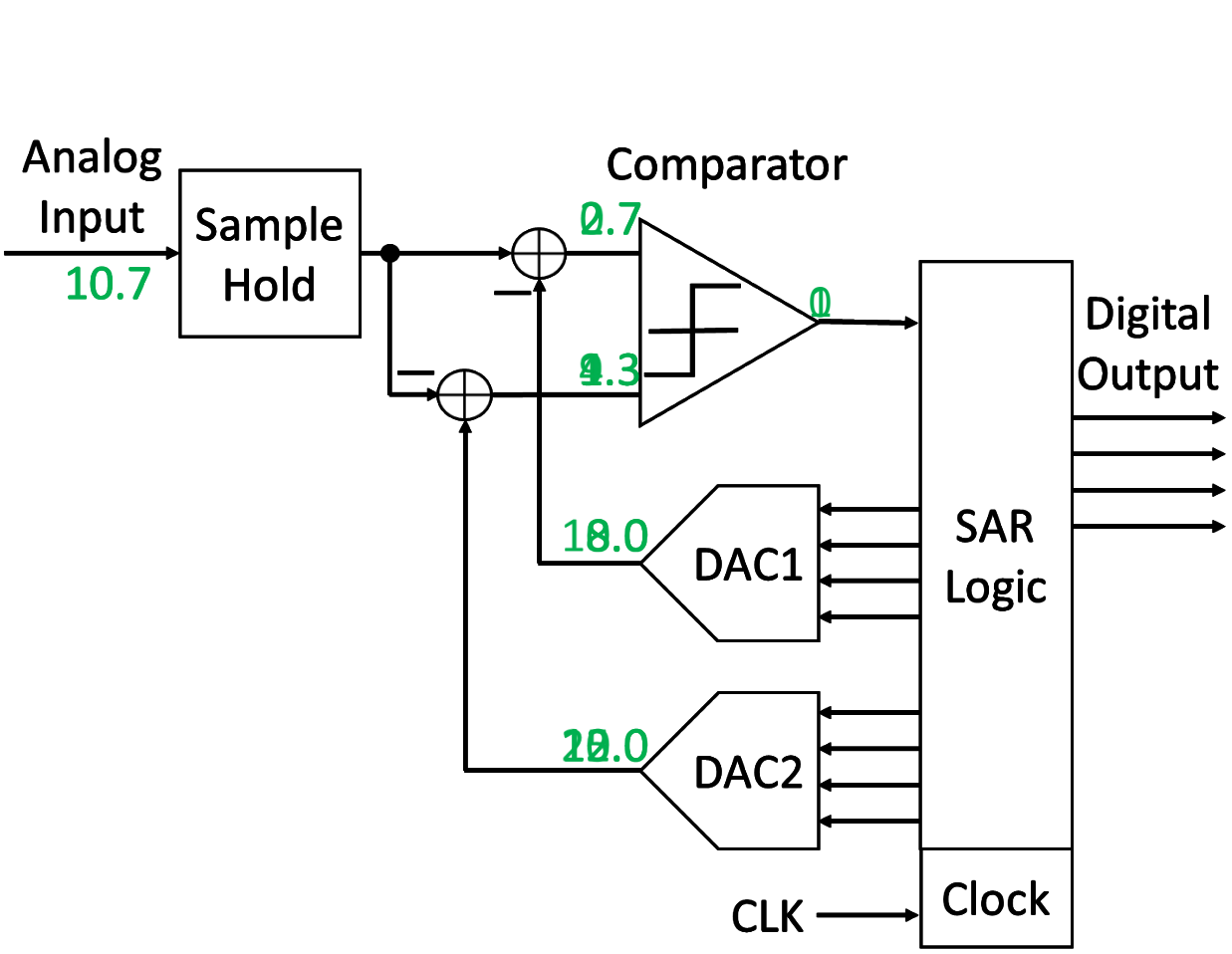
Operation of SAR ADC Based on Fibonacci Search



step	1st	2nd	3rd	4th	5th	output
20						20
19						19
18						18
17						17
16	9.3					16
15						15
14						14
13						13
12						12
11						11
10						10
9						9
8						8
7						7
6						6
5						5
4	10.7					4
3						3
2						2
1	1					1
0						0
−1						−1

Level

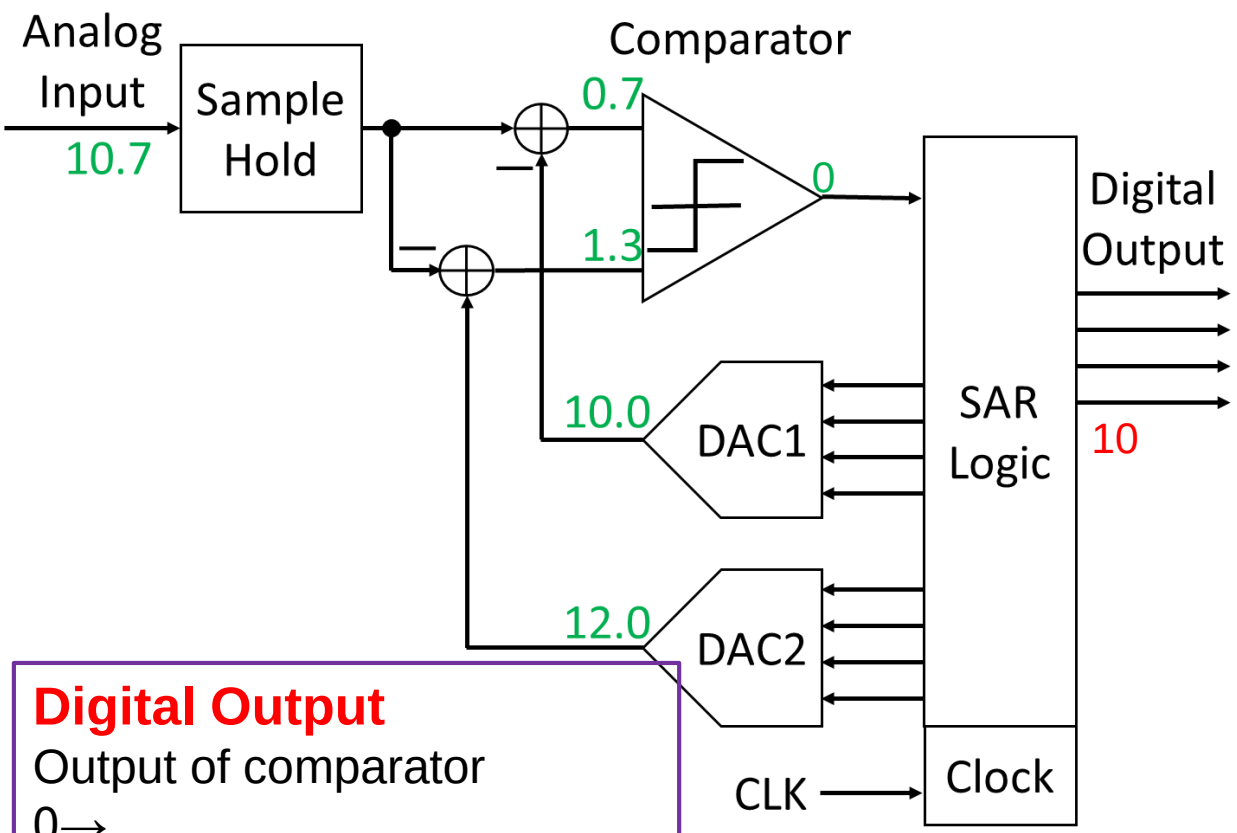
Operation of SAR ADC Based on Fibonacci Search



step	1st	2nd	3rd	4th	5th	output
20						20
19						19
18						18
17						17
16						16
15						15
14						14
13						13
12						12
11						11
10						10
9						9
8						8
7						7
6						6
5						5
4						4
3						3
2						2
1	1	0	0	1	0	1
0						0
-1						-1

Level

Operation of SAR ADC Based on Golden Section Search



step		1st	2nd	3rd	4th	5th	output
Level	20						20
	19						19
	18						18
	17						17
	16						16
	15						15
	14						14
	13						13
	12						12
	11						11
	10						10
	9						9
	8						8
	7						7
	6						6
	5						5
	4						4
	3						3
	2						2
	1	1	0	0	1	0	1
	0						0
	-1						-1

Digital Output

Output of comparator

0→

(Digital input of DAC1)

1→

(Digital input of ADAC1)+1

OUT LINE

- Introduction
- SAR ADC & Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
  - SAR ADC Based on Fibonacci Search
  - Revised SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

Revised SAR ADC Based on Fibonacci Search

Comparison method before change

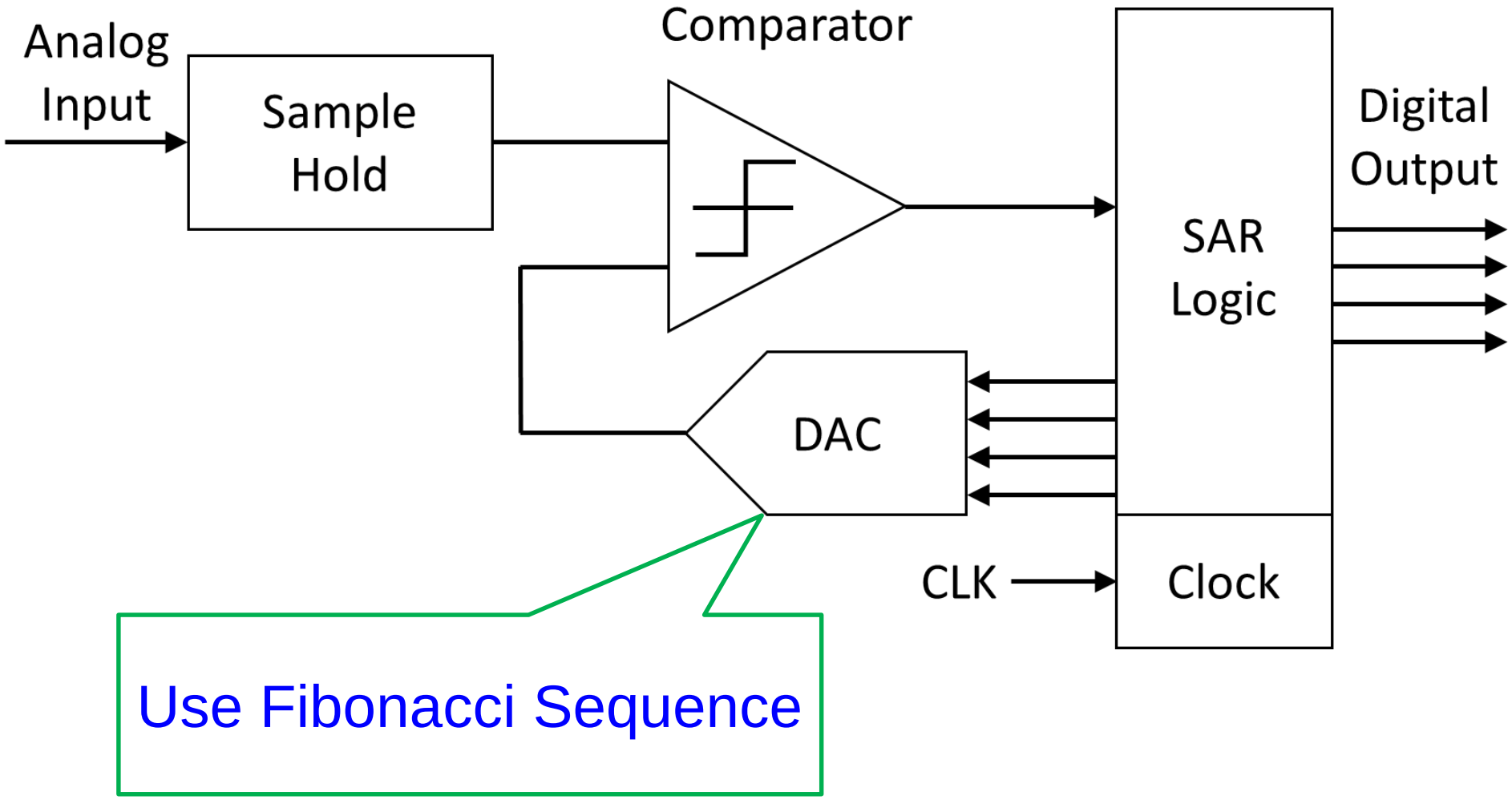
$$V_{in} - DAC1(\geq or \leq)DAC2 - V_{in}$$

$$2V_{in}(\geq or \leq)DAC1 + DAC2$$

$$V_{in}(\geq or \leq)\frac{1}{2}(DAC1 + DAC2)$$

Equivalent comparison method

Block Diagram of Revised SAR ADC Based on Fibonacci Search



Operation & DAC Revised SAR ADC Based on Fibonacci Search

Operation

1st step
Half the total current(20I)
$S_{L1}\sim S_{L6} \rightarrow ON$

Judgment:1

2nd step
Half the total current + 8I(28I)
$S_{L1}\sim S_{L6} + S_{R6} \rightarrow ON$

1

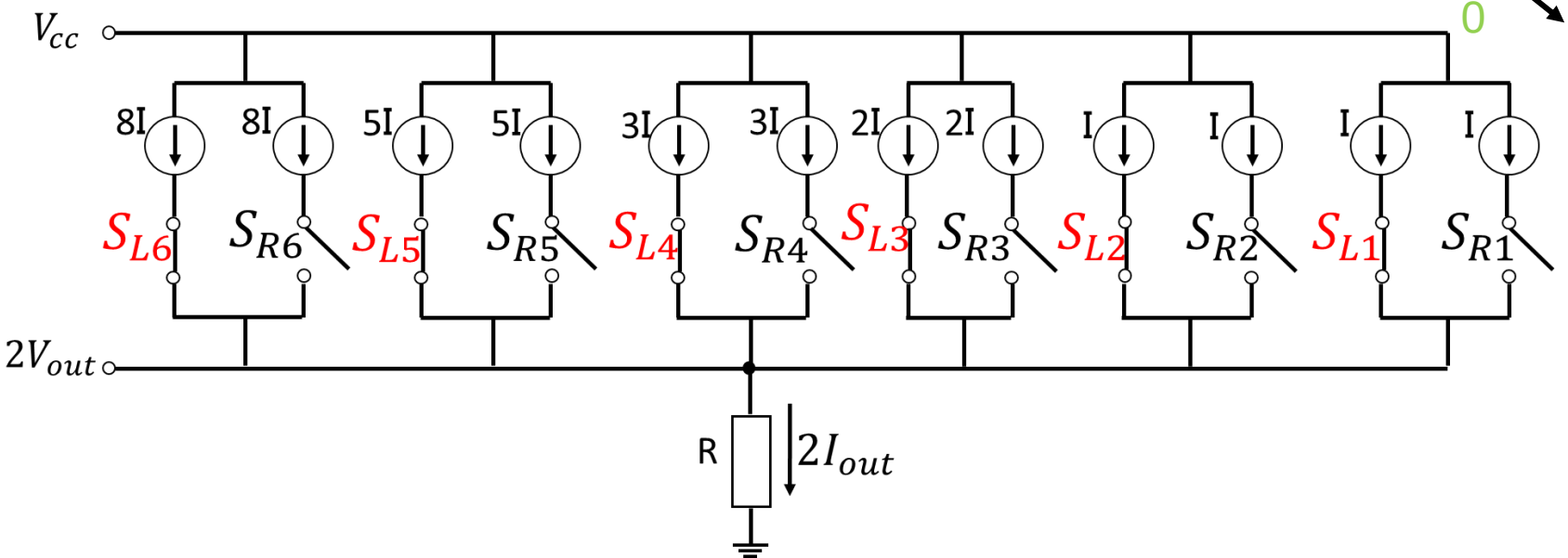
Judgment:0

2nd step
Half the total current - 8I(12I)
$S_{L1}\sim S_{L5} \rightarrow ON$

0

1

0



Revised SAR ADC Based on Fibonacci Search

Revised SAR ADC Based on Golden Section Search

Input 10.7

Output 10

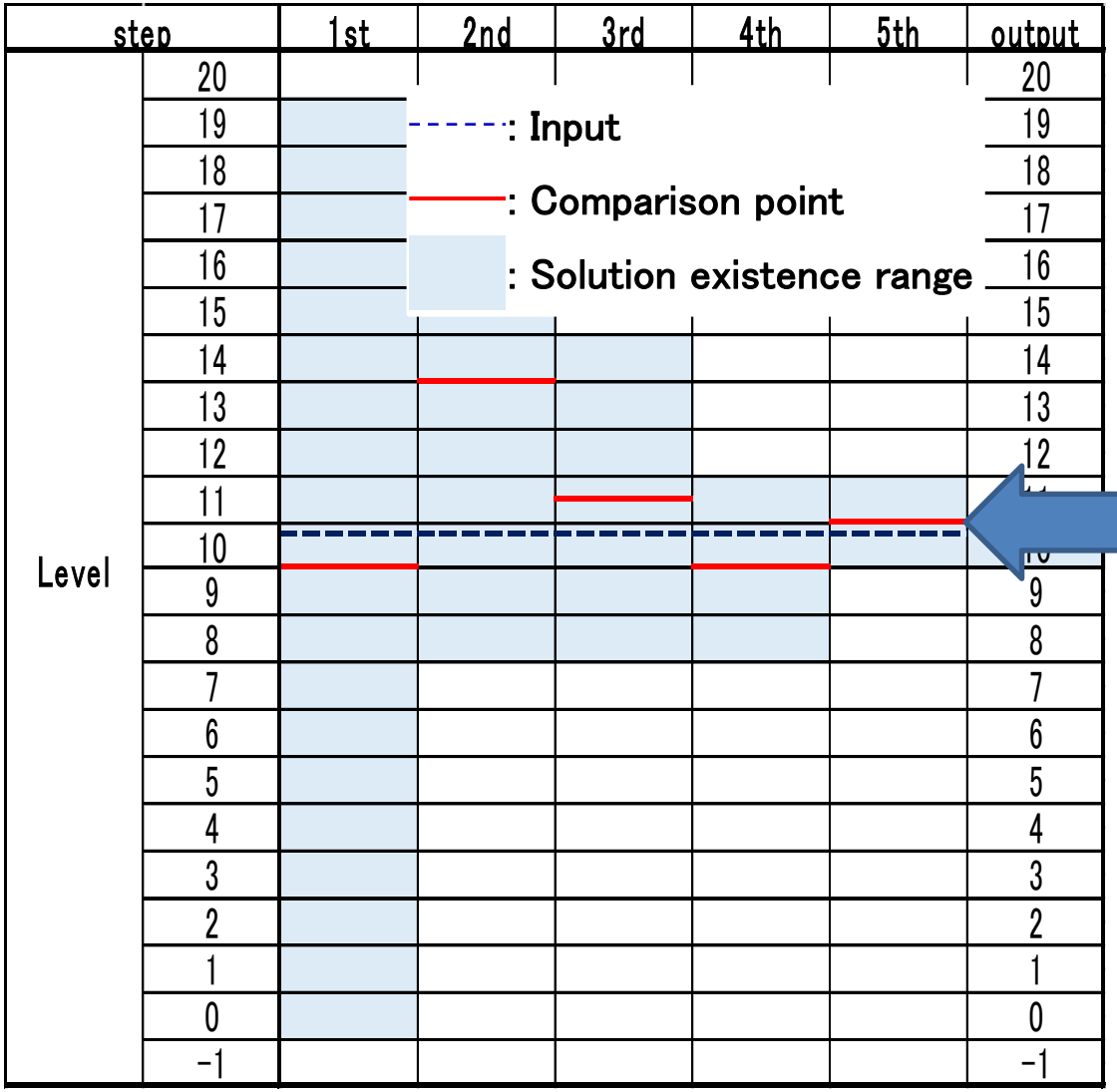
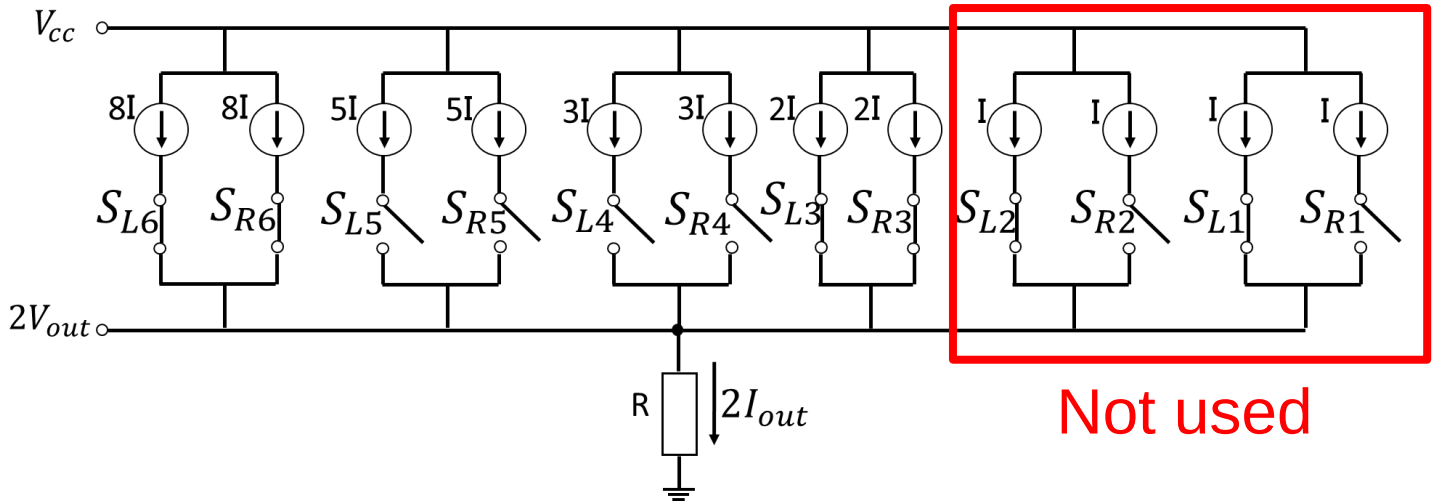


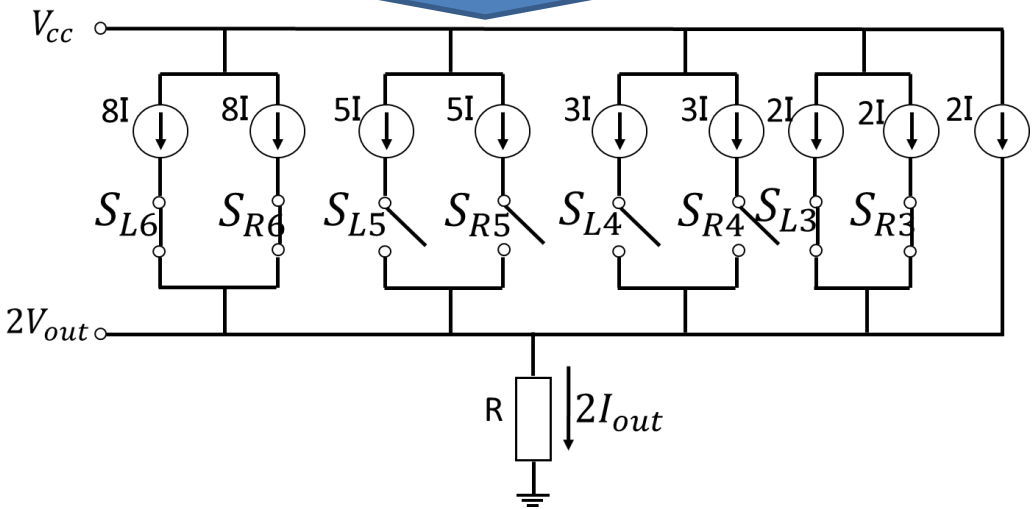
Figure of DAC at this time

Final Step of Revised SAR ADC Based on Fibonacci Search

DAC of final step



Further revised

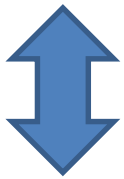


OUT LINE

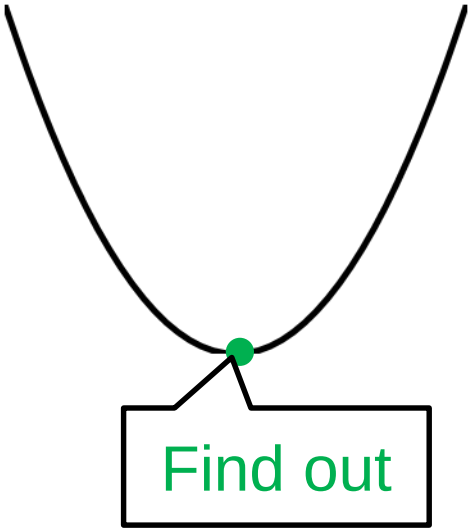
- Introduction
- SAR ADC & Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

Proof Contents

SAR ADC based on
golden section search
using unimodal function



equivalent



Fibonacci sequence weighted SAR ADC

Prove above

Proof by Mathematical Expression

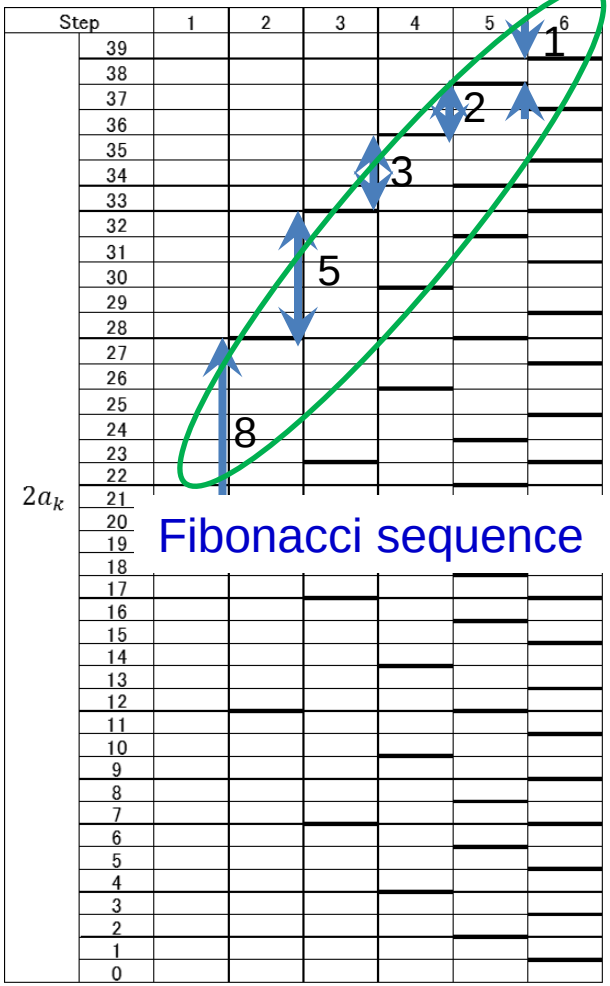
Fibonacci sequence

$$F_0 = 0$$
$$F_1 = 1$$
$$F_{n+2} = F_n + F_{n+1}$$

Comparison voltage

$$2a_k = (F_n + F_{n-1} + \cdots + F_1) + (\pm F_n \pm F_{n-1} \pm \cdots \pm F_1)$$

Comparison voltage when n=6



Difference of comparison voltages is Fibonacci sequence

Matches Fibonacci sequence weighted SAR ADC

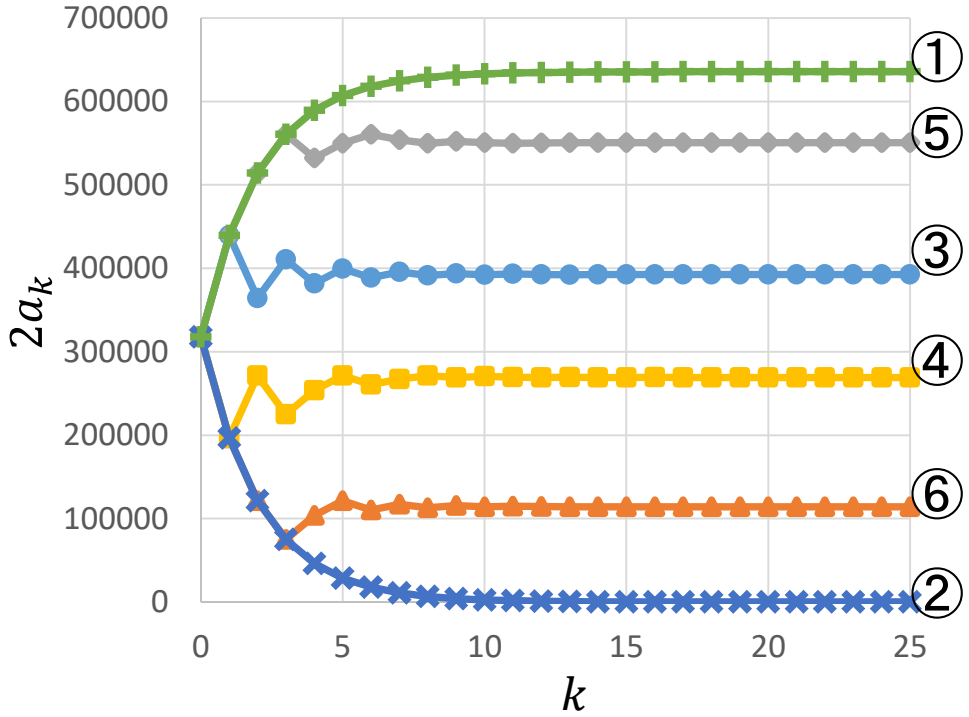
Simulation

Simulation condition

$$①V_{in} = 0,\ ②\ V_{in} = 317810,\ ③V_{in} = 196231.78,$$
$$④V_{in} = 57096.156,\ ⑤V_{in} = 275302.91,\ ⑥V_{in} = 134576.64$$

Convergence prediction

① 0, ② 635620, ③ 392462, ④ 114192, ⑤ 550604, ⑥ 269152



All converged to intended value

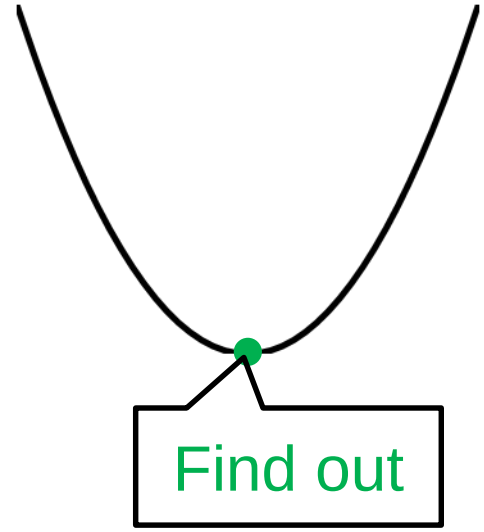
※ $n = 26$

OUT LINE

- Introduction
- SAR ADC & Redundancy Design
- Golden Section Search & Fibonacci Search
- Fibonacci Sequence Weighted SAR ADC
- SAR ADC Based on Fibonacci Search
- Proof & Simulation
- Conclusion

Conclusion

New Theorem

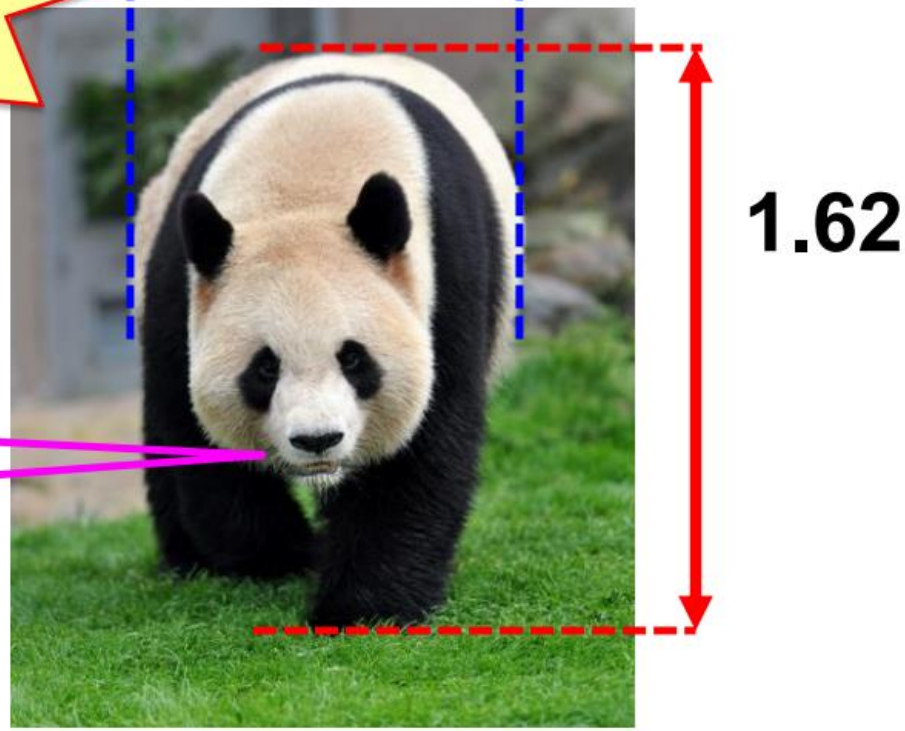


Equivalency

- SAR ADC using golden section search
- Fibonacci sequence weighted SAR ADC

Thank you for listening

Golden Ratio

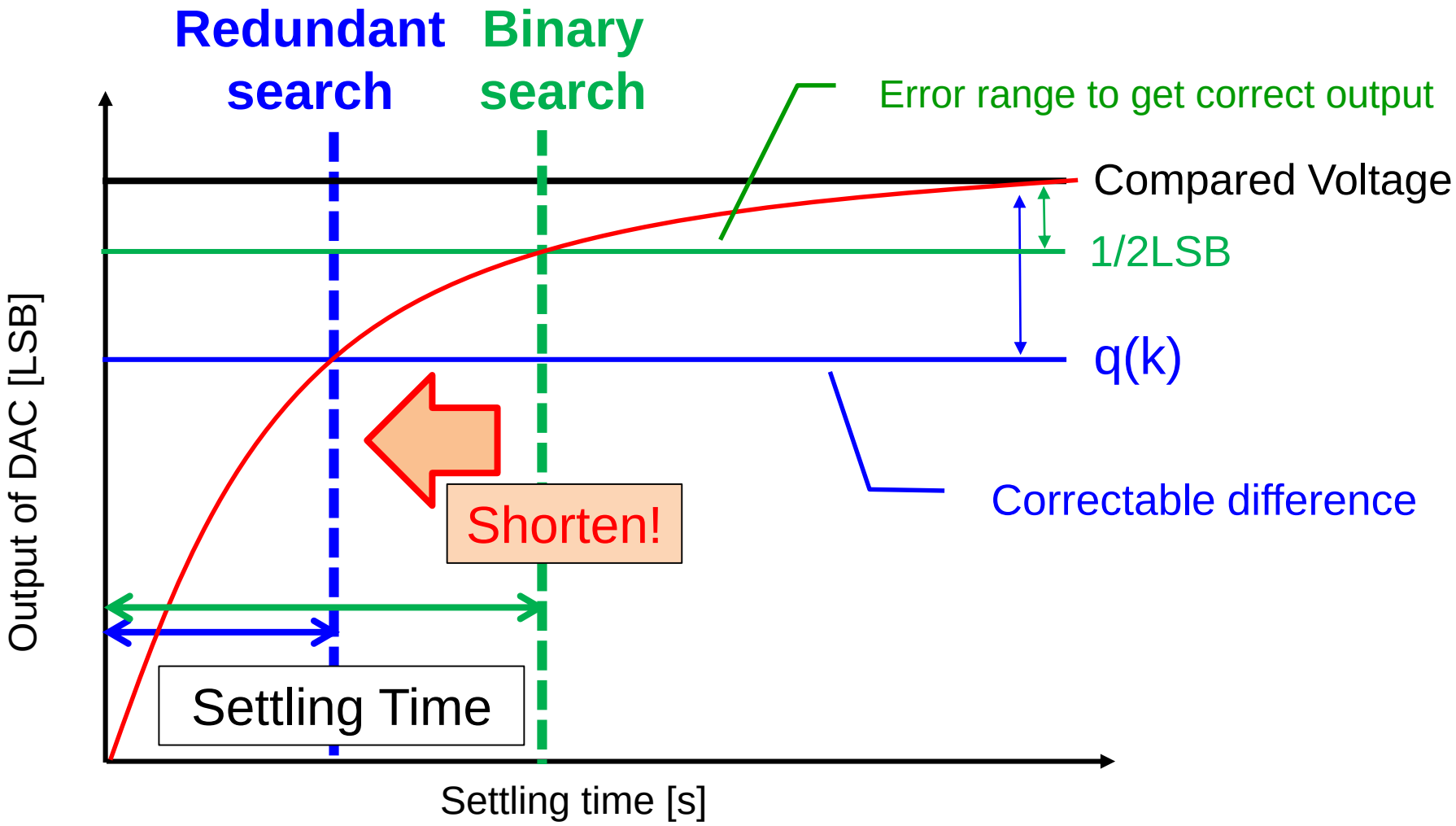


謝謝

appendix

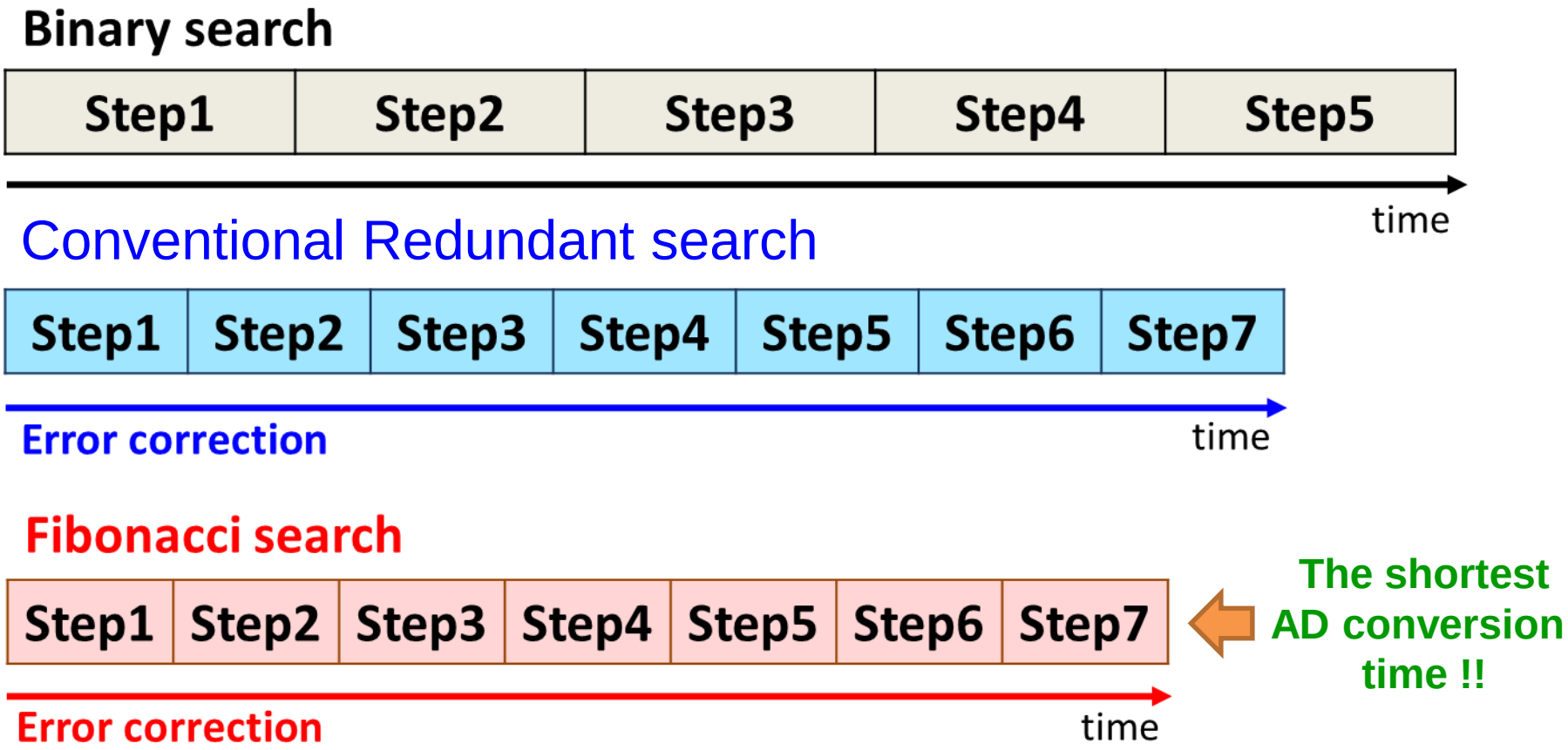
DAC Settling Time at Every Step

Shorten Conversion time

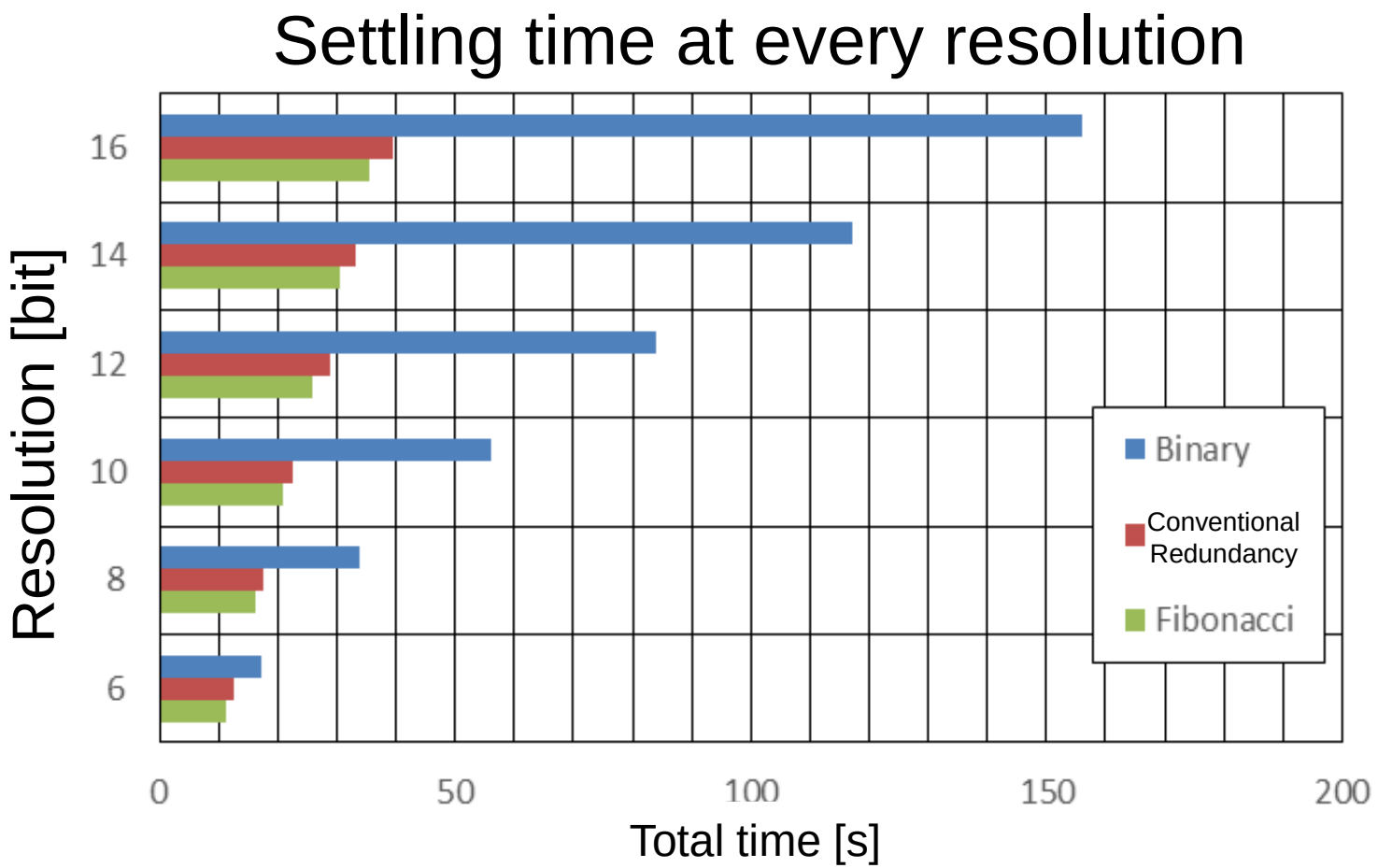


Reduction of Settling Time

5bit SAR ADC



Comparison of Incomplete Settling Time



At fixed clock,

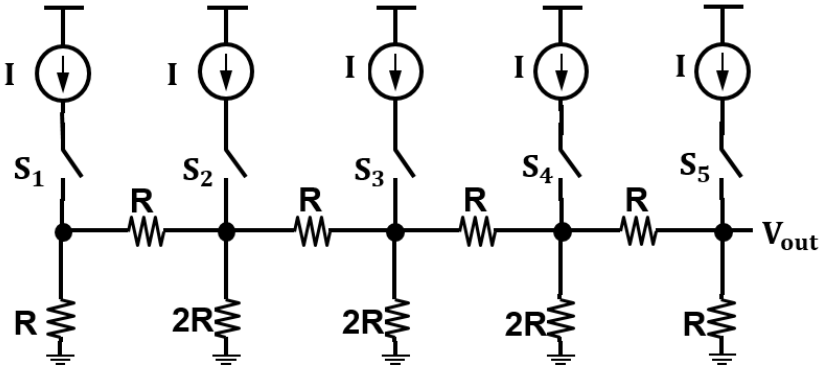
Fibonacci ⇨ the shortest AD conversion time !!

Conventional and Proposal DAC

Conventional

R-2R resistor ladder

⇒Generate **binary** voltage



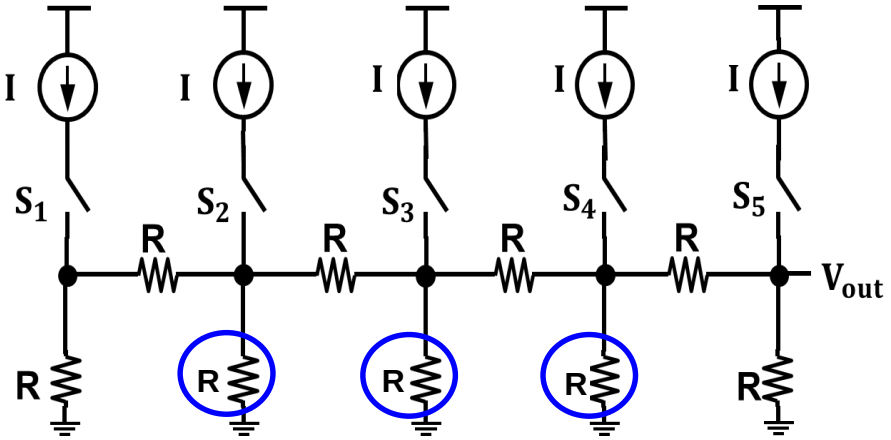
R-2R resistor ladder

Change all resistors to R

Proposal

R-R resistor ladder

⇒Generate **Fibonacci** voltage



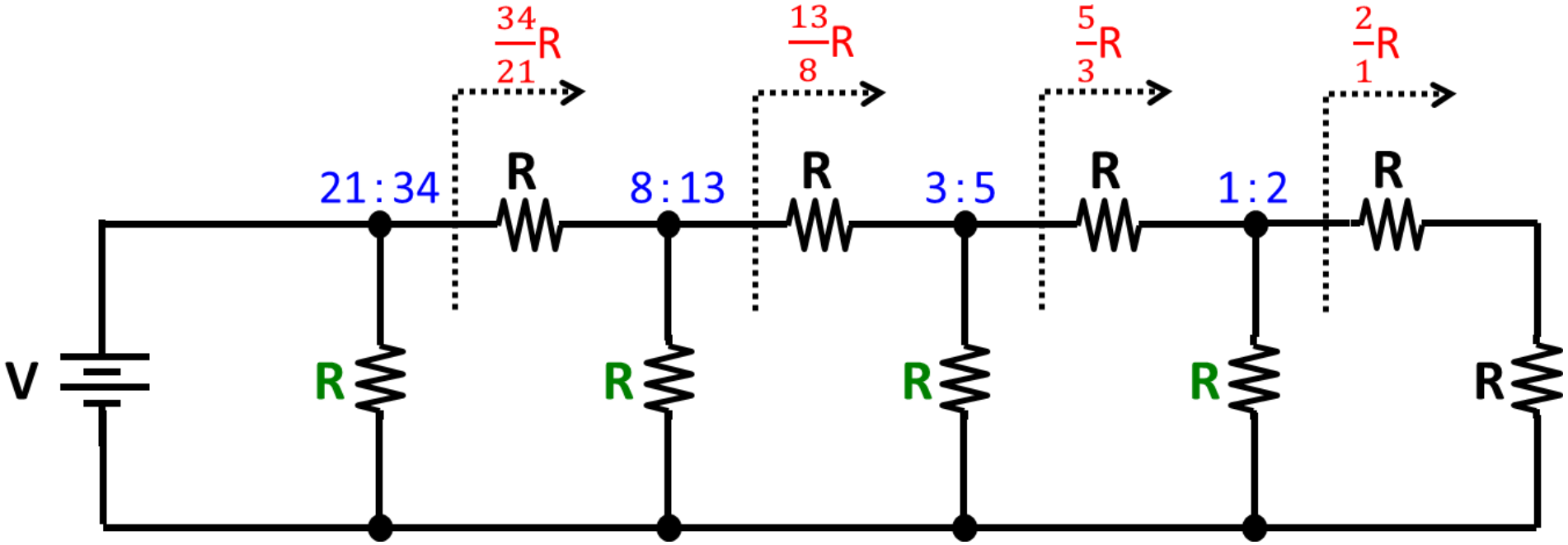
R-R resistor ladder

Realize Fibonacci DAC
by using simple circuit !

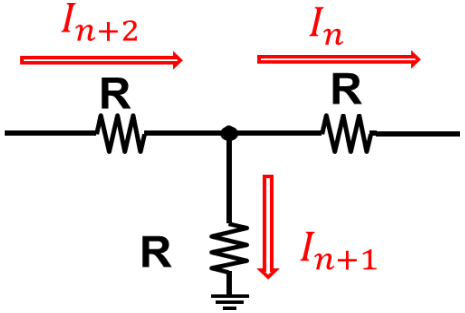
Principle of Fibonacci Voltage

New property

Divides current into **Fibonacci ratio** in each node



Principle



$$I_{n+2} = I_{n+1} + I_n$$

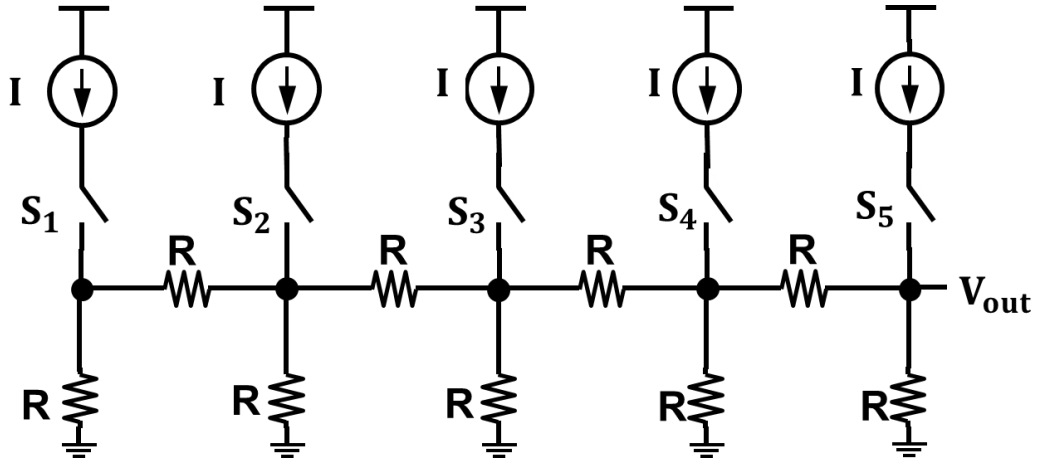
$$\Updownarrow$$

$$F_{n+2} = F_{n+1} + F_n$$

Proposal of R//R Fibonacci DAC

R-R resistor ladder

Generate
Fibonacci voltage
of **odd** term

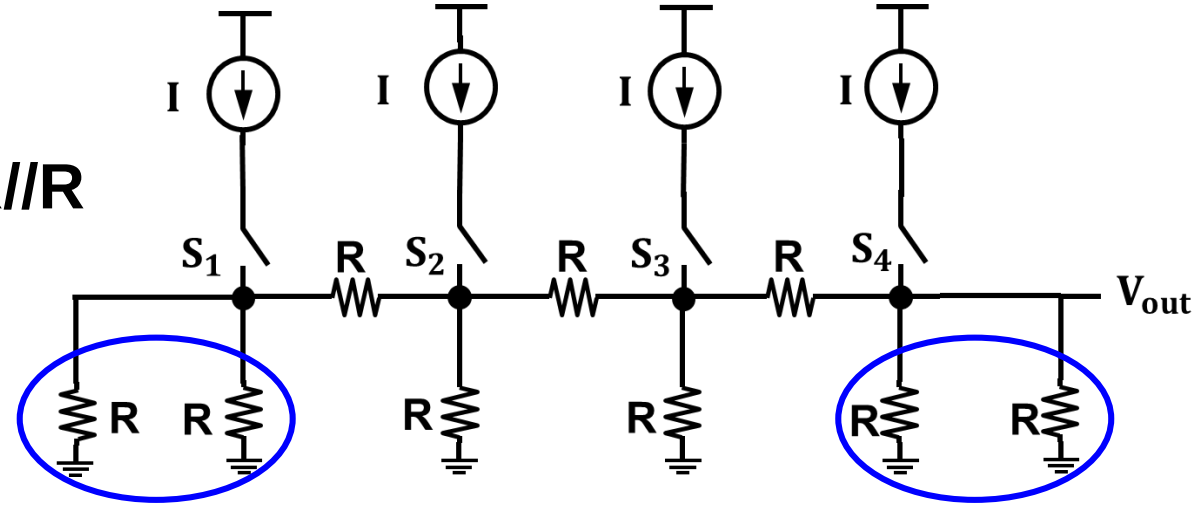


Change terminal resistors to
parallel resistors

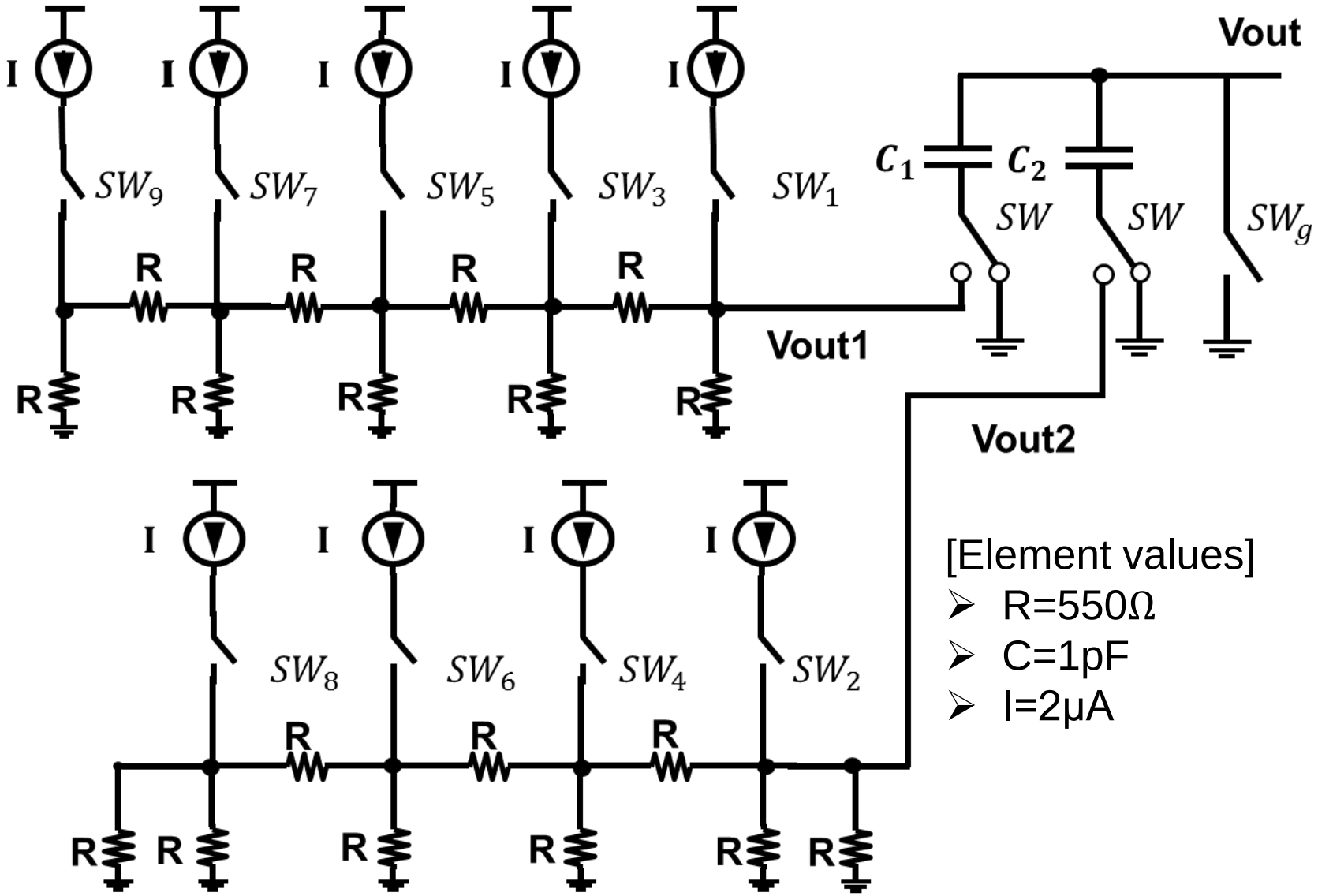
Proposal

R-R resistor ladder
with terminations of R//R

Generate
Fibonacci voltage
of **even** term



Fibonacci DAC simulation



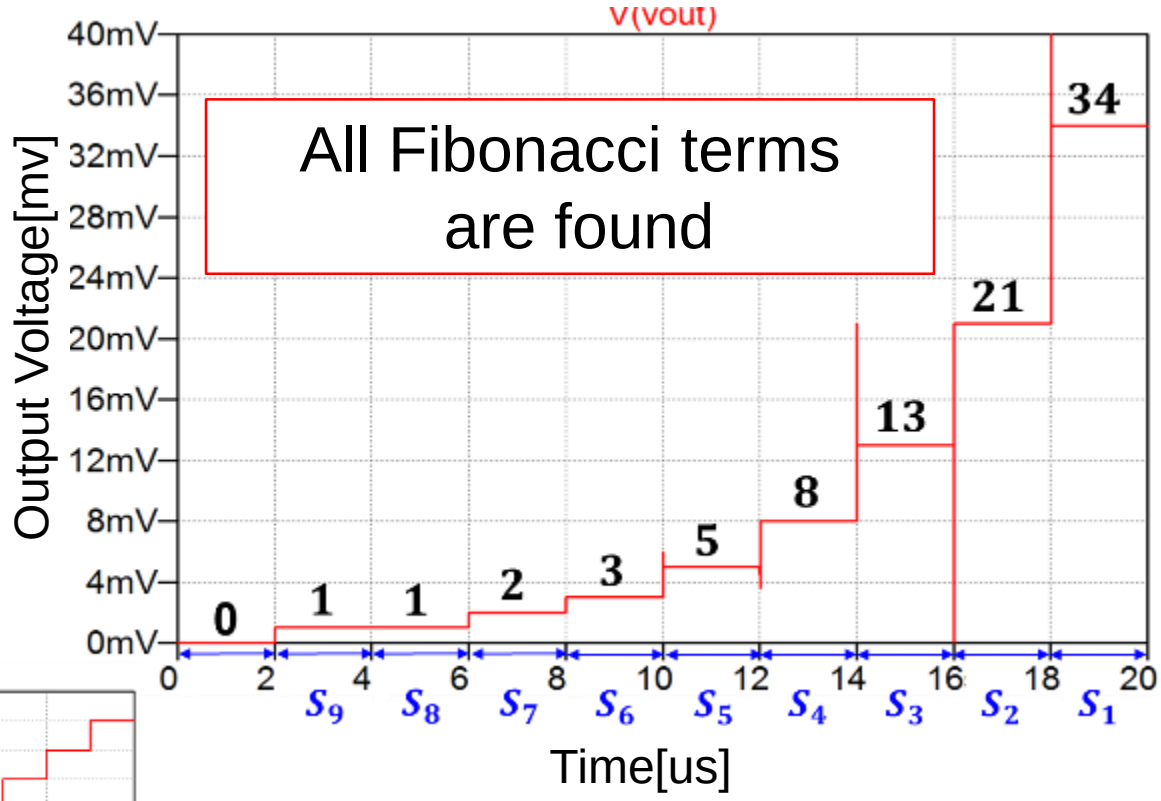
[Element values]

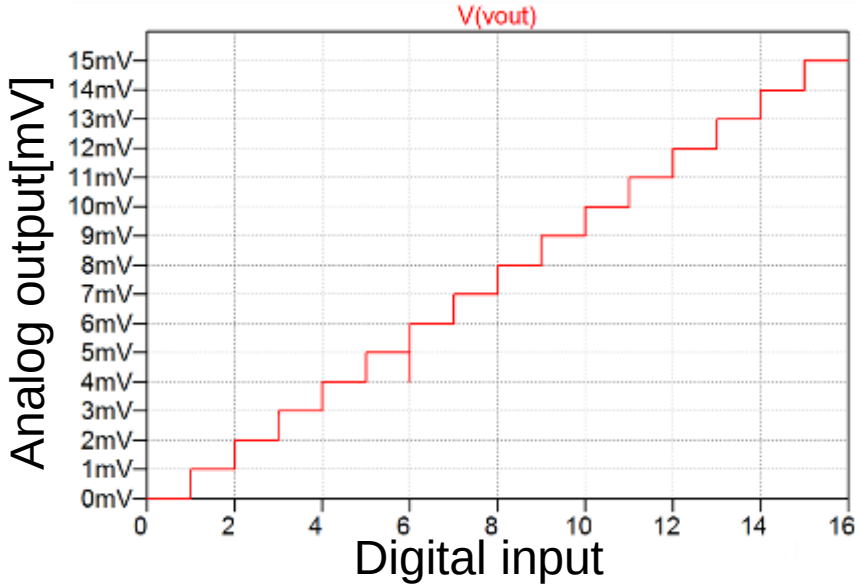
- R=550Ω
- C=1pF
- I=2μA

Simulation Result

Operation simulation

Each switch corresponds to a Fibonacci term





A-D conversion simulation

Combination of current sources realizes DAC function

Fibonacci DAC is realized

Journal of Technology and Social Science (JTSS)

Redundant SAR ADC Algorithm for Minute Current Measurement

Hirotaka Arai[1, a], Takuya Arafune[1], Shohei Shibuya[1], Yutaro Kobayashi[1]
Koji Asami[1], Haruo Kobayashi [1, b]

[1]Division of Electronics and Informatics, Faculty of Science and Technology, Gunma University
1-5-1 Tenjin-cho, Kiryu, Gunma 376-8515, Japan

[a]<t13304006@gunma-u.ac.jp>, [b]<koba@gunma-u.ac.jp>

Keywords: Minute Current Measurement, SAR ADC, Fibonacci Sequence, Golden Ratio, Redundancy

Abstract. This paper investigates a successive approximation register (SAR) AD conversion algorithm for measuring a minute current source. We consider the case that the input current is very small, and the sample & hold (SH) circuit in front of the SAR ADC takes relatively long time to settle completely. If a binary search SAR ADC is used, it has to wait until the signals in the SH circuit settle completely because the binary search has no redundancy. Then we propose to use a redundant search SAR ADC which can start to operate before its complete settling. Even if a decision error of successive comparisons occurs in the previous stage because of the incomplete setting of the SH circuit, it can be corrected in the subsequent stages, thanks to the redundancy. Then the SAR AD conversion time can be shortened. We will present its operation principle and simulation results.

1. Introduction

We consider here to measure a minute current, such as for precise current source trimming. However, it takes relatively long time to measure it using a conventional binary SAR ADC. The SH circuit in front of the SAR ADC takes relatively long time to settle completely for a minute current input. The binary search SAR ADC has no redundancy and it can start to operate only after the SH circuit settles completely; it takes a relatively long time. On the other hand, the redundant search SAR ADC can start to operate before incomplete settling of the SH circuit, because the wrong decisions in early SA stages can be corrected in latter SA stages thanks to the redundancy.

This paper presents that we can alleviate the affect of the settling time of the SH circuit by using a Fibonacci sequence weighted SAR ADC and shorten the measurement of the small current source. We have investigated its possibility and shown their simulation results. This paper is an extended version of our paper [1].

2. Problem and Solution for Minute Current Source Measurement

We consider a minute current source measurement using an SAR ADC. In this case, the settling time of the SH circuit of the preceding stage becomes longer, which affects the measurement time (Fig. 1). Therefore, changing the later stage from the binary type to the redundant type is considered for the measurement time of each step to be shortened and for the measurement speed to be increased.

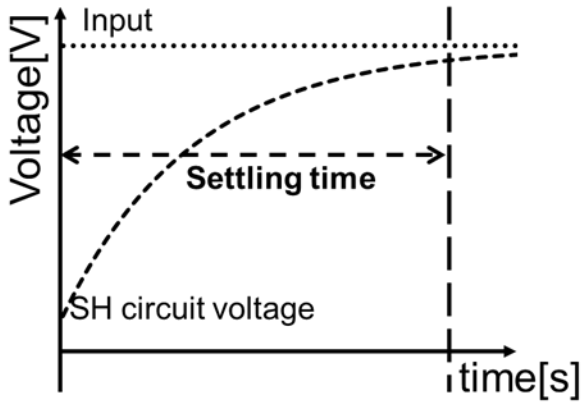


Fig. 1. Settling time of a SH circuit

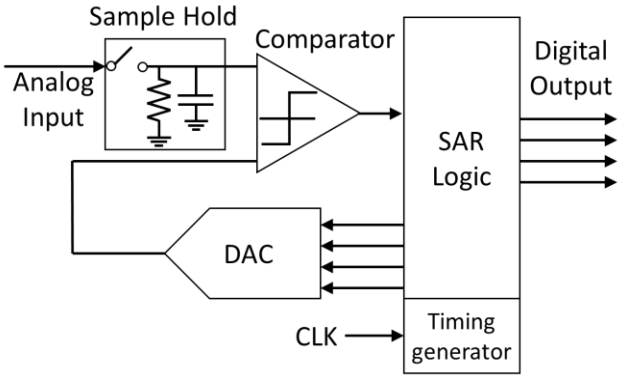


Fig. 2. Block diagram of an SAR

3. SAR ADC and Redundancy Design

3.1 SAR ADC

SAR ADCs are used for medium sampling speed and high-resolution applications. Since they have features of low power and small chip area, they are widely applied to such as automotive, factory automation. Furthermore, it does not require operational amplifiers, which is suitable for nano-CMOS implementation.

The SAR ADC consists of a SH circuit, a comparator, a DAC, SAR logic and a timing generator (Fig. 2). For precise AD conversion, enough accuracy of the SH circuit and the DAC is required.

Conversion of the SAR ADC is based on principle of balance and generally it uses the binary search algorithm. Firstly, the SH circuit acquires an analog input voltage. Secondly, the comparator compares the input analog voltage and the reference voltage that is generated by the DAC and decides 1-bit digital output. Thirdly, SAR logic provides the DAC input based on the comparator output. The input voltage and the updated DAC output voltage are compared by the comparator. This operation is repeated and finally the SAR ADC can obtain the whole digital output. Fig. 3 shows the binary search algorithm of a 4-bit SAR ADC. The bold line in Fig. 3 indicates the reference voltage value to compare with the analog input at each step. Their values are calculated by either sum or difference between the last step reference voltage and the weighted voltage p(k) of each step as shown in Fig. 3.

3.2 SAR ADC Redundancy Design

Redundancy design is a popular technique to improve circuit and system performance. To apply the redundancy design to the SAR ADC means adding extra comparison [1-8]. This method changes binary weights to non-binary weights for the DAC and realizes digital error correction with redundancy property.

Fig. 4 shows an example of two redundant search operations of a 4-bit 5-step SAR ADC. There, the input voltage is 8.3LSB and the reference voltage weights p(k) are 1, 2, 3, 6 and 8. The one operation (solid arrows) assumes that the comparison is correct, whereas the other (dotted arrows) assumes that it is incorrect. However, both obtain the correct digital output of 8 by digital error correction. In the 4-bit 5-step SAR ADC as shown in Fig. 4, there are 25 comparison patterns and 24 output patterns even though the SAR ADC digital output integer range is between -1 and 16. In other words, a given output level can be expressed by multiple comparison patterns. Thus, even if comparator decision is wrong at some steps, the correct ADC output may be obtained. Then we can make a reliable SAR ADC.

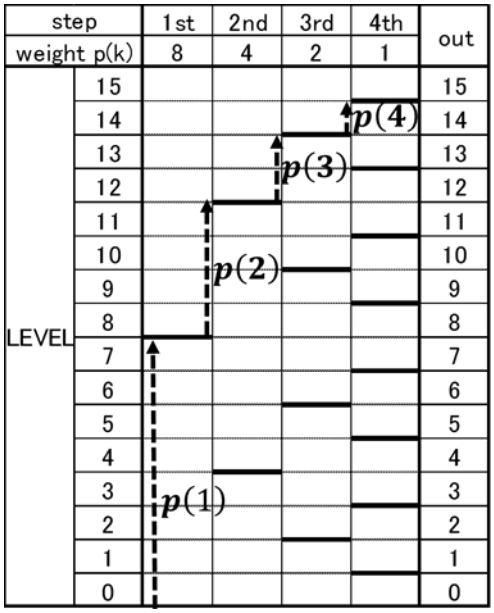


Fig. 3. Binary search algorithm of a 4-bit 4-step SAR ADC.

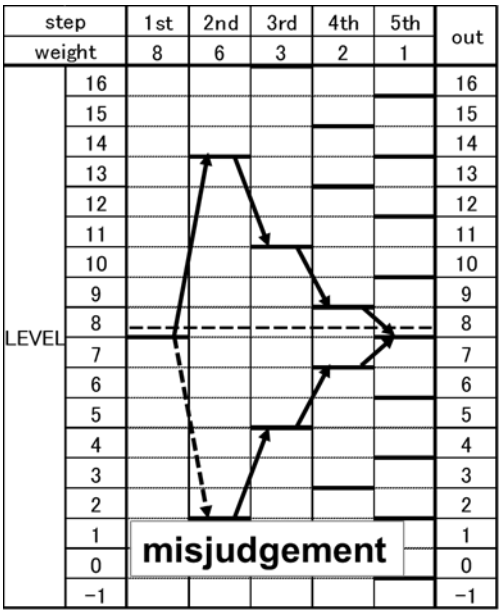


Fig. 4. Operation of a 4-bit 5-step SAR ADC in case of correct and incorrect judgments.

In addition, even if the number of the comparison steps is increased, the digital error correction enables high-speed AD conversion as a whole, because the digital error correction can take care of the DAC incomplete settling [1-7]; thus redundancy design has potential for reliable and/or high-speed SAR AD conversion.

3.3 Conventional Redundancy Design Issues

Reference voltage weight p(k) greatly affects redundant SAR ADC performance, and designers have selected p(k) as a k-th stage weight by using Eq. (1).

$$p(k) = R^{M-k} \tag{1}$$

Here, M is the number of the whole steps, k shows a comparison stage number and R represents a radix. However, conventional decision methods of the reference voltage weights p(k) [1-6] have several issues as follows:

(1) First, the reference voltage weight p(k) in Eq.(1) is not an integer which is not suitable for the circuit design. We must round p(k) values to use integer for easy design and accurate conversion. However, the rounding operation causes variability of the correction capability at each step and they may disturb performance improvement.

(2) Second, there is difficulty of an appropriate radix choice. ADC designers must choose a proper radix R ($1 \leq R < 2$) in Eq.(1). Fig. 4 shows an example in case of radix 1.80 and using rounding. However, in Fig.5, two-way arrows indicate that correctable input range cannot cover all input range, which means that there are some ranges that cannot be corrected. There is a trade-off between correction capability and conversion speed, and the SAR ADC designer is forced to search a radix that is the most suitable for SAR ADC.

(3) Third, there is an issue of the internal DAC configuration. In the binary search SAR ADC, its internal DAC is realized easily by using binary network topology. But it is difficult to design the internal DAC of the redundant SAR ADC. Conventional methods have realized the internal DAC by complicated and large circuits.

We have shown the first and second issues are solved by Fibonacci sequence redundancy algorithm [7]. Further, this paper shows that the Fibonacci sequence method also solves the third issue.

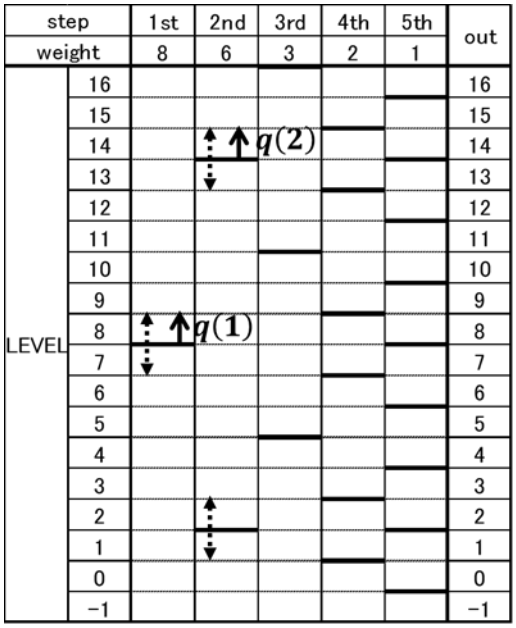


Fig. 5. 4-bit 5-step SAR ADC algorithm and definition of correctable difference q(k).

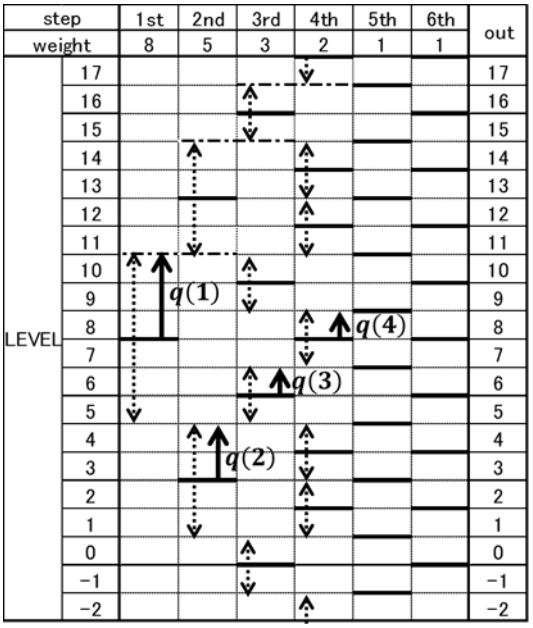


Fig.6. Redundant search algorithm of a 4-bit 6-step SAR ADC using Fibonacci sequence.

4. Redundancy Design Using Fibonacci Sequence

4.1 Fibonacci Sequence

Fibonacci sequence is defined by a recurrence relation as shown in Eq.(2), where n in Eq.(2) is an integer greater than or equal to 0. Fibonacci sequence was presented in 1202 by Leonardo Fibonacci, who was a mathematician in Italy and it is known as one of the most famous number theories [6].

$$F_{n+2} = F_n + F_{n+1} \quad \text{where } F_0 = 0, F_1 = 1 \tag{2}$$

Fibonacci numbers are expressed as the following by calculating Eq.(2).

0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233, 377, …

In short, the sum of neighboring two terms is next term.
In addition, the closest terms ratio of Fibonacci sequence converges approximately at 1.62 as shown in Eq.(3).

$$\lim_{n\to\infty} \frac{F_{n+1}}{F_n} = 1.6180339887 = \varphi \tag{3}$$

This ratio is called “Golden ratio” and it is widely recognized as the most beautiful ratio.
Fibonacci sequence and Golden ratio are based on very simple rules like the above. However, we can find them in various places of our surroundings such as nature and humanity, and they have many interesting and unique properties. Thus they have been studied by many researchers for more than 800 years.

4.2 Fibonacci Sequence Redundancy design

We have studied redundancy algorithm using Fibonacci sequence to solve the issues shown in Section 3.3. This algorithm selects Fibonacci sequence for reference voltage weights and realizes an approximate radix 1.62 with only integer terms. Then, we have shown several advantages as follows: Since Fibonacci sequence consists of integer terms, we do not require rounding operation. Fig. 6 using a Fibonacci sequence weighted SAR ADC shows that all input range is covered by correctable range

shown by two-way arrows. It means that it achieves high reliability.

Furthermore, we also showed Fibonacci method's advantage at speed as well as reliability. The Fibonacci method proved to be the fastest method at all resolutions. This was the result of simulations taking account of incomplete settling of the output of the internal DAC. Normally, the settling time of the output of the internal DAC is longer than the settling time of the SH circuit. However, the settling time of the SH circuit may be longer than the settling time of the output of the internal DAC in some cases. Section 5 shows that the Fibonacci sequence weighting SAR ADC is effective for such cases.

5. New Discovery of Fibonacci Sequence Weighted SAR ADC

5.1 Comparative simulation of binary and Fibonacci

Considering the settling time of the SH circuit, we consider that the Fibonacci type SAR ADC with redundancy has shorter measurement time than the binary type. By relaxing the comparative condition in the first half, the speed can be increased. The misjudgment can be corrected by strengthening the comparison condition in the latter half. As a result, the measurement time of each step decreases and the judgment speed rises. This is shown by simulation.

The simulation conditions are as follows:

- This simulation uses Scilab as a simulation tool.
- We replace the minute current source of the input signal with the voltage source and consider the settling time of the SH circuit.
- The SH circuit is an RC series circuit; in other words, it is a first-order system.
- The resolution is changed from 1 to 14 bits, and the accuracy is set to 1/2 LSB.
- The initial voltage of the capacitor is set to a half of the full scale.

The simulation method is as follows:

(1) When $V_{in} = 2^n$ which is the worst case, the time to be taken so that the difference between the output of the SH circuit and the input becomes 1/2 LSB is divided according to the number of steps, and based on this, a clock is generated (Fig. 7).
(2) V_{in} is changed from 0 to 2^n and a judgment is made using this clock.
(3) When the difference between the judgment result and the input is less than or equal to the LSB, the operation is terminated; otherwise, the clock is increased until it is within the range and the judgment is continued.

Fig. 8 shows a binary type determination example when $V_{in} = 2.5$. Fig. 9 shows a Fibonacci type determination example when $V_{in} = 2.5$. In Fig. 9, it can be seen that judgment errors occur in 1st step and 6th step

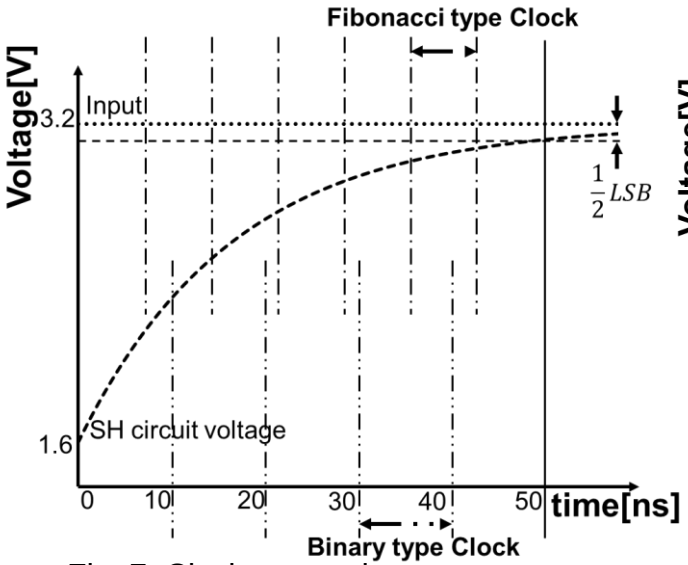


Fig. 7. Clock generation operation (5bit SAR ADC)

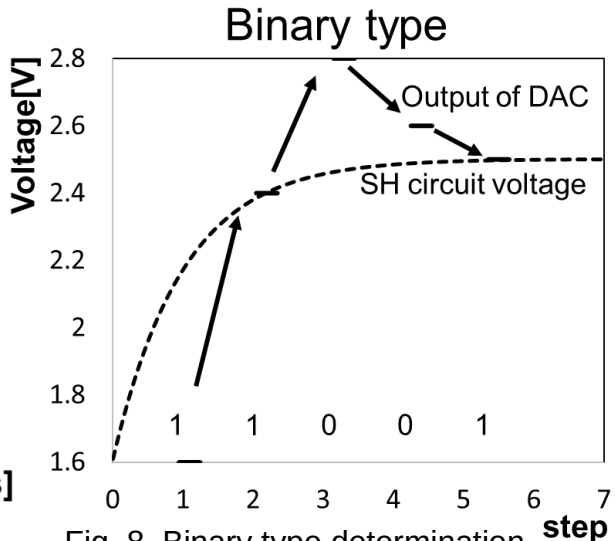


Fig. 8. Binary type determination example ($V_{in} = 2.5$)

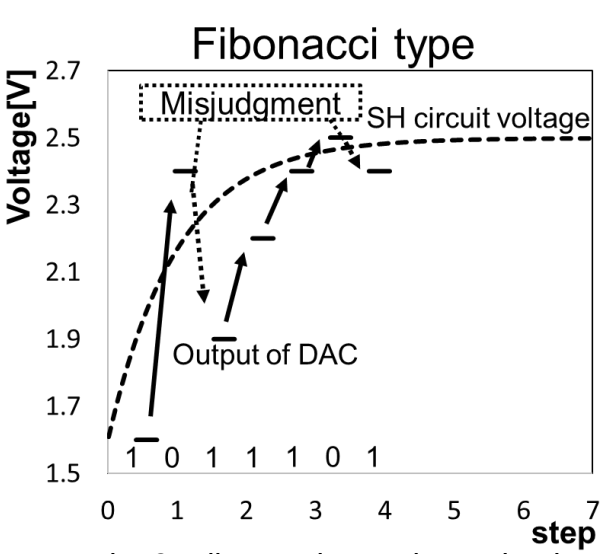


Fig. 9. Fibonacci type determination example ($V_{in} = 2.5$)

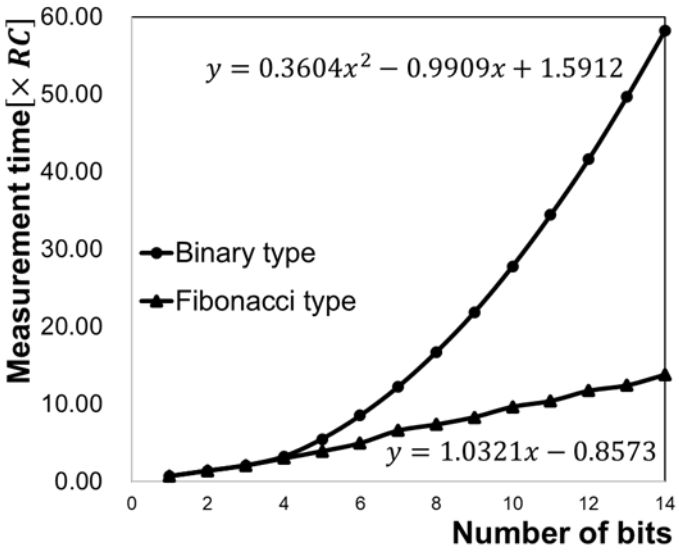


Fig. 10. Relationship between number of bits and measurement time

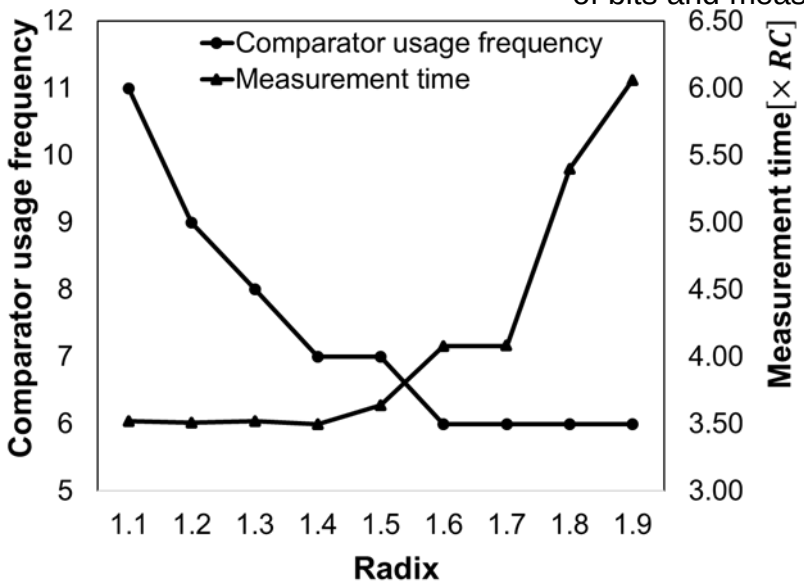


Fig. 11. Relationship among radix, measurement time and comparator usage frequency

Simulation results are shown in Fig. 10, and we see that the Fibonacci type SAR ADC requires only a shorter measurement time than that of the binary type, and as the number of bits (or resolution) increases, their difference in measurement time increases.

5.2 Simulation using radix method

We use a radix method that can change the degree of redundancy. We show simulation results of the relationship among radix, measurement time and comparator usage frequency. The comparator usage frequency leads to power consumption. In this simulation, the resolution was fixed to 5-bit and its radix was changed. Then the same simulation as in Section 5.1 was performed. The simulation result is shown in Fig.11, and we can see that the balance between the comparator usage frequency and the measurement time is good in case that the radix is around 1.6. Therefore, the Fibonacci method with radix 1.62 would be suitable.

6. Conclusion

In this paper we have investigated the settling time of the SH circuit when measuring a minute current source using an SAR ADC. We have shown that the SH circuit output for a binary type SAR ADC without redundancy has to be completely settled. On the other hand, Fibonacci type with redundancy can shorten the measurement time of each step thanks to incomplete settling and digital error correction. As a result, the total measurement time of the Fibonacci type is shorter than that of the binary type. Furthermore, using the radix method, the measurement time and the number of times of the comparator usage are obtained, and it is found that the Fibonacci method is suitable because the balance is good in the vicinity of radix = 1.6.

References

[1] H. Arai, T. Arafune, S. Shibuya, Y. Kobayashi, K. Asami, H. Kobayashi, "Redundant SAR ADC algorithm for minute current measurement", ***International Conference on Mechanical, Electrical and Medical Intelligent System*** (Kiryu, Japan) Nov. 2017.

[2] T. Ogawa, H. Kobayashi, Y. Takahashi, N. Takai, M. Hotta, H. San, T. Matsuura, A. Abe, K. Yagi, T. Mori, "SAR ADC algorithm with redundancy and digital error correction", ***IEICE Trans. Fundamentals,*** Vol.E93-A, No.2, pp.415-423, Feb. 2010.

[3] Y. Kobayashi, H. Kobayashi, "Redundant SAR ADC algorithm based on Fibonacci sequence", **A*dvanced Micro-Device Engineering VI, Key Engineering Materials,*** pp.117-126, 2016.

[4] Y. Kobayashi, S. Shibuya, T. Arafune, S. Sasaki, H. Kobayashi, "SAR ADC design using golden ratio weight algorithm", ***The 15th International Symposium on Communications and Information Technologies*** (Nara, Japan) Oct. 2015.

[5] T. Arafune, Y. Kobayashi, S. Shibuya, H. Kobayashi, "Fibonacci sequence weighted SAR ADC algorithm and its DAC topology", ***IEEE 11th International Conference on ASIC*** (Chengdu, China) Nov. 2015.

[6] W. H. Press, S. A. Teukolsky, W. T. Vetterling, B. P. Flannery, "Golden section search in one dimension", Numerical Recipes: The Art of Scientific Computing (3rd ed.), in Section 10.2, ***Cambridge University Press***, 2007

[7] H. Kobayashi, H. Lin, "Analog/mixed-signal circuit design based on mathematics", ***IEEE 13th International Conference on Solid-State and Integrated Circuit Technology*** (Hangzhou, China) Oct. 2016.

[8] H. Kobayashi, Y. Sasaki, H. Arai, D. Yao, Y. Zhao, X. Bai, A. Kuwana, "Unified methodology of analog/mixed-signal IC design based on number theory", ***IEEE 14th International Conference on Solid-State and Integrated Circuit Technology*** (Qingdao, China) Nov. 2018.