LETTER *Special Section on Analog Circuit Techniques and Related Topics*

A Practical Analog BIST Cooperated with an LSI Tester

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SUMMARY This paper proposes a new approach for analog portion testing, which can meet requirements for high-speed and high-accuracy testing simultaneously with reasonable cost. The key concept of the new method is cooperation of an LSI tester and some circuitry built in a target SoC device. We will explain the operation principle of the proposed method. The proposed method can be one of the methods to overcome today's expensive production test of analog portion on SoC (System on Chip) devices which heavily depends on LSI tester capability and will become harder in near future.

key words: *LSI testing, analog circuit, BIST, equivalent-time sampling, sampler*

1. Introduction

"Built-In-Self-Test" (BIST) is a well-known concept in semiconductor testing. By adding some circuitry aiming at production test of target devices, requirements for an LSI tester are relaxed and their testing cost is reduced. As for the digital portion testing, the BIST technique is successful to some degree [1], while as for the analog one, it is hard to say that the BIST helps much (only a few of them were successful [2]–[7]). Even though the basic concept of BIST, which utilizes the DUT performance for its testing, seems reasonable even in case of analog portion, BIST for analog circuitry does not prevail widely yet and its reasons would be considered as follows:

- The testing of analog portion is more complex and harder than that of digital; the main requirement for digital testing is the verification of its functionality, while requirements for analog testing are not only functionality, but also its quality described as parameter values like SNR.
- When we test the DUT and evaluate its quality, is it reasonable to assume the BIST circuit in the DUT works well with enough quality ? It seems that there is some contradiction.
- If the failure rate of BIST circuitry is not small enough compared to that of a whole DUT, adding BIST degrades the total failure rate.

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According to the above considerations, we recognize that BIST for practical use should be simple and insensitive against semiconductor process variations, and we consider that cooperation of BIST and an LSI tester would be reasonable; if we use only the BIST technique, it could not meet the demands for complex analog portion testing.

In the following sections, we will describe a new technique of analog BIST which cooperates with an LSI tester [8], [9]; this solves one of the most difficult problems in LSI testing, and enables the waveform measurement of high speed (i.e. >1 GHz) and high accuracy (i.e. >10 bit) simultaneously. We propose to implement a sampler at DUT output pin for testing purpose. The embedded part of the sampler in the DUT has to acquire wideband signal but does not need accuracy, which is suitable for fine CMOS devices. On the other hand, an LSI tester provides slow but accurate signal to the sampler. We remark that our BIST can make the high-speed signal measurement easy because it does not require a long wire line between a DUT and a digitizer in an LSI tester; a low power CMOS DUT is very hard to drive a long wire with enough accuracy.

2. Proposed Analog BIST

2.1 LSI Testing Assumption

In many cases, DUT testing is performed by a comparison of measured result with expected response, and there an LSI tester can control the signal waveform inside the DUT completely. For example, an LSI which handles natural human voice signal could be tested by simple sine wave signals. Hence, we can assume here that *the signals in the DUT during production test have repeated waveforms* (for which the equivalent-time sampling technique can be applied [10]–[12] (Fig. 1)), and the DUT is kept under control of the LSI tester especially as for its signal timing.

2.2 Analog BIST Structure and Operation

Figure 2 shows a basic block diagram of our proposed method. A simple comparator and a latch are located inside the DUT (as BIST), while a DAC with high accuracy, a clock generator and control circuitry like successive approximation resistor (SAR) are in an LSI tester. The circuits inside the DUT are required to operate at high speed but high accuracy is not required. On the contrary, LSI tester

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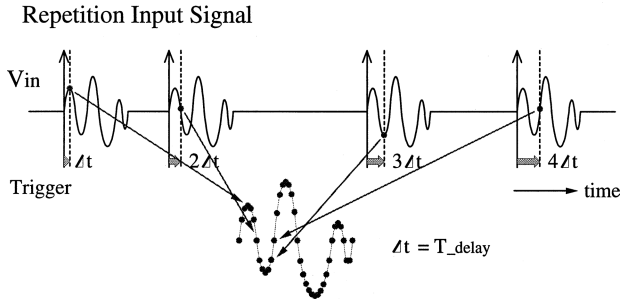

Fig. 1 Explanation of equivalent-time sampling for a repetitive signal. Equivalent-time sampling can be performed at the DUT outputs during its testing, because an LSI tester controls all of its input signals.

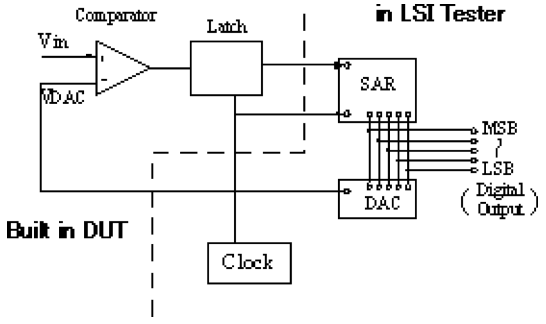

Fig. 2 A block diagram of our BIST for analog portion.

components have to operate with high precision, but at normal speed. In Fig. 2, the comparator in the DUT compares an input (Vin) from the point of interest in the DUT with a DC voltage (VDAC) from the LSI tester. Vin is high-speed signal, and hence the comparator output changes its polarity very frequently. Also since Vin is a repeated signal and an LSI tester can control the signal timing as we assumed before, the LSI tester can generate a clock which is synchronized with the repeated signal. After all, the latched comparator outputs the comparison result of Vin (at the timing of interest) with VDAC.

Then we can obtain the value of Vin at the timing of interest with some resolution by changing the value of VDAC in a binary search manner. Next, we change the clock timing for the latch by a slight fixed amount so that we obtain the value of Vin in another phase. With the repetitive use of this scheme, the whole waveform of Vin is obtained finally. In other words, we use the equivalent-time sampling technique here [10]–[12]. This proposed method uses a binary search method, and hence it is regarded as a variety of a successive approximation type ADC (SA ADC). However the proposed method does not require a wideband track/hold (T/H) circuit in front of the SA ADC because the input signal is repetitive, and next subsection elaborates the difference between our proposed method and a conventional SA ADC.

2.3 Comparison with Conventional SA ADC

Figure 3 shows a block diagram of a conventional SA ADC, where a T/H circuit (which dominates the performance of

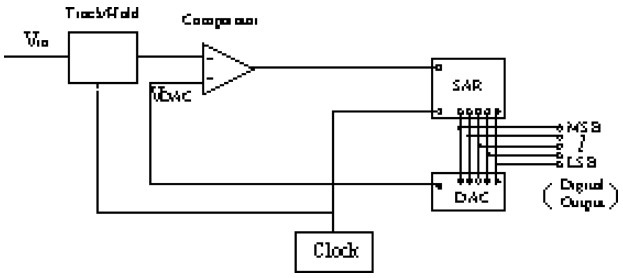

Fig. 3 A block diagram of a conventional SA ADC.

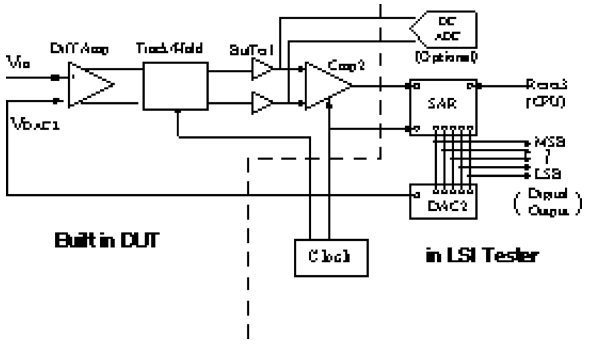

Fig. 4 A detailed block diagram of the proposed architecture.

the total ADC) is placed as the first stage of the SA ADC. In a conventional SA ADC, the T/H circuit has to acquire and keep the value of Vin at timing of interest during 1 cycle of the successive approximation operation, where the total ADC performance of bandwidth and accuracy is restricted by the T/H performance. Hence the conventional SA ADC embedded as BIST in a fine CMOS LSI is very hard to achieve good performance because a high performance T/H circuit with fine CMOS is hard to realize due to low power supply voltage.

On the other hand, our proposed architecture in Fig. 2 does not require a T/H circuit because the input signal is repetitive and the equivalent-time sampling technique is used there [5,6,7]. The components built in a CMOS LSI are required for only high-speed operation but not for accuracy; high-speed operation can be automatically achieved according to CMOS scaling progress. Also since the total amount of the circuit built in the CMOS LSI is small, its failure rate would be sufficiently low. In the proposed architecture of Fig. 2, the components which are outside of the CMOS DUT are simple digital circuits (a SAR and a clock generator) and a slow speed DAC with high accuracy, which are inexpensive and well-used components in LSI testers. As the results of the above consideration, we see that the architecture in Fig. 2 fulfills the requirements for practical analog BIST.

2.4 Detailed Circuits for Proposed Architecture

Figure 4 shows a detailed block diagram of the proposed architecture in Fig. 2. The basic operation in Fig. 4 is the same as that Fig. 2. However since the comparator in Fig. 2 has

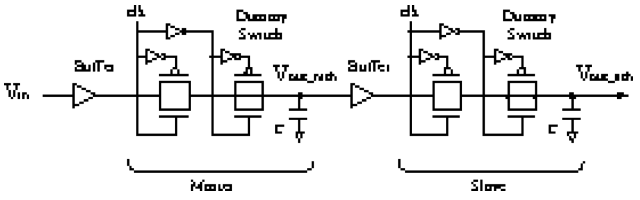

Fig. 5 A master-slave type T/H circuit.

to have high gain bandwidth for " GHz" range applications, a latched comparator in Fig. 2 is replaced with a differential amplifier and a relatively low accuracy T/H circuit in Fig. 4; the differential amplifier has a lower gain than that of the comparator, but when the input signal (the difference between Vin and VDAC) is large enough, it works as if a comparator. As the successive approximation process goes on, the difference becomes smaller and it works as a linear amplifier.

In Fig. 4, we use the differential amplifier output signal in two ways. The one is the input signal for a comparator (Cmp2 in Fig. 4), while the other is to lead the signal to the ADC located in the LSI tester. This pass is used after some cycles of successive approximation using Cmp2 pass has been done. Since the signal to the ADC on the LSI tester is still analog, we have to take care of its accuracy. But in this case the required accuracy can be achieved easily thanks to the help of the DAC. For example, to obtain 10bit accuracy in the total system without any help of DAC, the T/H circuit and the ADC have to have 10bit accuracy. However by using successive approximation cycles to decide upper 3-bit, the T/H circuit and the ADC require only 7bit accuracy.

Figure 5 shows the T/H circuit in Fig. 4. If conventional single stage T/H circuit is used, the input signal of the T/H circuit (e.g. 1 GHz) appears directly in output during T/H in track mode, and the comparator and the ADC (which can handle only DC signal) which follows the T/H circuit are exposed to this high frequency signal. This leakage signal would be an error seed, and to avoid this effect, we use a "Master-Slave Type" T/H circuit. With these modifications, the total amount of components built in DUT is slightly increased compared to Fig. 2. However the number of MOS transistors is still less than 100, and this simplicity is suitable for BIST.

We have described simulation results of the circuits in Figs. 4, 5 in [8], [9].

3. Concluding Remarks

In this paper we have proposed a new architecture of BIST for analog portion in CMOS system LSIs, which cooperates with an LSI tester; we have proposed to put a sampler at output pin for testing purpose. The embedded part of the sampler in the DUT has to acquire wideband signal but does not need accuracy, which is suitable for fine CMOS devices (in other words, it is CMOS scaling generation independent). Also since the embedded circuit part is small and simple, its failure rate would be small. On the other hand, an LSI tester provides slow but accurate signal to the sampler. The output signal waveform of DUT can be repetitive during LSI testing because the LSI tester controls all input signals, and hence the equivalent-time sampling method can be used.

Here we list the subjects for further research.

- Validation of the proposed analog BIST as an IP which can survive in several generations of CMOS scaling.
- Development of error correction algorithm. If the conversion error occurs in the sequence of the binary search, the following conversion does not work well, and we need to develop some algorithm to avoid this problem.
- Consideration of DUT noise effects. The proposed method may be tolerant for low accuracy of the CMOS DUT circuitry, but its noise would be an error source.
- Validation of this method through implementing a real chip.

This research started as a joint-project of industry and university for the development of a high-speed CMOS track and hold circuit, which can be used as BIST in deep submicron CMOS. But as its research progresses, we realized that it is difficult to achieve high-accuracy of a T/H circuit using fine CMOS process, and we also found that we need the same amount of efforts for designing the T/H circuit using next finer pitch CMOS process. This means that the T/H circuit design will not survive as a proven IP for the next CMOS scaling. Then we changed the research direction to find new architecture based on cooperation of BIST and outer equipment, and found the new architecture described here.

Many of analog BIST techniques have been published in conferences and journals, but only a limited number techniques among them have been used in real industry [4], [5]. We believe that the proposed architecture is suitable for practical use and it can be implemented and widely used in semiconductor industry through our LSI tester manufacturer.

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