SESSION 13: Image Sensors, Processors, and Displays

FAM 13.3: An Analog CMOS Network for Gaussian Convolution with Embedded Image Sensing

H. Kobayashi, J.L. White, A.A. Abidi
Integrated Circuits & Systems Laboratory, University of California
Los Angeles, CA

NATURAL IMAGES are smoothed by Gaussian convolution to suppress visual noise prior to edge enhancement and detection. Convolution with a variable width is useful in adaptively smoothing unfamiliar images, where the scale of the noisy features is not known in advance. Gaussian convolution is inherent in the retinae of biological systems, and has been shown to be mathematically optimal as a filter prior to edge enhancement by differentiation[1]. The circuit described here samples an image in two dimensions, and uses a resistive network to spatially average it according to a Gaussian weighting function whose width is controlled by an electronically variable resistor. A matrix of logarithmic photoreceptors fabricated on the surface of the IC drive currents into the nodes of a mesh consisting of appropriately-ratioed positive and negative resistors. The resulting voltage distribution on the network nodes constitutes the smoothed image. No clocking or digital functions is required in the action of the network.

A resistive mesh implements a spatial averaging operation, in that the voltage at a node is a weighted sum of the voltages at all other nodes. In a network of positive resistors only, the convolution function was necessarily cusped at the peak, so to obtain the flat (zero gradient) peak of a Gaussian, a combination of positive and negative resistors was required[2]. A 1D version of such a network consists of resistors R_1 connected to nearest neighbor nodes, negative resistors of magnitude $R_2 = 4R_1$ connected to second nearest neighbor nodes and resistors R_0 from every node to ground (Figure 1*a*). This may be generalized to two dimensions by implementing the network on a hexagonal grid, and repeating the 1D network at every node in three orientations 60° apart (Figure 1*b*). When excited by photosensor output currents, the node voltage represents the smoothed output corresponding to that point on the sampled image. The spatial extent of averaging (the convolution width) is changed by varying the resistor R_0. The network accepts a 2D input (the image), does 2D analog signal processing (the network action), but has a 1D output path (the pads along the periphery). Thus, a clocked addressing scheme is necessary to read out the node voltages from these pads, one row of the network at a time.

It is important to guarantee the spatial and temporal stability of the natural response of a mesh containing negative resistors in the presence of parasitic capacitances. For this mesh, it has been shown that the conditions for both types of stability are identical, and that the mesh is indeed stable in both ways with $R_2/R_1 = 4$.[2]

A prototype network of a 40x45 array of cells along a hexagonal grid is implemented in a standard 2μm p-well, double-metal, single-polysilicon CMOS process on a 7.9x9.2mm die. Every node of the network contains the sub-circuits described in the following. A 50x30μm parasitic bipolar transistor is used as the photodetector; its photocurrent is forced into a diode-connected MOSFET operating in subthreshold to obtain a log-compressed output voltage[3]. This is level shifted, applied to a resistively degenerated MOSFET acting as a V-I converter, and used to drive one node of the network. (Figure 2) Connecting resistors from every node to the nearest and second nearest neighbors in 6 directions with only three layers of interconnect poses the greatest challenge of layout: p-well resistors were used to implement R = 5kΩ compactly. The 20kΩ negative resistors were also p-wells with a current inversion circuit acting as a negative impedance converter at the confluence of the six resistors connecting to second nearest neighbors on each node. The circuit imposes the node voltage on the resistors through an op amp, but inverts the polarity of the sum of their currents, effectively making all six resistors appear negative. (Figure 3) A Class AB output stage together with a current mirror affects the current inversion.

The variable resistor is made using two MOSFETs operating in the triode region connected to cancel parabolic nonlinearity, and controlled by V_C. (Figure 4) The theoretical variation of the width of the Gaussian is as $(R_0/R_1)^{1/4}$, so a resistance variable over a range greater than 16:1 was sought to vary the the spatial averaging by a factor of two[2]. A level-normalizing circuit scales the photosensor current output to compensate for the greater attenuation in the network as R_0 is decreased. The network stimulus and response, in the form of the photosensor output voltages and the resulting node voltages on the network, could be measured at the pads one row at a time through analog switches controlled by a personal computer.

The convolution function affected by the network is determined by shining light on the chip through a pinhole, and deconvolving the measured network stimulus from the network response. A near-Gaussian kernel is thus obtained, whose full width at half maximum (FWHM) varies by a factor of 2, from 2.35 grid points to 4.7 grid points, for a 15:1 sweep in the value of R_0. An image of the character "T" was shown on the chip, and the defocusing action imposed by the network observed. (Figure 5) The network responds to a step change in the width control voltage in less than 2μs, but the photoreceptor is slower, responding to an optical step in about 20μs. The complete 1800-node network dissipates 2W, of which 75% is due to the quiescent current in the output stage of the current inverter circuit.

This parallel 2D analog computation IC with optical input performs variable Gaussian convolution on coarsely-sampled images in real-time, orders of magnitude faster and with less hardware than conventional digital signal processors (Figure 6). A 2D signal flow through the network could be preserved if its outputs were applied to a second mesh on the same chip customized for another function, making the resulting processor approximate even more closely the structure of a low-level natural vision system.

Acknowledgments

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[1] Poggio, T., Voorhees, H. and Yuille, A., "A Regularized Solution to Edge Detection", AI Memo, MIT, Cambridge, MA; May, 1985.

[2] Kobayashi, H., et al., "A 2D Analog Network for Real Time Image Smoothing", to appear in *IEEE Trans. on Pattern Analysis and Machine Intelligence.*

[3] Chamberlain, S.G. and Lee, J.P.Y., "A Novel Wide Dynamic Range Silicon Photodetector and Linear Imaging Array", *IEEE J. of Solid-State Circuits*, Vol. SC-19, p. 41-48; Feb., 1984.

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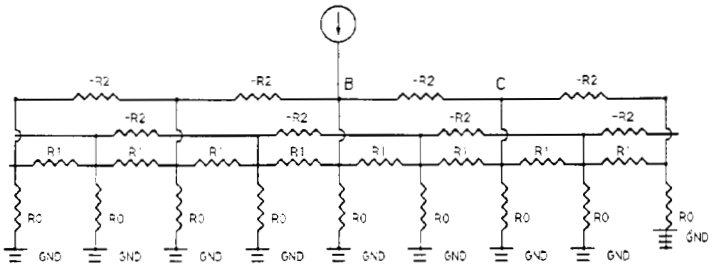


FIGURE 1a – 1D Mesh with positive and negative resistors to implement Gaussian convolution

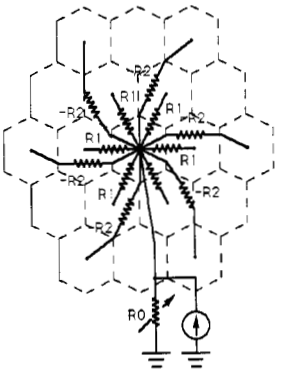


FIGURE 1b – Generalization of mesh to 2D on a hexagonal grid

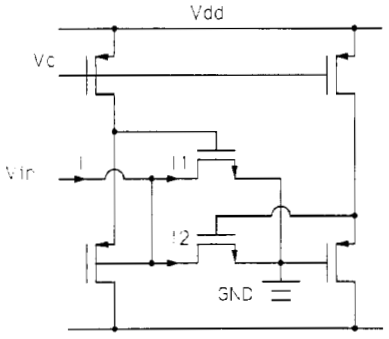
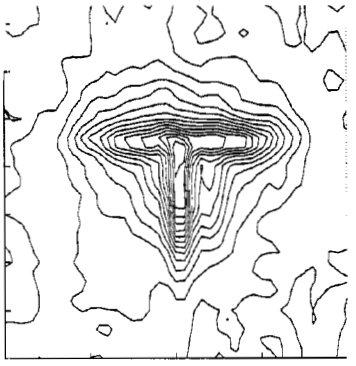


FIGURE 2 – Phototransistor, logarithmic compression FET and current output



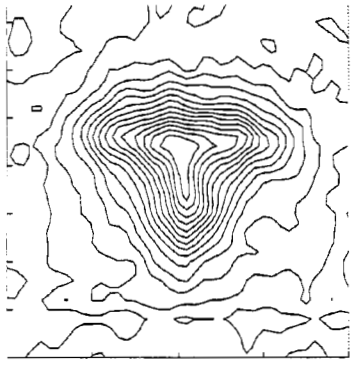


FIGURE 5 – Smoothed image (bottom) produced by network to character "T" stimulus (top)

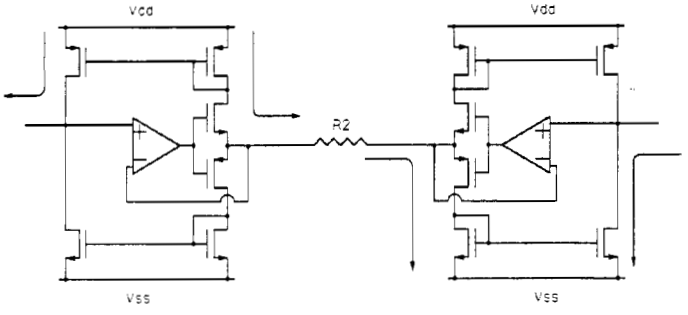


FIGURE 3 – Negative resistance implementation through current inverter circuit

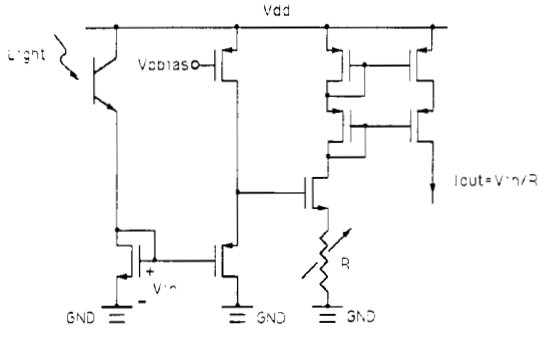


FIGURE 4 – Variable resistor circuit

FIGURE 6 – *See page 300*

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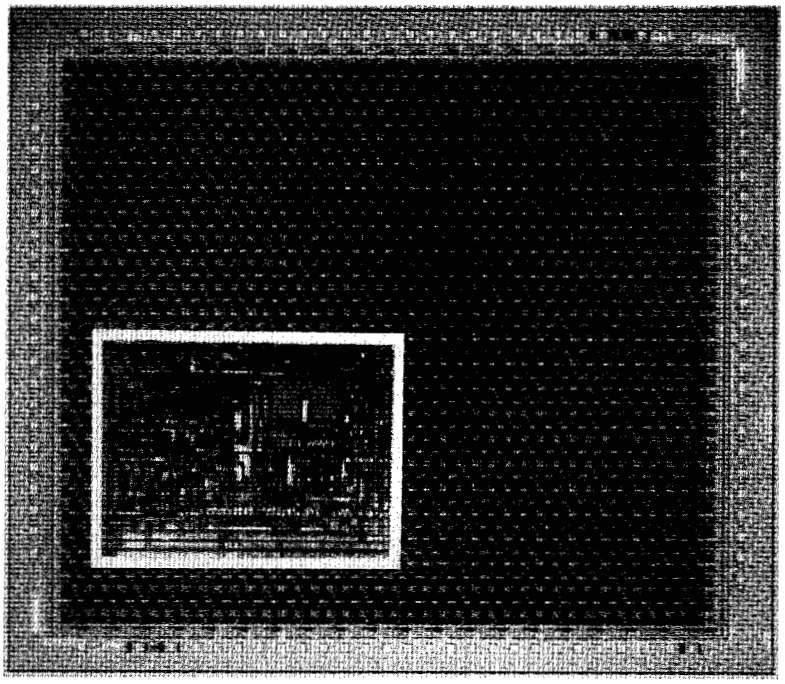

FIGURE 6 – Chip micrograph, on cell (170x200μm) magnified

FAM 13.4: A Full Fill-Factor CCD Imager with Integrated Signal Processors

(Continued from page 219)

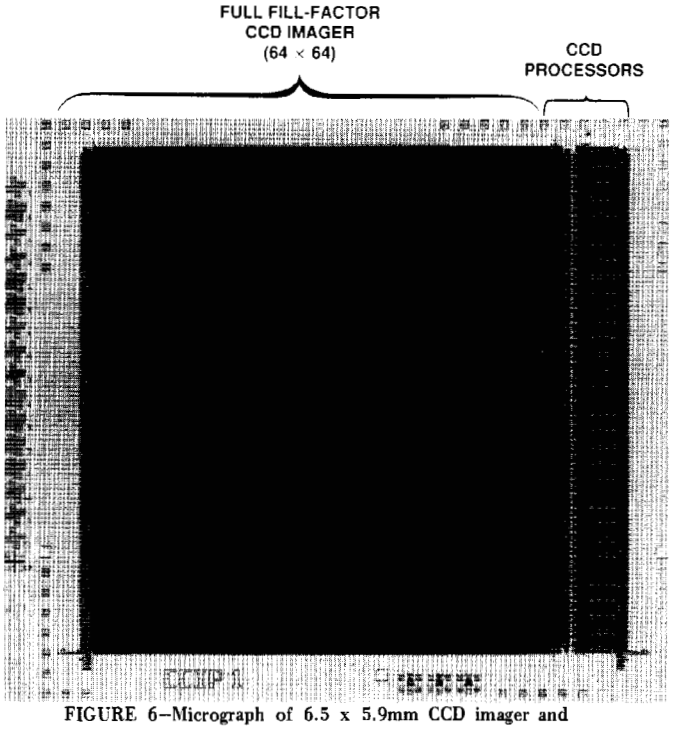

FIGURE 6–Micrograph of 6.5 x 5.9mm CCD imager and signal processor.