A Multibit Complex Bandpass ΔΣAD Modulator with I, Q Dynamic Matching and DWA Algorithm

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***Abstract*— A second-order multi-bit switched-capacitor complex bandpass ΔΣAD modulator has been designed and fabricated for application to low-IF receivers in wireless communication systems such as Bluetooth and WLAN. We propose a new structure of a complex bandpass filter in forward path with I, Q dynamic matching which is equivalent to the conventional one but it can be divided into two separate parts. As a result, the ΔΣ modulator which constituted with our proposed complex filter can be completely divided into two separate parts too, and there are not any signal line crossing between the upper and lower paths by a complex filter and feedback from DACs. Therefore, the layout design of the modulator can be greatly simplified. Nine-level two quantizers and four DACs are used in the modulator for lower power implementation and higher SNDR, but the nonlinearities of DACs are not noise-shaped and the SNDR of the ΔΣ ADC degrades. We have employed a new complex bandpass Data-Weighted Averaging (DWA) algorithm to suppress nonlinearity effects of multibit DACs in complex form to achieve high accuracy; it can be realized just by adding simple digital circuitry. Implemented in a 0.18-μm CMOS process and at 2.8V supply, the modulator achieves a measured peak signal-to-noise-and-distortion (SNDR) of 64.5dB at 20MS/s with a signal bandwidth of 78kHz while dissipating 28.4mW and occupying a chip area of 1.82mm^2.**

I. Introduction

In the RF receiver of communication systems such as cellular phones and wireless LANs, low-IF receiver architecture is frequently used so that more receiver functions, such as multi-standard and automatic gain control, can be moved to the digital part to provide more programmability. In conventional low-IF receiver architectures, two real (one input and one output) ΔΣAD modulators are used for In-phase (I) and Quadrature (Q) paths. Its disadvantage is that not only input signals but also image signals are converted by ADCs. On the other hand, a complex bandpass ΔΣAD modulator can provide superior performance to a pair of real bandpass ΔΣAD modulators of the same order. It processes just input I and Q signals not image signals, and AD conversion can be realized with low power dissipation. So they are desirable for such low-IF receiver applications[1]-[3]. The use of a low-order multibit ΔΣAD modulator makes higher resolution possible with lower OSR, and the stability problem is alleviated. It is attractive for low power implementation because it alleviates the slew-rate requirements of operational amplifiers with high dynamic range in the modulator. However, multibit DACs cannot be made perfectly linear and their nonlinearity in the feedback paths are equivalent to errors added directly to the input signals, and hence they may degrade the SNDR of the ΔΣAD modulator. Then we developed a data-weighted averaging (DWA) algorithm for complex bandpass modulators [4], which is implemented just by adding simple digital circuitry to suppress nonlinearity effects of multibit DACs in a complex form. Furthermore, in the realization of complex ΔΣAD modulators, their layout design becomes complicated because of signal lines crossing by a complex filter and feedback from DACs for I and Q paths in the modulator, and this increases required chip area. We proposed a new structure for a complex bandpass ΔΣAD modulator [5] which can be completely divided into two separate paths without crossing signal lines between the upper and lower paths, and its layou design can be simplified.

This paper presents the chip implementation with switched-capacitor circuits employing the above-mentioned two algorithms. Measured results of the implemented chip show that above two algorithms are effective.

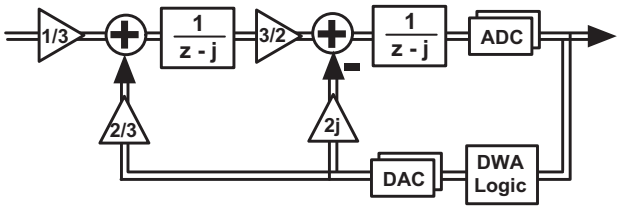

Fig. 1. Simplified block diagram of the complex bandpass ΔΣmodulator..

II. Complex Bandpass ΔΣAD Modulator Topology

A complex bandpass ΔΣAD modulator gains its advantage by implementing the poles and zeros of its loop filter without their conjugates, which will be wasted in the image band for a complex single side band signal. Fig.1 shows the simplified block diagram of the proposed complex bandpass ΔΣAD modulator; it is a second-order structure with two discrete-time complex integrators (or complex bandpass filters) and two 9-level quantizers surrounded by two feedback loops. The STF and NTF of complex modulator can be given by

$$STF(z) = 0.5z^{-2} \quad (1)$$

$$NTF(z) = (z-j)^2 z^{-2}. \quad (2)$$

Here, the passband center of the modulator is at $f_s/4$ (f_s is the sampling frequency of modulator). Complex poles can be

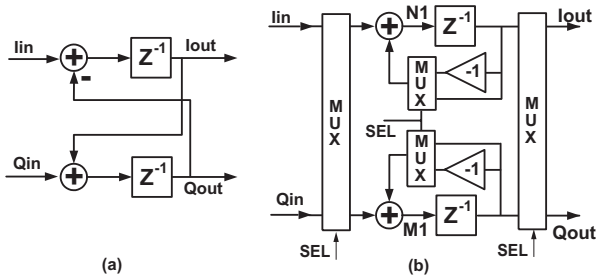

Fig. 2. (a) Basic complex bandpass filter. (b) Proposed equivalent implementation.

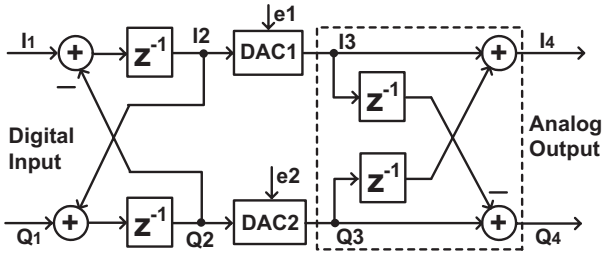

Fig. 3. Proposed architecture of DAC nonlinearity noise-shaping for a complex bandpass modulator. I1 is the Ichannel ADC output and Q1 is the Q-channel ADC output, while I4 is the I-channel DAC output and Q4 is the Qchannel DAC output. e1 and e2 denote the nonlinearities of DAC1 and DAC2 respectively. However, note that this architecture cannot be implemented directly.

implemented either with real integrators [6], or with a cascade of unit delay-cell architecture [7], which is shown in Fig.2(a). In our modulator design, we choose the delay-cell architecture since it operates fast and has simple coefficient values. DWA logic circuits realize our proposed complex DWA algorithm which will be described in section IV.

III. New Structure of Complex Bandpass Filter

Fig.2(a) shows a basic complex bandpass filter while Fig.2(b) shows its proposed equivalent implementation, where four multiplexers (MUX) are added and their select signal (SEL) toggles at half rate of CLK in z^{-1} block and they are synchronized. The proposed complex filter is divided into two separate parts without any crossing of signal lines. In our proposed configuration, the input I and Q signals alternate between the upper and lower paths of the complex filter by SEL signal, so that it is equivalent to the conventional one when their circuits are ideal with same transfer function is given by

$$H(z) = \frac{1}{z - j}, \tag{3}$$

and hence the I, Q mismatch problem in the forward path is alleviated.

IV. Complex Bandpass DWA Algorithm

Multi-bit ADCs/DACs are used inside the modulator to obtain high SNDR with a low-order loop filter and improve the stability problem. Smaller steps of the quantizer result in a lower quantization error, and relax the required performance for OP-Amps with larger overload level. Each DAC in our modulator has 9-level resolution with the segmented switched-capacitor architecture. Nonlinearities of the DAC due to mismatches of capacitors introduce errors in feedback loop will appear directly at output, which cause almost flat power spectrum in the entire band, and the SNDR of the modulator degrades.

Fig.3 shows our proposed architecture for complex bandpass noise-shaping of DAC nonlinearities. It consists of a digital complex bandpass filter at front-end, two DACs, and an analog complex band elimination filter at back-end. The transfer function of the digital complex bandpass filter at front-end is

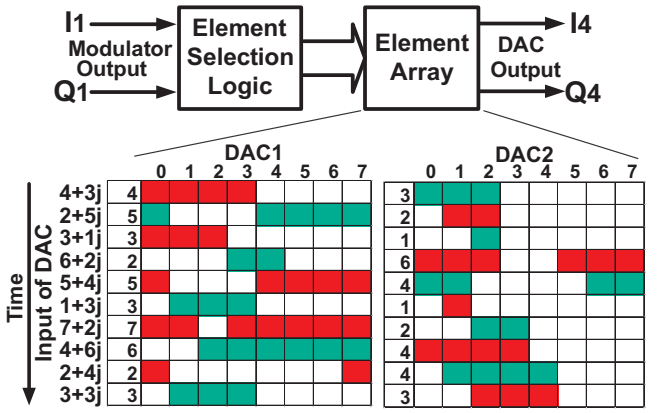

Fig. 4. Explanation of our complex bandpass DWA algorithm. The unit-current-cells in ON state are filled in black for a real part (I-path) and in gray for an imaginary part (Q-path), when the complex input data are sequentially given by 4+3j, 2+5j, 3+j, 6+2j, ...

the same as Eq.(3), while the transfer function of the analog complex band elimination filter at back-end is given by

$$H(z) = 1 - jz^{-1}. \tag{4}$$

Therefore, nonlinearities error of two DACs $e1 + je2$ can be noise shaped in a complex form at $f_s/4$, the notch of Eq.(4). In practice, however, this structure cannot be realized because the input signals may be infinite (out-of-DAC-input-range). Then the equivalent implementation called complex DWA algorithm is proposed to realize the architecture of DACs shown in Fig.3.

Our implementation uses only a digital filter at front-end of 2-channel DACs and does not require an analog filter at back-end. Element selection logic circuits (DWA1 and DWA2) are added between the two ADC outputs and DAC inputs to select the DAC unit-elements in a rotational manner [4] as shown in Fig.4. For the I-channel DAC output I_4, we apply a *highpass* DWA algorithm [8] with internal interaction between I, Q modulator output. For the Q-channel DAC output Q_4, we apply a *lowpass* DWA algorithm [9] with internal interaction between I, Q modulator output. DAC1, DAC2 are used alternately for I, Q-channels, and hence mismatch effects

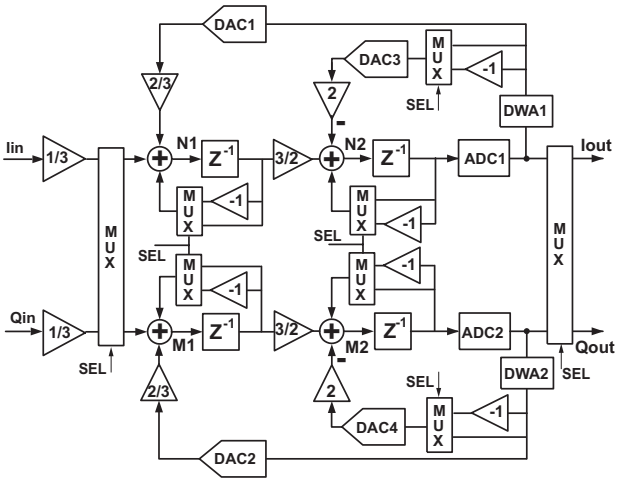

Fig. 5. Architecture of our complex bandpass $\Delta\Sigma$AD modulator.

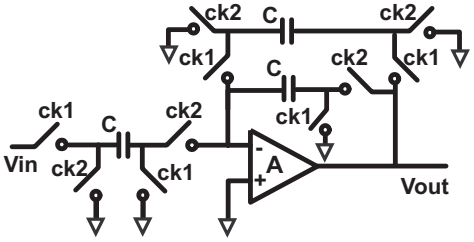

Fig. 6. Switched-capacitor delay cell.

between two DACs $e1 + je2$ are first-order complex bandpass noise-shaped at $f_s/4$. Our algorithm can be implemented by simple circuitry; analog and digital multiplexers, barrel shifters and adders/subtractors.

V. Circuit Implementation

Fig.5 shows our entire proposed complex bandpass $\Delta\Sigma$AD modulator. We see that the proposed second-order complex bandpass filter which shares some MUXs are used so that the proposed modulator has no crossing signal lines for either the forward paths of z^{-1} block or the feedback paths from DACs. Hence the proposed modulator can be completely divided into two separate parts and its layout design can be greatly simplified. Then its internal signal lines can be shorter, which leads to smaller chip area.

For the proposed architecture, we note that MUXs can be realized by MOS switches easily. Moreover we add MUXs which alternate the polarity of the fedback signals between +1 and -1 at every sampling time to the feedback paths of filters and DACs. This is to keep the polarity of internal complex signals so that they are processed as a complex signal form [10]. In fact we can realize this simply by chopping the two differential outputs at every sampling time.

The proposed modulator was designed with fully differential switched capacitor circuits. z^{-1} block realization by SC delay-cell [7] is shown in Fig.6 in its single-ended form, but the

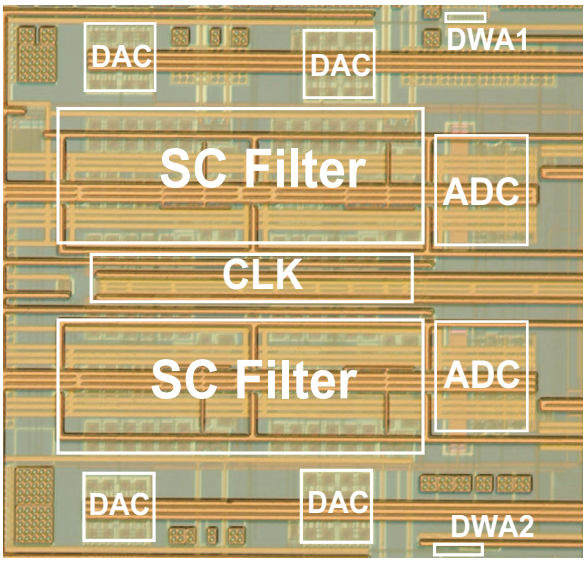

Fig. 7. Chip photopragh.

actual one is fully differential form in out modulator. Gate-boosted NMOS switches and dummy switches are used at the input sampling parts to cancel the effect from charge injection and clock feedthrough, while all the others are CMOS switches. $ck1$ and $ck2$ are non-overlapping clocks in our modulator to minimize the charge injection by sampling switches. Latched comparators with input offset-storage are used in the flash-type 9-level ADCs, where offset cancellation is applied to both preamplifier and the latch.

VI. Experimental Results

Proposed complex bandpass $\Delta\Sigma$ modulator was fabricated with a 1P6M 0.18μm CMOS technology without any option for precision capacitors and low-threshold voltages. Fig.7 shows its chip microphotograph and its core size is $1.4 \times 1.3mm^2$. The capacitors were realized using multiple unit-capacitor-cell for accurate ratio matching of coefficients. Unit-capacitor-cell was realized by MIM structure for high capacitance density in small chip area.

Fig.8 shows output power spectrum comparison of the modulator for zero input between at ON/OFF stage of DWA logic. We see that while DWA logic is at ON state, noise floor at the band of interest is about 3dB lower than that while DWA logic is at OFF state. Fig.9 shows the measured output power spectrum for a 4.92MHz sinusoidal input, while the reference voltages of the modulator were tied to $V_{ref+} = 1.9V$ and $V_{ref-} = 0.9V$.

The degree of the mirror image signal suppression in the modulator was evaluated by demodulating the complex IF-signal down to baseband with quadrature carriers in the digital domain and performing an FFT on the resulting complex-valued signal, The spectrum of the demodulated, complex valued baseband signal is shown in Fig.10. It is observed that the image signal is suppressed by 46 dB with respect to the desired signal.

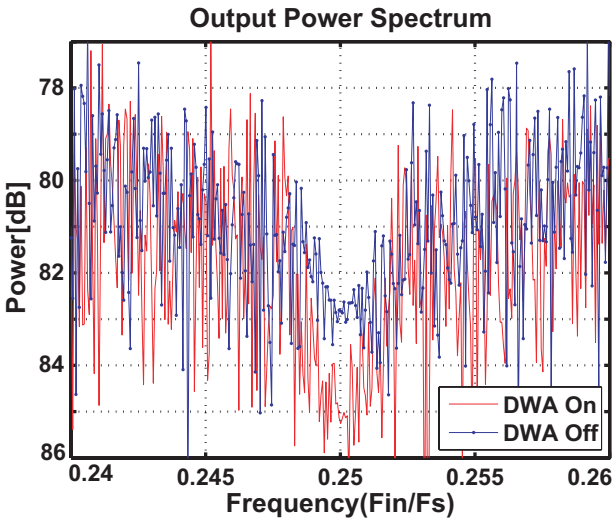

Fig. 8. Compared power spectrum while DWA on and off.

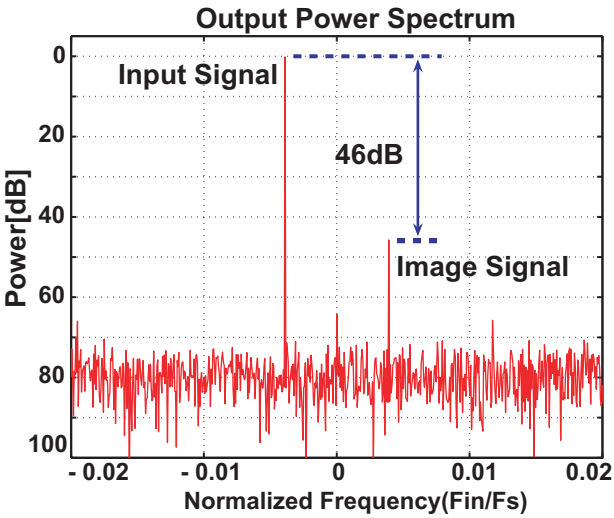

Fig. 10. Measured output power spectrum of the proposed modulator.

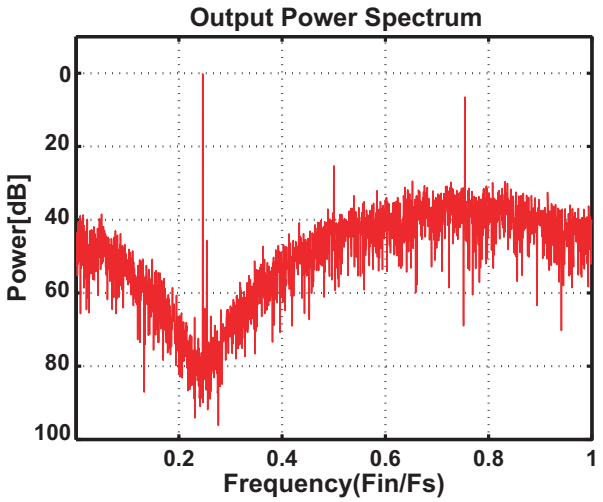

Fig. 9. Measured output power spectrum of the proposed modulator.

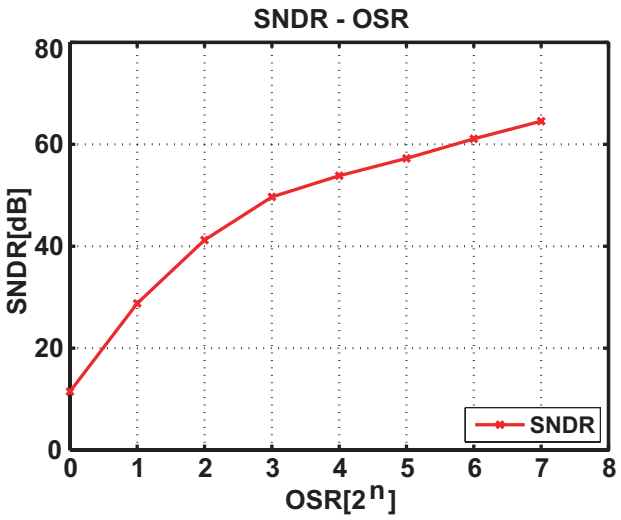

Fig. 11. Measured SNDR vs OSR of the proposed modulator.

Fig.11 shows SNDR vs OSR that and the peak SNDR is 64.5dB. Clocked at 20MHz the modulator consumes 28.4mW under 2.8V power supply voltage.

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