A Parallel Analog CMOS Signal Processor for Image Contrast Enhancement

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Abstract A 2D analog CMOS network with a 53 × 52 array of embedded photosensors implements a convolution function approximating the Laplacian of a Gaussian. Experimental results verify that high quality contrast enhancement of images of simple objects may be obtained in analog circuits with careful circuit design. The 7.9 × 9.2 mm IC dissipates 350 mW from a 5 V power supply.

Introduction

The ∇^2G (Laplacian-Gaussian) filter, also known as the DOG (Difference of Gaussians) filter, is known to enhance contrast in 2D images, and, under appropriate assumptions, the zero-crossings of the filtered image intensity locate the edges [1]. This paper reports a fully analog implementation of a ∇^2G like filter with an embedded array of image sensors. The chip is fabricated on a standard 2μm double metal CMOS process, and implements the architecture proposed in [2]. The ∇^2G-like operation is executed within microseconds by the concurrent analog computation.

Architecture

The single IC contains *two* superimposed resistive meshes. Each mesh implements a cusped exponential convolution [3], which may be regarded as a crude approximation to the Gaussian. The first mesh is excited by a photocurrent at every node proportional to the (log compressed) intensity of a sampled pixel from the incident image. The response of the first mesh is then again convolved by the second mesh. The *difference* between the two outputs may be shown to produce a ∇^2G-like response [2]. The nominal parameter values are

$$1/g_{m1} = 1/g_{m2} = 600\text{k}\Omega,\ 1/g_{s1} = 400\text{k}\Omega,\ T_1 = g_{m1} = g_{m2}$$

The horizontal conductance g_{s2} of the second layer controls the degree of contrast enchancement. $1/g_{s2}$ is designed to be variable between 20kΩ and 200kΩ.

Circuits

The IC consists of 53×52 unit cell circuits (Fig.2) arranged on a hexagonal grid to implement both meshes,

where v_{1k} (resp. v_{2k}) stands for the first (resp. second) layer voltage at node k, and x_k is the output $v_{1k}-v_{2k}$. Two series PMOSFETs convert the photocurrent induced in the (parasitic) vertical bipolar transistor into voltage. The FETs operate in subthreshold at this small current density, so the output voltage depends on the logarithm of the photocurrent. A transconductance amplifier with unity voltage feedback buffers the compressed photovoltage, and the amplifier output conductance, $g_{m1}(g_{m2})$, acts as the conductance to ground required at every node in the network. This implements the Thevenin equivalent of the current source in Fig.1. The six FETs connected to the v_{1k}-node are half of the six horizontal conductances g_{s1} of Fig.1. The lower part of Fig.2 represents the second mesh, whose circuitry is the same as that of the first layer. The differential pair in the lower left part computes $v_{1k}-v_{2k}$. The stimulus to the network (the compressed photovoltages), and the network response may be read out as analog quantities on to a shared data line through the column addressable pass transistors. An output buffer circuit (not shown) drives the pads, and data is digitized and stored in a frame buffer to reconstruct the 2D image. All subcircuits are simple. For example, the conductances are realized by a series connection of two PMOS transistors. Fig.3(a) shows the subcircuit which realizes g_{s2}. Suppose M1 and M2 operate in the triode region. Let V_n be the drain voltage of M1 and hence the source voltage of M2. If $V_1 > V_2$, then the drain currrents in M1 and M2 are given, respectively, by

$$I_1 = \beta[(|V_C|-|V_t|)(V_1-V_n)-(V_1-V_n)^2/2], \quad I_2 = \beta[(V_n-V_2-|V_C|-|V_t|)(V_n-V_2)-(V_n-V_2)^2/2]$$

where $\beta=k(W/L)$ is the same for M1 and M2. If $(V_1-V_2) << 2(V_C-V_t)$, then

$I = I_1 = I_2 \cong \beta(|V_c-V_t|)(V_1-V_2)$.

This realizes an approximately linear conductance $g = \beta(|V_C|-|V_t|)$. The value of g_{s2} may be modified by another PMOSFET in parallel with an externally adjustable gate bias (Fig.3(b)). The chip requires a single 5V power supply, and dissipates 350mW, inclusive of the output buffer circuits.

The circuit design attempted to strike a balance between reducing the effects of mismatches and offsets which plague the accuracy of all analog signal processors, and minimizing the power dissipation accumulated over the more than 2500 unit cells on the chip. Consequently, all MOSFETs following the photosensor were biased with $|V_{GS}-V_t| > 0.5\,\mathrm{V}$, but their operating currents were kept low by using the smallest possibleW/L ratios.

A resistive mesh previously reported [4] to implement Gaussian smoothing on images was different in several key respects from this work:

- That network performed smoothing only, while here the chip *enhances image contrast* after smoothing.
- Unlike the Gaussian filter [4], there are *no negative conductances* in this chip. Potential instability [5] in the spatial impulse response is thus circumvented.
- The architecture in [4] requires connections between nearest and second nearest neighbor nodes, which was difficult to lay out. This network requires *only nearest neighbor* connections.

Experimental Results

The spatial impulse response of the network (Fig.4) was measured by subjecting it to light through a tiny pinhole in the chip cover. An *antagonistic surround* appears as the negative response off the center, which is responsible for contrast enhancement. The response compares well with simulations of an ideal network

(Fig.5). A dark halo surrounds the response of the network (Fig.6(b)) to a circular disk of light (Fig.6(a)); the network also smooths out noise in front of the disk. Most dramatic is the contrast enhancement in the image of a plastic cup (Fig.7(b)) when compared to the incident image on the chip (Fig.7(a)). After differentiation of the intensity map, the halo on the outline of the cup will accentuate the object boundary. The expected variation of the extent of smoothing with g_{s2} has also been experimentally verified. The high quality of the sensed and smoothed images may be attributed to the precautions in circuit design described above. Finally, we note that our architecture (Fig.1) was inspired by physiological studies on the retina of lower vertebrates conducted by one of the authors (Yagi).

References

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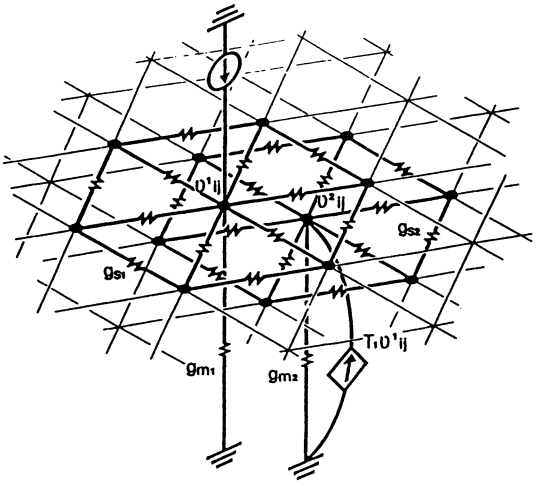


Fig.1. Network consists of two coexistent resistive meshes

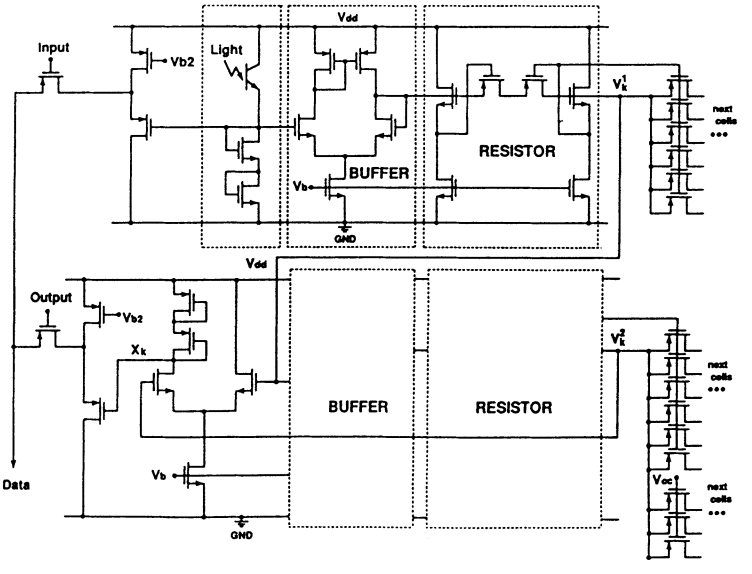


Fig.2. Schematic of the unit cell, including subcircuits for both meshes

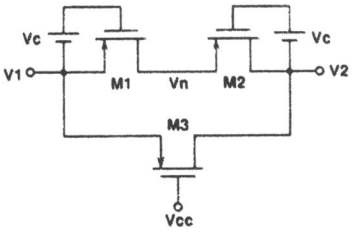


Fig.3 (a) Principle of linearized MOSFET resistor

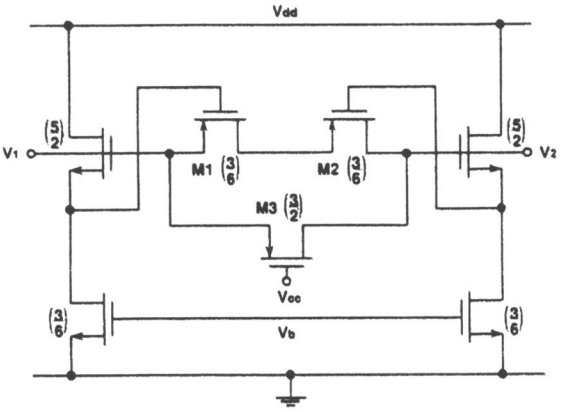


Fig.3 (b) Implementation of horizontal resistor

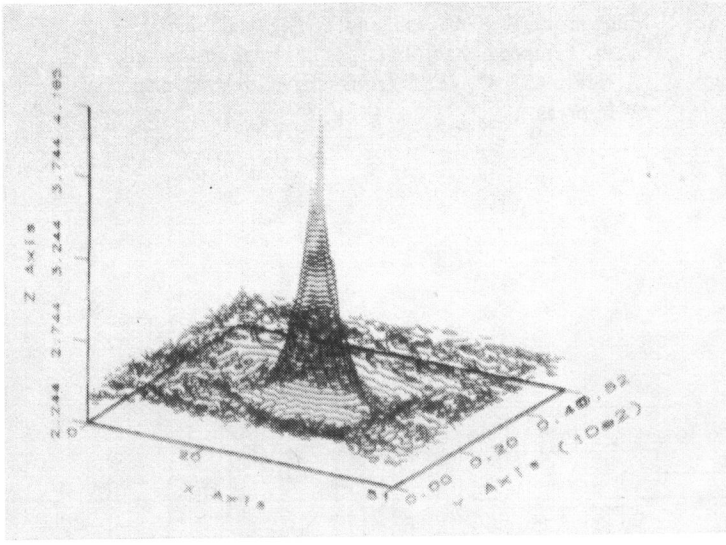


Fig.4. Measured spatial impulse response

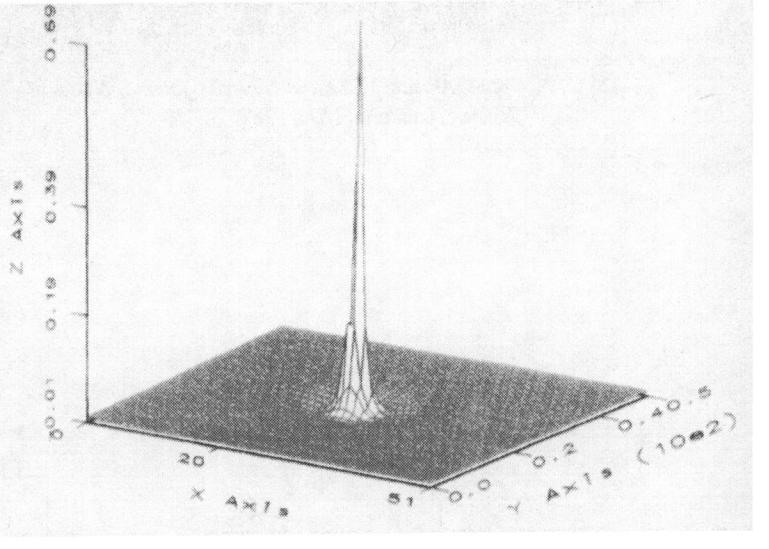
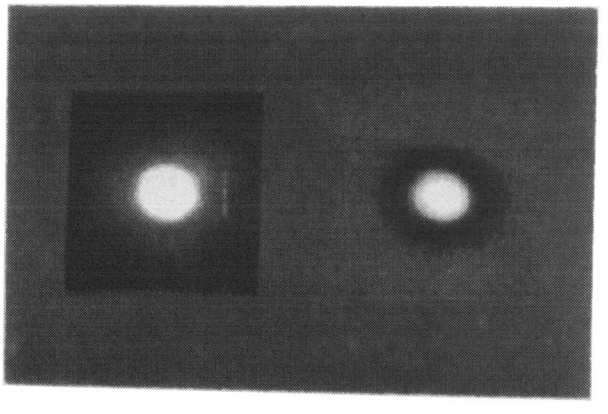


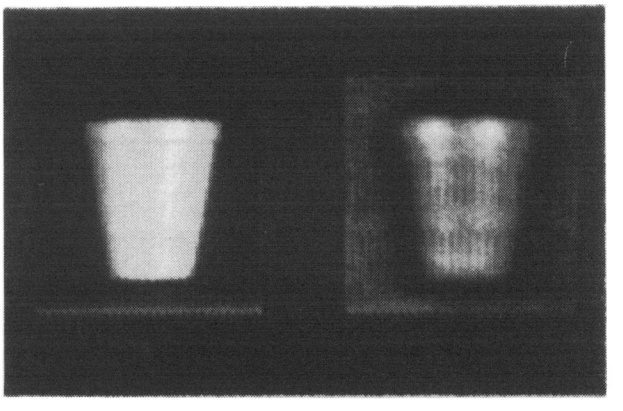
Fig.5. Simulated spatial impulse response



(a) Fig.6 (b)

(a) Measured input stimulus to network with disk image

(b) Measured network output of smoothed disk



(a) Fig.7 (b)

(a) Measured input stimulus to network with cup image

(b) Measured network output of smoothed cup