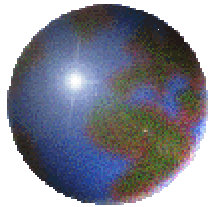
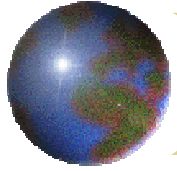


Spread-Spectrum Clocking in Switching Regulators to Reduce EMI



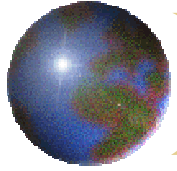
H. Sadamura, T. Daimon, T. Shindo,
H. Kobayashi, M. Kono
EE Dept. Gunma University, Japan

T. Myono, T. Suzuki, S. Kawai, T. Iijima
Sanyo Electric Co. Ltd., Japan



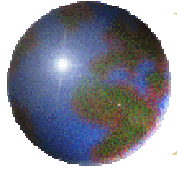
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- ⊕ Principle of DC-DC Converters
- ⊕ Proposal of Noise Power Spectrum Spread Method in DC-DC Converters
- ⊕ Implementation and Measurement Results
- ⊕ Summary



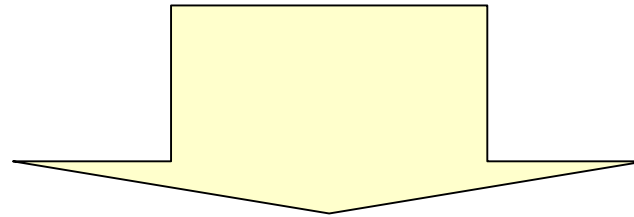
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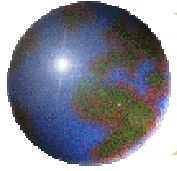


Research Background

- Mobile equipment prevails everywhere
- Mobile phone, Digital still camera, PDA



- Small size, High efficiency
- Multiple supply voltages
- Low-voltage supply



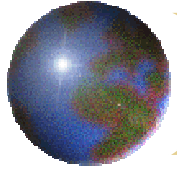
Features of Switching Regulator

☀ Merit

- ☒ High efficiency
- ☒ Continuously varying output voltage
- ☒ Large output current

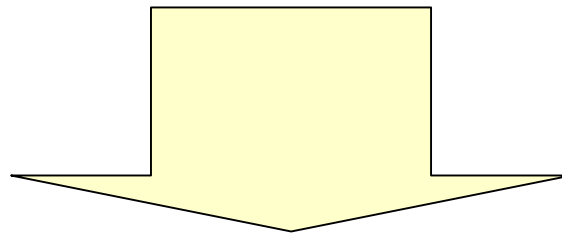
☀ Demerit

- ☒ Coil is required. ➡ bulky and costly
- ☒ Switching noise

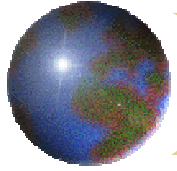


Research Goal

- ✚ We focus on a big problem of switching regulator:
“Switching and harmonic noises”

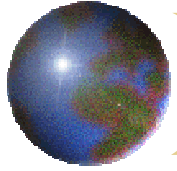


***Proposal of EMI reduction technique
by spreading noise power spectrum***

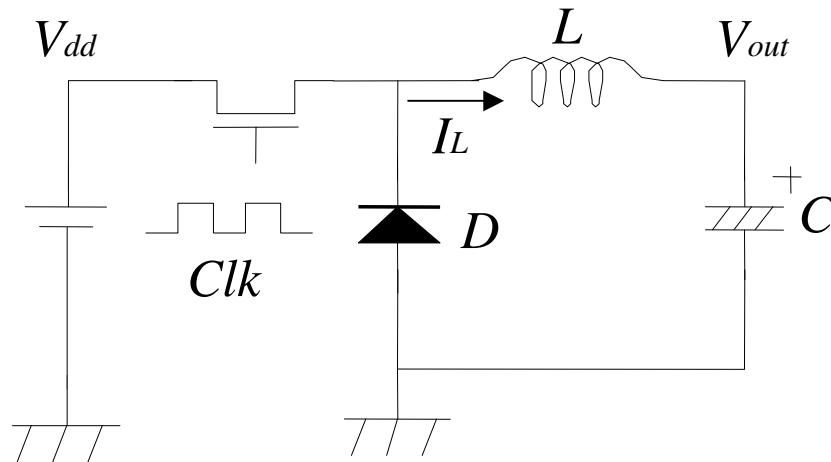


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Principle of DC-DC Converter(1)



◆ In case Clk=ON

$$\Delta I_{L1} = \frac{V_{dd} - V_{out}}{L} \times T_{on}$$

◆ In case Clk=OFF

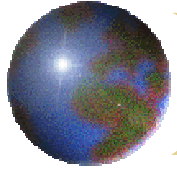
$$\Delta I_{L2} = -\frac{V_{out}}{L} \times T_{off}$$

$$V_{out} = \frac{T_{on}}{T} \cdot V_{dd}$$

$$\Delta I_{L1} = \Delta I_{L2}$$

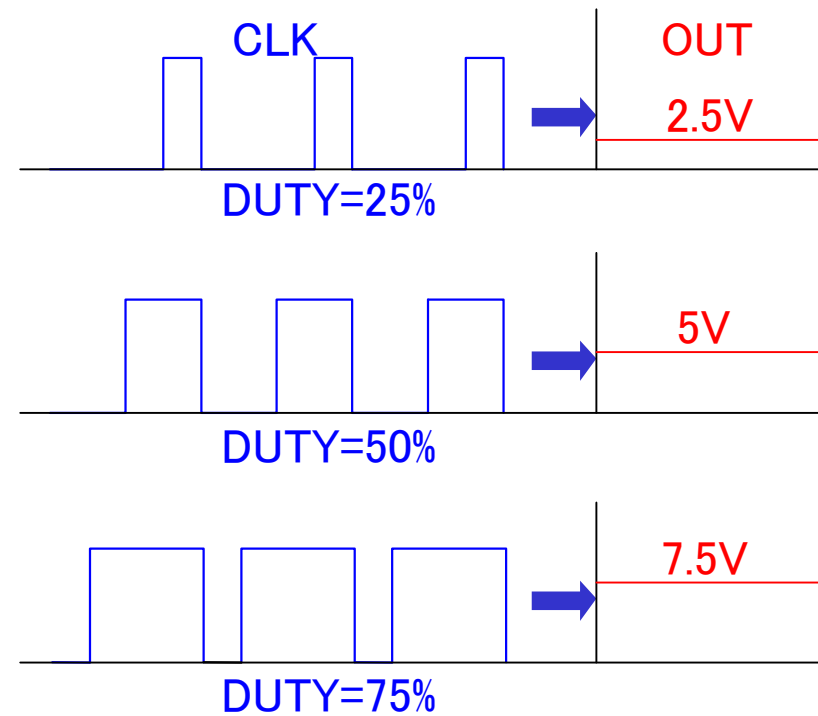
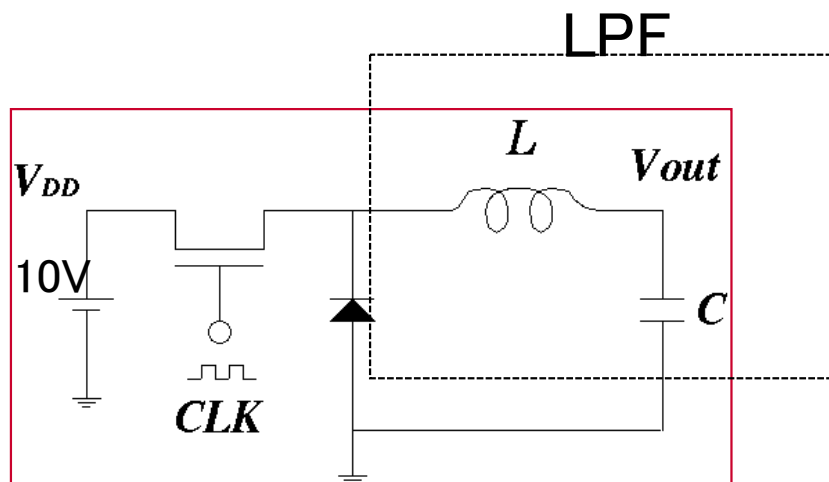
T; clock period

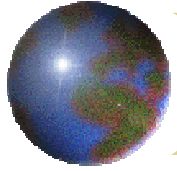
Output voltage V_{out} is determined by the clock duty.



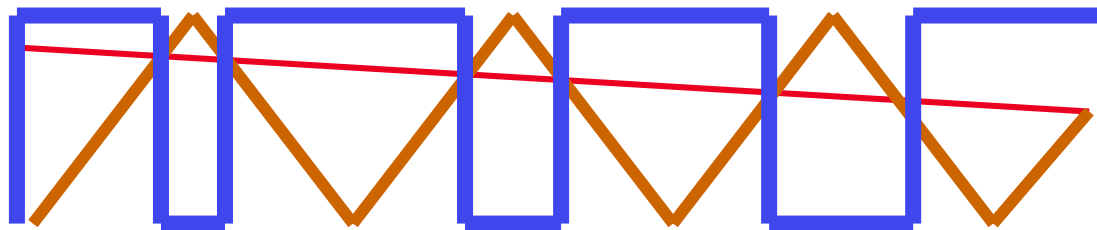
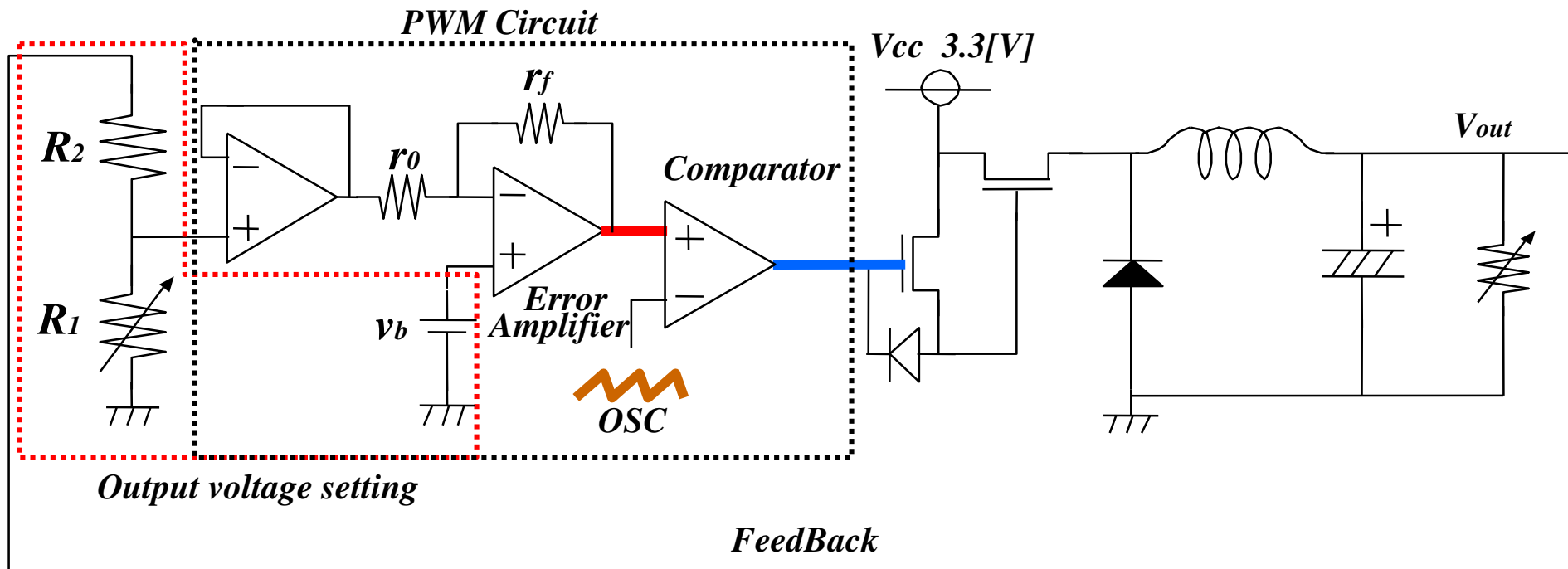
Principle of DC-DC Converter(2)

- **V_{DD}**: Input voltage
- **CLK**: Switching clock
- **L, C**: Low pass filter for smoothing
- **V_{out}** : Output voltage

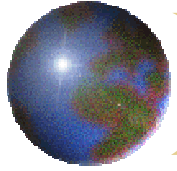




DC-DC Converter with PWM Controller



Comparator output
Error amplifier output
Triangular wave

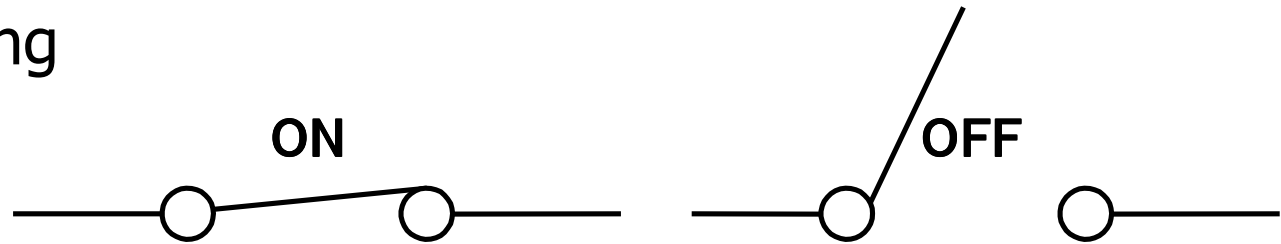


Features of PWM Control

Advantage

ON/OFF switching

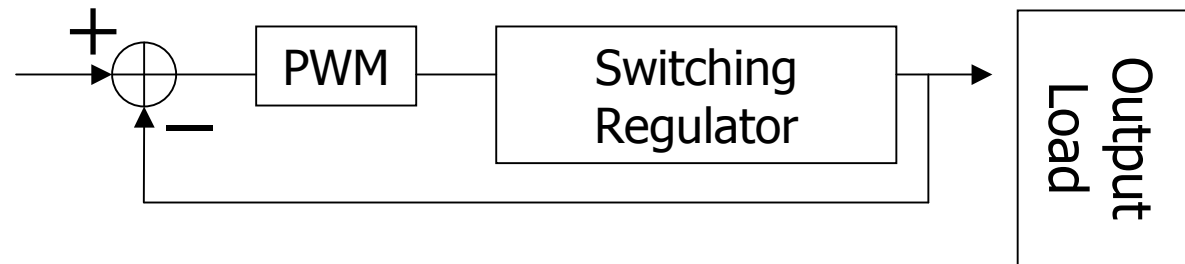
⇒ High efficiency



Negative feedback control

⇒ Output is stable regardless of output load.

Output voltage setting

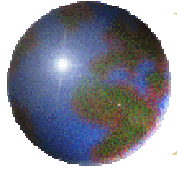


Disadvantage

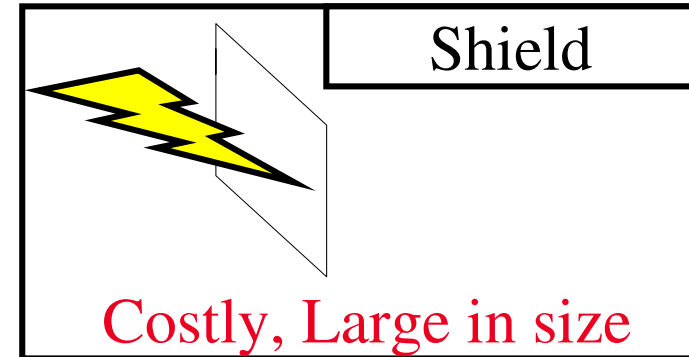
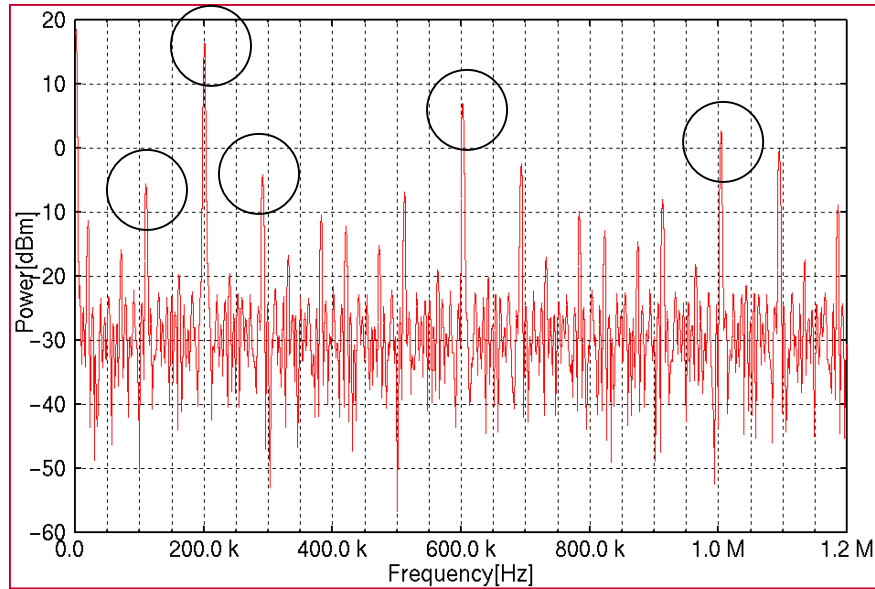
Synchronization with clock



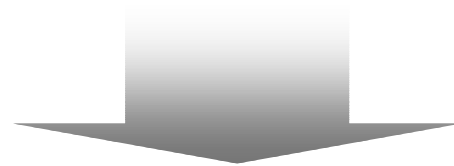
Harmonic noises
in specific frequencies



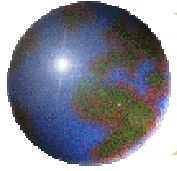
EMI and Switching Regulator



**Shield is required
to meet EMI Regulations**

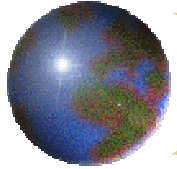


Proposal of EMI reduction circuit



Contents

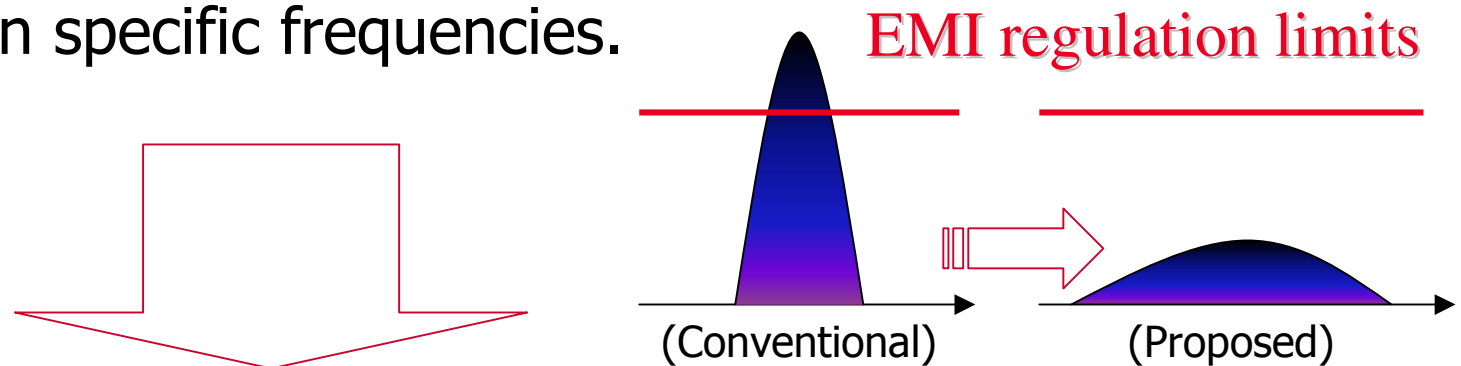
- Research Background and Goal
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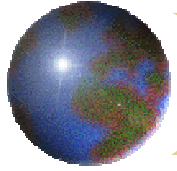
Proposed Method

**Conventional DC-DC Converter +
Extra Digital Control Circuit**

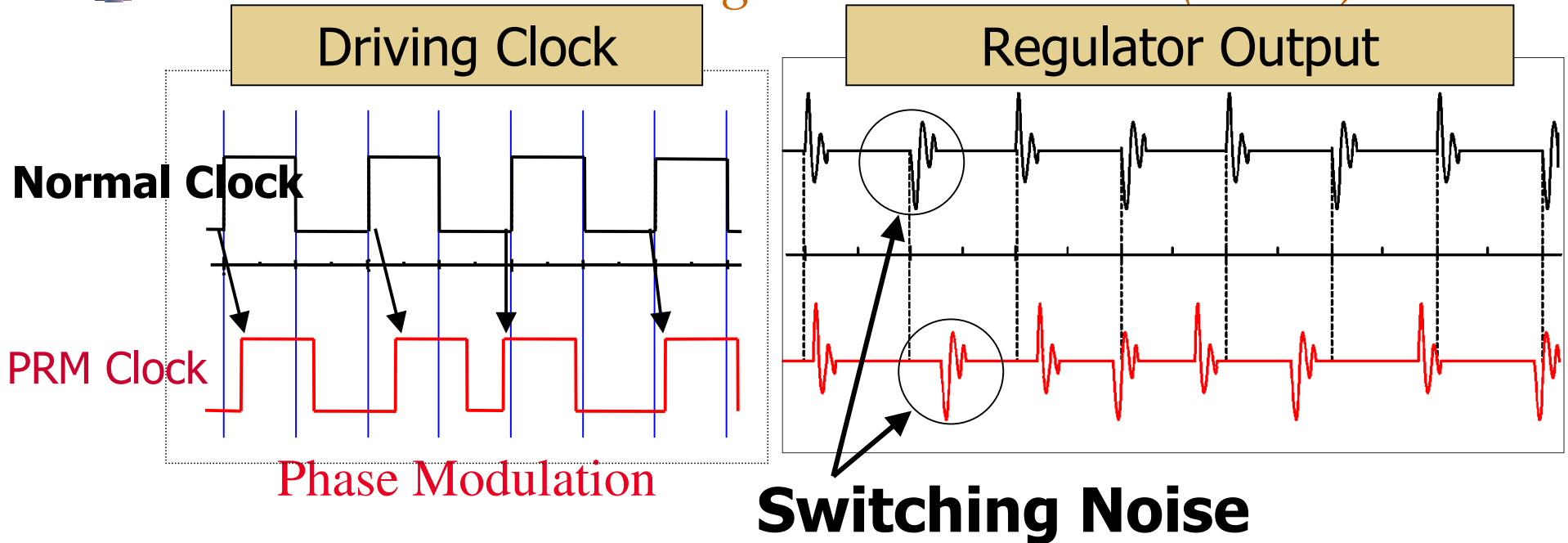
Generated switching noise power spectrum are
in specific frequencies.



By spreading the spectrum of switching noise power,
EMI reduction is realized.



Principle of Pseudo-Random Digital Modulation (PRM)



•Effect of $V = L \frac{di}{dt}$

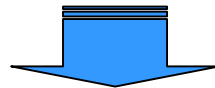
•Switching Control with Pulse



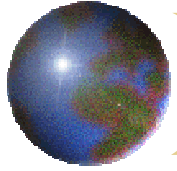
Large Switching Noises



Large Harmonic Noises

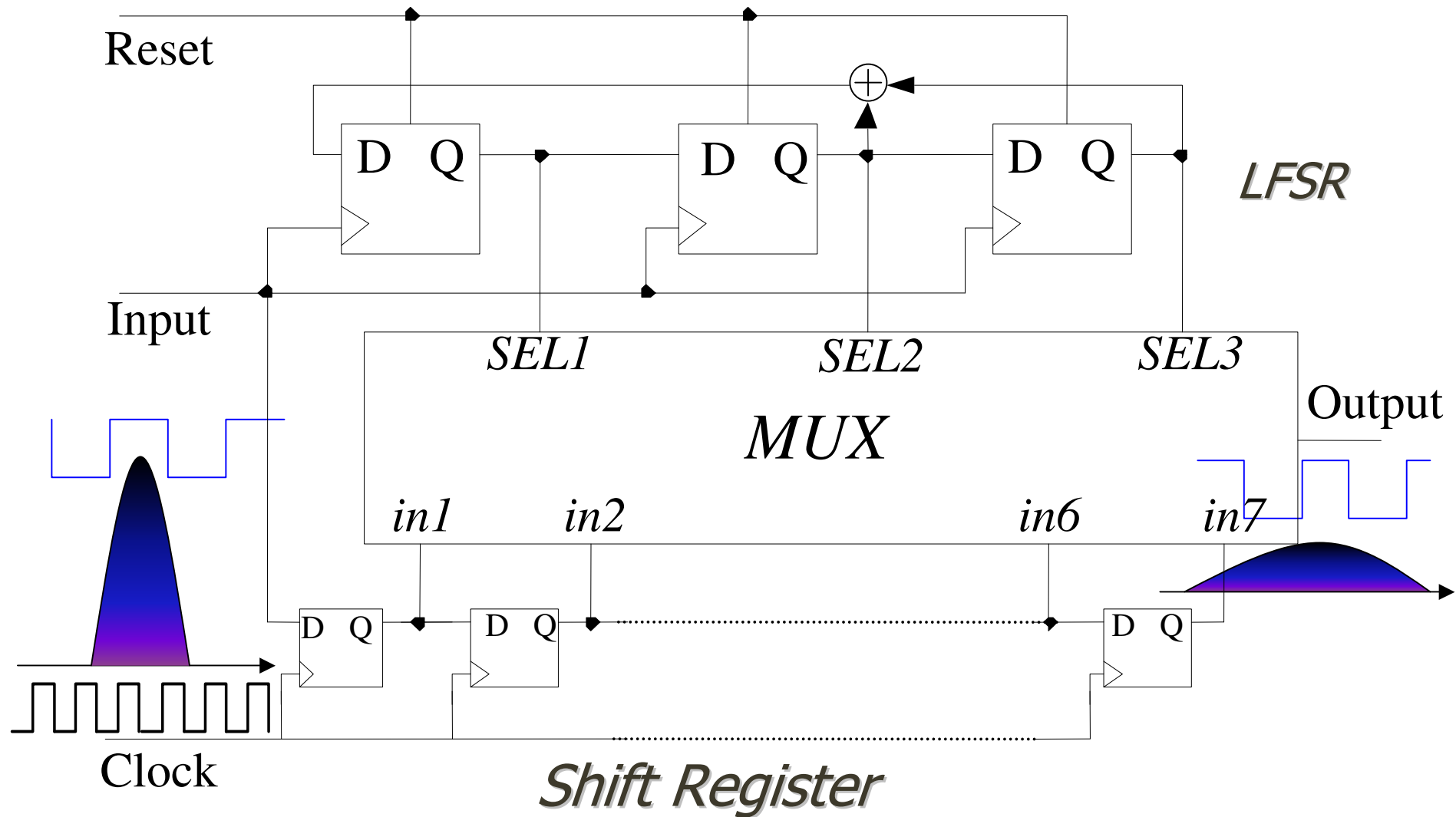


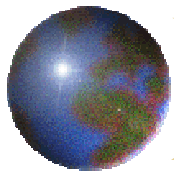
Pseudo-Random Spread Spectrum of Noise Power



PRM Circuit Implementation

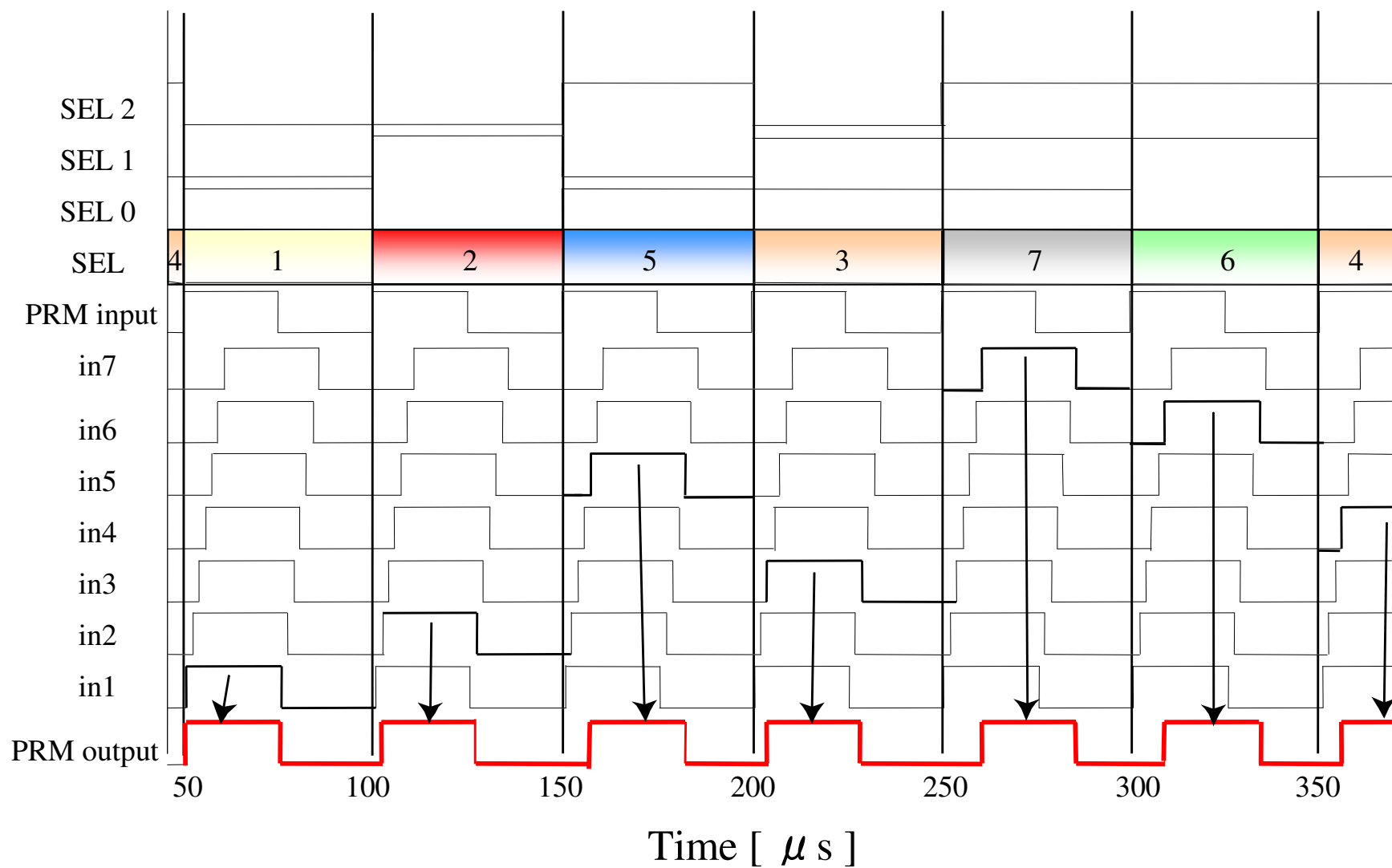
- 3bit LFSR case -

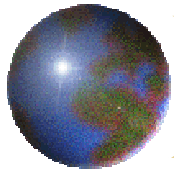




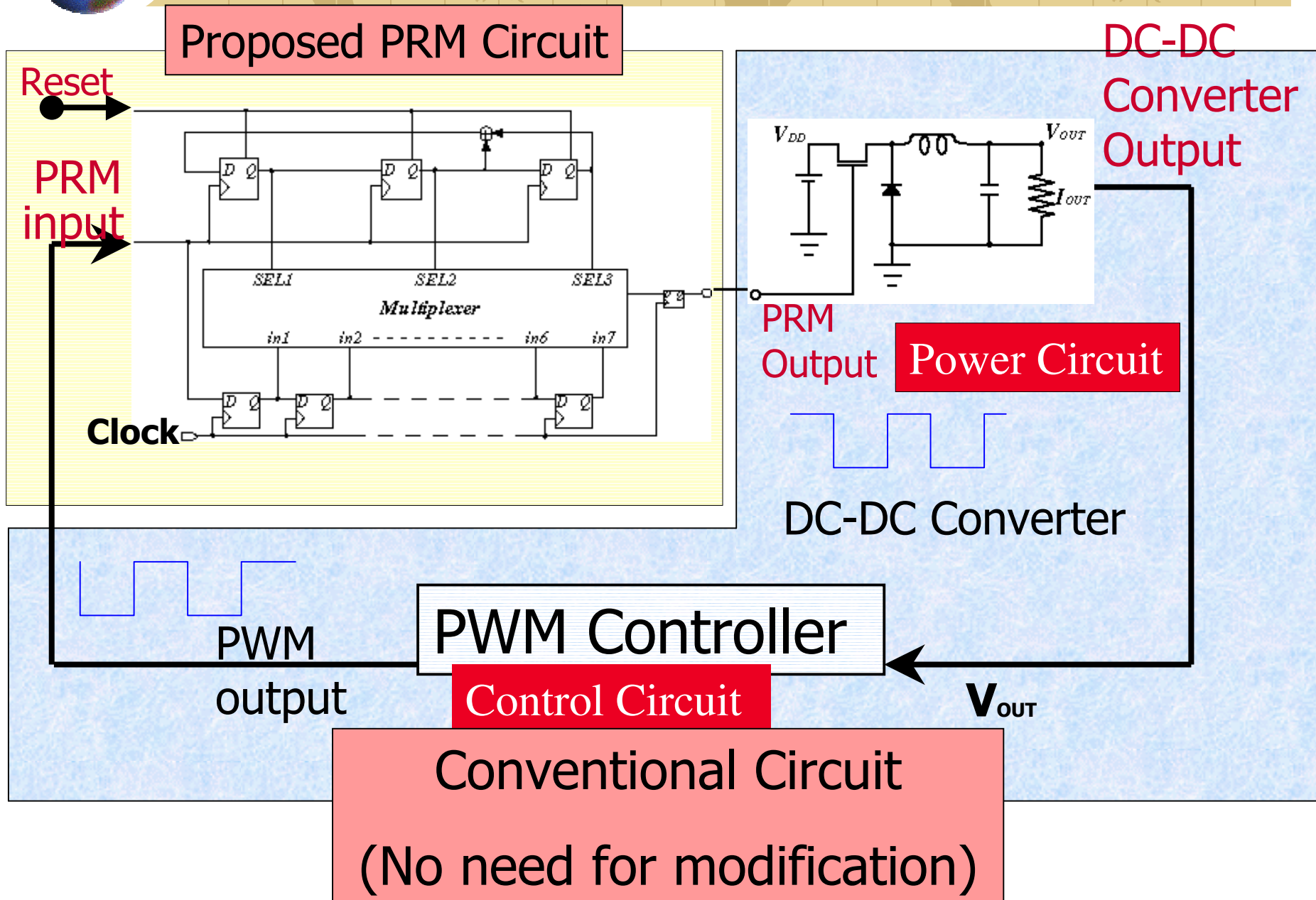
PRM Timing Chart

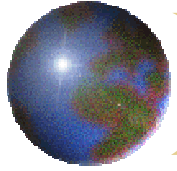
3bit LFSR case





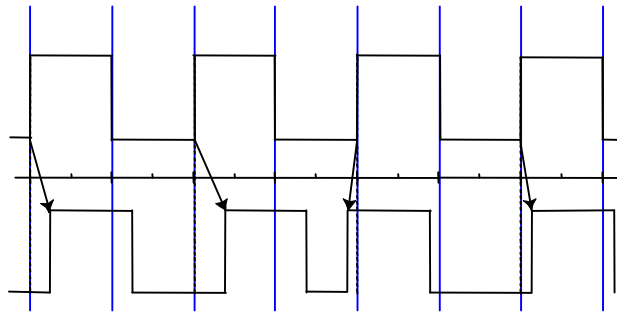
DC-DC Converter with PRM





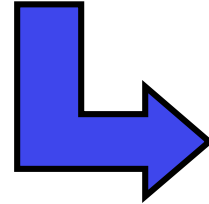
Optimal Clock Phase Shift(1)

Normal clock (Conventional)

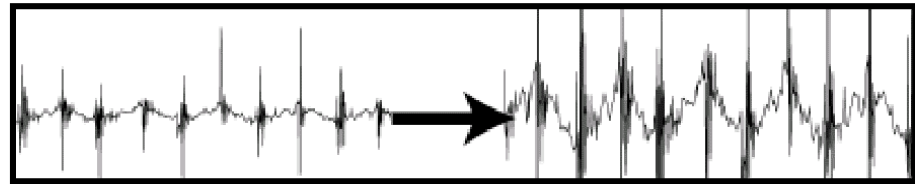


PRM clock (proposed)

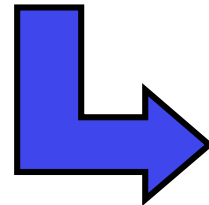
- When clock phase shift is too large,



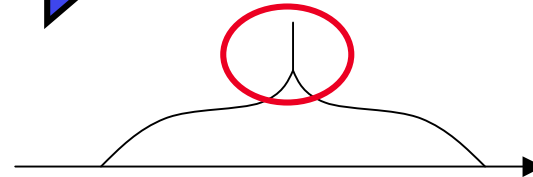
output ripple becomes too large



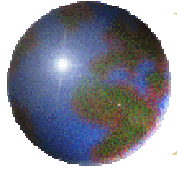
- When clock phase shift is too small,



noise spectrum are not spread sufficiently.



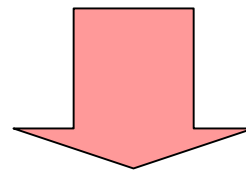
Optimal phase shift is obtained by measurement.



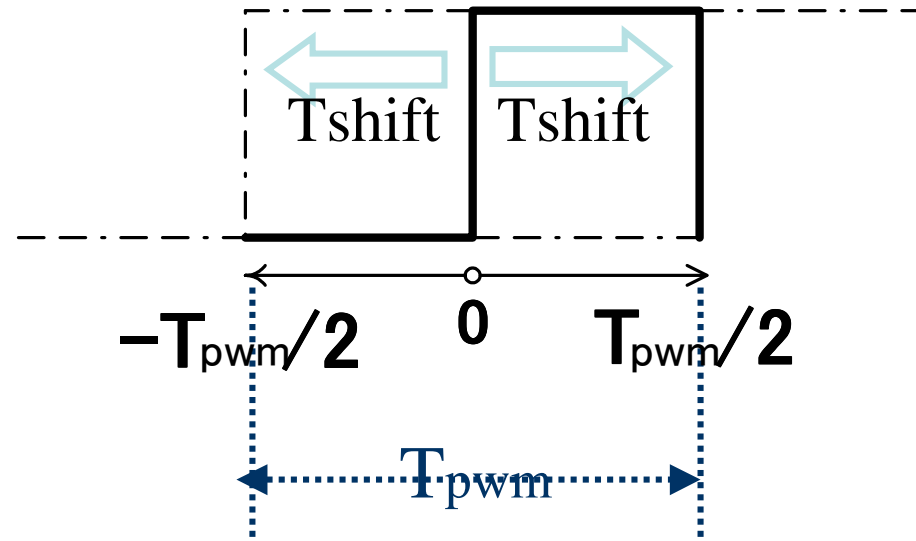
Optimal Clock Phase Shift(2)

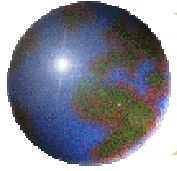
Optimal value of maximum phase shift (T_{shift})

$$T_{\text{shift}} = \frac{T_{\text{pwm}}}{2}$$



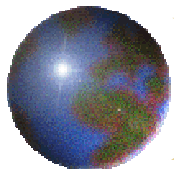
$T_{\text{pwm}} = \text{PWM clock period}$





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FPGA Design

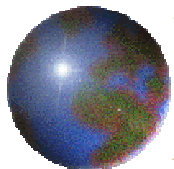
Evaluation Board

Design Item

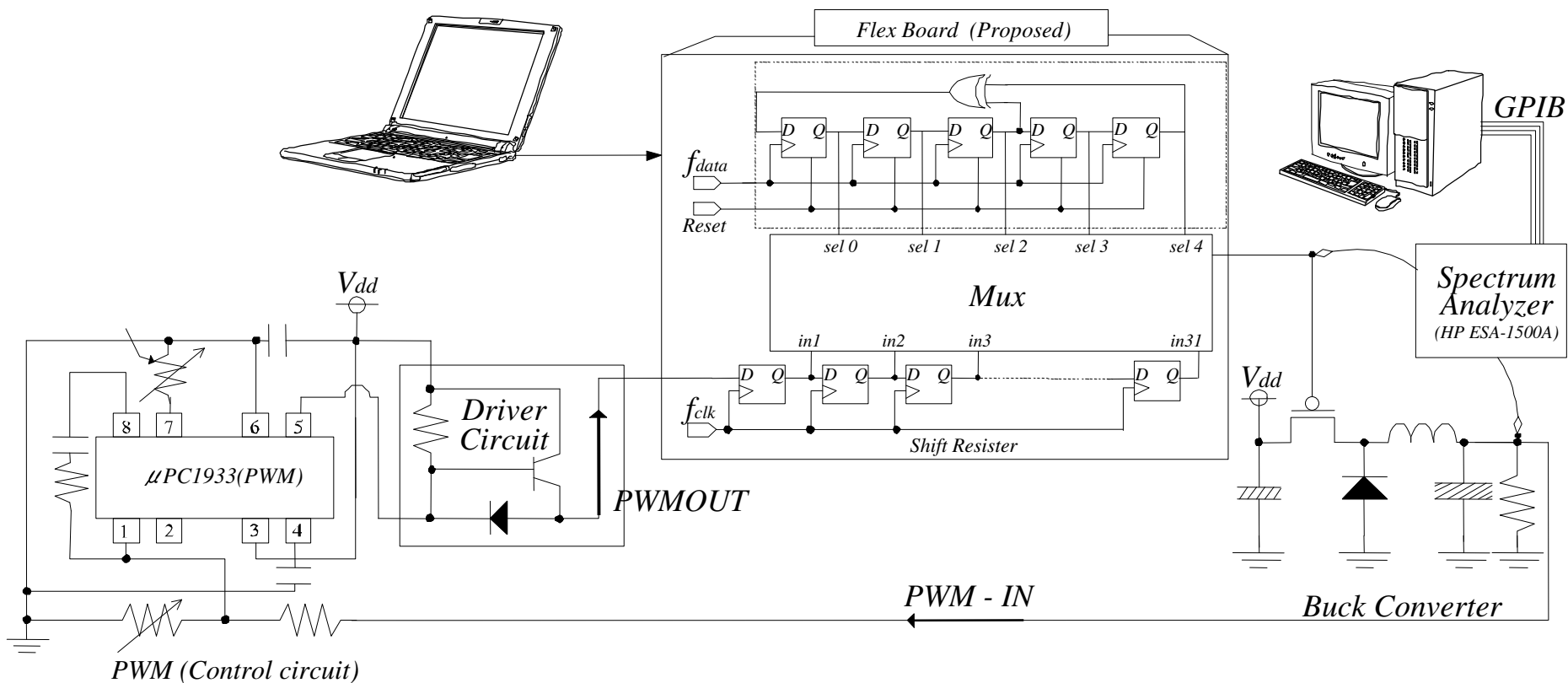
Technology:FLEX10K30EQC208 –3
(Altera)

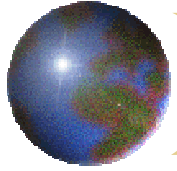


Item	Spec.
Spectrum Spread Method	Direct
Shift Register Clock	6MHz
PWM Input	187kHz
PN—code Control Clock	187kHz
Supply Voltage	3.3V
PN-code	M-Sequence
Code Length	31
The Number of DFFs	37

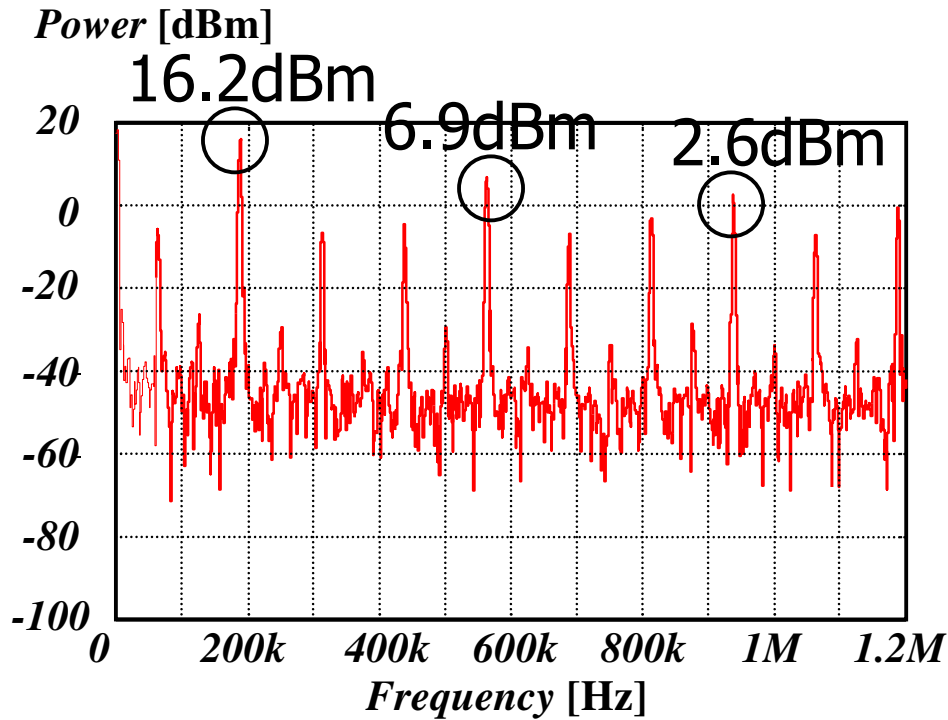


Measurement Setup

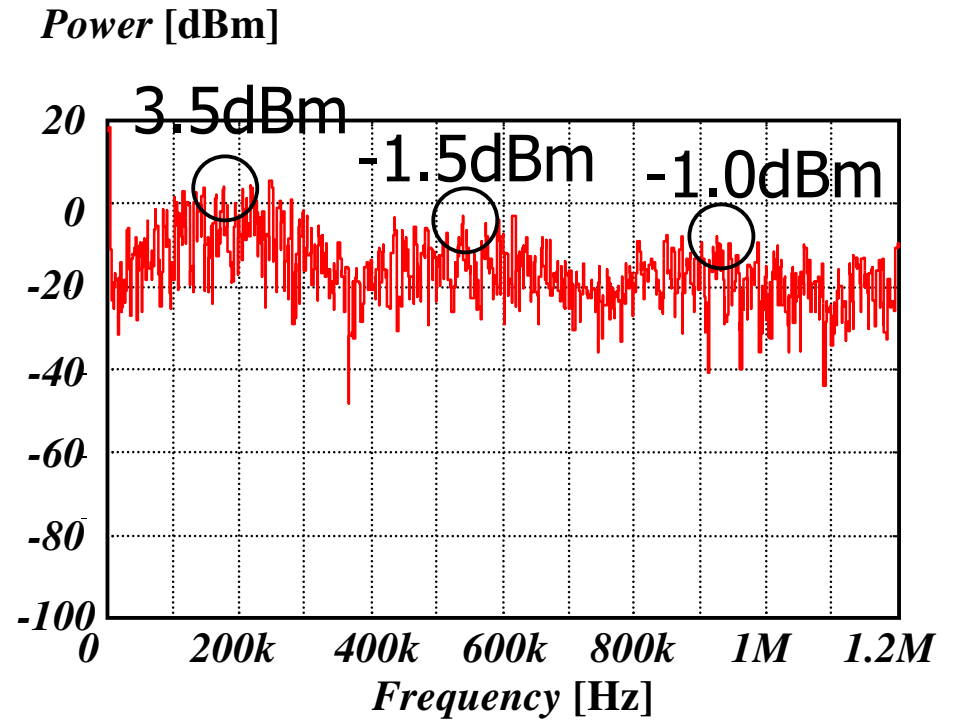




Measured Power Spectrum of Driving Clock

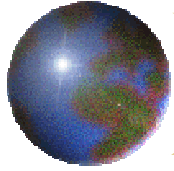


Power spectrum of
normal clock
(Conventional)



Power spectrum of
PRM output clock with
5bit M-sequencer
(Proposed)

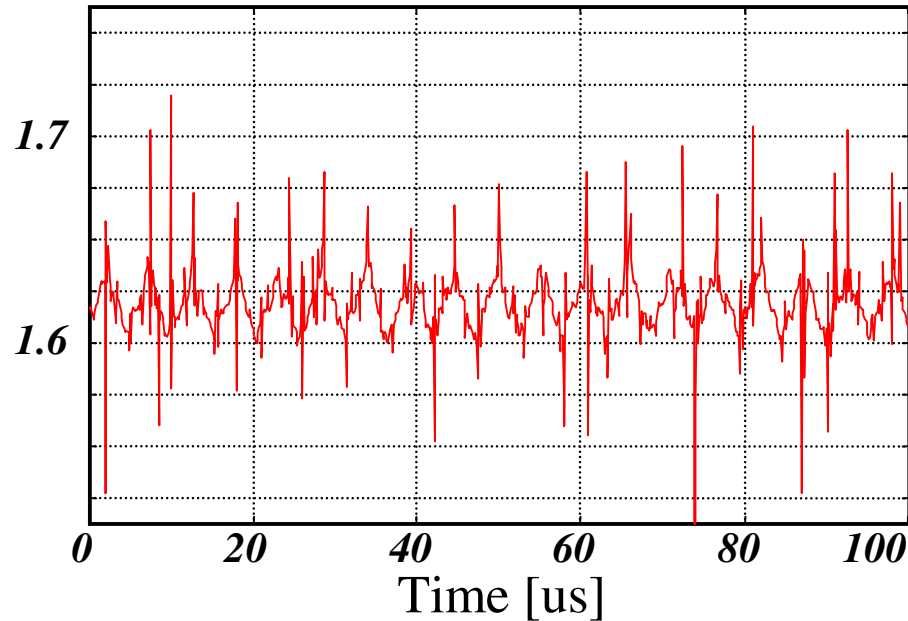
Maximum peak reduction by 12.7dBm



Measured Output Voltage Waveform of DC-DC Converter

Input voltage $V_{dd}=3.3V$, Clock duty = 50%

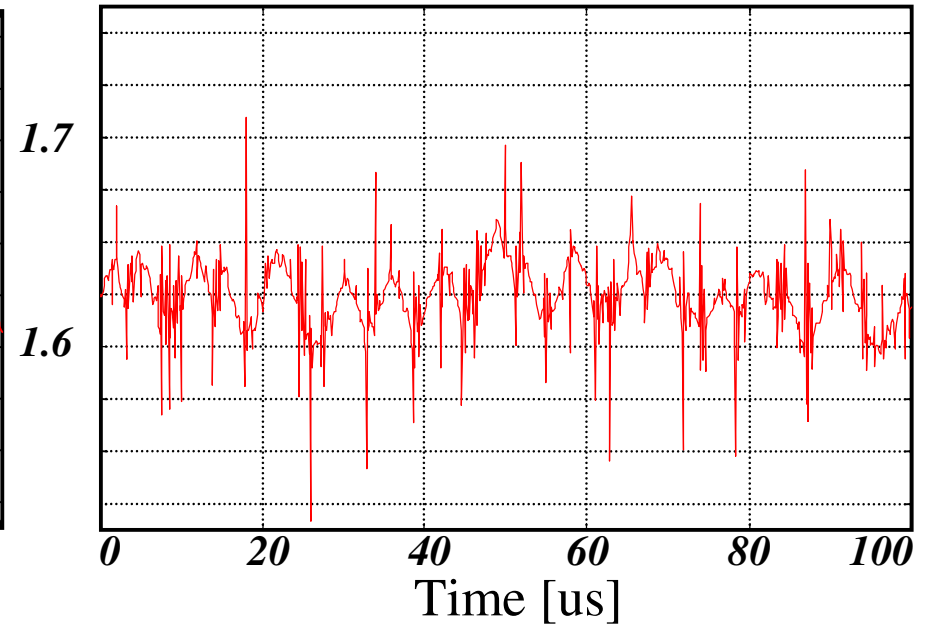
Amplitude [V]



Output waveform
with normal clock

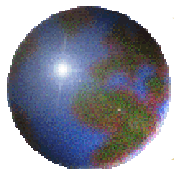
(Conventional)

Amplitude [V]

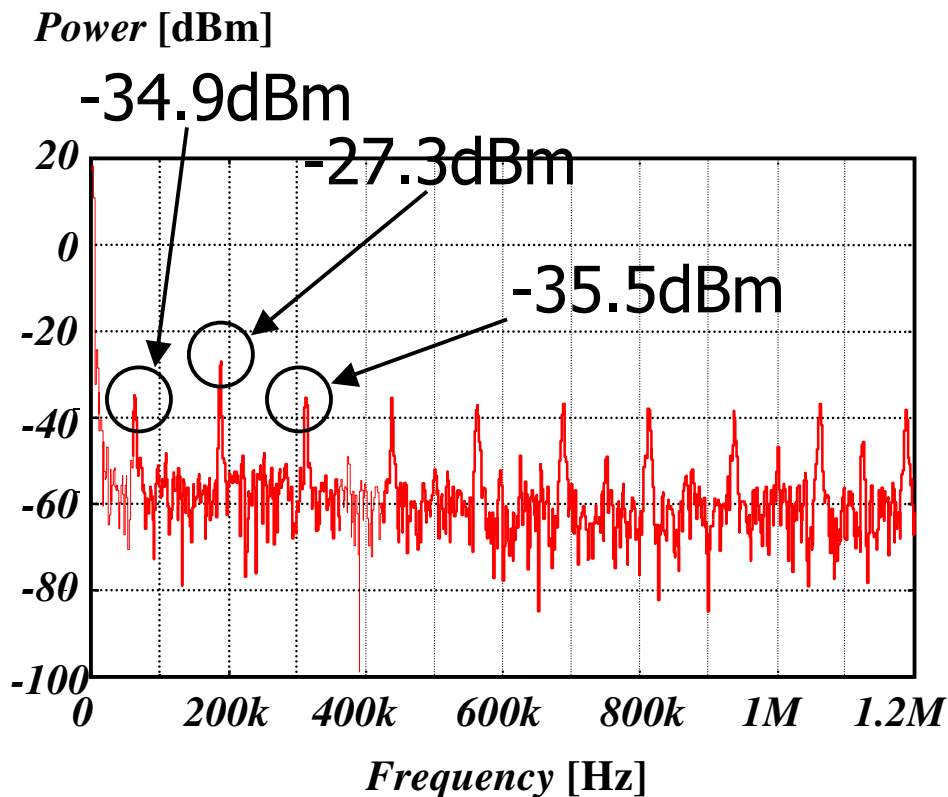


Output waveform
with PRM clock.

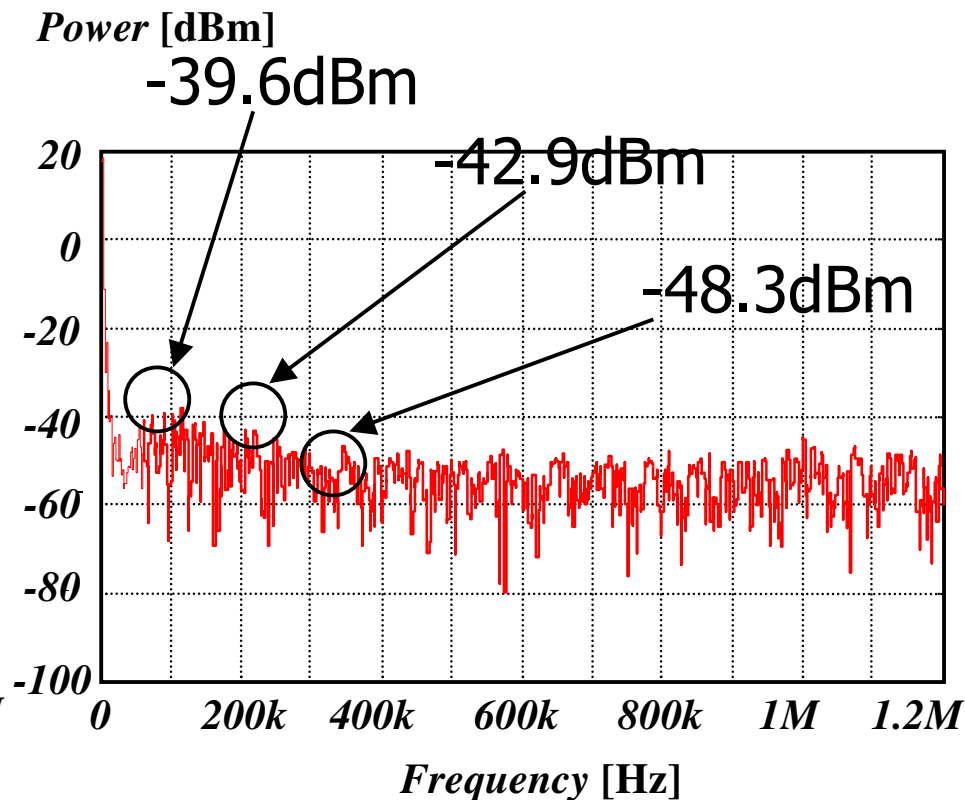
(Proposed)



Measured Output Power Spectrum of DC-DC Converter

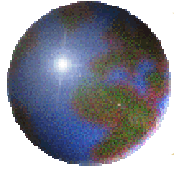


Output power spectrum with normal clock (Conventional)

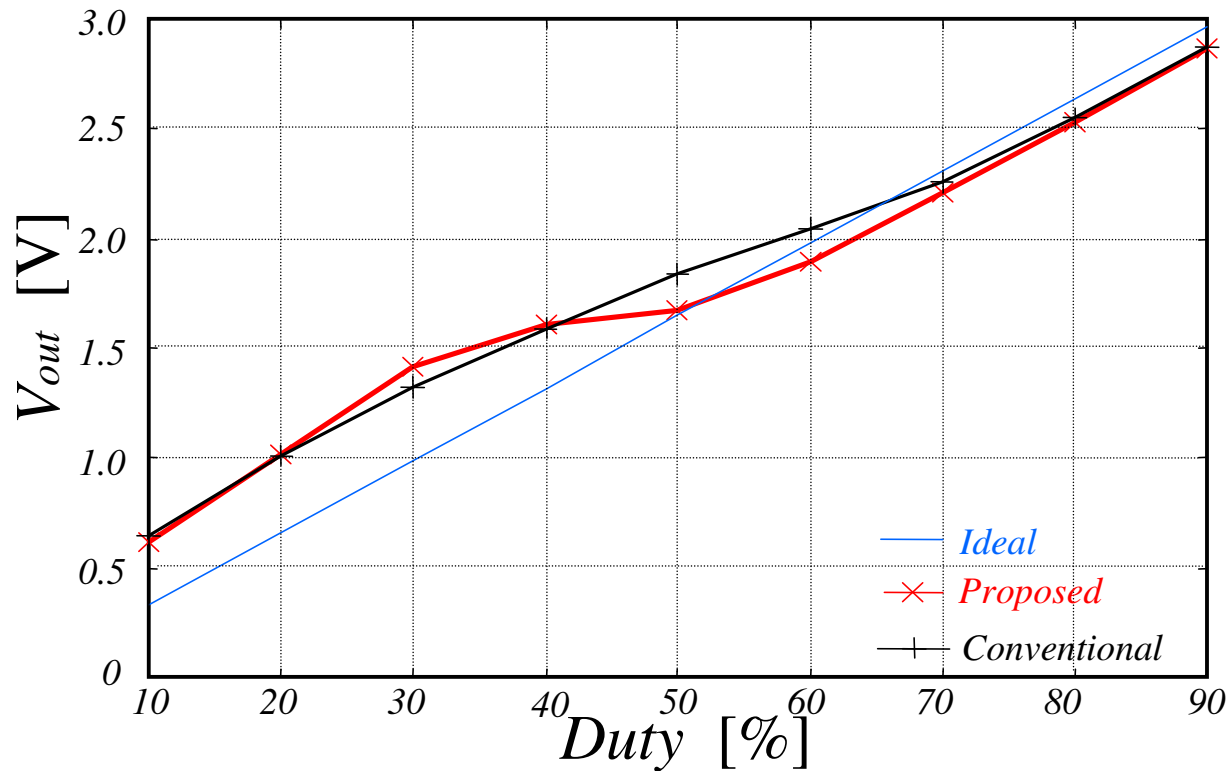


Output power spectrum with PRM clock (Proposed)

Maximum peak reduction by 12.3dBm



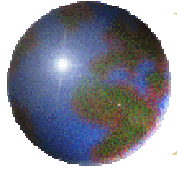
Clock Duty vs. Output Voltage



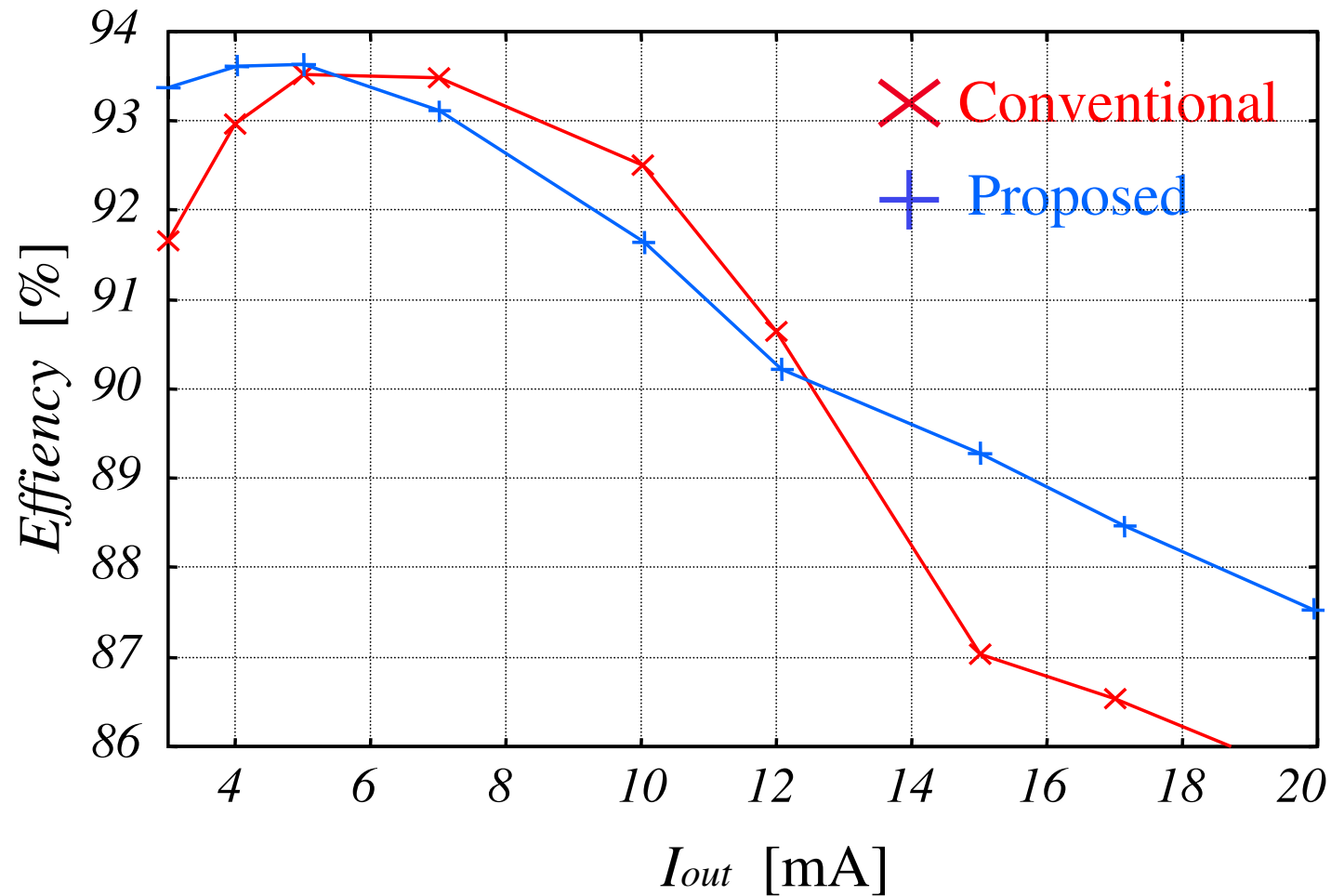
Match to the theoretical output voltage.



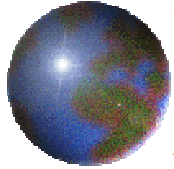
The proposed method does not affect the (average) output voltage.



Efficiency vs. Output Current

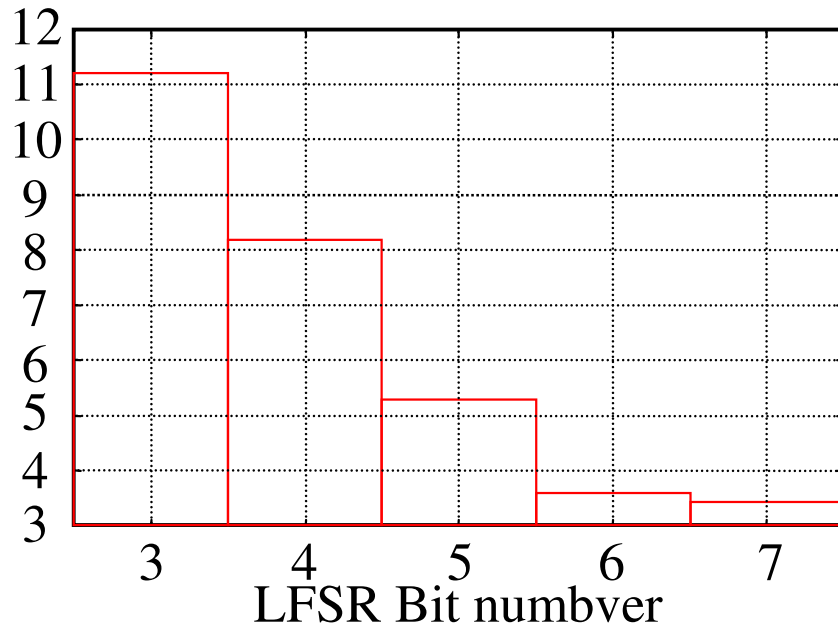


The proposed method does not affect efficiency.



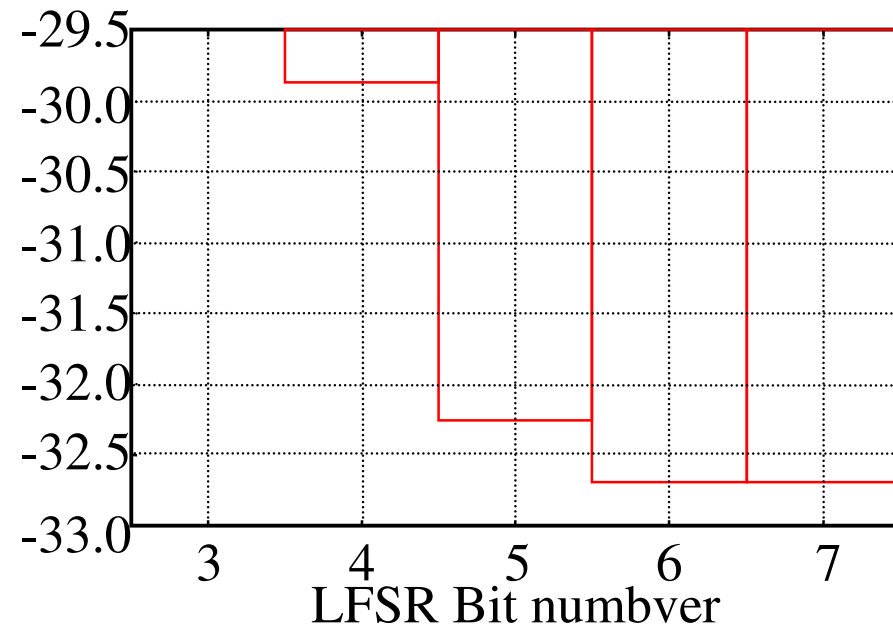
Peak Noise Power Spectrum vs. the Number of M-Sequencer Bits

Maximum Noise Power [dBm]



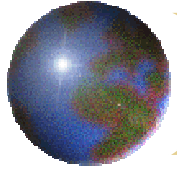
**Peak Noise Power Spectrum
of Driving Clock**

Maximum Noise Power [dBm]



**Peak Noise Power Spectrum
of Switching Regulator Output**

5-bit and 6-bit are reasonable trade-off.



Summary

- Proposal of Noise Power Spectrum Spread Technique
 - Addition of simple digital circuitry can realize EMI reduction.
 - Low cost, Low power
 - Robust against temperature variation, aging
 - No need for modification of the other parts.
 - Applicable also for voltage-boosting converter.

● Implementation with FPGA

● Confirmation of its effectiveness by measurements

Reduction by

Max. Peak	12.3dBm
Fundamental	5.7dBm
2nd-harmonics	15.6dBm
3rd-harmonics	12.8dBm