Dynamics of Dickson Charge Pump Circuit

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Abstract – This paper presents dynamics of Dickson charge pump circuits for high voltage generation. Several formulas regarding their output voltage, energy and efficiency in the transient state and the steady state are derived.

Keywords: Charge Pump, High Voltage Generator, Power Supply Circuit, State-Space Approach

I. Introduction

Charge pump circuits generate higher output voltages than the regular supply voltage [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11], and they have been used in non-volatile memories - such as EEPROM and flash memories - for their programming and erase operations through their floating gates. They are also used for liquid crystal display (LCD) systems and low-supply-voltage switched-capacitor systems that require high voltages to drive analog devices. Recently we have developed charge pump circuits for relatively large output current (several mA) for CCD driver [2, 3, 4]. Most of MOS charge pump circuits are based on Dickson [1], and Fig.1 shows a four-stage Dickson charge pump circuit. The drain-gate connected NMOS's (MD1 - MD5) are used as diodes there, so that the charges can be pushed only in one direction. CLK and $\overline{CLK}$ are two out-of-phase pumping clocks, whose amplitude is usually the supply voltage V_{dd}, and C_1 - C_4 are coupling capacitors with the same capacitance of C. The two clocks push the charge (and hence the node voltage) upward through the MOSFETs. When CLK goes from high to low and $\overline{CLK}$ from low to high, the voltage at node 1 is settled to $V_1 + \Delta V$, and the voltage at node 2 is to V_2, where V_1 and V_2 are defined as the steady-state lower voltage at nodes 1 and 2 respectively. Both MD1 and MD3 are reverse biased, and the charges are pushed from node 1 to node 2 through MD2 and the final voltage difference between nodes 1 and 2 is the threshold voltage of MD2.

In this paper we describe the dynamics of Dickson charge pump circuits systematically. For transient analysis, we assume that the circuit is ideal, and for steady state analysis, circuit nonidealities such as voltage drop across each switch, parasitic capacitance at each node and output current are incorporated. The derived formulas would be useful for design and analysis of charge pump circuits.

II. Basic Study of Power Electronics

Before discussing the dynamics of charge pump circuits, we would like to call for the reader's attention to the following two examples to understand the energy dissipation in a circuit which consists of capacitors and switches:

Example 1: Let us consider to charge a capacitor C in a RC circuit in Fig.2 where the voltage across the capacitor is zero at time $t = 0$. Its differential equation is given by

$$RC\frac{d}{dt}V_{out}(t) + V_{out}(t) = V_{dd}, \quad V_{out}(0) = 0,$$

and $V_{out}(t)$ is obtained as follows:

$$V_{out}(t) = V_{dd}(1 - \exp(-\frac{t}{RC})).$$

The energy E_{Supply} supplied from V_{dd} for $t = 0$ to ∞ is given by

$$E_{Supply} = CV_{dd}^2$$

because the charge CV_{dd} flows from V_{dd}. The energy stored in C at the steady state ($t = \infty$) is given by

$$E_C = \frac{1}{2}CV_{dd}^2.$$

Also the energy E_R dissipated through R from $t = 0$ to ∞ is obtained by

$$E_R = \frac{1}{R}\int_0^\infty (V_{dd} - V_{out}(t))^2 = \frac{1}{2}CV_{dd}^2.$$

Then we have the following relationships:

$$E_{Supply} = E_C + E_R, \quad E_C = E_R. \tag{1}$$

One half of the energy supplied from V_{dd} is stored in C and the other half is dissipated through R.

Example 2: Let us consider a circuit in Fig.3 which consists of a capacitors C_1, C_2 and a switch. When the switch is off and the voltages across C_1, C_2 are V_1, V_2 respectively, the charges Q_1, Q_2 and the energies E_1, E_2 stored in C_1, C_2 are given by

$$Q_1 = C_1V_1, \qquad Q_2 = C_2V_2,$$

$$E_1 = \frac{1}{2}C_1V_1^2, \qquad E_2 = \frac{1}{2}C_2V_2^2.$$

Then the total energy E is given by

$$E = E_1 + E_2 = \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2. \tag{2}$$

Next let the switch turn on, and the voltages across C_1 and C_2 becomes the same (V_M) at the steady state. Then we obtain the followings:

$$Q_1' = C_1V_M, \qquad Q_2' = C_2V_M \tag{3}$$

Since the charges are conserved between the states in Fig.3 (a) and Fig.3 (b), we have the following relationships:

$$Q_1 + Q_2 = Q_1' + Q_2'. \tag{4}$$

Then it follows from eqs.(3) and (4) that

$$C_1V_1 + C_2V_2 = C_1V_M + C_2V_M$$

and

$$V_M = \frac{C_1V_1 + C_2V_2}{C_1 + C_2}.$$

Hence the energies E_1', E_2' stored in C_1, C_2 in Fig.3 (b) are given by

$$E_1' = \frac{1}{2}C_1V_M^2 = \frac{C_1(C_1V_1 + C_2V_2)^2}{2(C_1 + C_2)^2},$$

$$E_2' = \frac{1}{2}C_2V_M^2 = \frac{C_2(C_1V_1 + C_2V_2)^2}{2(C_1 + C_2)^2}.$$

Thus the total energy E' in Fig.3 (b) yields to

$$E' = E_1' + E_2' = \frac{(C_1V_1 + C_2V_2)^2}{2(C_1 + C_2)}. \tag{5}$$

It follows from eqs.(2),(5) that the energy difference ΔE between the states in Figs.3 (a) and (b) is given by

$$\Delta E := E - E' = \frac{C_1C_2(V_1 - V_2)^2}{2(C_1 + C_2)} \tag{6}$$

Note that when $V_1 \neq V_2$, then $\Delta E > 0$ and the energy ΔE was dissipated through the switch. On the other hand, when $V_1 = V_2$, ΔE is equal to zero and this is called Zero-Volt Switching (ZVS).

III. Transient Analysis of Dickson Charge Pump Circuit

This section derives a formula for the node voltage in the transient state of an ideal three-stage charge pump circuit and also shows that one half of the energy E_{Supply} supplied from V_{dd} and clock drivers for $t = 0$ to ∞ are stored in the capacitors C at $t = \infty$ and the other half is dissipated through the switches from $t = 0$ to ∞.

Proposition 1: In an ideal three-stage charge pump circuit in Fig.4, the output voltage node $V_o(n)$ and the internal node voltage $V_1(n)$ at n-th clock cycle are given by

$$V_o(n) = \frac{1}{2}(\lambda_1^n + \lambda_2^n)V_o(0) + \frac{1}{\sqrt{2}}(\lambda_1^n - \lambda_2^n)V_1(0) + [-(2 + \frac{3}{\sqrt{2}})\lambda_1^n - (-2 + \frac{3}{\sqrt{2}})\lambda_2^n + 4]V_{dd}, \tag{7}$$

$$V_1(n) = \frac{1}{\sqrt{2}}(\lambda_1^n - \lambda_2^n)V_o(0) + \frac{1}{2}(\lambda_1^n + \lambda_2^n)V_1(0) + [-(2 + \frac{3}{\sqrt{2}})\lambda_1^n - (2 - \frac{3}{\sqrt{2}})\lambda_2^n + 3]V_{dd}, \tag{8}$$

where

$$\lambda_1 = \frac{2 + \sqrt{2}}{4}, \quad \lambda_2 = \frac{2 - \sqrt{2}}{4}.$$

Proof : See Appendix 1.

Remark (i) Since $|\lambda_1| < 1$ and $|\lambda_2| < 1$,

$$\text{as } n \to \infty, \quad \lambda_1^n \to 0, \quad \lambda_2^n \to 0,$$
$$V_o(n) \to 4V_{dd}, \quad V_1(n) \to 3V_{dd}.$$

(ii) The proof of Proposition 1 in Appendix 1 uses so-called a state-space approach. With this approach we can derive output node and internal node voltages at n-th cycle in an N-stage charge pump circuit for any positive integer N.

Proposition 2: When the charges in all the capacitors are zero at $t = 0$ in Fig.4, we have the following:

$$E_{Supply} = E_C + E_R, \quad E_C = E_R. \tag{9}$$

Here E_{Supply} is the energy supplied from V_{dd} and clock drivers for $t = 0$ to ∞, E_C is the energy stored in all the capacitors C at the steady state ($t = \infty$) and E_R is the dissipated power through the switches for $t = 0$ to ∞.

Proof : See Appendix 2.

Remark Propositin 2 is a general case of Example 1.

IV. Steady State Analysis of Dickson Charge Pump Circuit

Next we will consider the charge pump circuit at the steady state which includes circuit nonidealities.

4.1 Effects of Voltage Drop Across Switch

Let us consider the case that the switch is realized with a diode or a diode-connected MOSFET and it has some voltage drop V_d when it is ON (Fig.5).

Proposition 3: (i) For 3-stage charge pump circuit, the output voltage at the steady state is given by

$$V_o(\infty) = 4(V_{dd} - V_d). \tag{10}$$

(ii) The energy dissipation $P_{loss}(\infty)$ during one clock cycle T in the circuit at the steady state is given by

$$P_{loss}(\infty) = 0.$$

Proof See Appendix 3.

4.2 Effects of Parasitic Capacitance

Let us consider the case that each node has parasitic capacitance C_p (Fig.6).

Proposition 4: (i) For a 3-stage charge pump circuit, the output voltage at the steady state is given by

$$V_o(\infty) = (4 - \frac{3C_p}{C + C_p})V_{dd}. \tag{11}$$

(ii) The energy dissipation $P_{loss}(\infty)$ during one clock cycle T in the circuit at the steady state is given by

$$P_{loss}(\infty) = \frac{3CC_p}{C + C_p}V_{dd}^2. \tag{12}$$

Remark Example 2 helps us understand intuitively why the parasitic capacitance causes the energy loss given by eq.(12).

4.3 Effects of Output Current

Let us consider the case that the output node provides load current I_{out} (Fig.7).

Proposition 5: (i) For a 3-stage charge pump circuit, the output voltage at the steady state is given by

$$V_o(\infty) = (4 - \frac{7TI_{out}}{C})V_{dd}. \tag{13}$$

(ii) The energy dissipation $P_{loss}(\infty)$ during one clock cycle T in the circuit at the steady state is given by

$$P_{loss}(\infty) = 8TI_{out}V_{dd}. \tag{14}$$

Remark Examples 1 and 2 help us understand intuitively why the parasitic capacitance causes the energy loss given by eq.(14).

Proposition 6 : Efficiency η for a 3-stage charge pump circuit at the steady state is given by

$$\eta = \frac{\text{Output Power from } V_o}{\text{Supplied Power from } V_{dd} \text{ and Clock Drivers}}$$

$$= 1 - \frac{3}{2}\frac{TI_{out}}{CV_{dd}}. \tag{15}$$

4.4 Effects of Switch Voltage Drop, Parasitic Capacitance and Output Current Altogether

Let us consider the case that the charge pump circuit has the switch voltage drop V_d, parasitic capacitances C_p and output load current I_{out} (Fig.8).

Proposition 7: For a 3-stage charge pump circuit, the output voltage at the steady state is given by

$$V_o(\infty) = (1 + 3\frac{C}{C + C_p})V_{dd} - 4V_d - \frac{7TI_{out}}{C}. \tag{16}$$

Proof See Appendix 7.

Proposition 8 : Efficiency η for an N-stage charge pump circuit at the steady state is given by

$$\eta = 1 - \frac{NCC_pV_{dd}^2 + 2(N+1)(C+C_p)V_dTI_{out} + 4NT^2I_{out}^2}{NCC_pV_{dd}^2 + 2(N+1)CV_{dd}TI_{out} + 2C_pV_{dd}TI_{out}}. \tag{17}$$

Proof See Appendix 6.

Note that Eq.(17) yields to the following:

$$\eta = 1 - \frac{N\alpha + 2(N+1)(1+\alpha)\beta x + 4Nx^2}{N\alpha + 2\gamma x} \tag{18}$$

where x, α, β and γ are dimensionless, and defined by

$$x := \frac{TI_{out}}{CV_{dd}}, \quad \alpha := \frac{Cp}{C}, \quad \beta := \frac{V_d}{V_{dd}}, \quad \gamma := N + 1 + \alpha.$$

Proposition 9 : Effeciency η given by eq.(18) has a peak value when x has the following value:

$$x = \frac{-N\alpha + \sqrt{N^2\alpha^2 + [(1-\beta)\gamma - N\alpha\beta]\gamma\alpha}}{2\gamma}. \tag{19}$$

Proof By calculating $\partial\eta/\partial x = 0$ and $x > 0$, we obtain eq.(19).

We conclude this paper by remarking that Proposition 9 can theoretically explain our measurement result that the efficiency of our charge pump circuit [3] has a peak for a certain value of the output current I_{out} and also for a certain value of the clock period T when the other conditions are fixed.

We would like to thank K. Wilkinson for valuable discussions.

References

[1] J. F. Dickson, "On-Chip High-Voltage Generation in NMOS Integrated Circuits Using an Improved Voltage Multiplier Technique," *IEEE J. of Solid-State Circuits,* vol.11, pp.374-378, June 1976.

[2] H. San, H. Kobayashi, T. Myono, T. Iijima and N. Kuroiwa, "Highly-Efficient Low-Voltage-Operation Charge Pump Circuits Using Bootstrapped Gate Transfer Switches", *IEEJ*, vol.120-C, No.10, pp.1339-1345 (Oct. 2000).

[3] T. Myono, S. Kawai, A. Uemoto, T. Iizima, and H. Kobayashi, "Highly Efficient Charge-Pump Circuits with Large Output Current Load for Mobile Equipment Applications," *IEICE Trans. Electron*, vol.E84-C, no.10, pp.1602-1611 (Oct. 2001).

[4] T. Myono, T. Iijima, A. Uemoto, S. Kawai and H. Kobayashi, "High-efficiency charge-pump circuits by 0.5Vdd pumping up method", *Proc. of the 13th Workshop on Circuits and Systems in Karuizawa,* pp.479-484 (April 2000).

[5] J. T. Wu and K. L. Chang, "MOS Charge Pumps for Low-Voltage Operation," *IEEE J. of Solid-State Circuits,* vol.33, no.4, pp.592-597 (April 1998).

[6] H. Lin, K.-H. Chang and S.-C. Wong, "Novel High Positive Pumping Circuits for Low Power Supply," *Proc. of ISCAS99*, pp.1238-1241 (May 1999).

[7] K.-W. Min and S.-H. Kim, "A High-Voltage Generator Using Charge Pump Circuit for Low Voltage Flash Memories," *IEICE Trans. Electron,* vol.E82-C, no.5, pp.781-784 (May 1999).

[8] T. Tanzawa and S. Atsumi, "Optimization of Word-Line Booster Circuit for Low-Voltage Flash Memories," *IEEE J. of Solid-State Circuits*, vol. 34, no.8 pp. 1091-1098, (Aug. 1999).

[9] J. S. Witters, G. Groesenken, and H. E. Maes, "Analysis and Modeling of On-Chip High-Voltage Generator Circuit for Use in EEPROM Circuits," *IEEE J. of Solid-State Circuits*, vol.24, no.5 pp. 1372-1380, (Oct. 1989).

[10] A. Umezawa, S. Atsumi, M. Kuriyama, H. Banba, K. Imamiya, K. Naruke, S. Yamada, E. Obi, M. Oshikiri, T. Suzuki, and S. Tanaka, "A 5-V-Only Operation 0.6- μ m Flash EEPROM with Row Decoder Scheme in Triple-Well Structure", *IEEE J. of Solid-State Circuits,* vol. 27, no.11, pp. 1540-1546 (Nov. 1992).

[11] C. Lauterbach, W. Weber and D. Romer, "Charge Sharing Concept and New Clocking Scheme for Power Efficiency and Electromagnetic Emission Improvement of Boosted Charge Pumps," *IEEE J. of Solid-State Circuits*, vol.35, no.5, pp. 719-723 (May 2000).

Appendix 1 (Proof of Proposition 1)

Using the charge conservation law, we have the following state equation in Fig.4:

$$\mathbf{v}(n+1) = A\mathbf{v}(n) + \mathbf{b}V_{dd}$$

where

$$\mathbf{v}(n) := \begin{bmatrix} V_1(n) \\ V_o(n) \end{bmatrix}$$

$$A := \begin{bmatrix} \frac{1}{4} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix}, \qquad \mathbf{b} := \begin{bmatrix} \frac{1}{2} \\ \frac{1}{2} \end{bmatrix}$$

Then

$$\mathbf{v}(n) = A^n\mathbf{v}(0) + \sum_{k=0}^{n-1} A^k\mathbf{b}V_{dd}$$

and eqs.(7), (8) are obtained.

Appendix 2 (Proof of Proposition 2)

Using the charge conservation law for each cycle, the energy loss $E_{loss}(n)$ and the energy stored in all capacitors $E_c(n)$ at n-th cycle are given by

$$E_{loss}(n) = \frac{C}{16}[10V_1(n)^2 + 5V_o(n)^2 + 74V_{dd}^2$$

$$-8V_1(n)V_o(n) - 16V_o(n)V_{dd} - 28V_1(n)V_{dd}],$$

and

$$E_c(n) = \frac{C}{2}[2V_1(n)^2 + 2V_{dd}(n)^2 - 2V_1(n)V_{dd} + V_o)n)^2].$$

Then considering an initial condition E_{loss0},

$$E_R := \sum_{n=0}^{\infty} E_{loss}(n) + E_{loss0} = 15CV_{dd}^2,$$

$$E_c := \lim_{n\to\infty} E_c(n) = 15CV_{dd}^2,$$

and eq.(9) is obtained.

Appendix 3 (Proof of Proposition 3)

We have the following state equation in Fig.5.

$$\mathbf{v}(n+1) = A\mathbf{v}(n) + B\mathbf{v_m}$$

where

$$B := \begin{bmatrix} \frac{1}{2} & 0 \\ \frac{1}{2} & -1 \end{bmatrix}, \quad \mathbf{v_m} := \begin{bmatrix} V_{dd} \\ V_d \end{bmatrix}.$$

When $n \to \infty$, we have

$$\mathbf{v}(\infty) = A\mathbf{v}(\infty) + B\mathbf{v_m}$$

and eq.(10) is obtained.

Appendix 4 (Proof of Proposition 4)

We have the following state equation in Fig.6:

$$\mathbf{v}(n+1) = A\mathbf{v}(n) + \mathbf{c}V_{dd}$$

$$\mathbf{c} := \begin{bmatrix} \frac{C}{2(C+C_p)} \\ \frac{2C+C_p}{4(C+C_p)} \end{bmatrix}.$$

When $n \to \infty$, we have

$$\mathbf{v}(\infty) = A\mathbf{v}(\infty) + \mathbf{c}V_{dd}$$

and eq.(11) is obtained.

Appendix 5 (Proof of Proposition 5)

We have the following state equation in Fig.7.

$$\begin{bmatrix} V_1(n+1) \\ V_o(n+1) \end{bmatrix} =$$

$$\begin{bmatrix} \frac{1}{4} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_1(n) \\ V_o(n) \end{bmatrix} + \begin{bmatrix} \frac{1}{2} & -\frac{3}{2} \\ \frac{1}{2} & -\frac{1}{4} \end{bmatrix} \begin{bmatrix} V_{dd} \\ \frac{TI_{out}}{C} \end{bmatrix}$$

When $n \to \infty$, we have

$$\begin{bmatrix} V_1(\infty) \\ V_o(\infty) \end{bmatrix} = \begin{bmatrix} \frac{1}{4} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_1(\infty) \\ V_o(\infty) \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{1}{2} & -\frac{3}{2} \\ \frac{1}{2} & -\frac{1}{4} \end{bmatrix} \begin{bmatrix} V_{dd} \\ \frac{TI_{out}}{C} \end{bmatrix}$$

and eq.(13) is obtained.

Appendix 6 (Proof of Propositions 6 and 8)

Consider the steady state in Fig.8. Then the energy E_{load} supplied from the output node during one clock cycle T is given by

$$E_{load} = [2V_{dd} - 8V_d + 6\frac{C}{C+C_p}V_{dd} - 12\frac{TI_{out}}{C+C_p}]TI_{out}.$$

Also the energy $E_s(\infty)$ supplied from V_{dd} and clock drivers during one clock cycle T is given by

$$E_s(\infty) = 3CV_{dd}^2 - 3\frac{C^2}{C+C_p}V_{dd}^2$$

$$+6\frac{CV_{dd}TI_{out}}{C+C_p} + 2V_{dd}TI_{out}.$$

Then

$$\eta = \frac{E_{load}}{E_s(\infty)}$$

and eqs.(15),(17) have been obtained.

Appendix 7 (Proof of Proposition 7)

In Fig.8 we have the following state equations:

$$V_1'(n) = \frac{1}{2}V_1(n) + \frac{1}{2}V_{dd} - V_d,$$

$$V_o'(n) = \frac{1}{2}V_1(n) + \frac{1}{2}V_o(n) - V_d + \frac{CV_{dd} - TI_{out}}{2(C+C_p)},$$

$$V_1(n+1) = \frac{1}{2}V_1'(n) + \frac{1}{2}V_o' + V_d,$$

$$V_o(n+1) = \frac{1}{2}V_o'(n) - \frac{TI_{out}}{C+C_p}.$$

Then eq.(16) has been obtained.

Figure Captions

Fig.1: A four-stage Dickson charge pump.

Fig.2: A RC circuit.

Fig.3: Two capacitors and switch. (a) In case that switch is OFF, the voltages across C_1 and C_2 are V_1 and V_2 respectively.
(a) In case that switch is ON. The charges in C_1 and C_2 moves so that the voltages across C_1 and C_2 becomes the same (V_M) and some energy is dissipated through the switch.

Fig.4: An ideal three-stage Dickson charge pump circuit.

Fig.5: A non-ideal three-stage Dickson charge pump circuit where voltage drop V_d across each switch is considered.

Fig.6: A non-ideal three-stage Dickson charge pump circuit where parasitic capacitance C_p at each node is considered.

Fig.7: A non-ideal three-stage Dickson charge pump circuit where output load current I_{out} is considered.

Fig.8: A non-ideal three-stage Dickson charge pump circuit where voltage drop V_d across each switch, parasitic capacitance C_p at each node, and output load current I_{out} are considered.

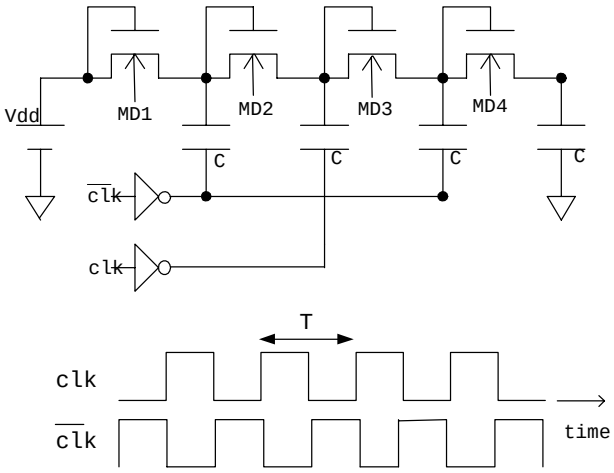

Fig.1

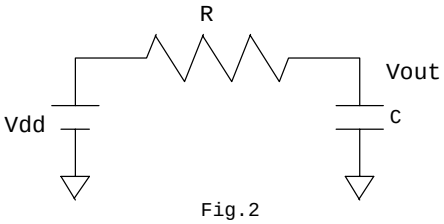

Fig.2

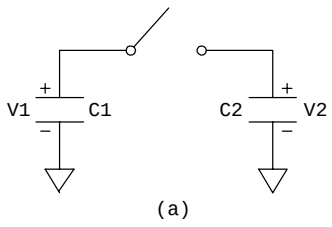

Fig.3

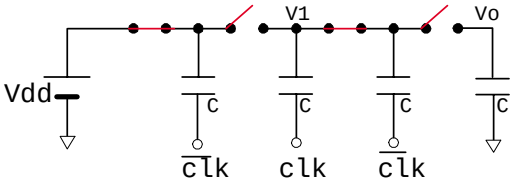

Fig.4

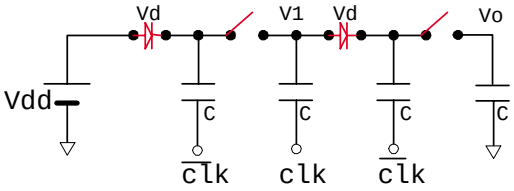

Fig.5

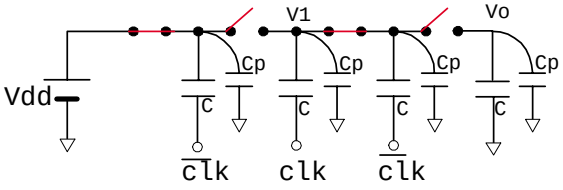

Fig.6

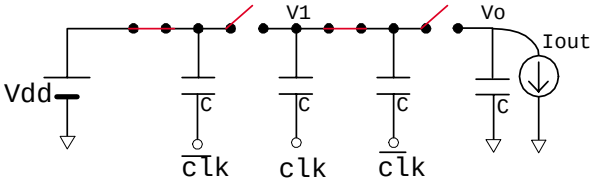

Fig.7

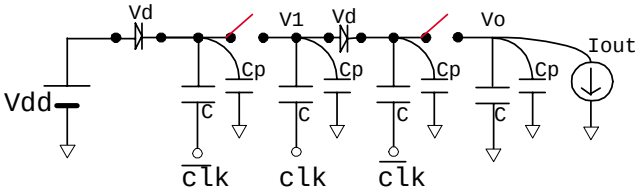

Fig.8