発表内容

- ナノCMOS時代のアナログ回路　私論
- マルチバンドパスΔΣAD変調器
- 連続時間バンドパスΔΣAD変調器
  - RF サンプリングを目指して
- **複素バンドパスΔΣAD変調器**
- まとめ

A Multibit Complex Bandpass ΔΣ AD Modulator with I,Q Dynamic Matching and DWA Algorithm

H. San, Y. Jingu, H. Wada, H. Hagiwara, A. Hayakawa, J. Kudoh[2], K. Yahagi[2], T. Matsuura[2], H. Nakane[2], H. Kobayashi, M. Hotta[3], T. Tsukada[2], K.Mashiko[4], A.Wada[5]

1) Gunma University
2) Renesas Technology Corp.
3) Musashi Institute of Technology
4) STARC
5) Sanyo Electric Co., Ltd.

Outline

- Motivation
- Complex Bandpass Delta-Sigma AD Modulator
- Proposed Architecture
  - I, Q Dynamic Matching
  - Complex DWA Algorithm
- Measured Results
- Conclusion

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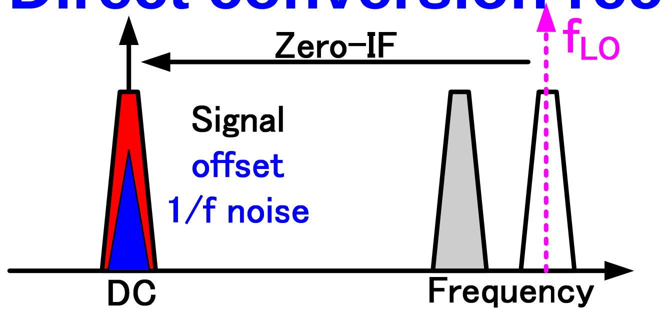
Motivation

Low power ADC in low-IF receiver targeted for bluetooth, wireless LAN.

Complex bandpass delta-sigma AD modulator

Receiver Architecture Comparison

Direct conversion receiver



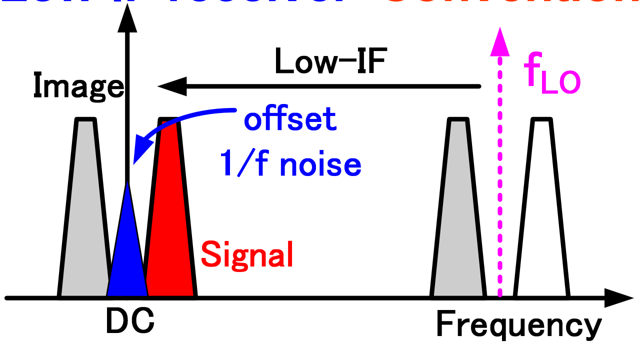
RF → Baseband

Zero-IF

⇒ No mage

Problem of DC offset, flicker noise

Low-IF receiver Conventional



RF → Low-IF

No problem of DC offset, flicker noise.

Image as well as signal are AD converted ⇒ Power is wasted

Quadrature-IF

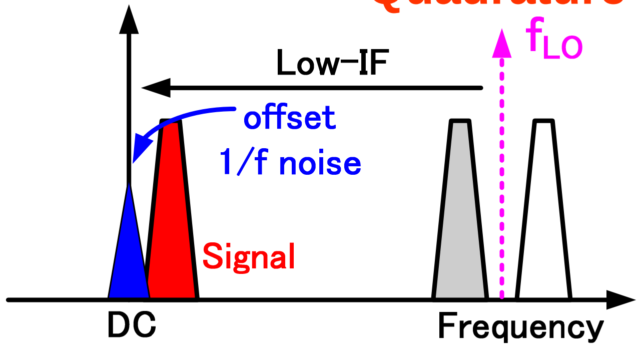


Image is not AD converted.

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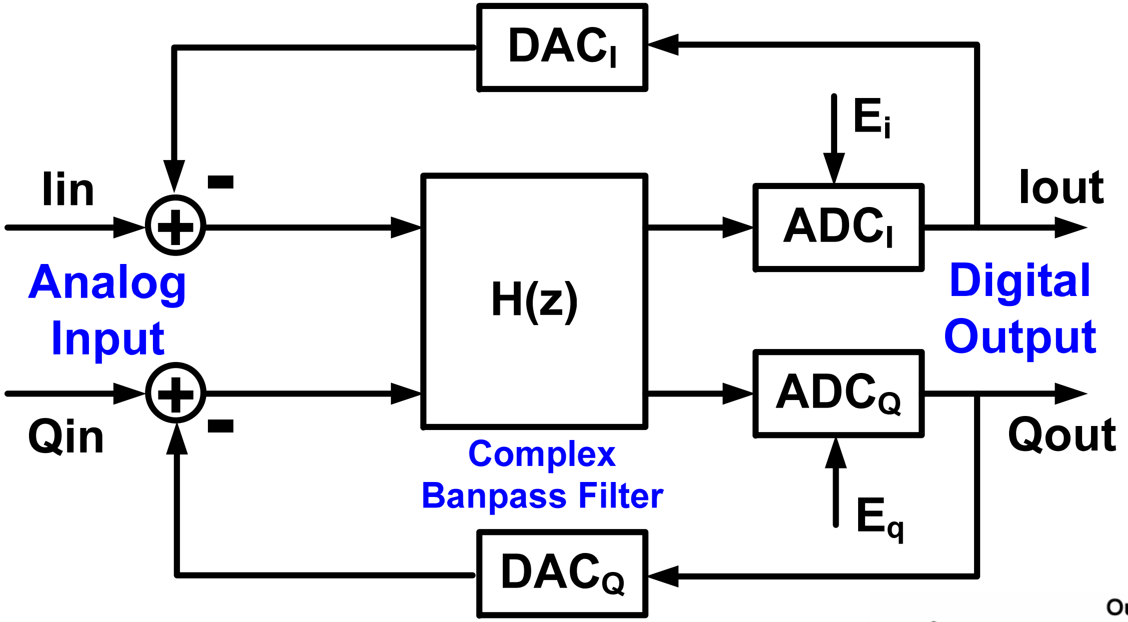
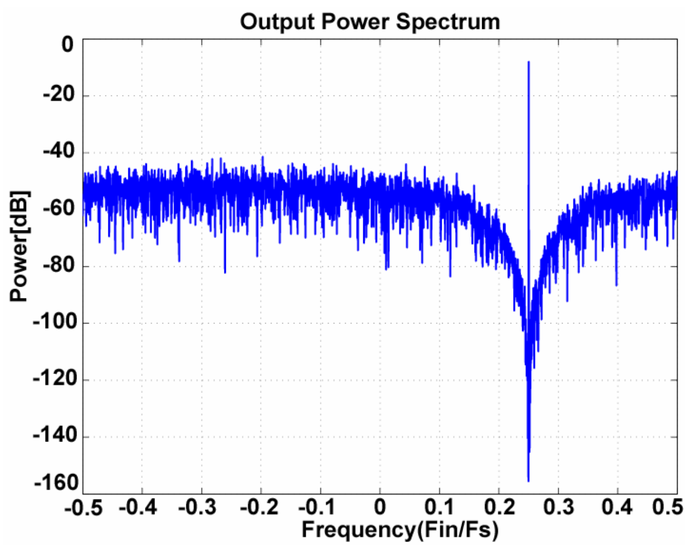
Complex Bandpass Delta-Sigma Modulator



$$I_{out} + jQ_{out} = \frac{H}{1+H}(I_{in} + jQ_{in}) + \frac{1}{1+H}(E_i + jE_q)$$



Complex bandpass noise-shaping

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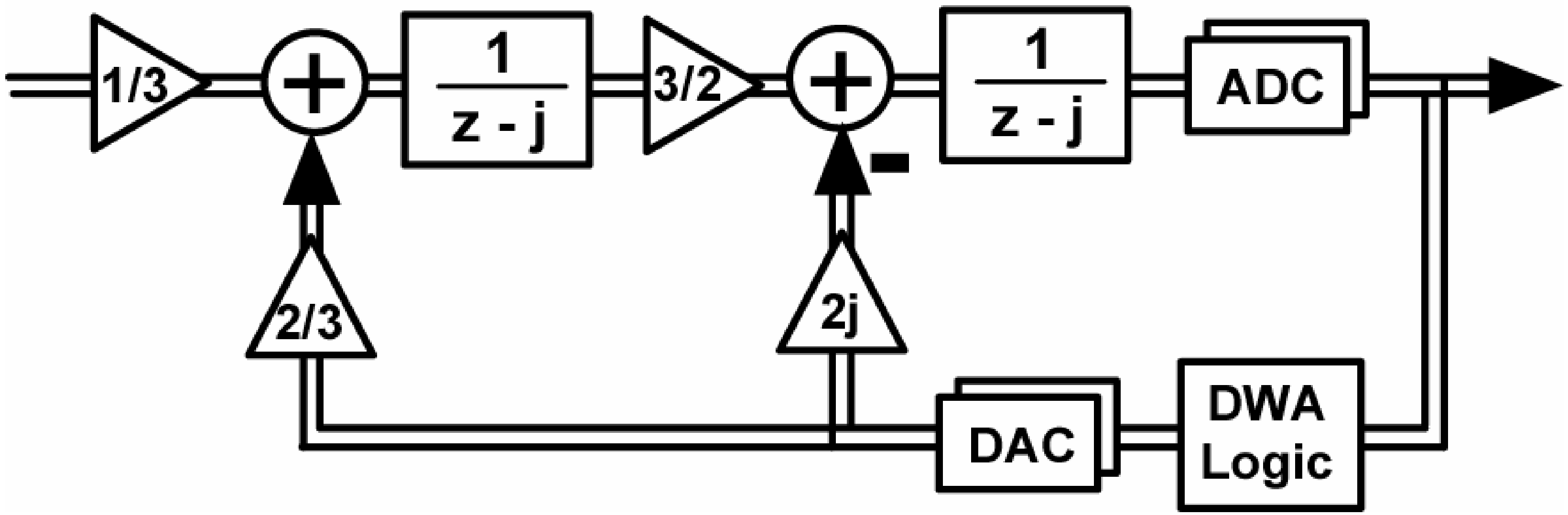
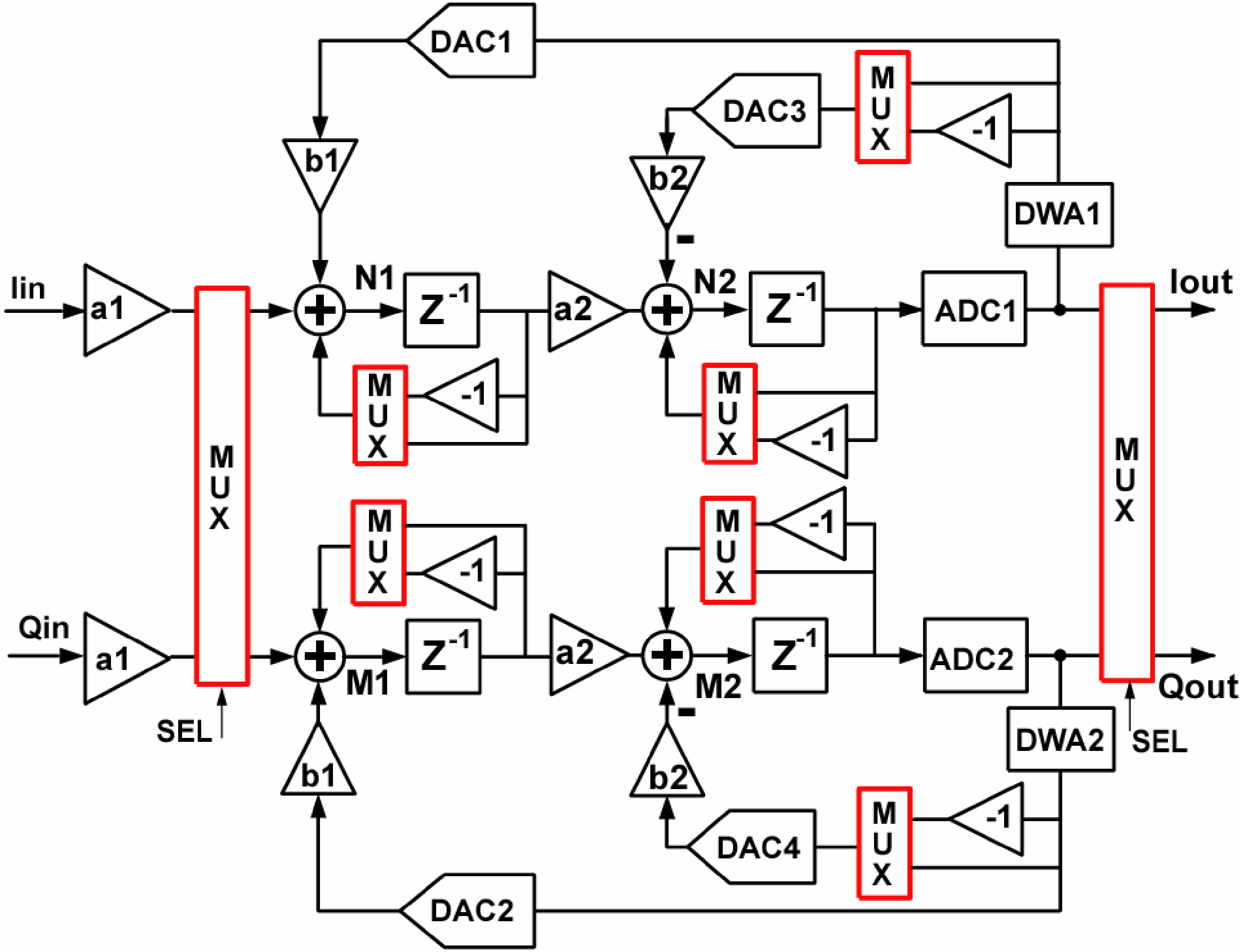
Proposed Architecture

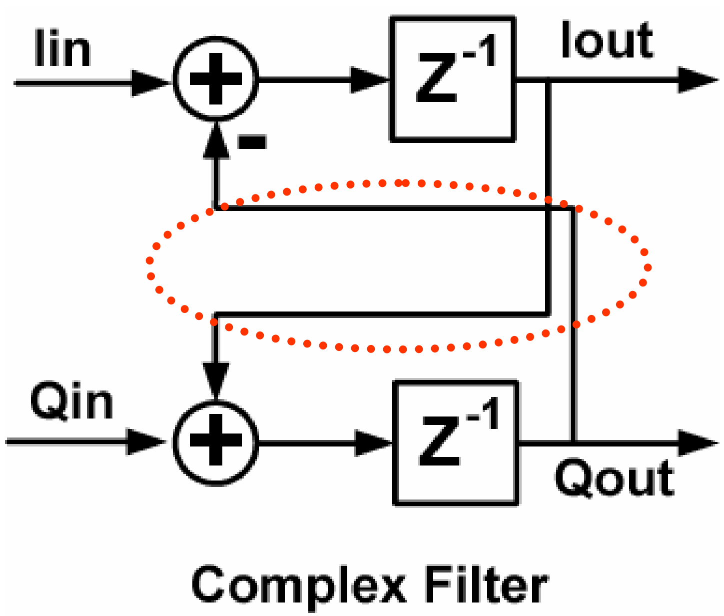


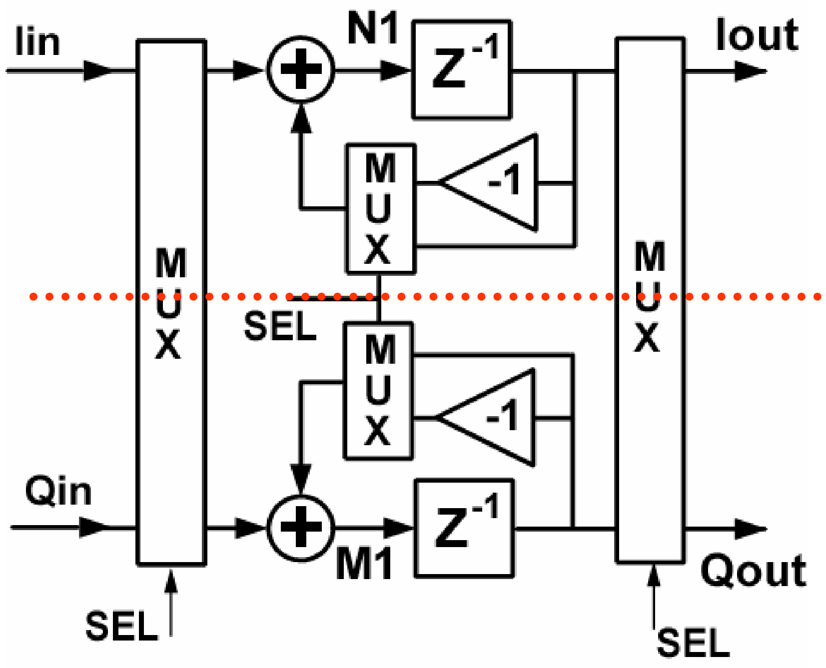
- New complex bandpass filter
- Multi-bit ADCs/DACs
- Complex DWA algorithm

Proposed Structure



I,Q Dynamic Matching of Complex Filter



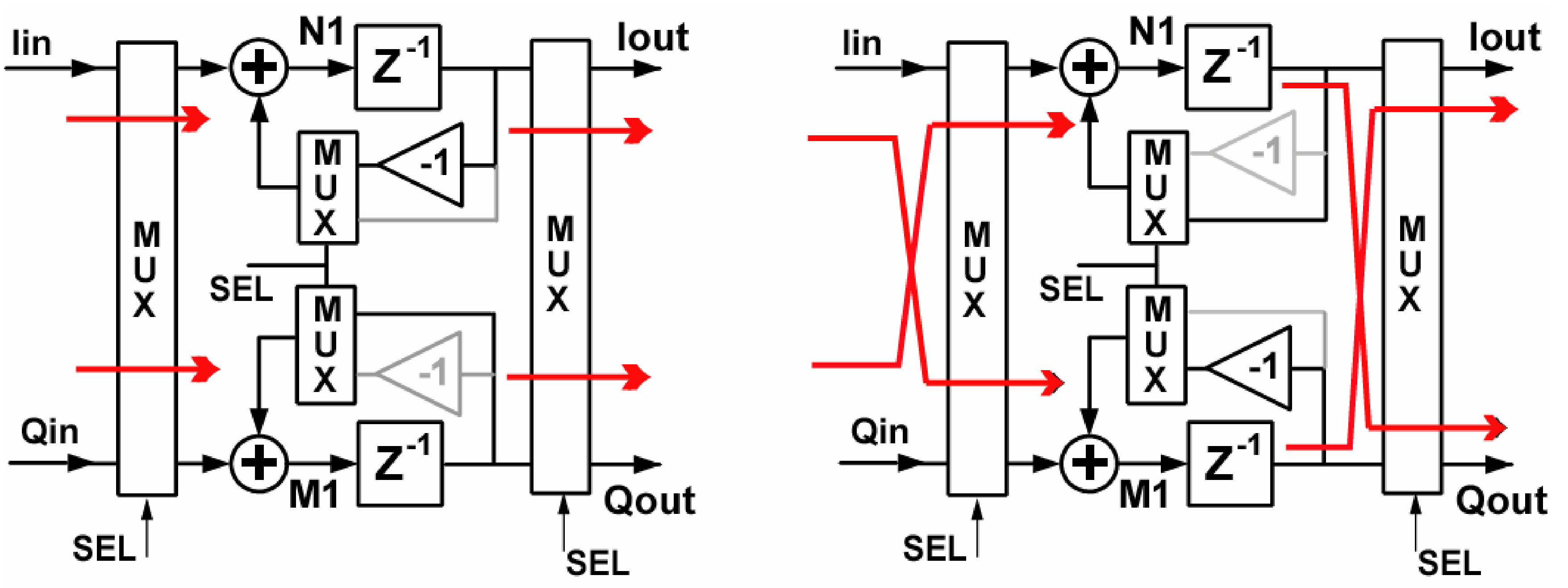


Conventional complex filter
I &Q crossing paths

Proposed complex filter
Upper, lower separated paths

- **I,Q mismatch reduction.**
- **Layout simplification.**

Operation of Proposed Complex Filter



$$Iout(n) = Iin(n-1) - Qout(n-1)$$

$$Qout(n) = Qin(n-1) + Iout(n-1)$$

Complex BPDSM with Low-power

- 2nd order ---- low power
- 9-level ADCs/DACs
    - Stability improvement
    - Low quantization error
    - Power reduction of amplifiers

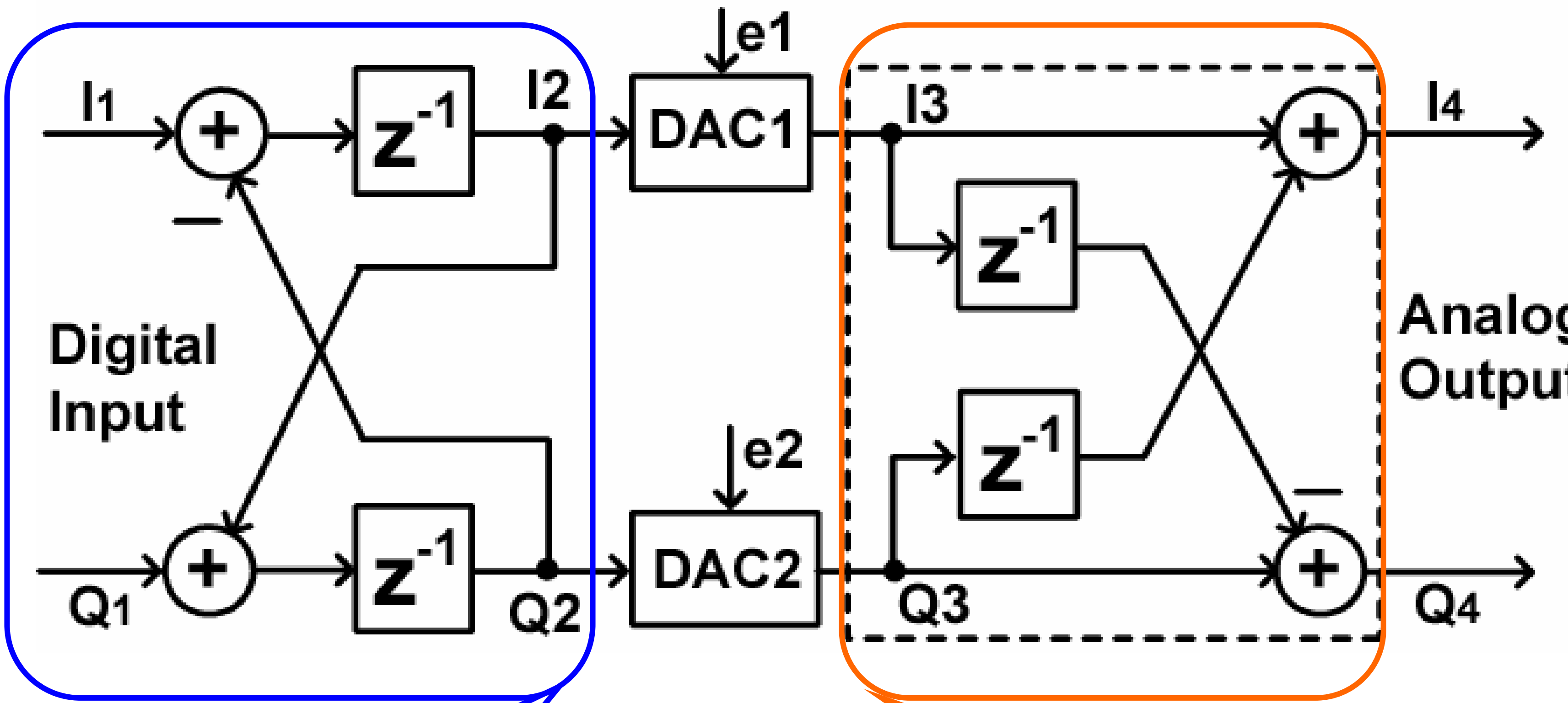
I,Q mismatch

- Solved by dynamic matching

Nonlinearities of multibit DAC

- Solved by complex DWA

Complex DWA (1)



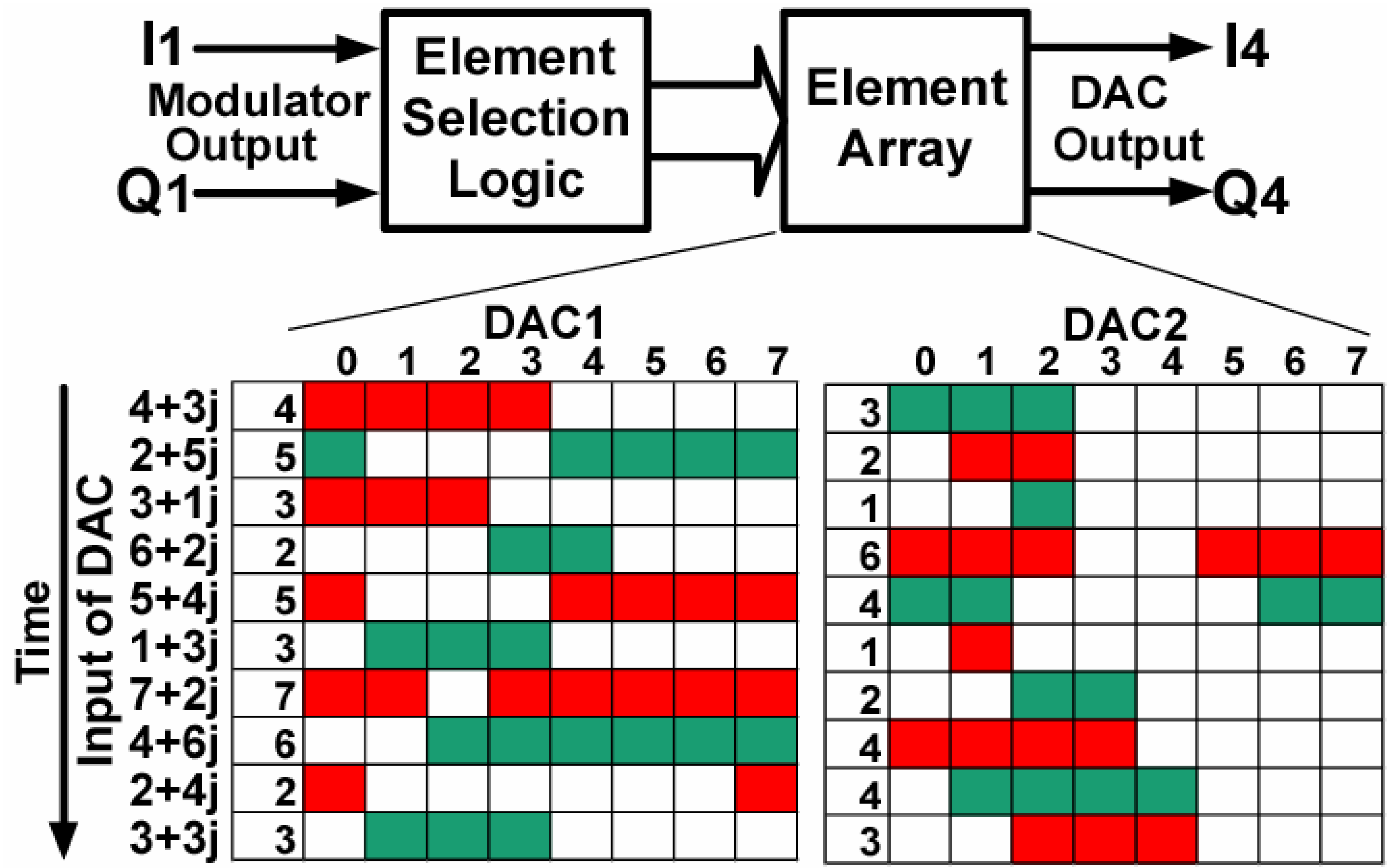
$$H_1(z) = \frac{1}{z - j}$$

$$H_2(z) = z - j$$

Digital bandpass filter

Analog band elimination filter

Complex DWA (2)



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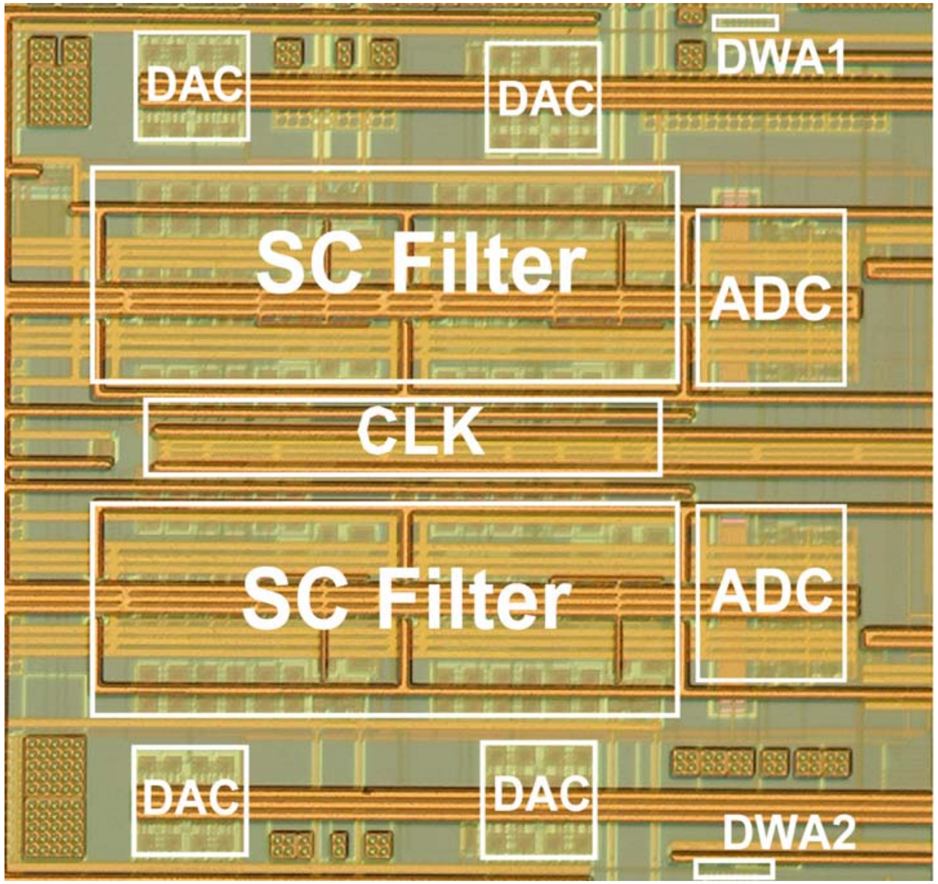
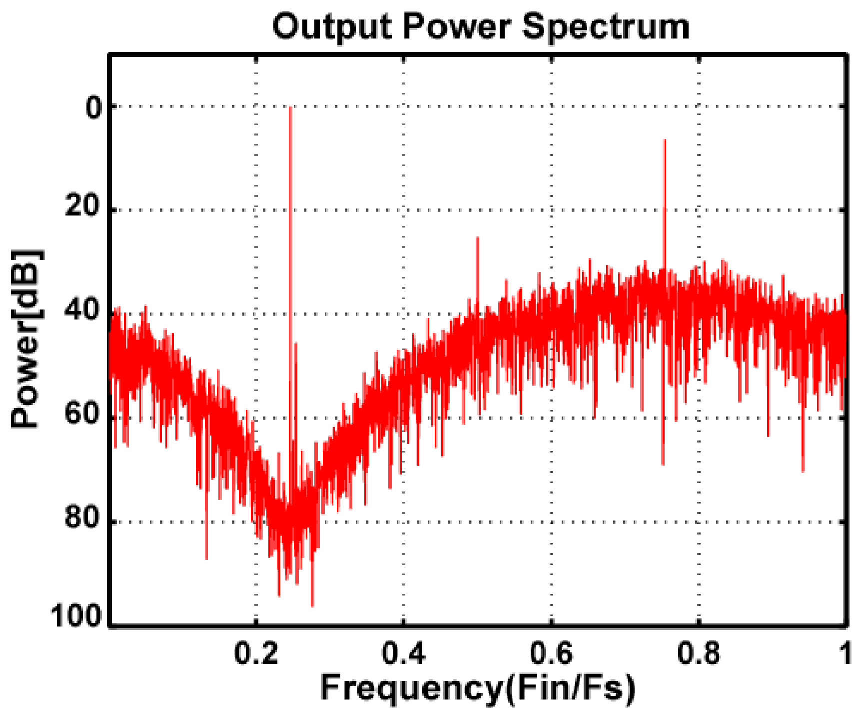
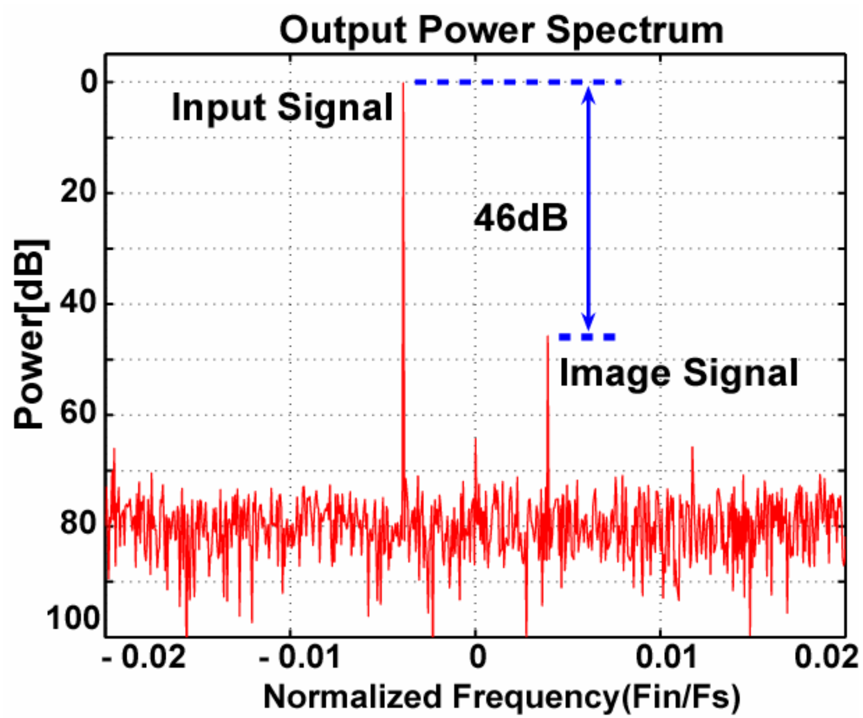
Chip Implementation



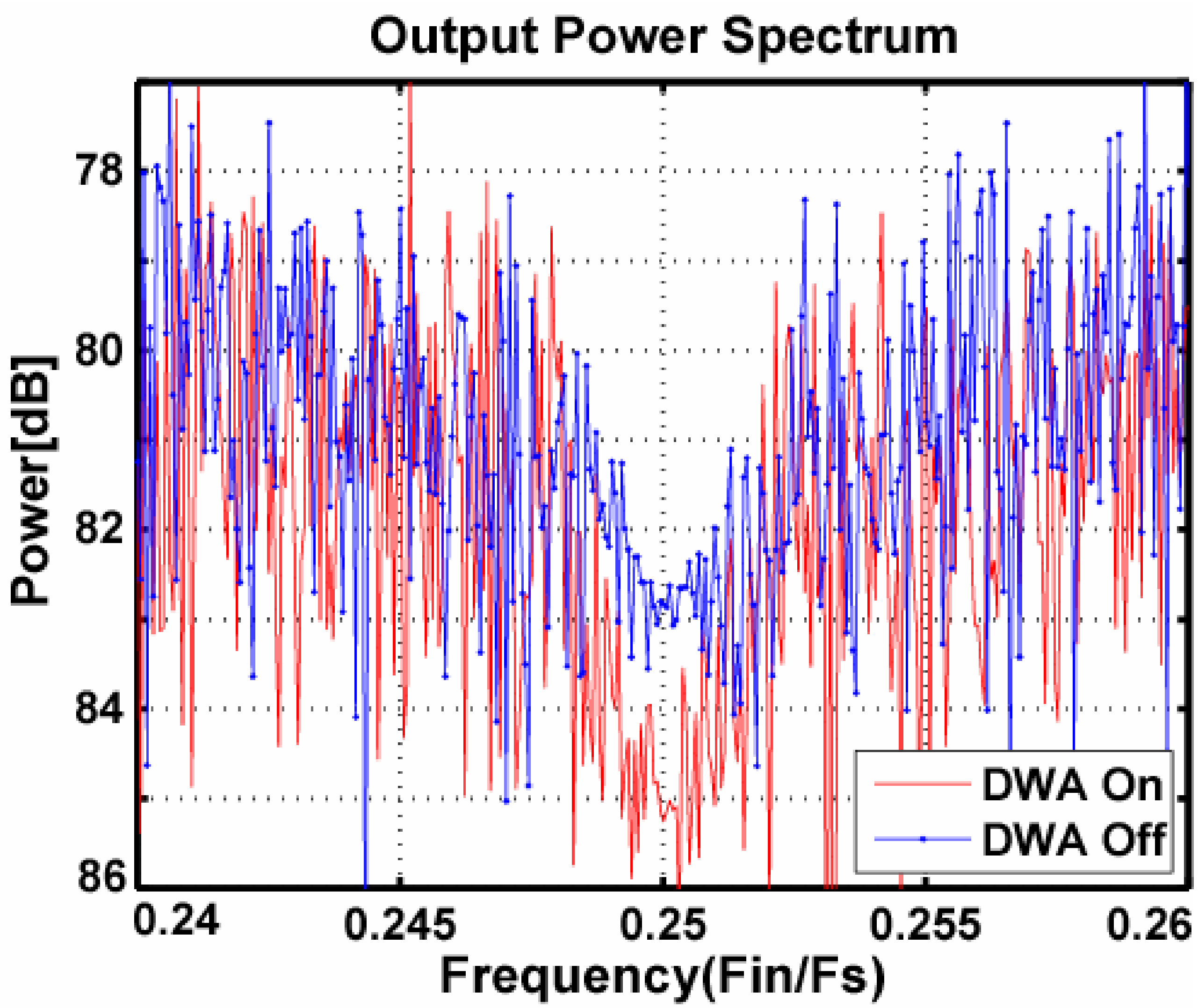
- **1P6M 0.18μm CMOS Process**
- **Core size 1.4 *1.3mm^2.**

Measured Output Power Spectrum





Effect of Complex DWA



Summary of Modulator Performance

Technology	0.18-μm CMOS 1P6M
Supply voltage	2.8V
Sampling Frequency	20MHz
SNDR	64.5dB @ BW=78kHz
Power consumption	28.4mw
Active area	1.4mm*1.3mm

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Conclusion

- A 2nd-order multi-bit complex bandpass delta-sigma modulator

⇩

Low power

- Complex filter with dynamic matching
  - I,Q mismatch reduction
  - Layout simplification
- Complex DWA
  - Suppression of multibit DACs nonlinearities
- Chip measurements demonstrated these

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まとめ

- ナノCMOS時代のアナログ回路
  デジタルリッチな構成
  高速サンプリングを利用
- 両方を利用するΔΣAD変換器は
  より高性能（広帯域、高精度）化して
  応用が広がる。
- ３つの例を紹介
  1） マルチバンドパスΔΣAD変調器
  2） RFサンプリング用
  連続時間バンドパスΔΣAD変調器
  3） 複素バンドパスΔΣAD変調器