Conversion Rate Improvement of SAR ADC with Digital Error Correction

Shintaro SHIMOKURA†, Masao HOTTA†, Nan ZHAO,
Yosuke TAKAHASHI, Haruo KOBAYASHI
† Department of Information Network Eng., Musashi Institute of Technology
Electronic Engineering Department, Faculty of Engineering, Gunma University
e-mail: mhotta@sc.musashi-tech.ac.jp

Abstract - This paper describes a conversion rate of a high-performance successive approximation (SAR) ADC using three comparators operating in parallel, instead of just one as in conventional ADCs. This comparator redundancy enables faster operation, higher reliability and comparator-error correction. We describe advantages on the novel SAR ADC with reliability-enhancement and error-correction algorithm. Higher-conversion-rate and higher-accuracy SAR ADCs with lower power and smaller area have possibility to replace pipelined ADCs as video use. Embedded microcontrollers containing this SAR ADC would be also suitable for automotive applications.

Keywords: Successive Approximation ADC, Error Correction, Automotive Electronics, Microcontroller

1. Introduction

Recently much attention is being paid to automotive electronics [1, 2]. Successive Approximation Register (SAR) ADCs in embedded microcontrollers are widely used in such applications where reliability, speed, accuracy, and low power consumption are required. On the other hand, SAR ADCs are expected to replace pipelined ADCs which require high performance Opamps as sample-hold amplifiers in finer technology era[3, 4]. Because SAR ADC does not require high performance amplifiers, it is convenient to achieve high performance ADC in beyond 90 nm technology, in which performances of MOS transistors such as output resistance are degraded.

The novel architecture of SAR ADC with three comparators and its error correction algorithm have been proposed to achieve a high-reliability ADC suited to automotive applications with higher resolution (12-14bit), higher speed (20MS/s) [5]. In previous paper, we described how this comparator redundancy can enhance reliability and enables correction of comparator errors.

This paper describes some specific problems to implement the SAR ADC and the improvement of conversion rate of the SAR ADC compared with conventional binary search SAR ADCs using only one comparator.

2. Proposed SAR ADC Architecture [5]

We proposed using an SAR ADC that has three comparators (or, equivalently, a 2-bit flash ADC) and a DAC with three reference voltage outputs (Fig.1). A conventional SAR ADC has only one comparator, so a wrong comparator decision in any comparison step can not be corrected in a later comparison step. However, our proposed ADC has three redundant comparators; this has the following advantages:

(1) Reliability: Even if the comparator decision is wrong in any comparison step, comparator redundancy allows this error to be corrected in later comparison steps; this is ideal for (e.g. automotive) applications that require high reliability.

(2) High Speed: When such error correction is used, we do not have to wait for DAC comparator-reference voltage outputs to settle completely, hence the converter can operate at a higher frequency.

2.1 Digital Error Correction Algorithm

This section describes our digital error correction algorithm (Fig.2) in the proposed SAR ADC (Fig.1).

In the first clock period, three reference voltages and comparators divide the full scale to 4 ranges. In the first step, the range in which the analog input can be found,

and the first and second MSBs are decided. By narrowing the range step by step, we can find the nearest DAC output voltage to the input signal. The input digital data of the DAC which generate the output nearest to the analog input signal becomes the output of the SAR ADC.

The three reference voltages comparison algorithm is shown bellow.

(1) In First Step :
Three reference voltages are set as follows:
Vh(1) = (3/4)Vref
Vm(1) = (1/2)Vref
Vl(1) = (1/4)Vref
Vr(n) = Vh(n) - Vm(n) (= Vm(n) - Vl(n))
Vr(n+1) = Vr(n)/2
Vr(1) = (1/4)Vref
Where, Vh, Vm and Vl means higher level, middle level and lower level reference voltage, respectively. And, Vr is meant as the deference voltage between Vh and Vm, or Vm and Vl.

In the n-th step, Vm is set according to the outputs of three comparators as shown in Table 1.

Table 1: Reference Voltage Vm at (n+1)-th step

C3	C2	C1	Dout(n)	
1	1	1	11	Vm(n+1) = Vh(n) + Vr(n+1)
0	1	1	10	Vm(n+1) = Vm(n) + Vr(n+1)
0	0	1	01	Vm(n+1) = Vm(n) - Vr(n+1)
0	0	0	00	Vm(n+1) = Vl(n) - Vr(n+1)

And, Vh and Vl are set according to next equations.
Vh(n+1) = Vm(n+1) + Vr(n+1)
Vl(n+1) = Vm(n+1) - Vr(n+1)

In Fig. 2, the comparison algorithm is explained by more visible representation. In the first step, three reference voltages, Vh(1), Vm(1) and Vl(1), are generated by the internal DAC. First 2 MSBs are decided by detecting the range in which the analog input signal is. According to the output of the comparators, next three reference voltages are set. For example, when the analog input signal is in the range between Vm(1) and Vh(1), next reference voltages are set to cover this range, and 3rd MSB can be determined by finding the range which includes the analog input signal. Then, this three-reference-voltage setting and comparison method continues in this manner.

Next, the error correction algorithm is explained. In the first step, the error which is shown in broken line occurs and the comparators decide that the input signal is in the range between Vl(1) and Vm(1). Then, 1st and 2nd MSBs are decided as “01” and next reference voltages are set to cover the range between Vl(1) and Vm(1) as shown in Fig. 3. In the second step, the comparators detect that the analog input signal level is over the Vh(2). This fact means the 3 MSBs should be “100”, and the error correction is achieved by changing the 2 MSBs which was decided prior clock period. In the case of the error which the input signal is in the range between Vl(1) and Vm(1), the error correction is achieved in same manner.

3. Conversion rate of the SAR ADC

3.1 Considerations on the offset of comparators

Suppose that the proposed SAR ADC is 10-bit ADC. Although the ADC has large redundancy in upper bit decision steps, the accuracy of comparators becomes severe in the last step, that is , the errors of comparators must be less than +/- 1/2 LSB in 9th step and less than +/- 1 LSB in 8th step in case of 10-bit ADC as shown in Fig. 4. If error collection step is added as 10th step, the errors of comparators are relaxed to less than +/- 1/2 LSB and less than +/- 1 LSB in 9th step and 8th step respectively. These high accurate comparisons by three comparators are needed to correct the errors occurred at prior steps.

Idea for generation of reference voltages: Figure 5 shows an idea for generation of three reference voltages. The middle reference voltage, Vm is generated by the binary weighted DAC, and the deference voltage, Vr is generated by using the remainder of current source which is not used for generation of Vm. Moreover, three-level comparison is done by adding or subtracting Vr to Vm at the comparators as shown in Fig. 6. This implementation has less penalty for chip size and power consumption and the error of middle reference voltage,

Vm, generated by the DAC must be less than +/- 1/2 LSB to achieve ADC's accuracy. Because the higher reference voltage Vh and lower reference voltage are generated by the remainder of current sources of the DAC and adding or subtracting Vr to Vm at the comparators, these three reference voltages have accuracy of 10-bit (Generally N-bit for N-bit ADC). Therefore, the offset voltages of the three comparators must be less than +/- 1LSB to achieve error correction in case of adding error correction step followed by last step.

3.2 Considerations on the conversion rate

When proposed error correction is used, we do not need to wait for the DAC outputs as comparator-references to settle completely, hence a higher conversion rate can be achieved. In the case of N-bit conventional SAR ADC, a settling time of internal DAC into +/- 1/2LSB should be Nτln2, where τ is time constant of the DAC output which is supposed to settle exponentially. This means that the conversion time of the ADC becomes (2N x Nτln2) at least, because N steps are needed to convert for N-bit ADC, if the comparison is done in a half clock period. For example, in case of N=10bit, conversion time is (2N x 6.9τ), and in case of N=14bit, it becomes (2N x 9.4τ). On the other hand, when the proposed error correction algorithm is used, the maximum settling time of the DAC output for the three reference voltages must be considered.

At first, the settling time for largest voltage change, that is, change from 1/4 V_{FS} to 3/4 V_{FS} for lower voltage reference at 2nd step, Vl(2) is calculated by using following equation.

$$\left[\frac{3}{4}V_{FS} - \frac{1}{4}V_{FS}\left(1 - e^{-\frac{T}{\tau}}\right)\right]\left(1 - e^{-\frac{T_D}{\tau}}\right) \geq \left[\frac{3}{4}V_{FS} - \frac{1}{4}V_{FS}\left(1 - e^{-\frac{T}{\tau}}\right)\right] - \frac{1}{16}V_{FS} \quad (1)$$

where, T is clocking period and T_D is comparison time for input signal and reference voltage which is roughly equal to a half of clock period :

$T_D = T/2$

From Equation (1), we obtain

$$T_D \geq 2.08\tau$$

Secondly, the settling time to minimum deviation from settled value, that is, change from 7th step to 8th step for 10-bit ADC as shown in Fig. 8. In this case, the settling time is calculated by following equation.

$$(8LSB + a)\left(1 - e^{-\frac{T_D}{\tau}}\right) \geq (8LSB + a) - 1LSB \quad (2)$$

From this equation (2), we obtain

$$T_D \geq 2.1\tau$$

Therefore, the conversion time of proposed SAR ADC is estimated as (2N x 2.1τ) . This conversion time is roughly 3 times faster than that of conventional ADC for 10-bit, and 4.5 times faster for 14-bit.

4. Simulation results of conversion time

We have performed MATLAB simulations to confirm the effect of error correction algorithm we proposed and the improvement of the conversion rate of proposed SAR ADC. Figure 9 shows the process of conversion of the 10-bit SAR ADC with comparison time of 2.5τ, and we see that three reference levels are converged and correct converted digital data are obtained. In figure 10, the conversion process with comparison time of only 1.25τ is demonstrated. In this case, the converted digital data have error of 1 LSB. This means that the architecture and error correction algorithm we proposed is effective to suppress the large conversion error.

5. Conclusions

A high-performance SAR ADC architecture that achieves both high speed and high reliability by using triple (redundant) comparators and a new error correction algorithm is proposed. We discussed the conversion rate and the proposed 14-bit SAR ADC enables 4.5 times faster conversion rate than that of conventional SAR ADC.

Next we plan to implement this architecture and algorithm efficiently on an IC.

Acknowledgement

We would like to thank STARC (Semiconductor Technology Academic Research Center) which is supporting this research. Thanks are also due to T. Matsuura, A. Abe, M. Kondo, K. Mashiko, N. Takai and H. San for valuable discussions.

References

[1] H. Casier, P. Moern, K. Appeltans, "Technology Consideration for Automotive," Proc. of ESSCIRC, pp.37-41, Leuven, Belgium (Sept. 2004).

[2] ISSCC Short Course, Automotive Technology and Circuits, San Francisco (Feb. 2005).

[3] F. Kuttner, "A 1.2V 10b 20MS/S Non-Binary Successive Approximation ADC in 0.13µm CMOS," Tech. Digest of ISSCC (Feb. 2002).

[4] M. Hesener1, T. Eichler1, A. Hanneberg1, D. Herbison1, F. Kuttner2, H. Wenske1, "A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13µm CMOS," Tech. Digest of ISSCC, 13.6 (Feb 2007).

[5] M, Hotta, A. Hayakawa, N. Zhao, Y. Takahashi, H. Kobayashi, "SAR ADC Architecture with Digital Error Correction," Tech. Digest of Analog VLSI Workshop 2006, (Nov. 2006).

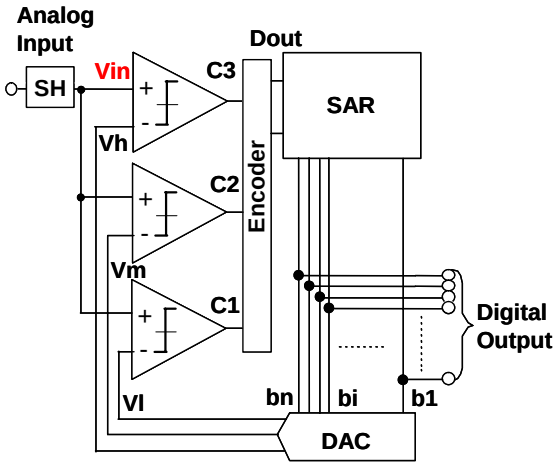

Fig.1: Proposed SAR ADC with three comparators.

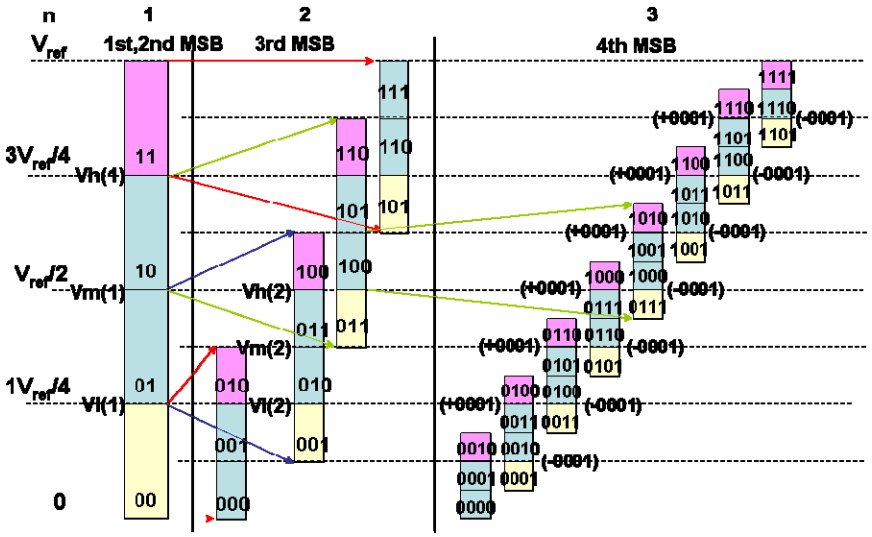

Fig.2: Three reference voltages comparison

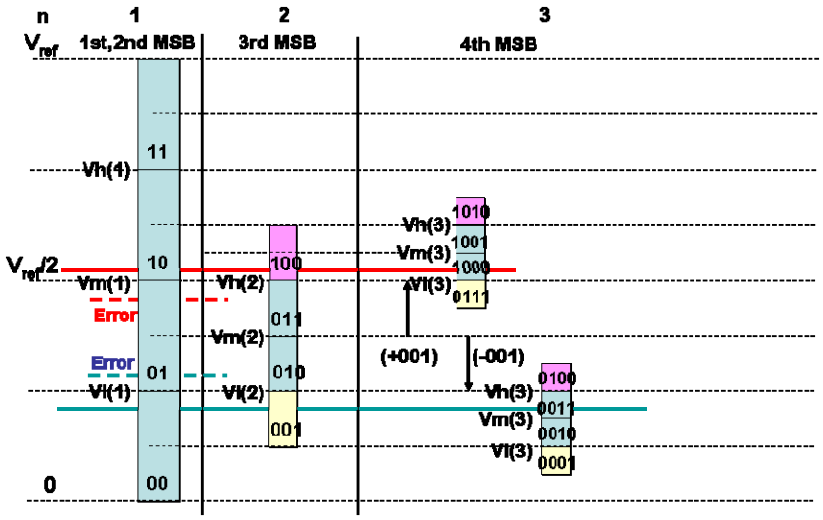

Fig.3:Error Correction Algorithm

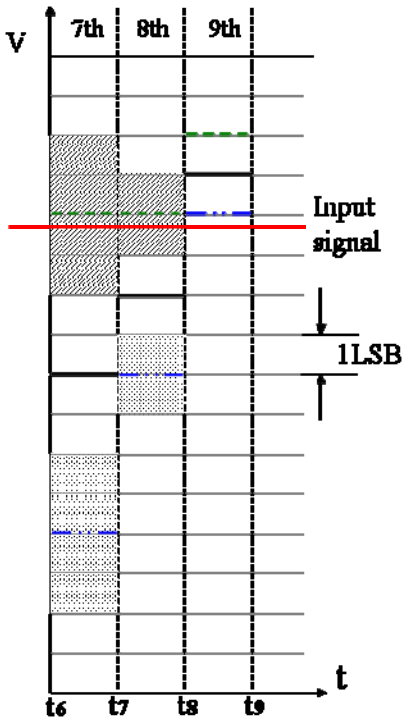

Fig.4: Redundancy of comparators

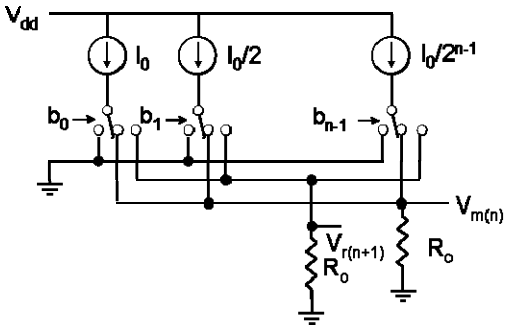

Fig.5: DAC configuration as a reference voltage generator

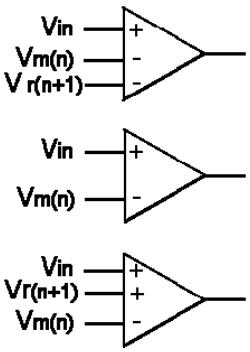

Fig.6: Comparators for three-level comparison

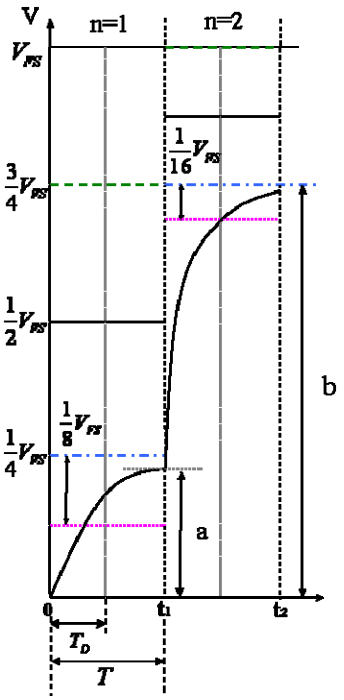

Fig.7: Settling time for largest voltage change in the second step

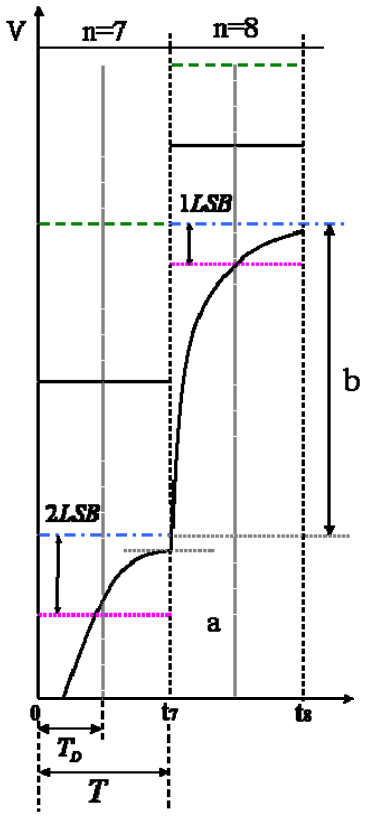

Fig.8: Settling time for largest voltage change in the last three steps

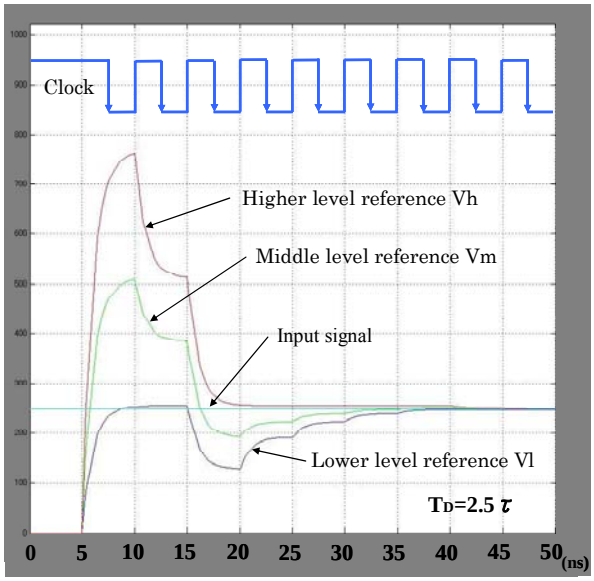

Fig.9: MATLAB simulation results of conversion process for the 10-bit SAR ADC with comparison time of 2.5τ

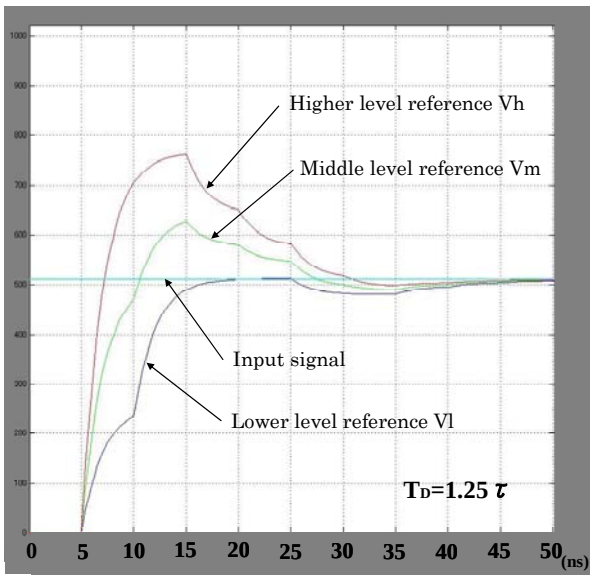

Fig.10: MATLAB simulation results of conversion process for the 10-bit SAR ADC with comparison time of 1.25τ