Noise-Coupled ΔΣAD Modulator with Shared OP-Amp

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Keywords: ΔΣAD Modulator, Switched-Capacitor, Noise-coupling, Noise-shaping enhancement

This paper proposes a new architecture of the noise-coupled ΔΣAD modulator with OP-Amp sharing technique.

ΔΣAD modulators realize high resolution by oversampling and noise-shaping techniques, which are suitable for low power and high resolution application with nano-meter CMOS technology. The performance of ΔΣAD modulators is limited by dynamic range of the input signal and non-idealities of circuit building blocks. In nano-meter CMOS technology, the device characteristics degradation (such as matching and drain resistance r_{ds}) and the low supply voltage evidently reduce the accuracy of analog circuits. Therefore, the performance of analog circuits is significantly degraded and non-idealities of circuit building blocks, especially non-linearities of amplifiers generate more harmonic distortion. Furthermore, since allowable signal swings are reduced due to lower supply voltage, the dynamic range will be decreased and the performance of the modulator would be degraded. In order to realize higher SQNDR (Signal to Quantization Noise and Distortion Ratio) for a ΔΣAD modulator, higher oversampling ratio (OSR) is needed which demands higher sampling rate, and/or a high-order filter inside a modulator (as well as a high-order digital filter following the ΔΣAD modulator) is required, which need more hardware. Either of above techniques for higher SQNDR will cause more power dissipation for the modulator.

Recently, the noise-coupled structure of the ΔΣAD modulator is proposed, by applying a quantization noise injection to the front-end of internal ADCs, so that the order of the modulator can be effectively raised. The noise-coupled ΔΣAD modulator enhances the order of noise-shaping efficiently by adding some passive capacitors and switches.

However, in this conventional noise-coupled ΔΣAD modulator with feedforward path, an analog adder is needed before the quantizer, and especially in a multibit modulator, an additional amplifier is necessary at the front-end of internal ADCs to realize the summation of feedforward signals and coupled quantization noise, which leads to extra chip area and power dissipation.

In this paper, we propose a novel architecture of the noise-coupled ΔΣAD modulator with OP-Amp sharing technique, which realizes the summation of feedforward signals and coupled quantization noise without an additional amplifier. By the techniques of quantization noise injection and amplifier-saving, the proposed modulator provides a higher-order NTF using a lower-order loop filter. The additional integrator circuit using an operational amplifier is not necessary, and the performance of the ΔΣAD modulator can be effectively raised without more power dissipation. The proposed architecture is functionally equivalent to the conventional noise-coupled modulator with smaller chip area and low power dissipation.

We have performed simulation with MATLAB and SPICE to verify the effectiveness of the proposed architecture and modulator circuits. The simulation results show that the proposed modulator can realize the noise-shaping enhancement effectually as the same as the conventional noise-coupled modulator with small overhead.

Paper

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This paper proposes an improved architecture of the noise-coupled ΔΣAD modulator with OP-Amp sharing technique. The noise-coupled ΔΣAD modulator enhances the order of noise-shaping efficiently by adding some passive capacitors and switches. However, in a conventional noise-coupled ΔΣAD modulator with feedforward path, an analog adder is needed before the quantizer, and especially in a multibit modulator, an additional amplifier is necessary to realize the summation of feedforward signals and coupled quantization noise, which leads to extra chip area and power dissipation. In this paper, we propose a novel architecture of the noise-coupled ΔΣAD modulator with OP-Amp sharing technique, which realizes the summation of feedforward signals and coupled quantization noise without an additional amplifier. The proposed architecture is functionally equivalent to the conventional noise-coupled modulator with smaller chip area and low power dissipation. We have performed simulation with MATLAB and SPICE to verify the effectiveness of the proposed architecture and modulator circuits. The simulation results show that the proposed modulator can realize the noise-shaping enhancement effectually as the same as the conventional noise-coupled modulator with small overhead.

Keywords: ΔΣAD Modulator, Switched-Capacitor, Noise-coupling, Noise-shaping enhancement

1. Introduction

ΔΣAD modulators realize high resolution by oversampling and noise-shaping techniques, which are suitable for low power and high resolution application with nanometer CMOS technology. The performance of ΔΣAD modulators is limited by dynamic range of the input signal and non-idealities of circuit building blocks. In nano-meter CMOS technology, the device characteristics degradation (such as matching and drain resistance r_{ds}) and the low supply voltage evidently reduce the accuracy of analog circuits. Therefore, the performance of analog circuits is significantly degraded and non-idealities of circuit building blocks, especially non-linearities of amplifiers generate more harmonic distortion. Furthermore, since allowable signal swings are reduced due to lower supply voltage, the dynamic range will be decreased and the performance of the modulator would be degraded. In order to realize higher SQNDR (Signal to Quantization Noise and Distortion Ratio) for a ΔΣAD modulator, higher oversampling ratio (OSR) is needed which demands higher sampling rate, and/or a high-order filter inside a modulator (as well as a high-order digital filter following the ΔΣAD modulator) is required, which need more hardware. Either of above techniques for higher SQNDR will cause more power dissipation for the modulator. Noise-coupled structure of the ΔΣAD modulator is proposed [1], by applying a quantization noise injection to the front-end of internal ADCs, so that the order of the modulator can be effectively raised. However, an additional amplifier is necessary to realize the noise-coupling at the front-end of internal ADCs, which leads to extra chip area and power dissipation.

In this paper, we propose a novel noise-coupled architecture of the ΔΣAD modulator with OP-Amp sharing technique. The order of the ΔΣAD modulator can be effectively raised, and it is functionally equivalent to the conventional noise-coupled one. However, in the proposed ΔΣAD modulator, the additional amplifier circuit is not necessary. Therefore, it can achieve higher SQNDR with small chip area and low power dissipation.

2. Noise-Coupled ΔΣAD Modulator

Figure 1 shows a full feedforward ΔΣAD modulator [2], and its input and output can be expressed as:

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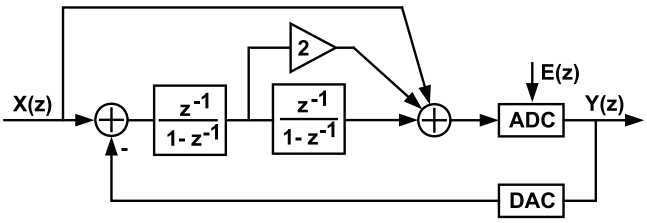

Fig. 1. Feedforward ΔΣAD modulator.

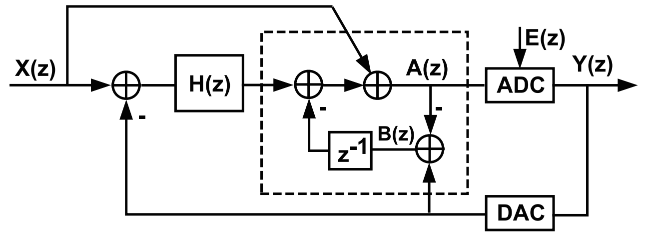

Fig. 2. Noise-coupled ΔΣAD modulator.

$$Y(z) = X(z) + (1 - z^{-1})^2 E(z). \quad \cdots\cdots\cdots\cdots\cdots (1)$$

Here X(z) is the input signal, Y(z) is the output signal and E(z) is the quantization noise of the modulator. Then the signal transfer function (STF) and noise transfer function (NTF) are given by

$$STF(z) = 1 \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (2)$$
$$NTF(z) = (1 - z^{-1})^2. \quad \cdots\cdots\cdots\cdots\cdots\cdots (3)$$

The NTF provides a second-order noise-shaping function for the quantization noise E(z).

Fig.2 shows a noise-coupled ΔΣAD modulator with the quantization noise injection technique [3]. It is a full feedforward ΔΣAD modulator with an additional noise injection structure of the quantization noise. Notice the noise injection structure surrounded by the dotted line, we see that:

$$A(z) = Y(z) - E(z) \cdots\cdots\cdots\cdots\cdots\cdots\cdots (4)$$
$$B(z) = Y(z) - A(z) = E(z) \quad \cdots\cdots\cdots\cdots\cdots\cdots (5)$$

which means that the quantization noise E(z) is obtained by subtracting the internal ADC's input from the DAC's output. After through a filter of z^{-1}, a delayed replica of the quantization noise E(z) is fed back to the input node of ADC again. This quantization noise injection technique is similar to the error-feedback structure [4] of the noise shaper in ΔΣDA modulator [5] [6]. While the noise transfer function of the ΔΣAD modulator without the additional noise injection structure is given by NTF(z), the transfer function of noise-coupled ΔΣAD modulator shown in Fig.2 can be written as follows:

$$Y(z) = X(z) + NTF'(z)E(z) \quad \cdots\cdots\cdots\cdots\cdots (6)$$
$$NTF'(z) = NTF(z)(1 - z^{-1}). \quad \cdots\cdots\cdots\cdots\cdots (7)$$

As shown in Eq.(7), we see that by providing an additional noise-coupled structure with the error-feedback topology, the $NTF'(z)$ of ΔΣAD modulator increments the NTF(z) by an extra $(1 - z^{-1})$ factor, the order of the modulator is increased by one, which is equivalent to obtaining more noise-shaping in low frequency signal band, and achieving higher SQNDR of the modulator.

In a noise-coupled ΔΣAD modulator, the injection method of the quantization noise to the modulator is similar to a second-stage cascade (or MASH) modulator, which provides a higher-order noise shaping using a lower-order loop filter. However, in a second-stage MASH structure, a higher SQNDR is achieved by accurate cancellation of the first-stage quantization noise. Any mismatch errors for analog implementation will change the transfer function, and cause the noise leakage in the MASH modulator. As contrast with MASH architecture, noise-coupled structure realizes higher-order noise shaping with injection of the quantization noise to the modulator again. Since only one quantizer is used in the noise-coupled modulator, there is no mismatch error of the noise leakage at all. Furthermore, while a multibit quantizer is used for the modulator, the quantization noise can be assumed under busy signal conditions, which reduces tones and harmonic spurs. Thus, the noise coupling method can raise the order of a noise transfer function, at the same time, and the stability condition of the original modulator is preserved in the multibit modulator [7].

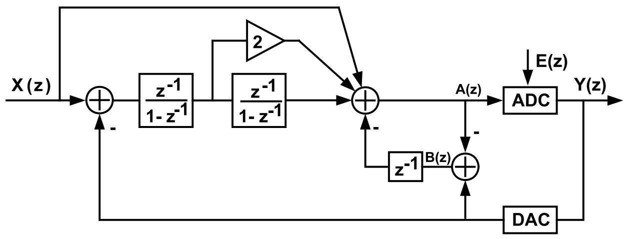

Fig. 3. ΔΣAD modulator with two integrators and noise-coupling structure.

Fig.3 shows a ΔΣAD modulator which consists of two discrete integrators and a noise-coupling structure. It is a ΔΣAD modulator shown in Fig.1 with an additional noise-coupling structure. The transfer function of the ΔΣAD with noise-coupled rejection shown in Fig.3 can be expressed as

$$\begin{aligned} Y(z) &= X(z) + (1 - z^{-1})^2(1 - z^{-1})E(z) \\ &= X(z) + (1 - z^{-1})^3 E(z). \quad \cdots\cdots\cdots\cdots\cdots (8) \end{aligned}$$

We see that the noise transfer function of the second-order ΔΣAD modulator without additional noise-coupling structure is the same as Eq.(3). Then, the noise transfer function of the ΔΣAD with noise-coupled rejection shown in Fig.3 can be written as

$$NTF'(z) = (1 - z^{-1})^3. \cdots\cdots\cdots\cdots\cdots\cdots (9)$$

We see from Eqs.(7) and (9) that, by providing this error-feedback topology, the $NTF'(z)$ of the noise-coupled ΔΣAD modulator increases an extra $(1 - z^{-1})$ factor, which has an extra zero at $z = 1$. Therefore, the NTF of the proposed modulator shows the third-order noise-shaping characteristics.

Note the summation point of feedforward and noise injection paths in front of the quantizer in Fig.3, a signal addition circuit is necessary to realize all the analog signals summed together; this creates complexity for full feedforward ΔΣAD modulators. In some implementations[8][9], this adder is realized by passive switched-capacitor network. However, this approach reduces the signal level into the quantizer and is only suitable for single-bit implementation. In the noise-coupled ΔΣAD modulator, a multibit implementation is required to ensure the stable of the ΔΣAD modulators, then the switched-capacitor adder has to be used and a weighted summation amplifier is required before the quantizer[10], that leads to extra chip area and power dissipation.

3. Proposed Noise-Coupled ΔΣAD Modulator with Shared OP-Amp

We propose here an improved architecture of a noise-coupled ΔΣAD modulator with shared OP-Amp[11]. It extends the OP-Amp sharing technique for feedforward ΔΣAD modulator[12] to the noise-coupled ΔΣAD modulator architecture.

3.1 Proposed ΔΣAD Modulator Architecture Figure 4 shows the block diagram of the proposed ΔΣAD modulator, and it consists of a single DAC-feedback, two integrators and a noise injection path. Compared with the conventional noise-coupled ΔΣAD modulator shown in Fig.3, we moved the summation point of feedforward and noise injection paths from input node of the quantizer to the input node of the second-stage integrator. The feedforward signals and replica of quantization noise are merged into the output of the first-stage integrator, and then are fed to the second stage.

The transfer function of the proposed ΔΣAD modulator architecture can be expressed as the same as Ep.(8). Therefore, the proposed modulator is an equivalent structure to the modulator shown in Fig.3. By the proposed technique, the feedforward signals and injected quantization noise are summed at input node of the second stage integrator, and no more additional summation amplifier is necessary. The amplifier in the second stage can be shared to realize signal summation, integration and noise coupling. As such, circuit complexity is reduced by not requiring an additional weighted summation amplifier before the quantizer. In the implementation of the full feedforward ΔΣAD modulator, the summation amplifier in front of the quantizer should consume about 8% of total power[10], and we estimate that this amount of power reduction would be possible in the modulator topology of[10] with our proposed OP-Amp sharing technique.

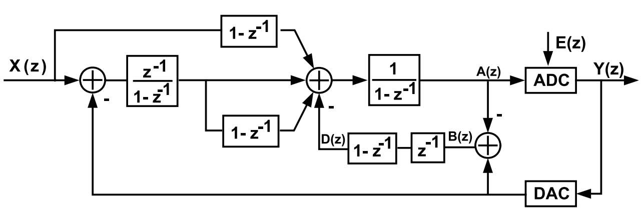

Fig. 4. Proposed noise-coupled ΔΣAD modulator with shared OP-Amp.

3.2 Circuit Implementation of Proposed ΔΣAD Modulator Figure 5 shows the fully differential switched-capacitor circuit implementation of the proposed ΔΣAD modulator (shown in Fig.4) with shared OP-Amp to realize the signal summation. The implementation circuit without error-feedback path is the same as the realization of the 2nd-order ΔΣAD modulator[12]. Parasitic-insensitive switched-capacitor structures are used for integrators[13], and negative capacitors in the modulator are easily implemented by changing the polarity of input signals in the fully differential circuit. It should also be noted that the $(1 - z^{-1})$ term in the feedforward path of the proposed modulator can be implemented just by a capacitor and switches.

The error-feedback path of the modulator shown in fig.5 is implemented by passive capacitors and multi-phase clock signals. The transfer function of error-feedback $[(1 - z^{-1}) \cdot z^{-1}]$ shown in Fig.4 is realized by combining the output of the implementation circuit block of z^{-1} with $-z^{-2}$ shown in Fig.6. And Fig.7 shows the timing chart of clock signals used in the proposed modulator. The analog signals A_1 and A_2 are delayed by controlling switched-capacitors with multi-phase clock. The ADC's output signals Y_1 and Y_2 are delayed by flip-flops, and then used as DAC's input signals. Delayed outputs of internal ADC are used to determine the charge voltage for the capacitors, and the subtraction of analog signals in error-feedback path is realized simply. The coefficients in Fig.4 are realized by the ratios of capacitors around the amplifiers. In our proposed modulator, all coefficients are 1, which is easily imple-

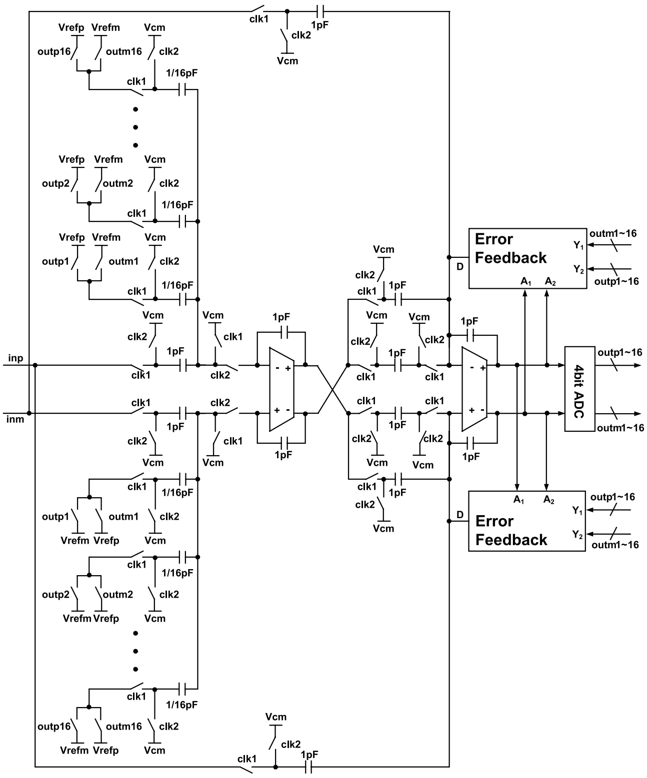

Fig. 5. Switched-capacitor implementation of the proposed modulator.

mented with the same capacitor size, and the size of all capacitors can match well for implementation.

Normally, the error-feedback structure is often applied for the digital loops in ΔΣDA modulators, and it is not practical for ΔΣAD modulators, since it is very sensitive to variations of its parameters in analog implementation. However, in the proposed noise-coupled modulator architecture, because the error-feedback structure is in the backend of feedback loop, so that the coefficient error caused by capacitors mismatch in the second stage can be noise-shaped by the first stage loop filter, and the influence from the variations of analog parameters in the noise-coupled block will be suppressed by the feedback loop. Also, the multibit DACs in the modulator cannot be made perfectly linear and their nonlinearity in the feedback paths are equivalent to errors added directly to the input signals; hence, they may degrade the SQNDR of the ΔΣAD modulator. However, a data-weighted averaging (DWA) algorithm can be provided for the modulator to suppress nonlinearity effects of multibit DACs in the modulator (14). Furthermore, in the proposed modulator, additional DACs composed of capacitors and switches are used to realize the proposed architecture. However, these passive components are only small overhead from conventional noise-coupled modulator.

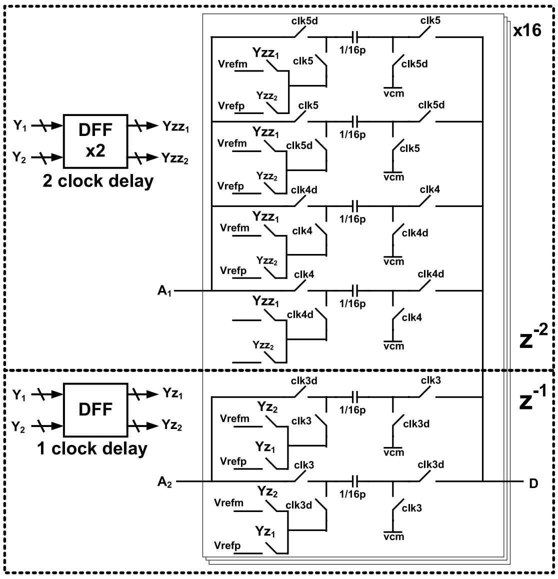

Fig. 6. Switched-capacitor implementation of error-feedback circuit in the proposed modulator.

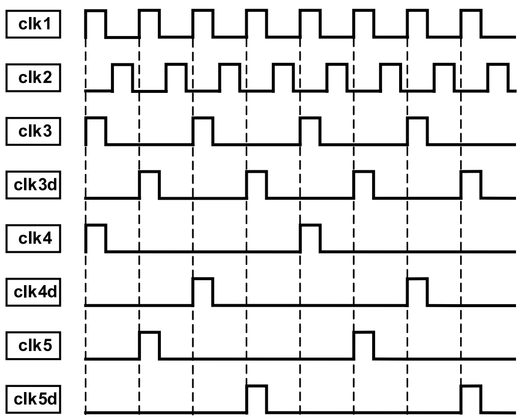

Fig. 7. Clock signals in the proposed modulator.

4. Simulation Results

We have conducted MATLAB simulations to evaluate the effectiveness of the proposed noise-coupled ΔΣAD modulator with OP-Amp sharing technique. We made comparison between behavioral models in Figs. 3 and 4. In the behavioral model of Fig.3, a conventional noise-coupled ΔΣAD modulator is used, and in the behavioral model of the proposed modulator shown in Fig4, we moved the summation point of feedforward signals and injection of quantization noise from input node of the quantizer to the input node of the second-stage integrator. Fig.8 shows simulation results comparison of output power spectrum for behavioral models of above modulators. Fig.9 shows simulation result comparison

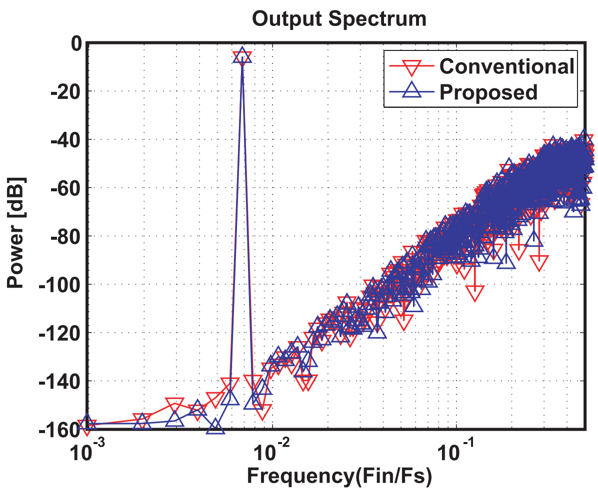

Fig. 8. MALAB simulattion results comparison of output power spectrum between the conventional noise-coupled ΔΣAD modulator and the proposed ΔΣAD modulator.

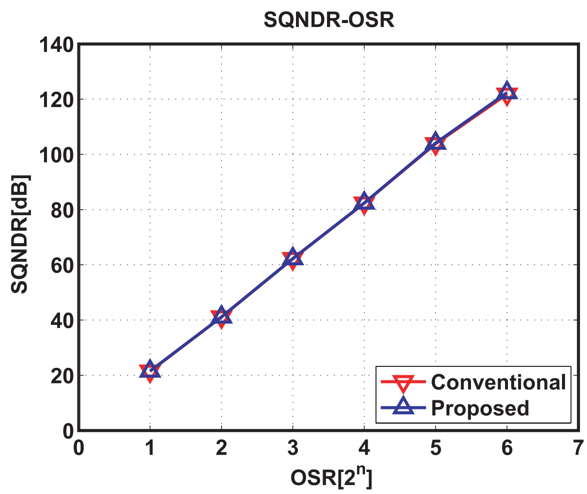

Fig. 9. MATLAB simulation results comparison of SQNDR-OSR between the conventional noise-coupled ΔΣAD modulator and the proposed ΔΣAD modulator.

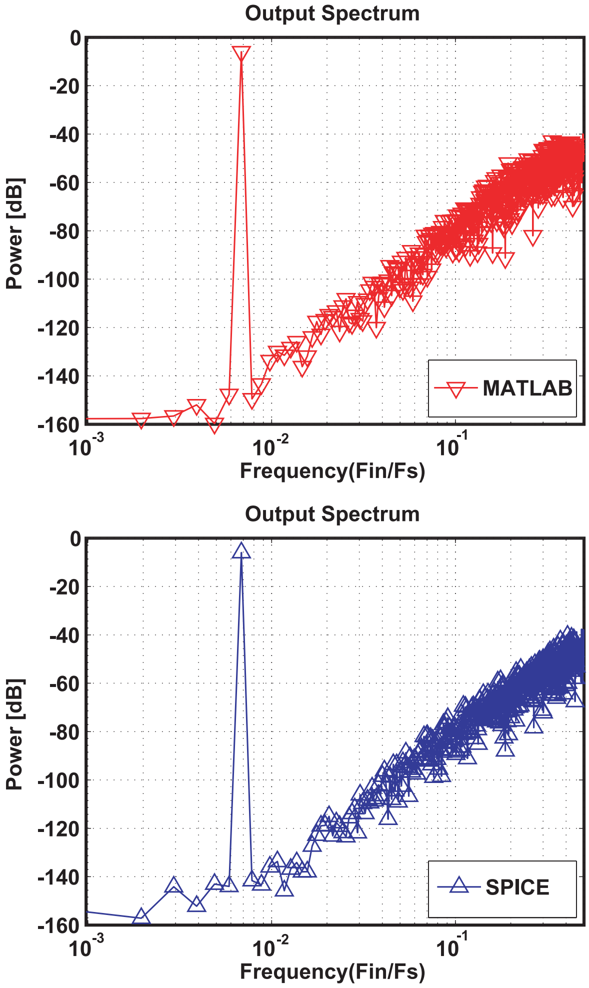

Fig. 10. Simulation result comparison of output power spectrum in behavioral models with MATLAB and behavioral circuit with SPICE.

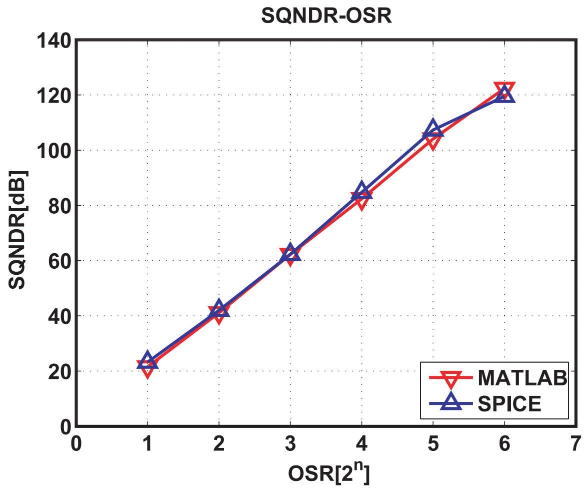

Fig. 11. Simulation result comparison of SQNDR–OSR in behavioral models with MATLAB and behavioral circuit with SPICE.

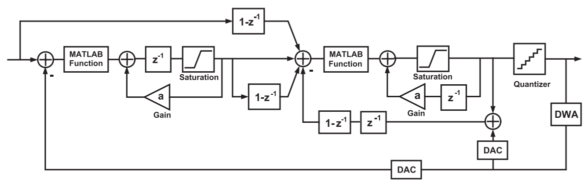

Fig. 12. MALAB simulation model of proposed ΔΣAD modulator with non-idealities.

Table 1. Non-ideality of SC Cicuit

Amplifier	$DCGain$=40 dB GBW=600$M\ Hz$ $Slewrate$=300 $V/\mu s$
Capacitor Mismatch	=0.1 %

of SQNDR vs OSR which are calculated from above of their output power spectrum of the behavioral models. According to simulation results of Fig.8, we see that the output power spectrum of conventional and proposed modulators are almost the same, and from Fig.9 we see that the SQNDR value of the modulators are almost the same, too. It suggests that the proposed modulator is equivalent to the conventional noise-coupled modulator, and it can realize the noise-shaping enhancement as the same as the conventional noise-coupled ΔΣAD modulator but with smaller hardware.

We also have conducted SPICE simulations to evaluate the behavioral circuit of the proposed modulator which is shown in Fig.5. In SPICE simulation, ideal amplifiers and switches are used, and the values of capacitors are shown in Fig.5. We assume that supply voltage is V_{dd}=1.8V, reference voltages are V_{refp}=1.4V, V_{cm}=0.9V and V_{refm}=0.4V, input signals are differential sine waves with V_{pp}=0.5V and common mode voltage of 0.9V. Fig.10 shows simulation result comparison of output power spectrum, which used behavioral models with MATLAB and behavioral circuit with SPICE. Fig.11 shows comparison of SNDR-OSR which are calculated from the output power spectrum shown in Fig. 10. We can see from Figs.10 and 11 that the SPICE behavioral simulation results agree with MATLAB simulated results, and hence the proposed circuit realizes the noise-shaping enhancement as well as at system level of the proposed architecture.

In the implementation of ΔΣAD modulator with switched-capacitor circuits, non-idealities of amplifiers and mismatches among capacitors should reduce the resolution of the modulator. We conducted MATLAB behavioral simulation with non-ideal model (15) to evaluate the performance reduction of the proposed modulator. We used the model shown in Fig.12 which includes the practical limitation caused by finite DC gain, bandwidth, slew-rate of the op-amps and capacitor mismatches in Table 1. In our simulation, an ideal internal 9-level ADC in the ΔΣAD modulator is used. However two 9-level DACs in the modulator are assumed as normal segmented switched-capacitor DACs with mismatches among unit capacitor-cells. DWA circuit is used to shape out the non-linearity of DACs which is caused by the mismatches among capacitors. Fig.13 shows simulation result comparison of output power spectrum, and Fig.14 shows comparison of SNDR-OSR with/without non-idealities in proposed modulator. We see that the performance reduction is very slight (below

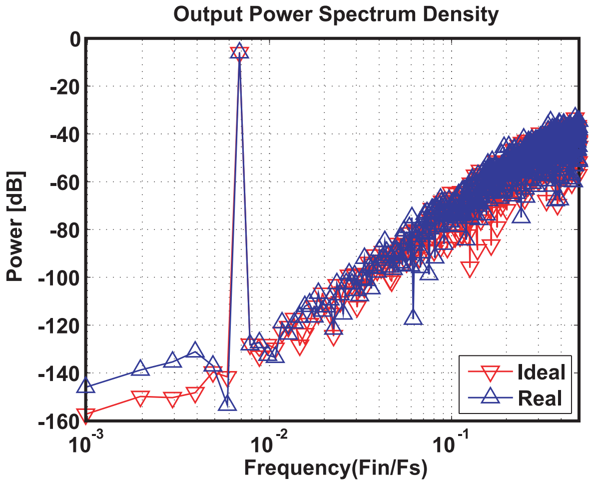

Fig. 13. MALAB simulation results comparison of output power spectrum between the proposed ΔΣAD modulator with and without non-idealities.

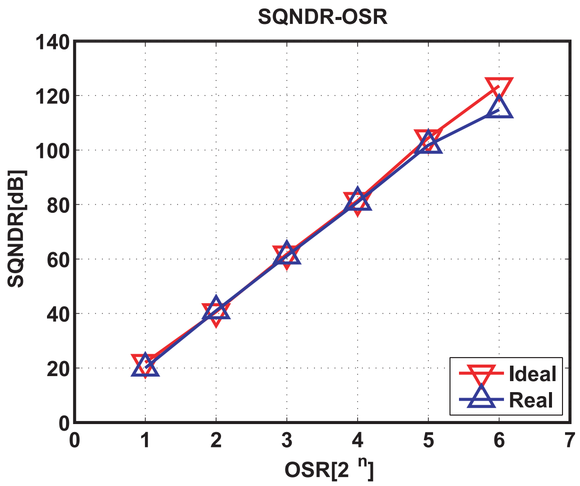

Fig. 14. MATLAB simulation results comparison of SQNDR-OSR between the proposed ΔΣAD modulator with and without non-idealities.

5dB while OSR=64), which benefit from the feedforward architecture and DWA algorithm.

5. Conclusion

We have proposed an improved architecture of the noise-coupled ΔΣAD modulator with shared OP-Amp. By the techniques of quantization noise injection and amplifier-saving, the proposed modulator provides a higher-order NTF using a lower-order loop filter. The additional integrator circuit using an operational amplifier is not necessary, and the performance of the ΔΣAD modulator can be effectively raised without more power dissipation. The MATLAB simulation results with behavioral model show that the proposed architecture can effectively raise the order of the modulator, and improve the SQNDR of a ΔΣAD modulator.

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