Production Test Consideration for Mixed-Signal IC with Background Calibration

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Outline

- Research purpose
- Proposed algorithm for
  calibration time reduction during the test
- Case study of
  digitally-assisted pipelined ADC
- Simulation results
- Conclusion

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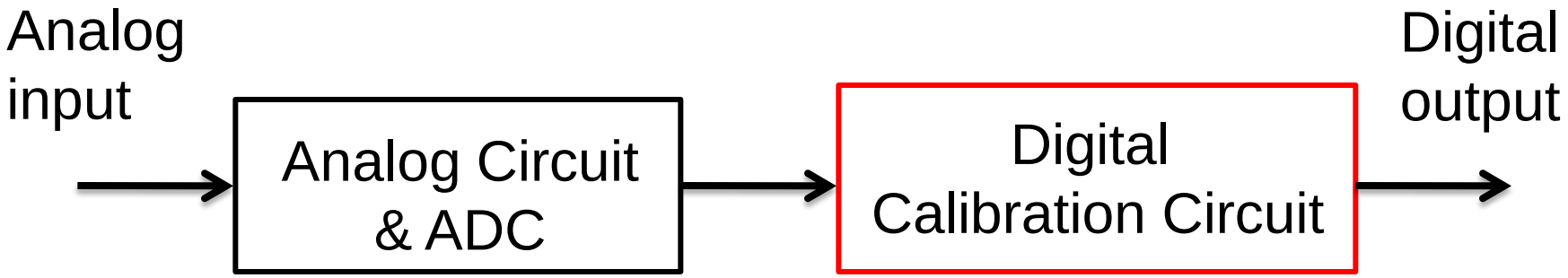
Digitally-Assisted Analog Circuit in Nano CMOS Era

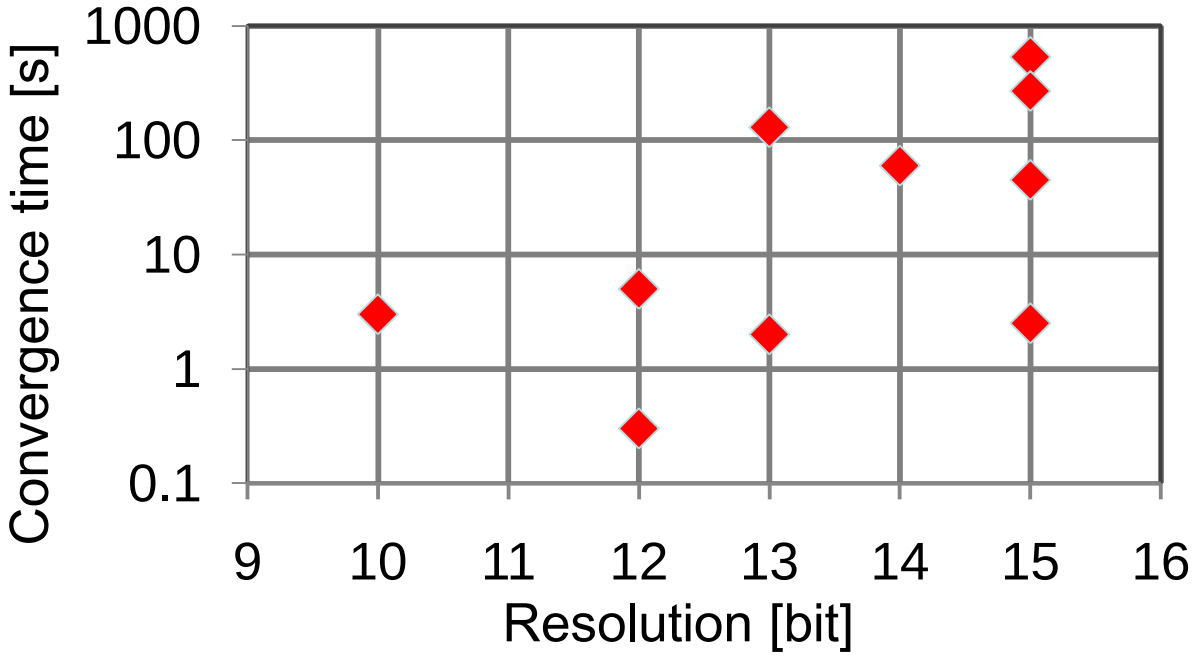


- Digital: Benefit from nano CMOS
- Analog: Accuracy constraints
- Digitally-assisted analog:
  → Relax analog circuit performance

Digitally-Assisted Analog Circuit Test

- Background calibration time → Long

[Pipelined ADC with calibration research paper in recent years]



- Total testing time = Background calibration time + Functional testing time
- Long testing time → increase testing cost

Research purpose

- Background calibration time reduction during the test
  - ✓Algorithm Proposal:
    Load the converged calibration data of chip1 to chip2, chip3, …as their initial data
  - ✓ Consideration of correlation among chips within the same wafer
  - ✓ Small additional read/write circuits for on-chip memory
  - ✓ Cooperation with ATE

(ATE: Automatic Test Equipment)

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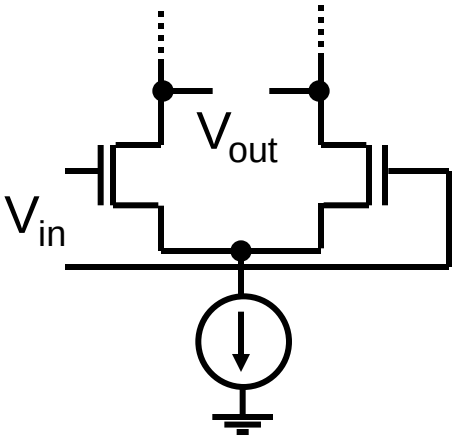
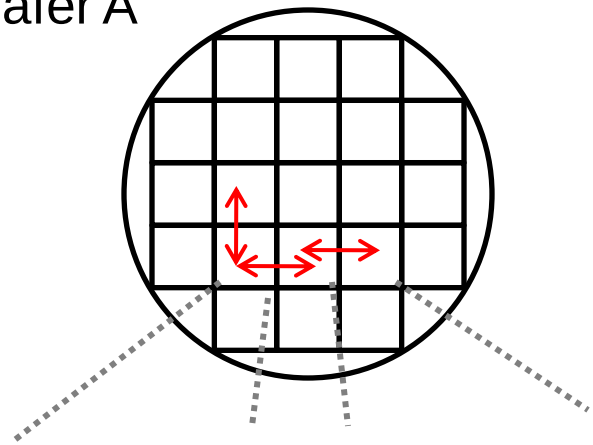
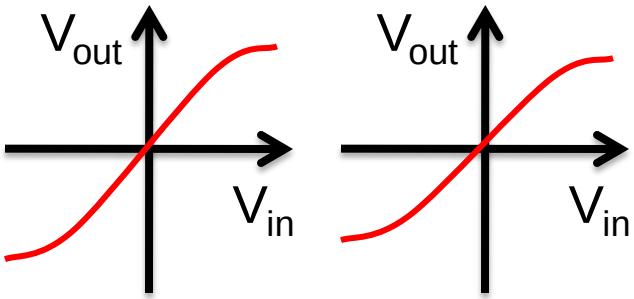
Correlation among Chips within the Same Wafer

Ex.)
Nonlinear Amplifier



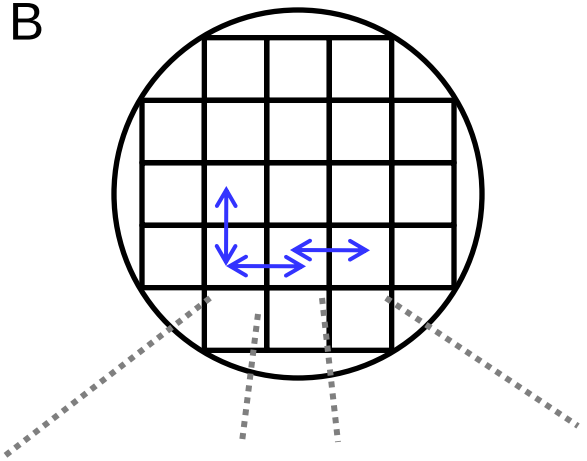
Wafer A

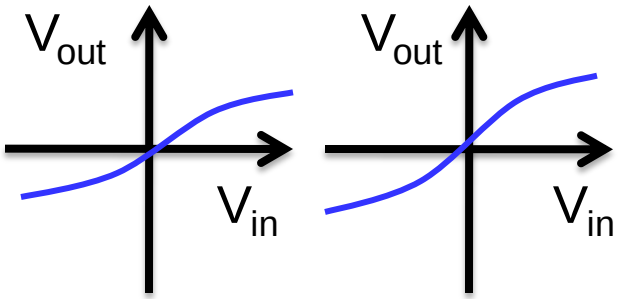




Correlation

Wafer B

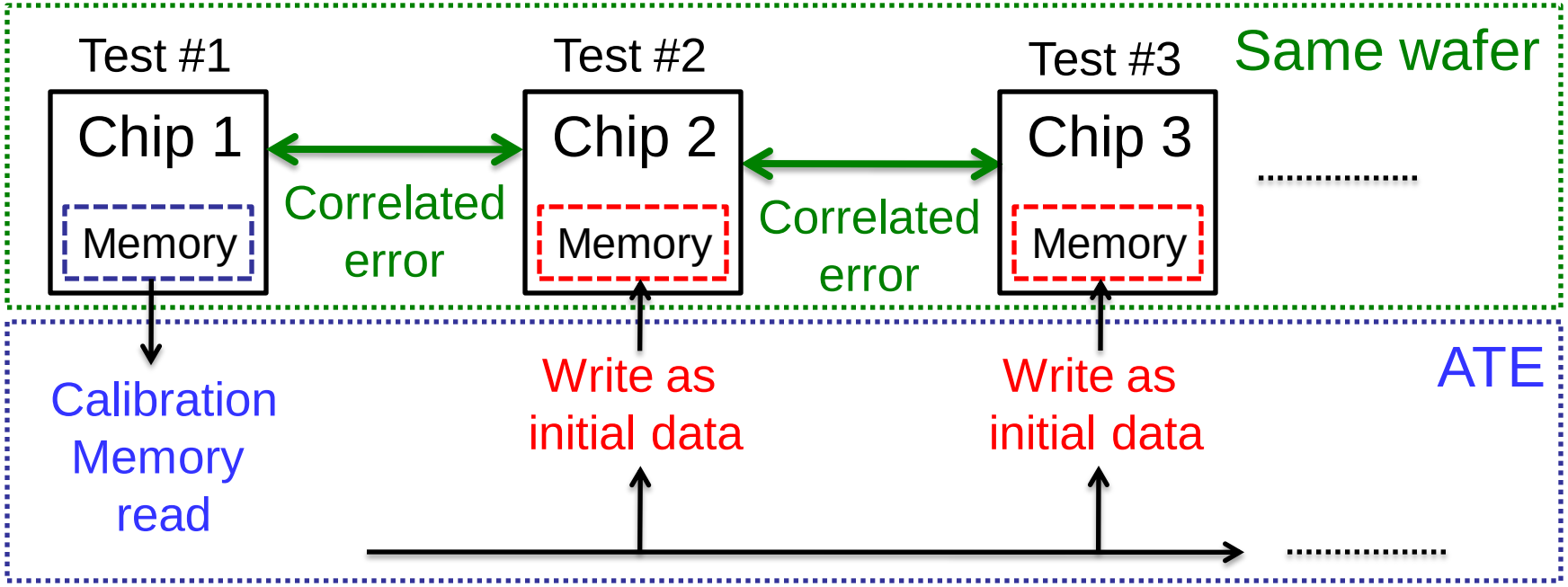




Correlation

- Strong correlation among die-to-die nonidealities can be used
- Converged calibration parameter values would be close among chips within the same wafer

Proposed Algorithm for Calibration Time Reduction during Test



- ATE reads converged calibration data in memory of chip1
- Load them to memory of chip2, chip3 … as initial data
- Calibration of chip2, chip3 … converges quickly

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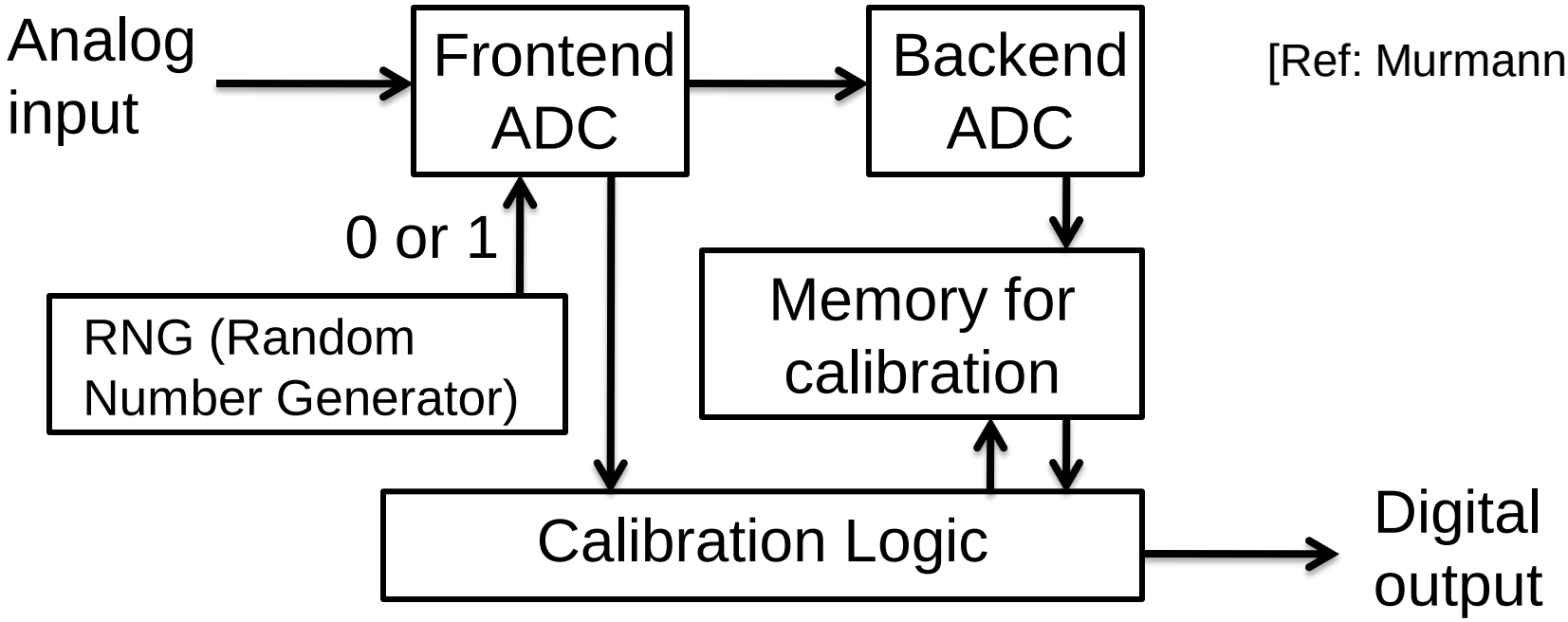
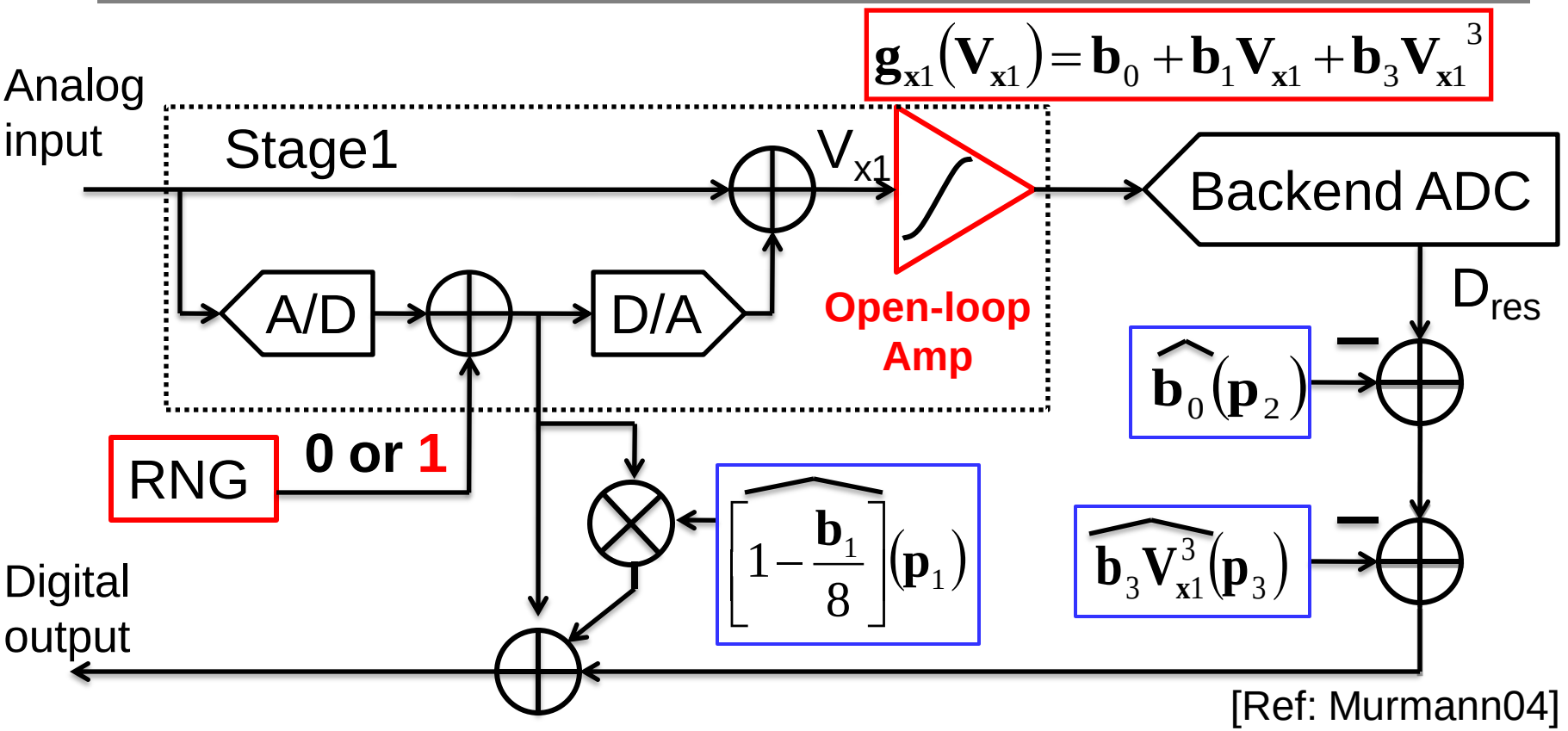
Digitally-Assisted Pipelined ADC



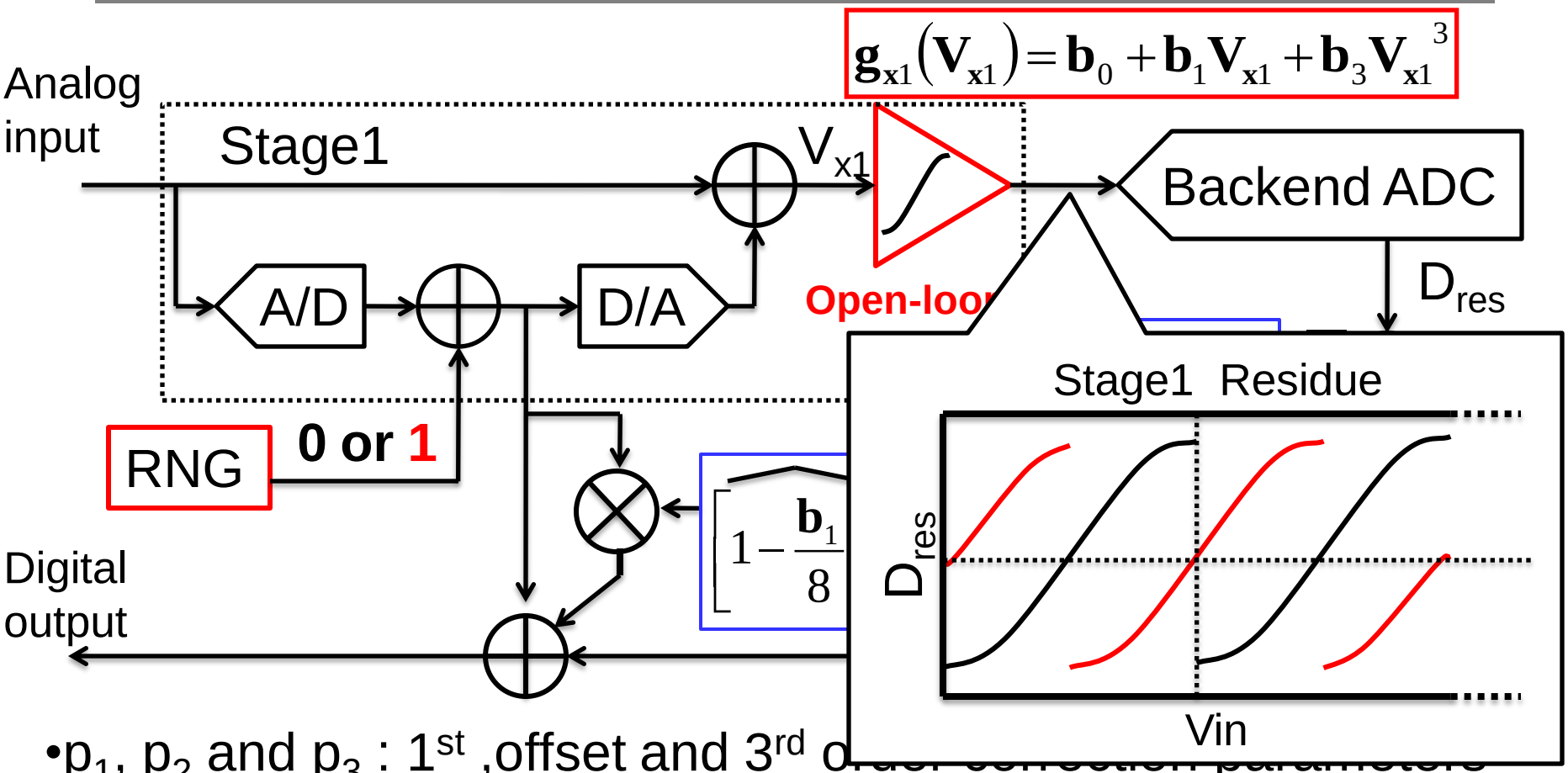
- Use open-loop amplifier in frontend ADC
  - ✓ High speed + low power
  - ✓ Amplifier Nonlinearity
    - ↳ Digital background calibration

Digital Calibration of Amp Nonlinearity



- p_1, p_2 and p_3 : 1st ,offset and 3rd order correction parameters
  - ✓ Estimated by "Distance Estimation"
  - ✓ Background calibration using LMS loop (LMS: Least Mean Square)

Digital Calibration of Amp Nonlinearity



- p_1, p_2 and p_3 : 1st ,offset and 3rd order correction parameters
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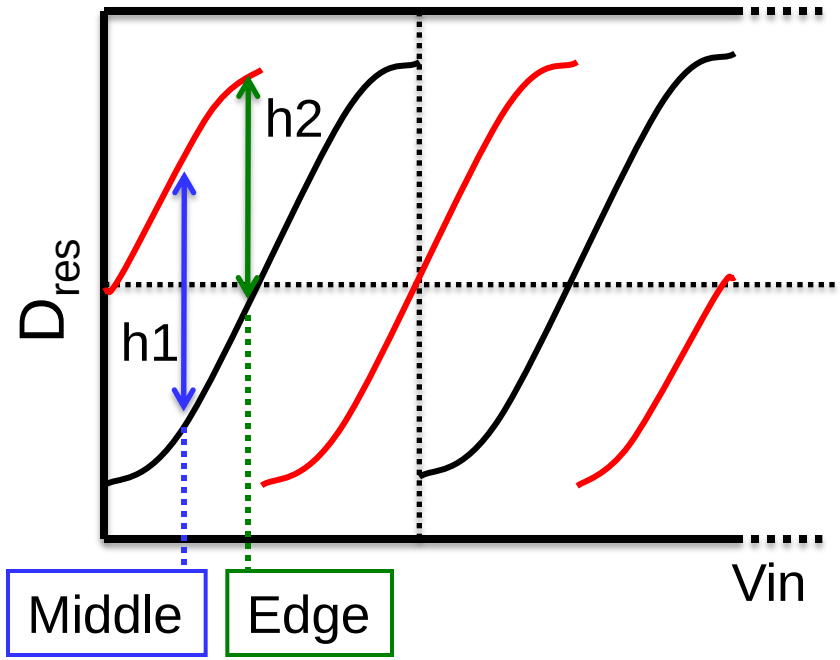
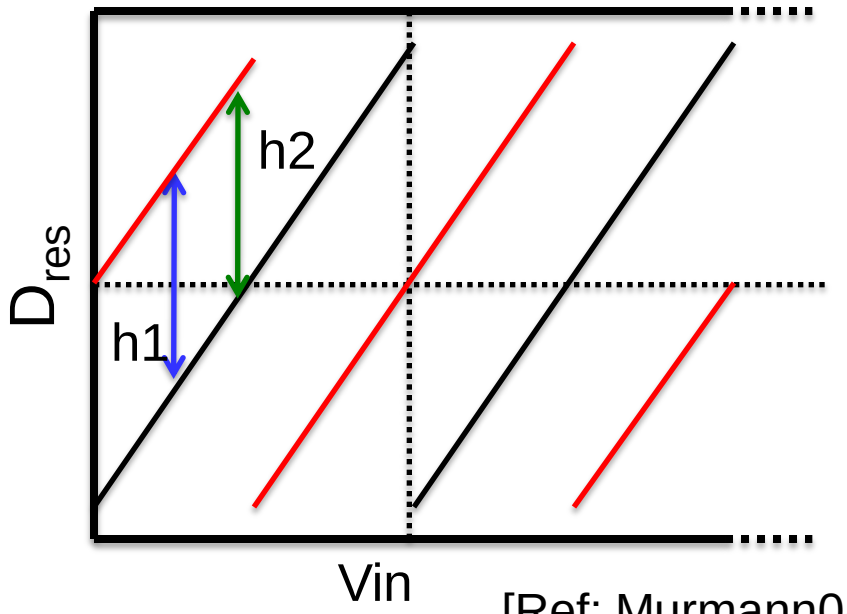
Distance Estimation (1)

•Before calibration: h2<h1



•After calibration: h2=h1



[Ref: Murmann04]

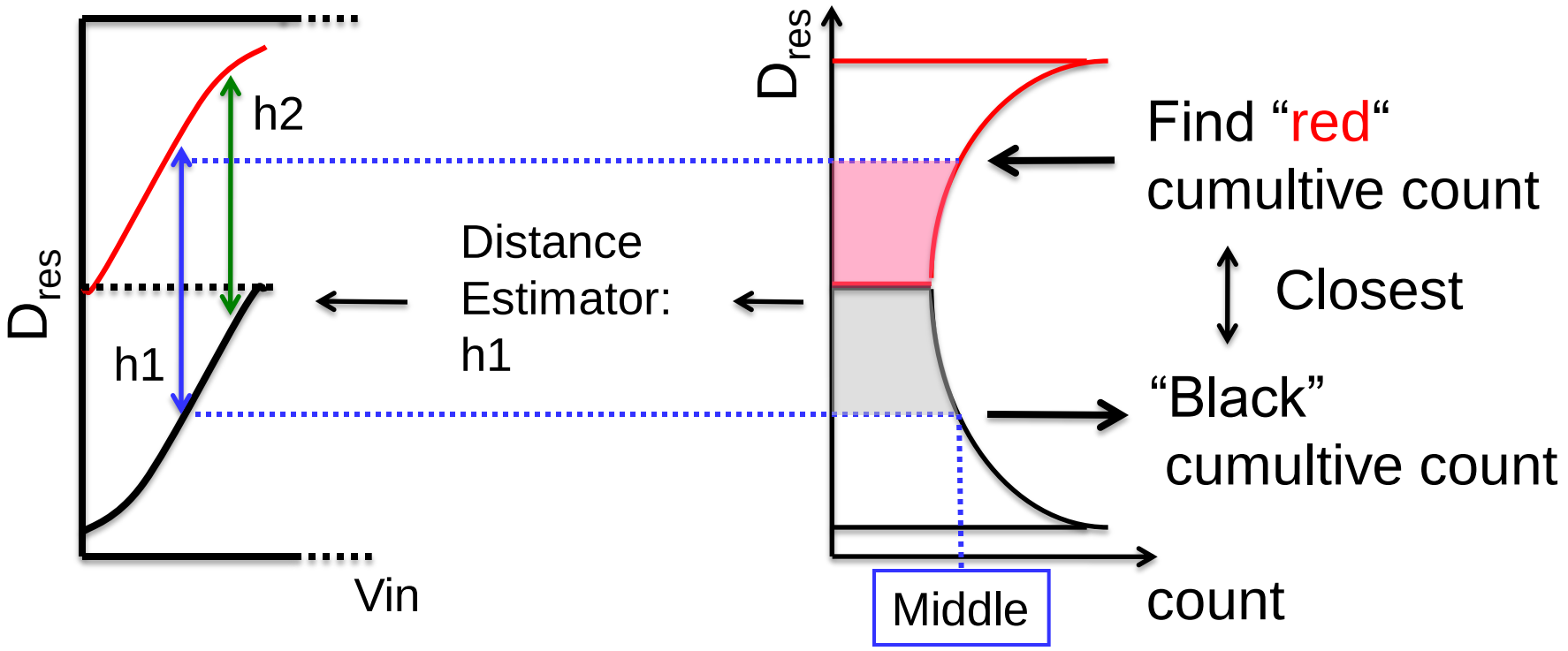
•Two-residue pipeline stage added by random number, 0 or 1

•Measure h_1, h_2 and force difference (h_1-h_2) to 0

✓ Statistics-based measurement (using histogram)

Distance Estimation (2)

- Two residue
- Histogram [Ref: Murmann04]

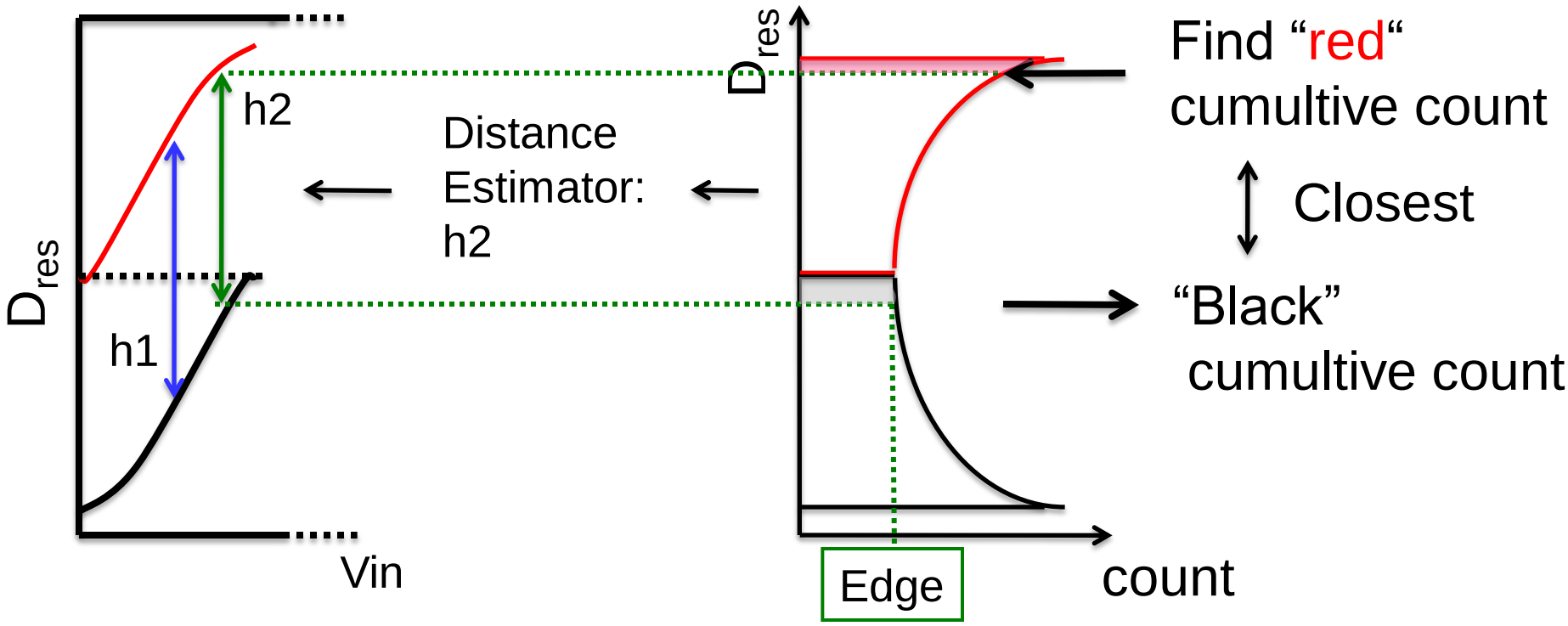


- Use hitstogram to measure h_1, h_2
  - ✓ 30,000 samples are collected for histogram evaluation

Distance Estimation (3)

- Two residue
- Histogram

[Ref: Murmann04]



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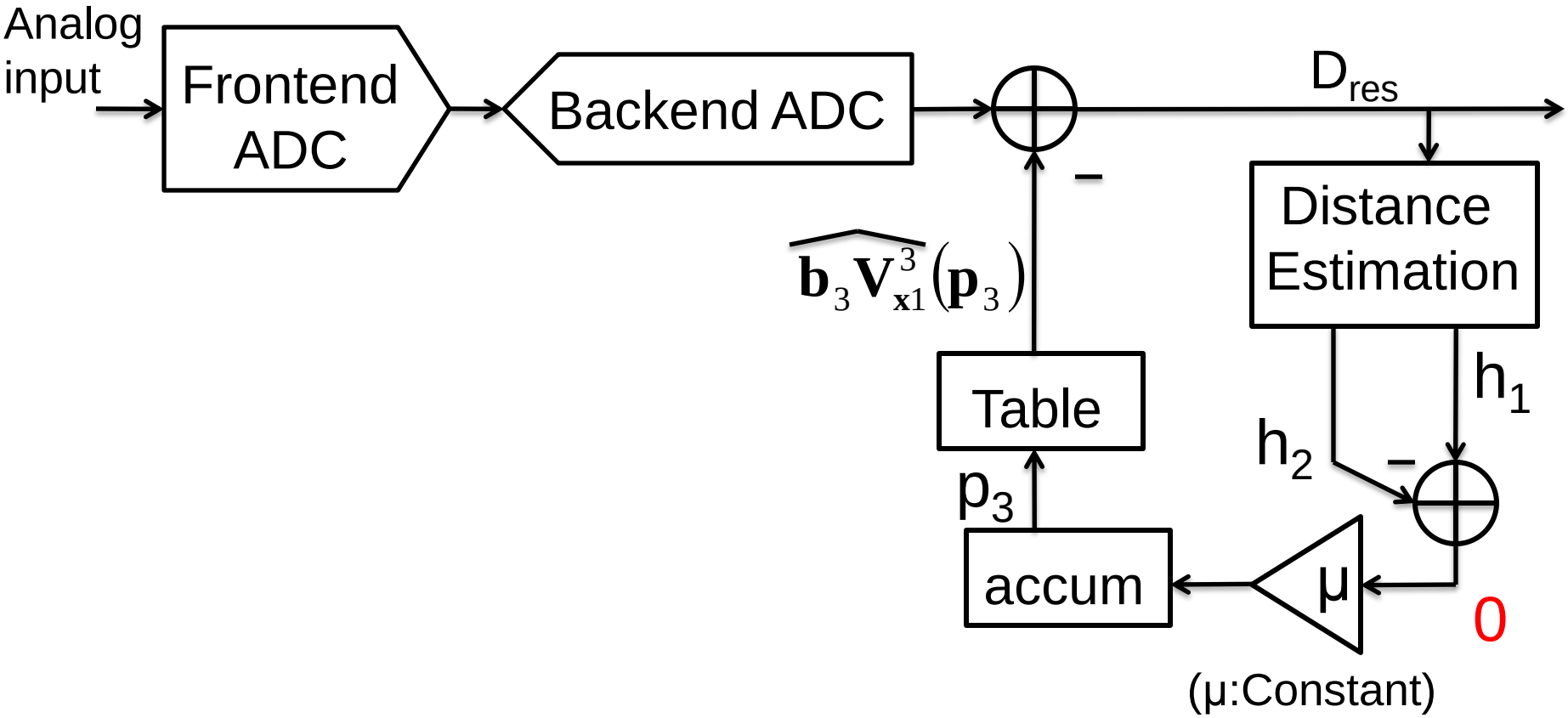
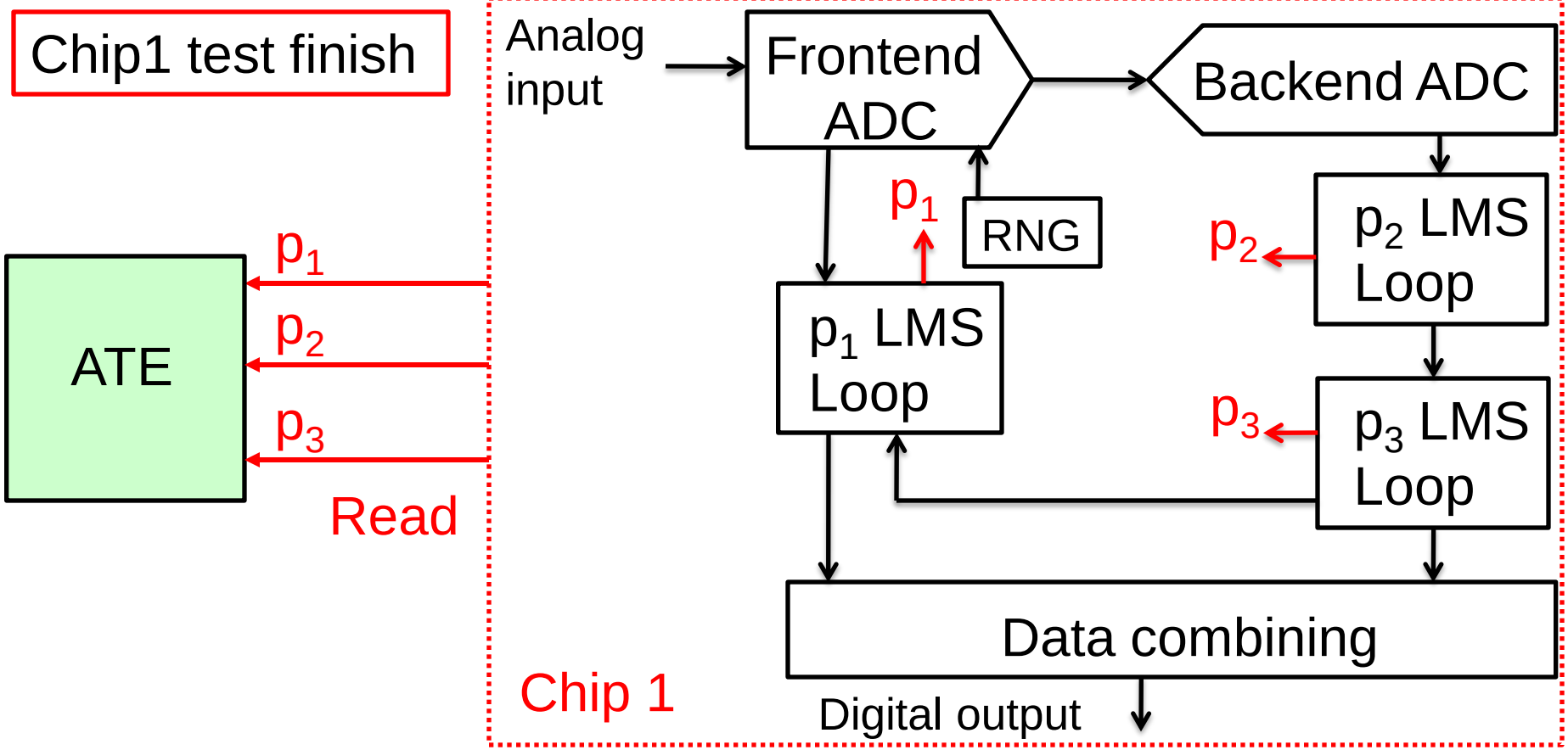
LMS Loop



- Parameter p_3 (also p_1 and p_2)
- Accumulator forces (h_1-h_2) to zero
- Need many samples (about $5*10^7$) to converge LMS loop

Apply Proposed Algorithm to Digitally-Assisted Pipelined ADC



- ATE reads converged parameters p1, p2 and p3 of chip1
- Load them to registers of chip2 as their initial data

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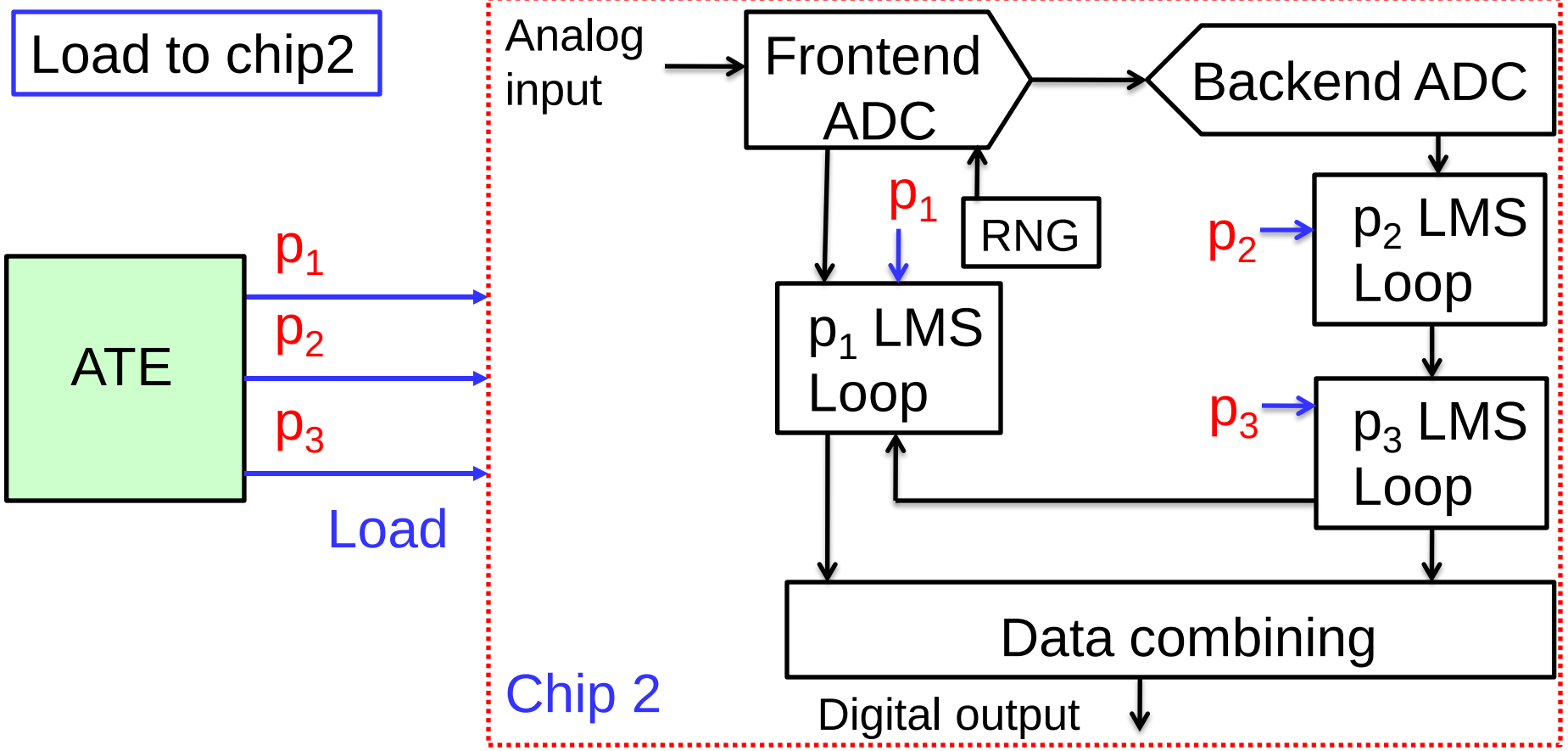

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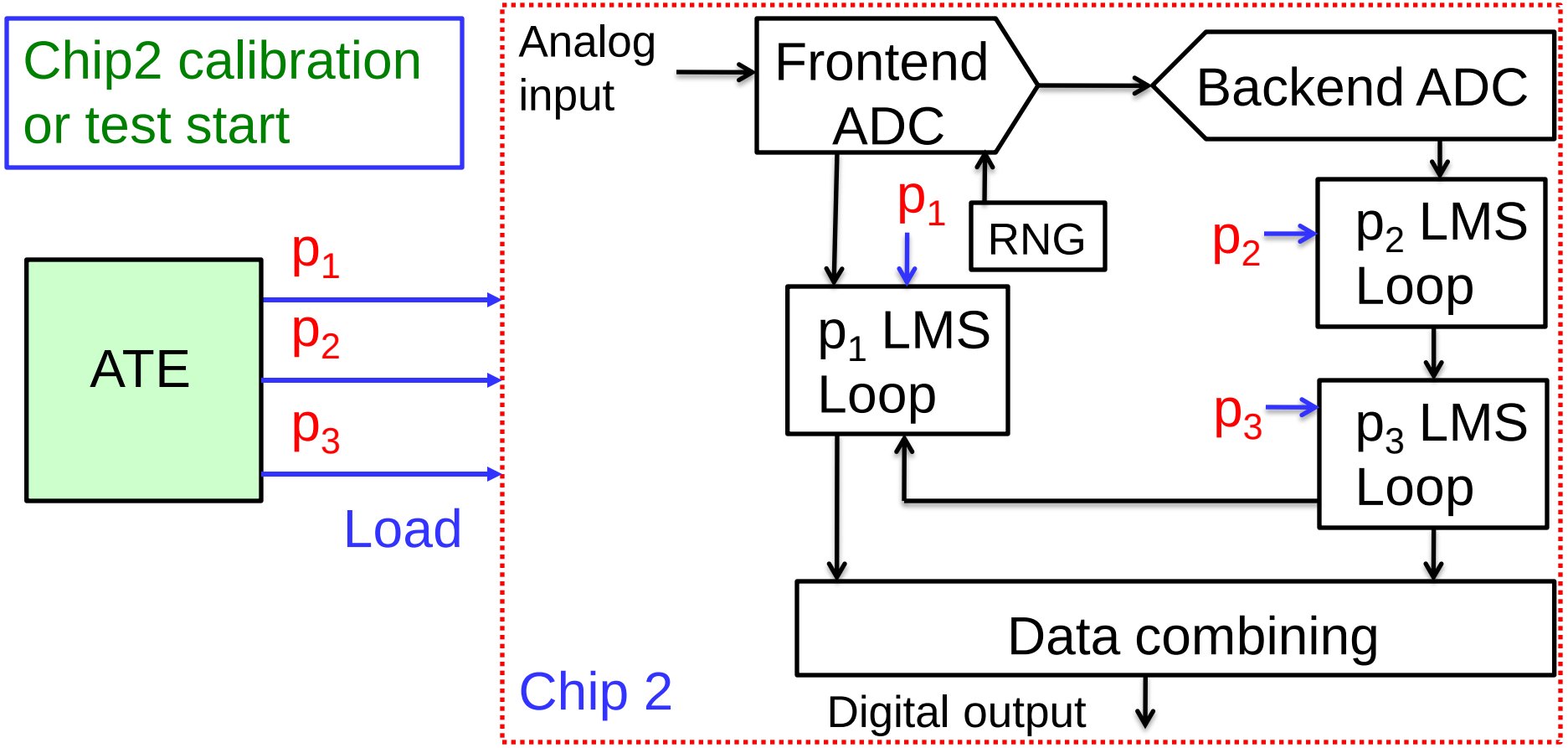

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Matlab simulation

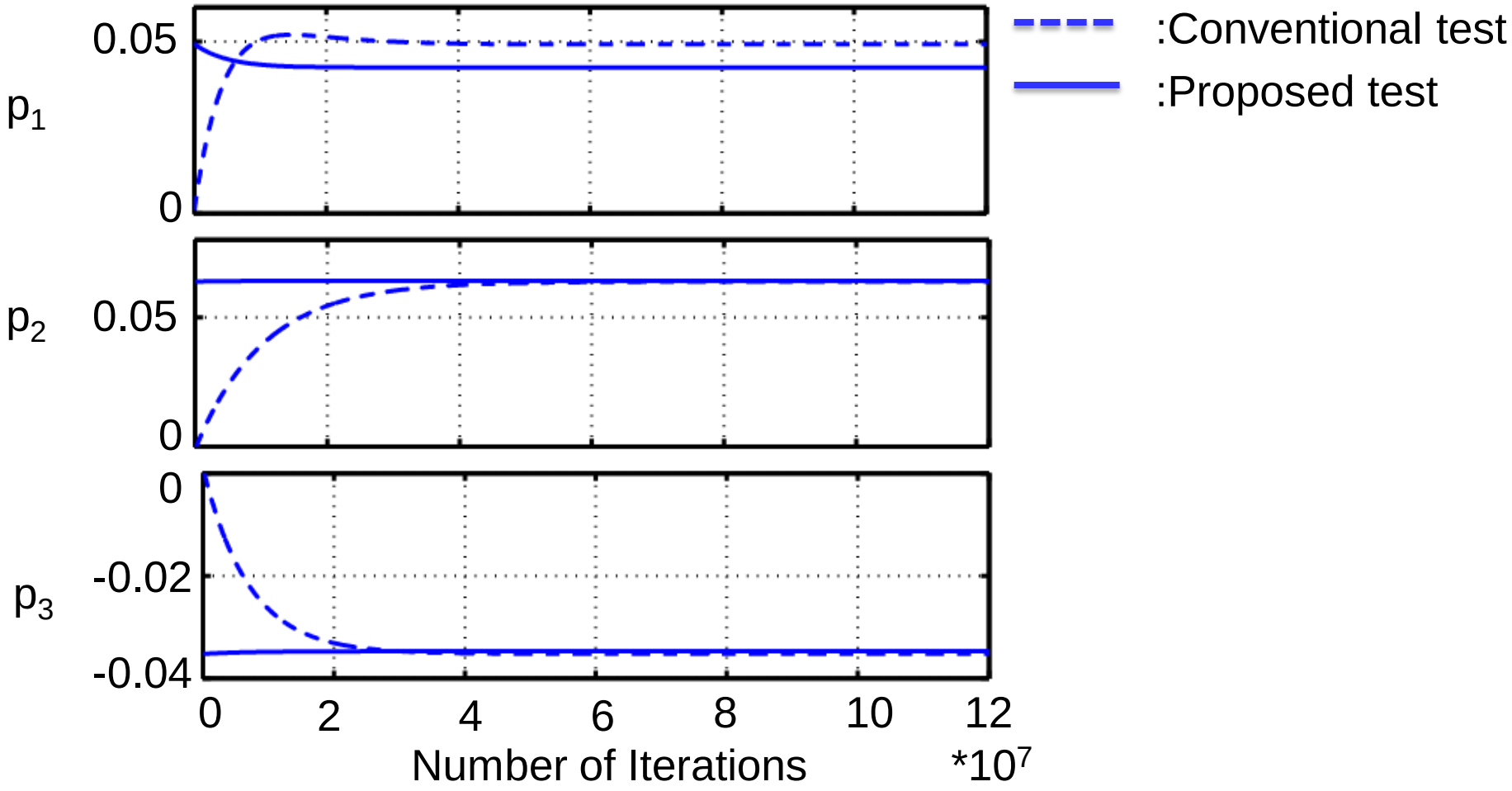
- 12bit Pipelined ADC
  - ✓ 4bit / stage + 2bit / stage + 7*1.5 / stage + 3bit flash ADC
- Residue Amplifier Nonlinearity [Ref: Murmann04]

$$\mathbf{g_x(V_x) = g_m R}\left[\left(\frac{\mathbf{V_x}}{\mathbf{V_{ref}}}\right)+\frac{1}{4}\frac{\Delta\beta}{\beta}\left(\frac{\mathbf{V_{ref}}}{\mathbf{V_{ov}}}\right)\left(\frac{\mathbf{V_x}}{\mathbf{V_{ref}}}\right)^2-\frac{1}{8}\left(\frac{\mathbf{V_{ref}}}{\mathbf{V_{ov}}}\right)^2\left(\frac{\mathbf{V_x}}{\mathbf{V_{ref}}}\right)^3\right]$$

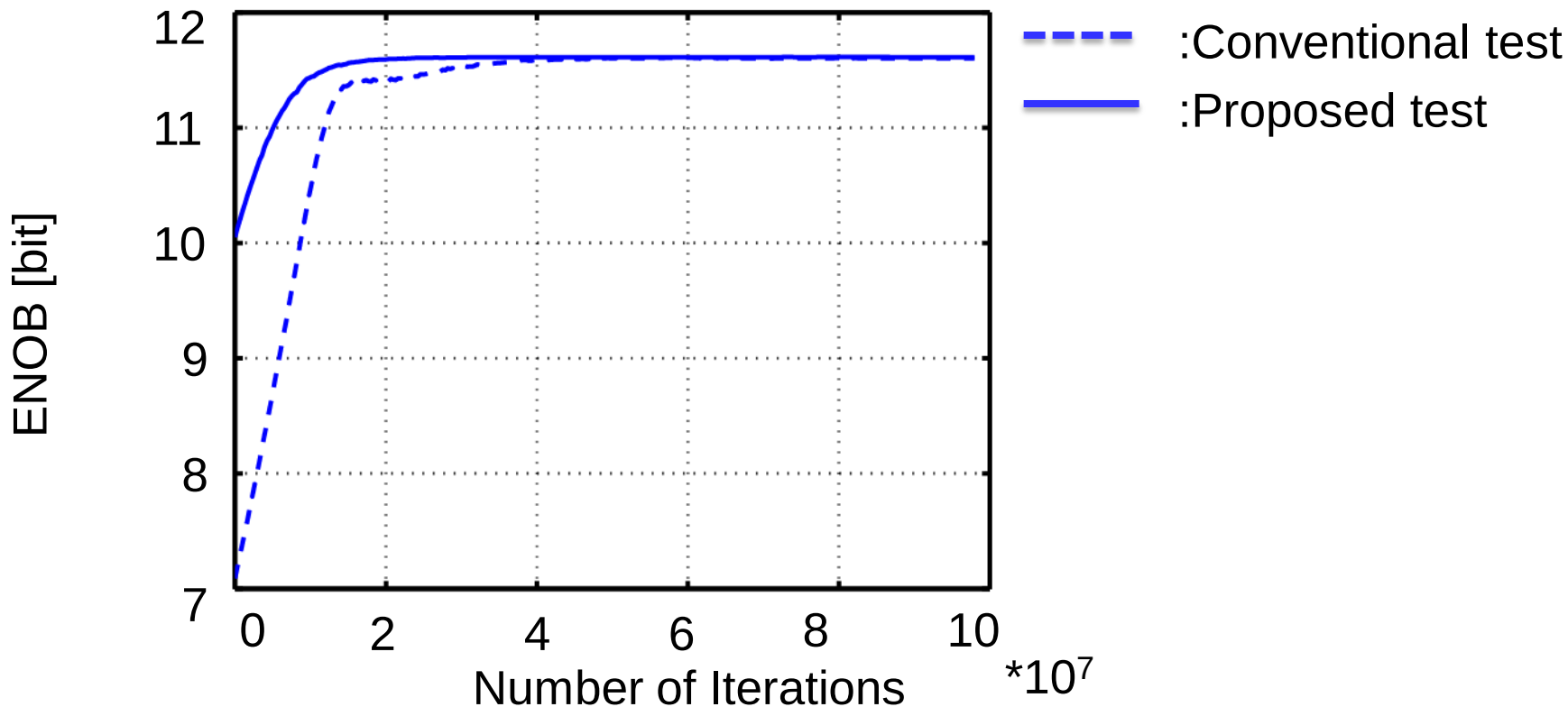
Vref	:	Converter reference voltage	1 V
$g_m R$	:	Linear amplifier gain term	7.6 ± 0.5%(σ)
Vov	:	Differential pair gate overdrive	0.25 V
$\Delta\beta/\beta$	:	Transistor mismatch	+5% ± 0.5%(σ)

- Consider 16 chips per test
  - ✓ Total number of tested chips is 1024

Parameter Convergence

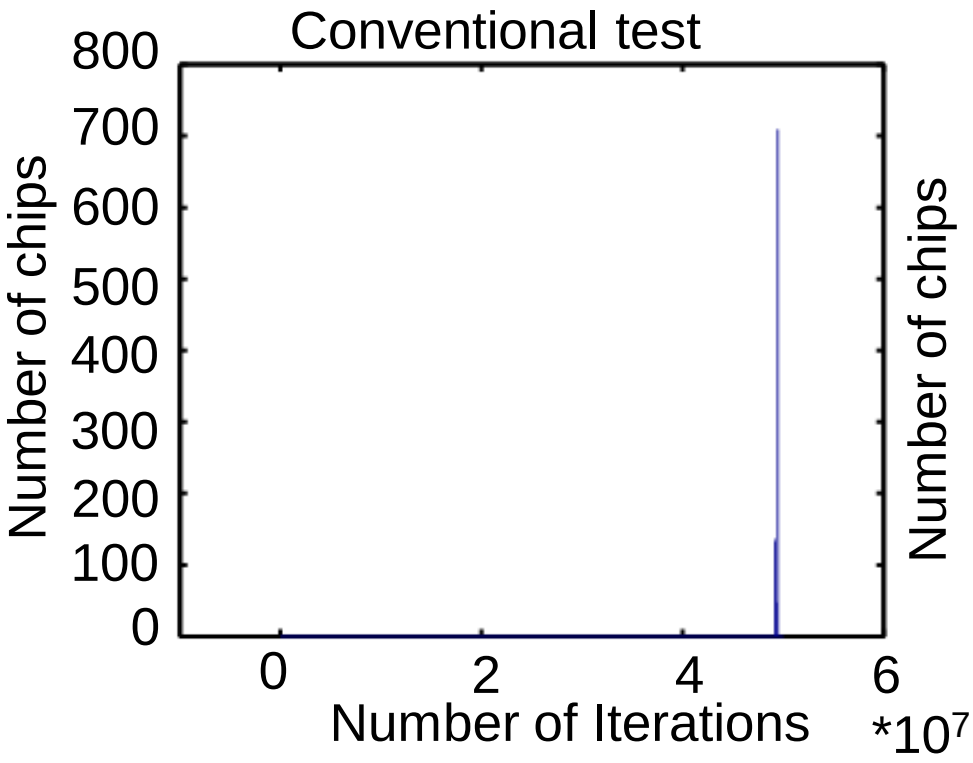


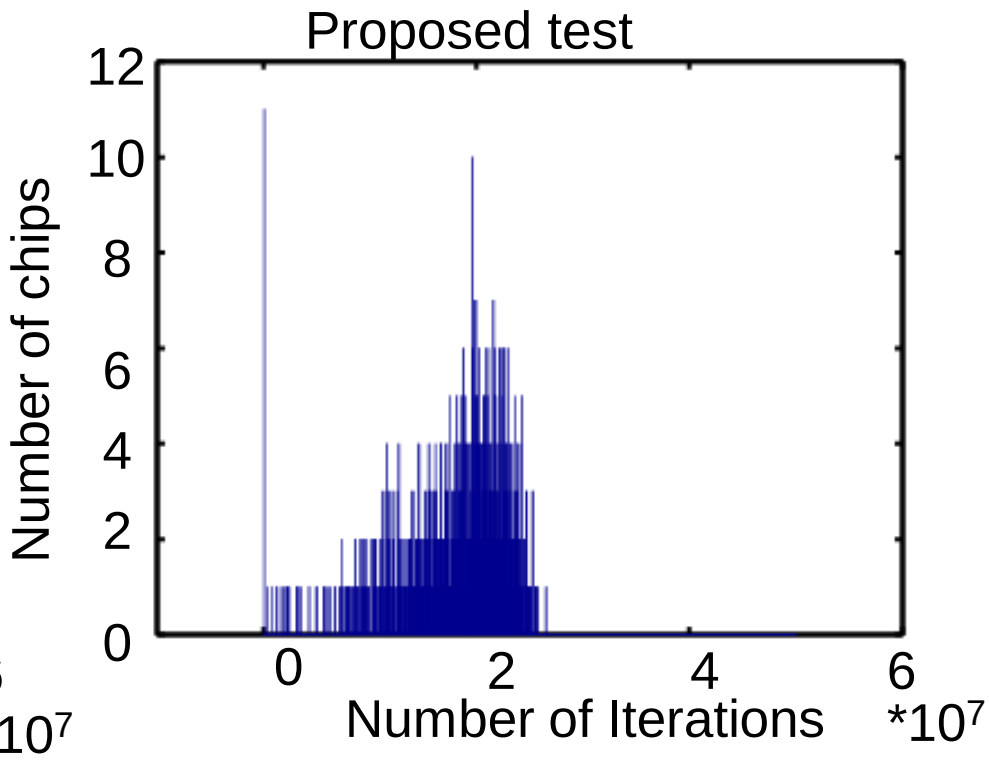
ENOB Convergence



- Conventional test converged at ~ $5*10^7$ iterations
- Proposed test converged at ~ $2.5*10^7$ iterations

Comparison of Convergence Time





- Conventional test : ~ $5*10^7$ iterations
- Proposed test : ~ $2.5*10^7$ iterations (Worst case)
  - ✓ Reduced convergence time by 1/2 during the test

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Conclusion

- Propose testing method for digitally-assisted analog circuit
  - ✓Die-to-die correlation reduces calibration time combing on-chip calibration logic with external low-cost ATE
- Calibration time reduction during the test
  - ✓ Consideration of correlation among chips within the same wafer
  - ✓ Case study of digitally-assisted pipelined ADC [Ref: Murmann04]

Reduced convergence time by 1/2 during the test