Issues and Challenges of Analog Circuit Testing in Mixed-Signal SOC

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Contents

Cost is the most important

- Analog portion continues to be difficult part of SOC test.
- Concept of "cost" makes "issues and challenges of analog circuit testing in mixed-signal SOC" clear and logical.
- Everything converges to "cost" in LSI testing technologies.

Contents

Management Strategy

- Strategy 1 :

  Use low cost ATE and develop analog BIST

  to make testing cost lower.

- Strategy 2 :

  Use high-end mixed-signal ATE

  as well as its associated services & know how.

  Fast time-to-market & no BIST

  can make profits much more than testing cost.

Save or Earn

ATE: Automatic Test Equipment

BIST: Built-In Self-Test

Low Cost Testing

Ideal :

- 100% chips work well. No testing

Reality :

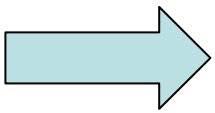
- Low cost ATE
- Short testing time
- Multi-site testing
  (Simultaneous multiple-chip test)
- Minimum or no chip area penalty for BIST

A penny saved is a penny earned.

Additional Benefits of Testing

- Diagnosis

  Automotive application IC

   very high reliability

  Diagnosis is important.

- Yield enhancement

  Testing and DFT can help

  yield enhancement

DFT: Design For Testability

Test and Measurement are different

- Production Test : 100% Engineering

  Decision of “Go” or “No Go”

  For example, it can be performance comparison between DUT and “Golden Device”.

  LSI testing is production/manufacturing engineering.

- Measurement : 50% Science, 50% Engineering

  Accurate performance evaluation of circuit

Measurement can be costly, but testing should be at low cost.

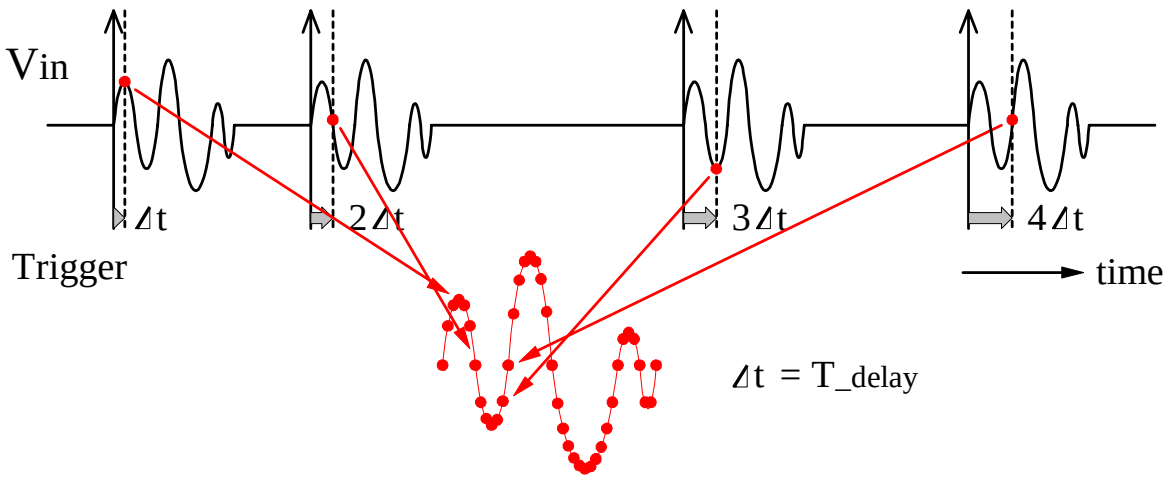
DUT: Device Under Test

Equivalent-time Sampling in Testing

- Production Test :

  Input signal is controllable

  ⇨ Equivalent-time sampling



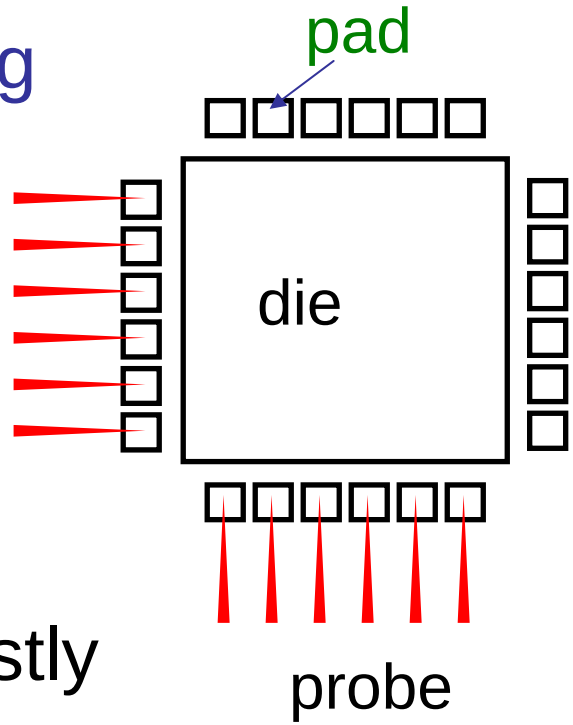
Waveform reconstruction of repetitive signal

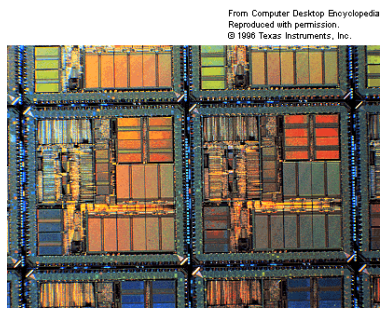
- Measurement : Input signal is unknown

Equivalent-time sampling can test high frequency signal at low cost.

On-Wafer Probing Testing

- On-wafer testing before packaging reduces IC cost.
- Probing has some issues:
  - On-resistance of probing
  - Probing damages PAD
    - ⇨ MEMS probe may alleviate it.
  - High-frequency signal probe is costly
    - ⇨ No test after yield becomes better.
  - Multi-site probing is difficult.
- Wireless communication technology may realize contact-less probing.





Analog BIST

- BIST for digital : Successful
  (scan path, memory BIST)
  BIST for analog : Not very successful
- Digital test : Functionality ⇨ Easy
  Analog test : Functionality & Quality ⇨ Hard

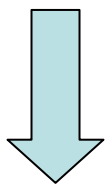
Analog: parametric fault as well as fatal fault.

Prof. A. Chatterjee
Specification-based Test Alternative Test Defect-based Test

- In many cases
  - Analog BIST depends on circuit.
  - No general method like scan path in digital.
  - One BIST, for one parameter testing

Two Contradictions of Analog BIST

- Analog BIST has to have no defects.
- Analog BIST often has to have better performance than circuit under test.

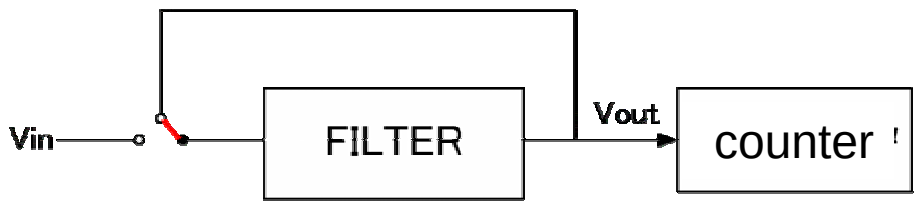


To solve these contradictions,
analog BIST must be small & simple.

Analog BIST chip area and testing cost are trade-off.

Analog BIST Example

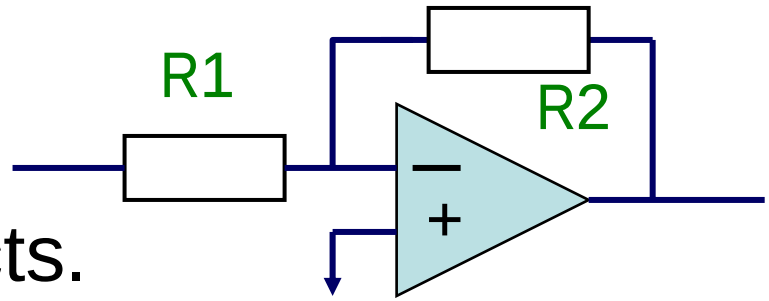
- **Δ Σ** modulation for signal generation
- Time-domain analog processing
- Analog boundary scan
- Use of power supply line
- Oscillation during test (analog filter, OpAmp)



- "Controllability", "Observability" are useful concepts.

Robust Design and Testing

Robust design makes its testing difficult.



- Feedback suppresses parameter variation effects.
- Self-calibration and redundancy hide defects in CUT.
- Background calibration takes long time for its testing due to calibration convergence.

Robust design (yield enhancement) and testing cost reduction are trade-off.

ADC Testing (DC Linearity)

- DC linearity test is the most important.
  - Precise ramp generation is challenging.
  - High resolution ADC ⇨ long testing time

- DC testing time is proportional to

  number of codes / sampling frequency

  large slow

High resolution ADC DC linearity test takes long time and is costly.

ADC Testing (AC Performance)

- ADC AC performance testing
  - Sampling clock jitter
  - High frequency input signal
- We have to build low clock jitter system and apply high frequency input signal.

  No alternative method so far.

Development of ADC AC performance testing system is costly.

RF Testing

- RF testing technology is different from analog testing technology.
- Testing item examples:
  - EVM test
  - System level testing, GSM/EDGE
  - AM/PM distortion
  - Jitter, Phase noise
- High-speed I/O testing is another challenging area.

VCO, PLL Testing

- Phase noise measurement

  takes long time

  (several times average is required.)

- Method of

  phase noise testing in short time

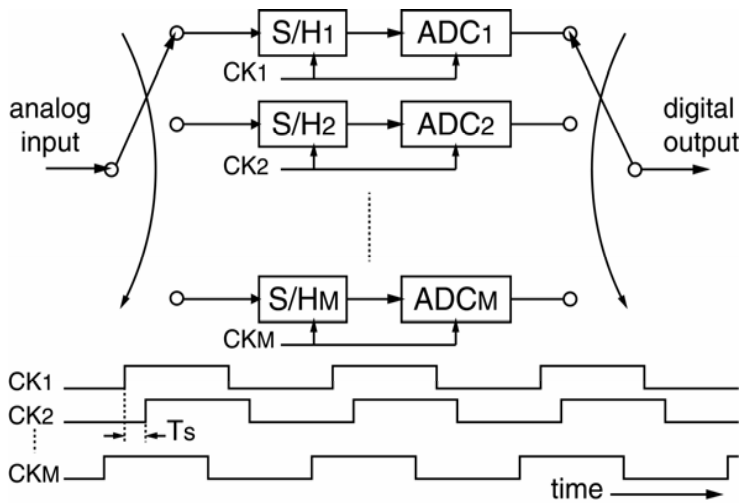
  has to be developed.

Phase noise testing takes long time and it is costly.

ATE for Mixed-Signal Testing

- Analog part is costly for development.
- Analog BIST is also beneficial
  for mixed-signal ATE manufacturer
- ATE must be designed with today's technology for next generation higher performance chip testing.

Interleaved ADC used in ATE
to realize very high sampling rate
with today's ADCs



Low Cost ATE

- Digital ATE
  - No analog option such as
    Arbitrary Waveform Generator: AWG
  - Input/output are mainly digital.
- Replacement of analog ATE
  with digital ATE
  - Multi-site testing becomes possible.
  - Still short testing time is important.
- Secondhand ATE

Cooperation among Engineers

- Collaboration is important
  - Circuit designer
  - LSI testing engineer
  - ATE manufacturer engineer
  - Management
  - LSI testing researcher in academia
- For example, analog BIST acceptance by circuit designer is needed.
- Strong background of analog circuit design as well as LSI testing is required for analog testing research.

Contents

Research Topics 1

Fast Testing of Linearity and
Comparator Error Tolerance of SAR ADCs

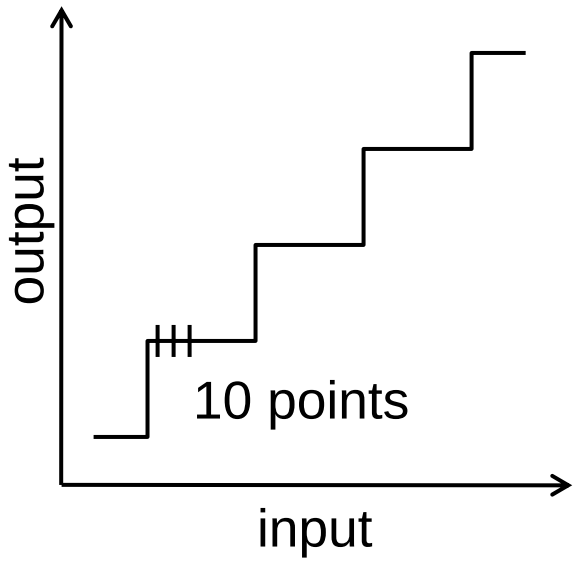
Presented at IEEJ International Analog VLSI Workshop
Chiangmai, Thailand (Nov. 2009).

SAR ADC DFT for short testing time

SAR ADC : Successive Approximation Register ADC
DFT: Design for Testability

Testing time of SAR ADC

- High resolution (10bit)
- Low sampling speed (1MS/s)
- DC linearity testing time



10 bit → 1024 LSBs

10 points / 1LSB

10240 points x 1us = 10 msec

→ 90 msec

x3 Vdd change

x3 Temperature change

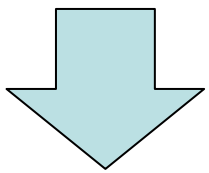
1$ chip → 1sec testing time is reasonable.

Mass volume → Even 1msec testing time reduction is significant for cost reduction.

Fast testing of SAR ADC DC linearity

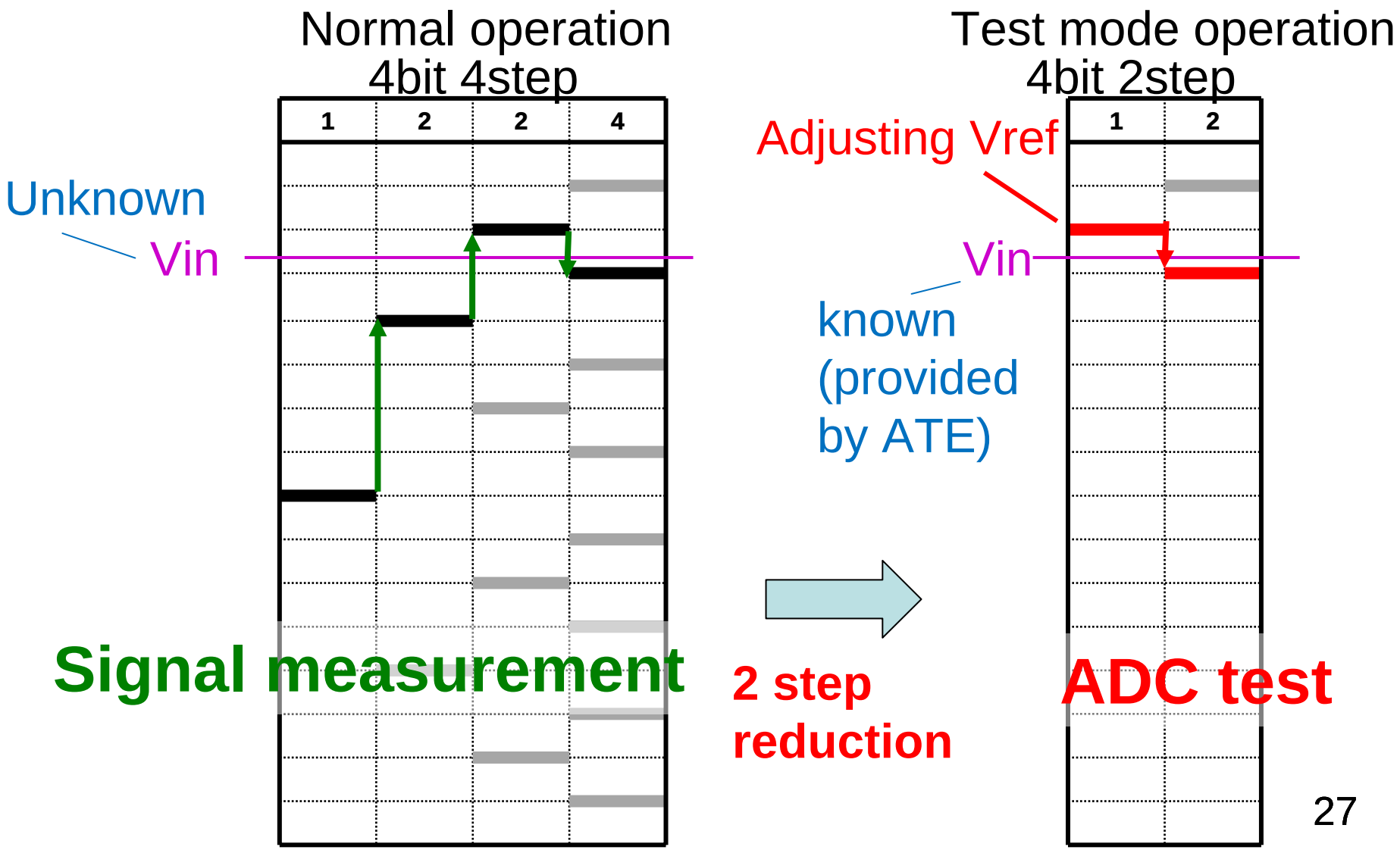
- DC linearity is the important testing item.
- Testing time reduction

  ⇨ cost reduction

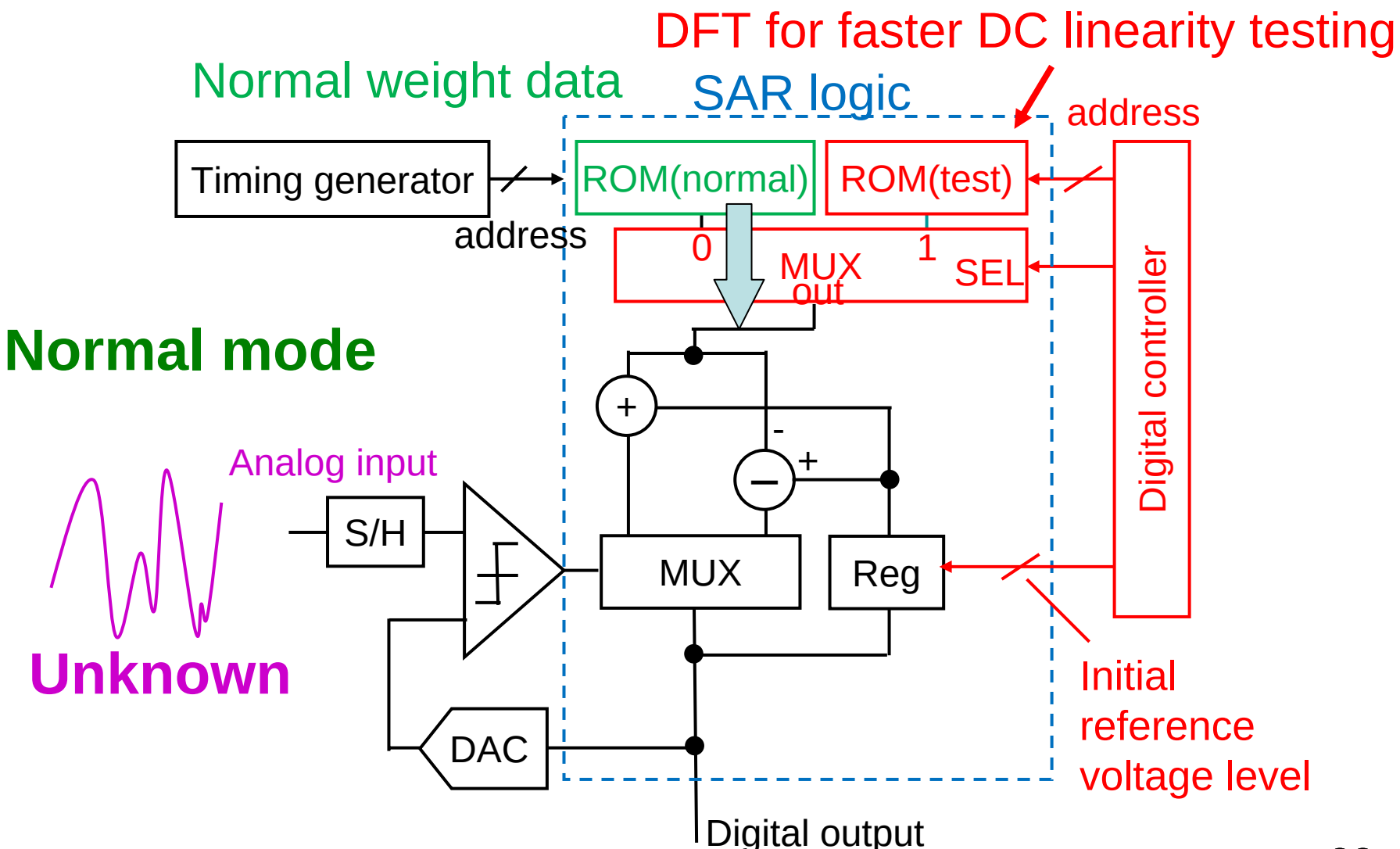


- The number of SAR conversion steps reduction during DC linearity testing.

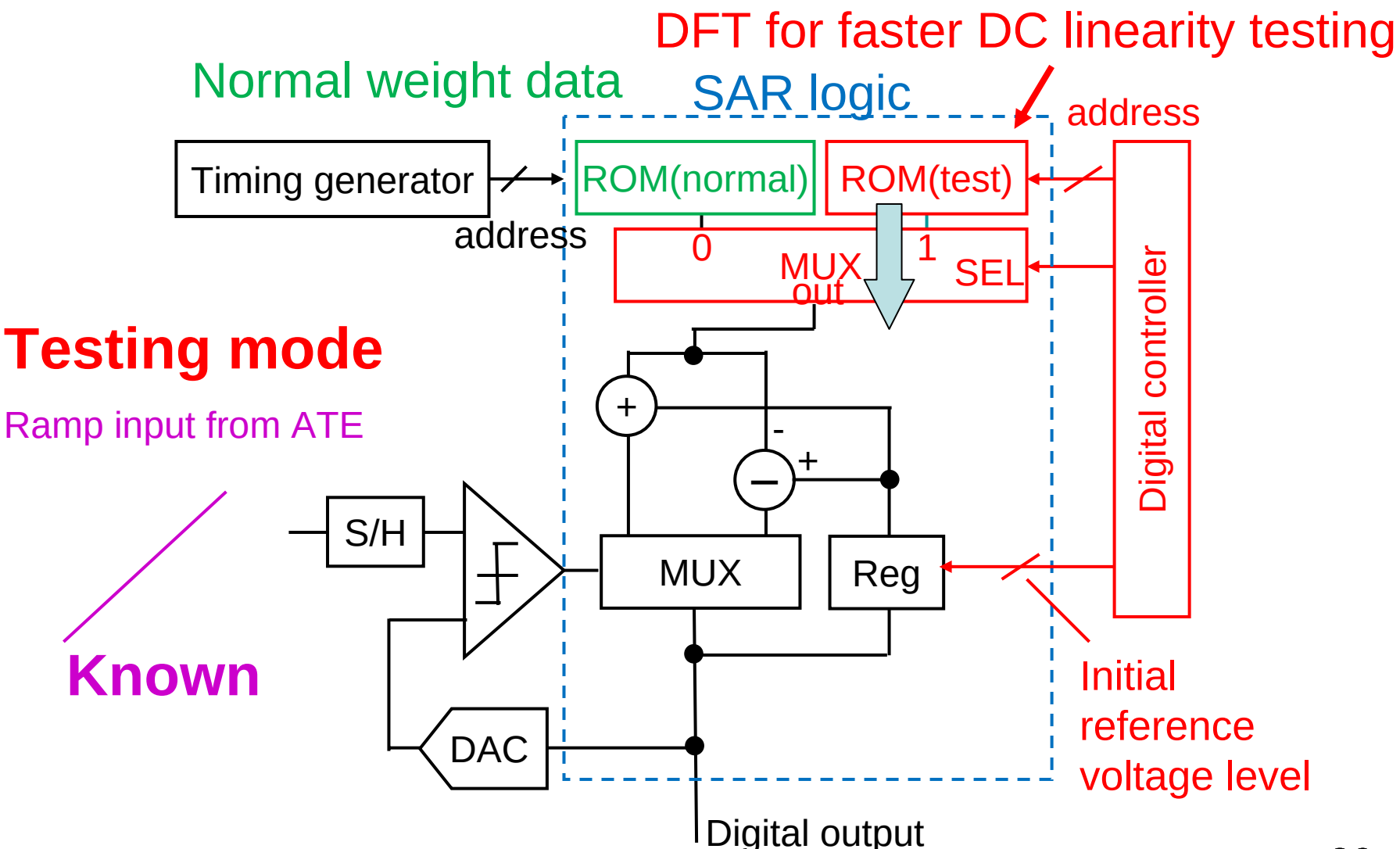
Operation of SAR ADC with DFT



SAR ADC Implementation with DFT

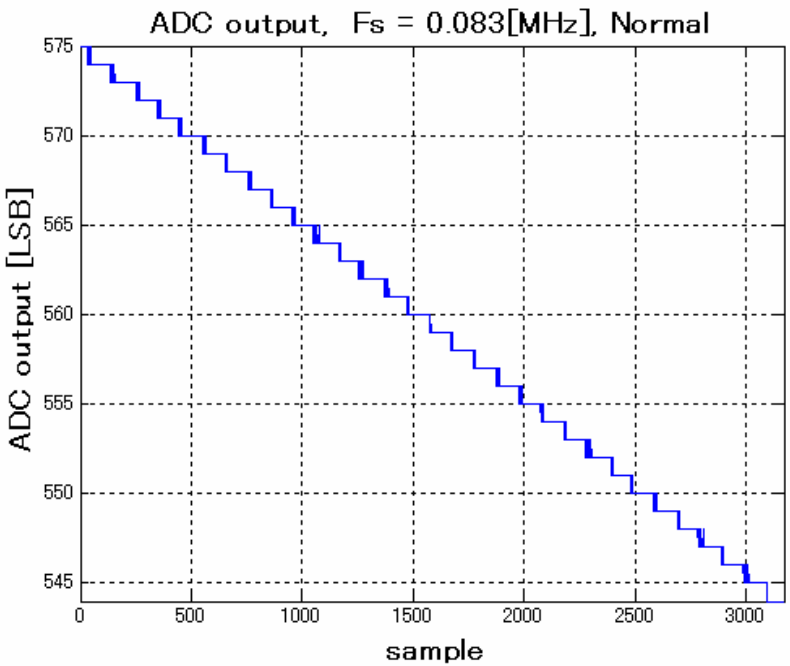


SAR ADC Implementation with DFT

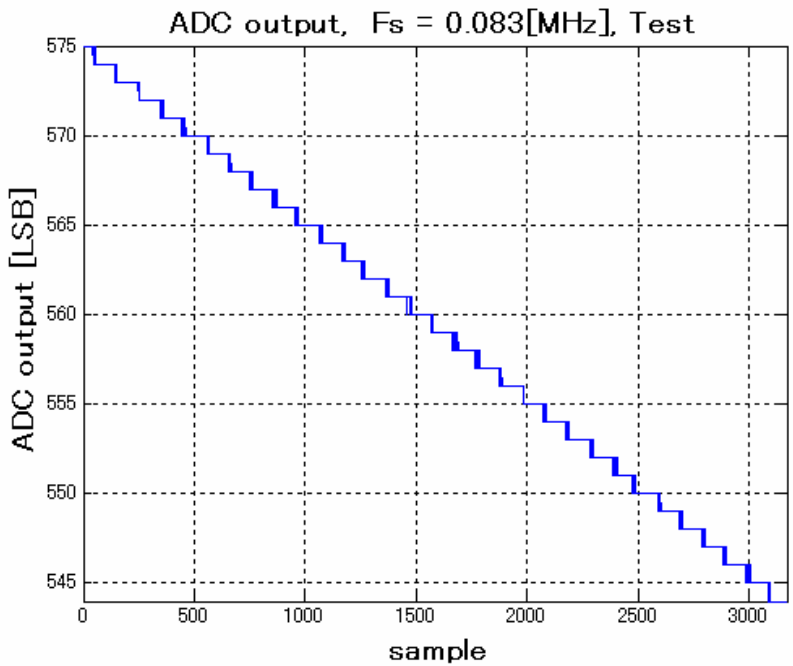


Measurement results of 10bit SAR ADC chip

10 steps normal binary operation



5 steps testing mode operation

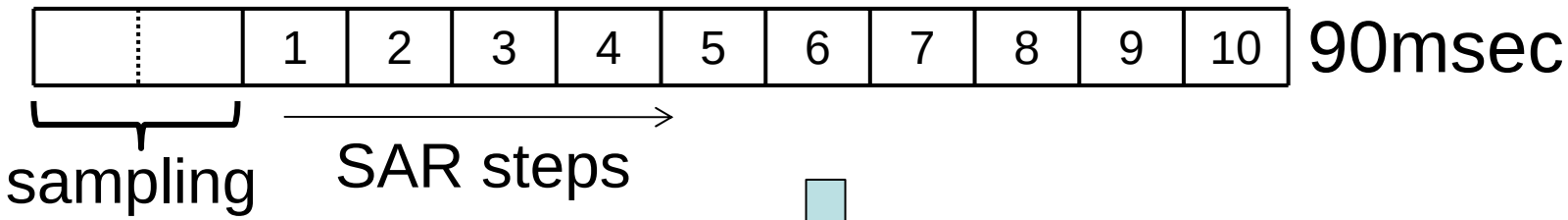


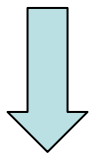
Results are equivalent.

The basic concept is validated.

Testing time reduction

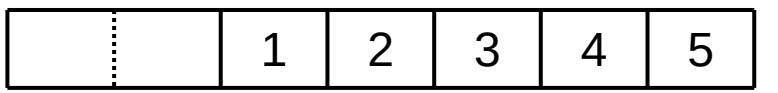
- Time of setup, settling : 10 msec
- Normal





5step reduction

- Proposed testing



- Data transfer and processing : 10 msec

Conventional : 110 msec

Proposed : 73 msec

33% reduction

Research Topics 2

A Practical Analog BIST

Cooperated with an LSI Tester

Published in IEICE Trans. Fundamentals (Feb. 2006)

Cooperation between BIST and ATE
for high-frequency signal measurement.

BIST for High-Frequency Signal Testing

- Target:

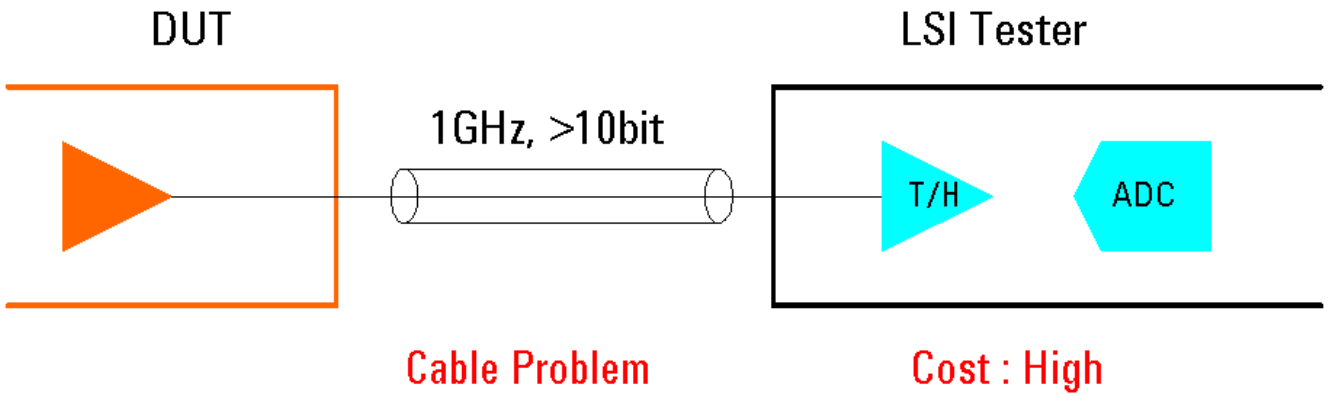
  To measure >1GHz signal with >10bit accuracy at low cost, for **SOC**.

- Cooperation with **ATE**

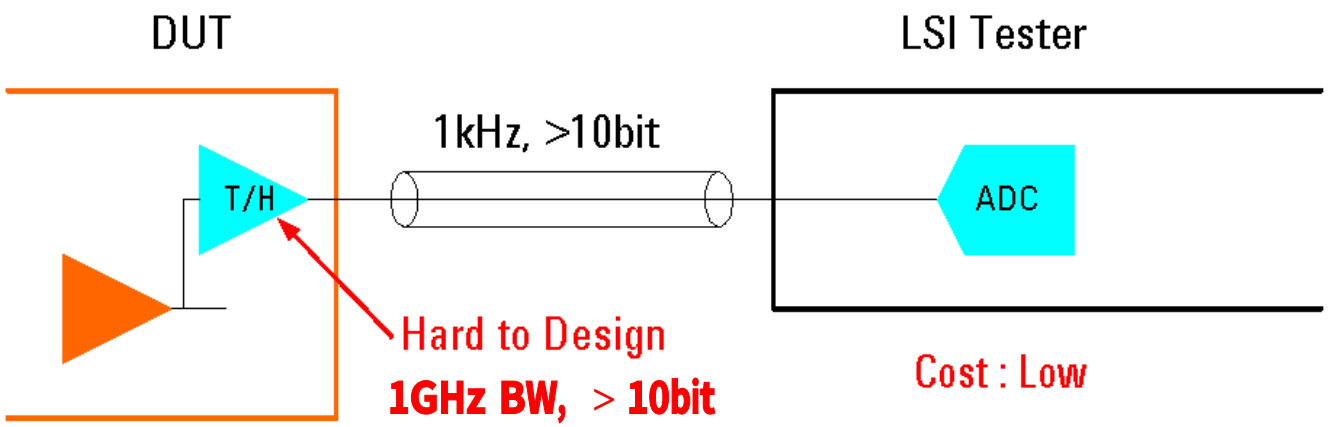
  - ATE provides repetitive input signals to DUT.
  - ATE generates DC signals with high accuracy.
  - ATE controls every timing of digital portion.

System Level Consideration for High-Frequency Signal Measurement

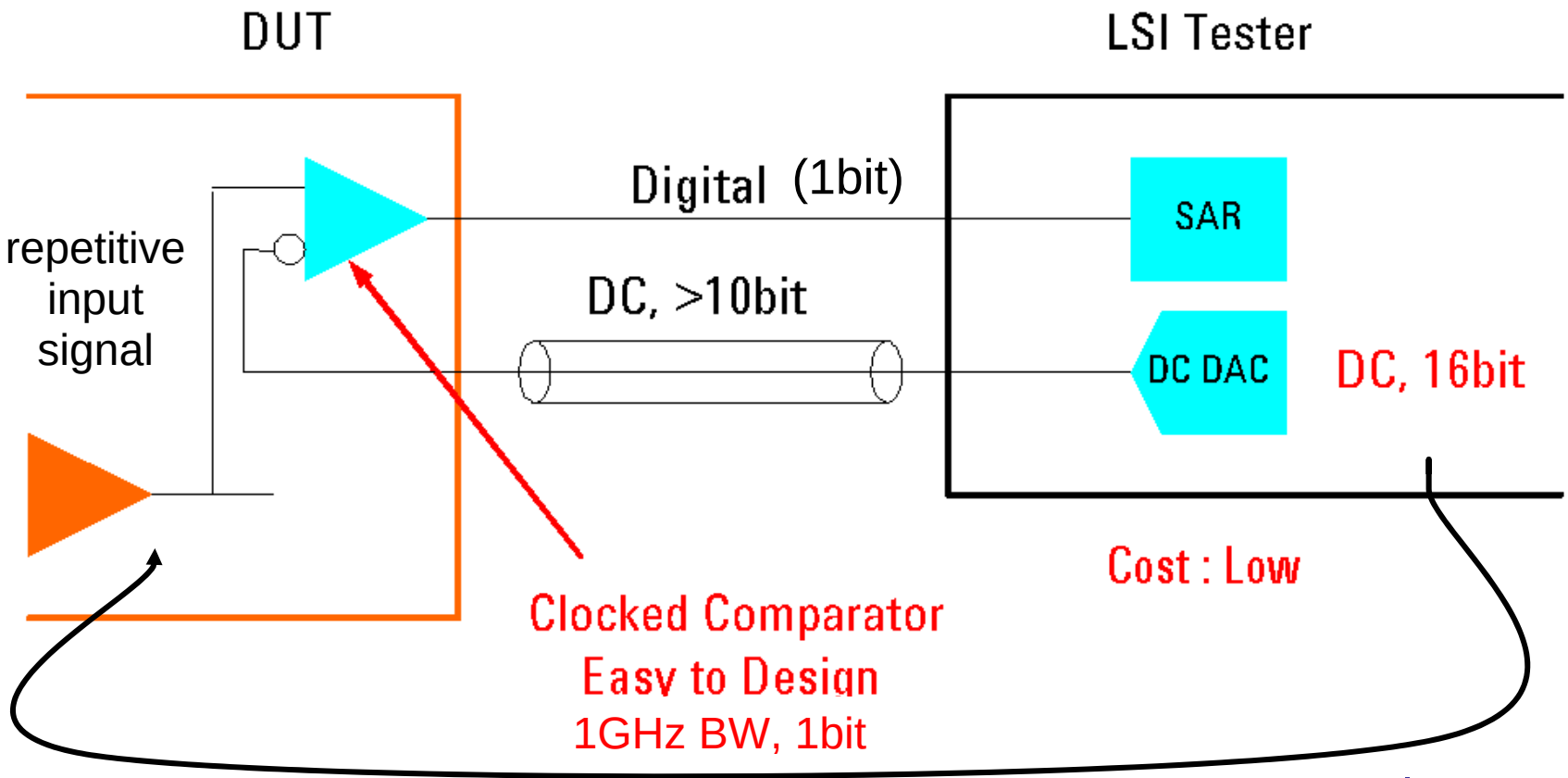
[Conventional Way]



[Sampler in DUT]



Proposed Method



- **Simple BIST in DUT**
- **Cooperation with ATE**

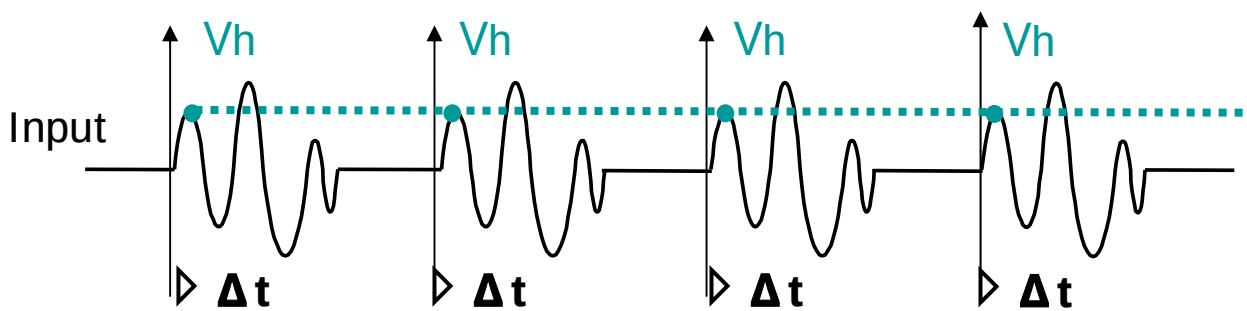
Control all inputs of SOC

This works as a modified SAR ADC

Repetitive Waveform Input Eliminates T/H Circuit

- Output signals from SOC can be repetitive by controlling all inputs to SOC with ATE.
- Proposed SAR ADC samples the input signal in the same phase of the repetitive waveform.

repetitive waveform

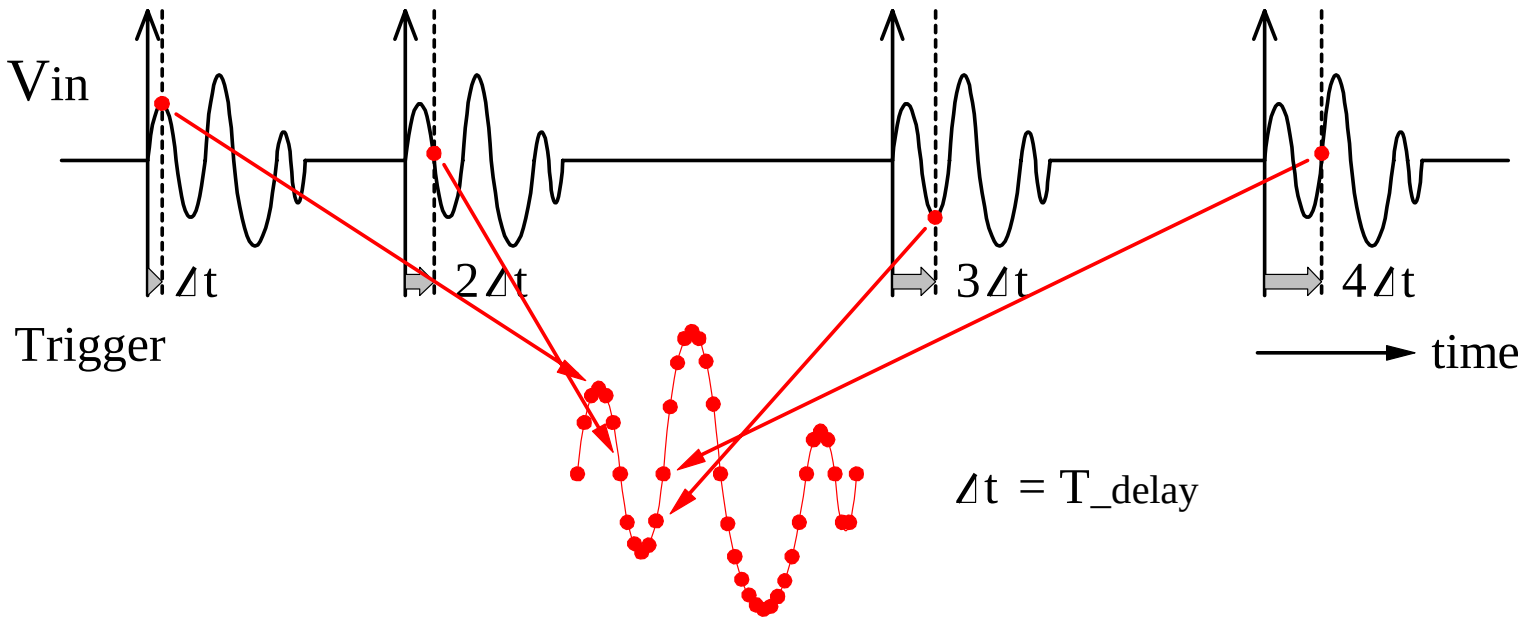


SAR ADC operation

1-step 2-step 3-step 4-step

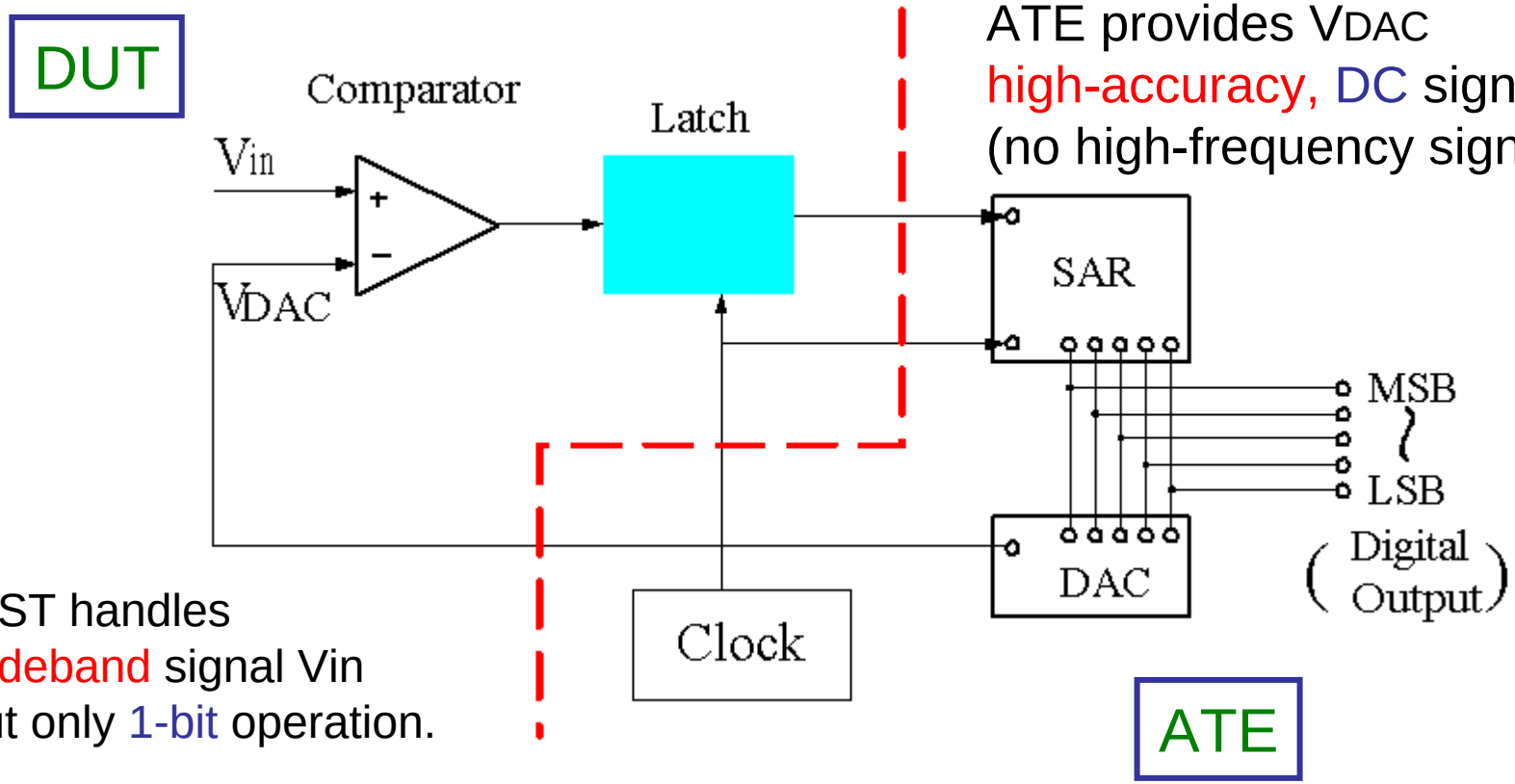
No need for wideband high-accuracy T/H circuit

Waveform Reconstruction by Equivalent-Time Sampling



Repetitive signal waveform reconstruction from measured points in different phases.

Proposed SAR ADC



Repetitive input signal Vin is compared with VDAC.

High-frequency measurement at low cost

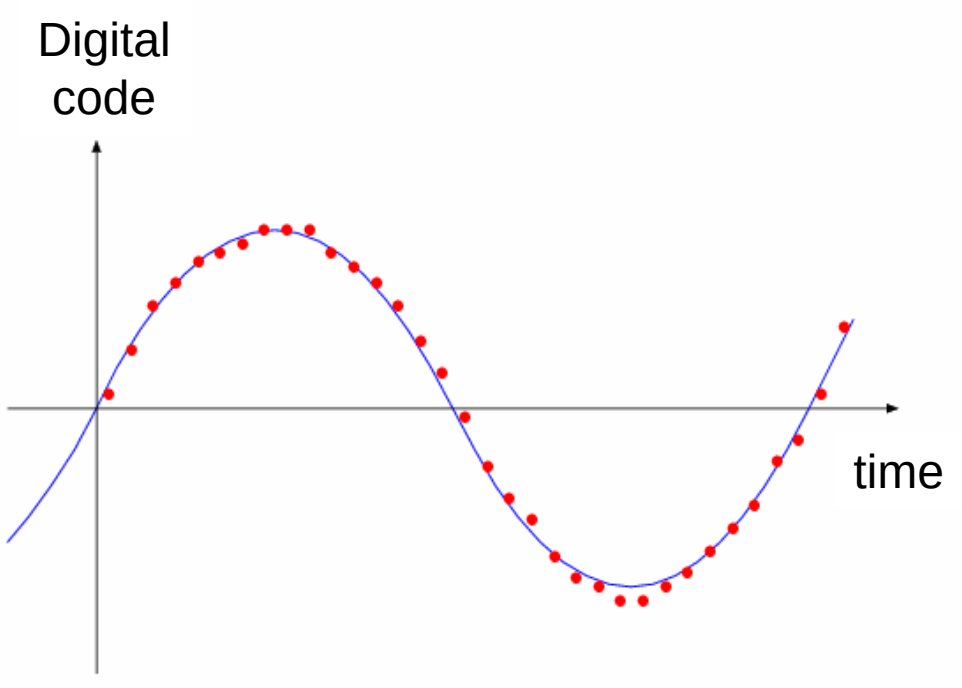
Research Topics 3

Multi-Tone Curve Fitting Algorithms
for Communication Application ADC Testing

Published in Electronics and Communication in Japan:
Part 2, Wiley Periodicals Inc. (2003).

ADC evaluation algorithm

Sine Curve Fitting Algorithm for ADC testing

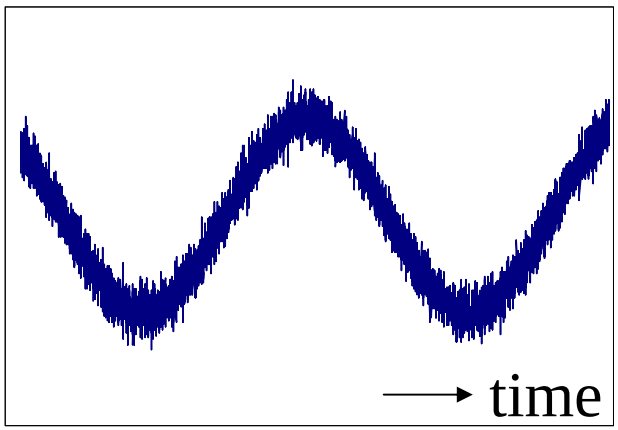


Estimate the signal component (-)
from the ADC output data (·) for a sinusoidal input

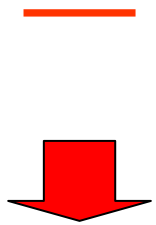
Window function is NOT required.

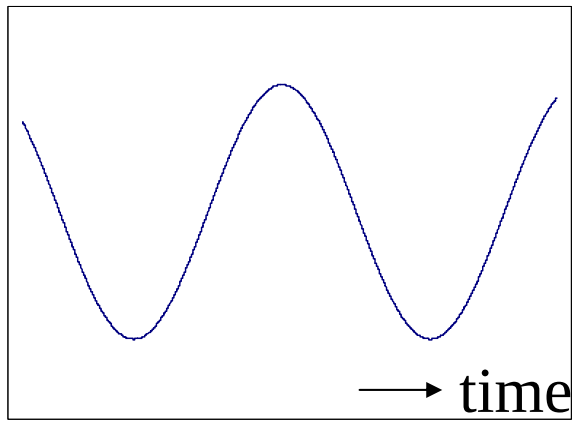
➡ High accuracy ADC testing

Extraction of Noise, Distortion Components

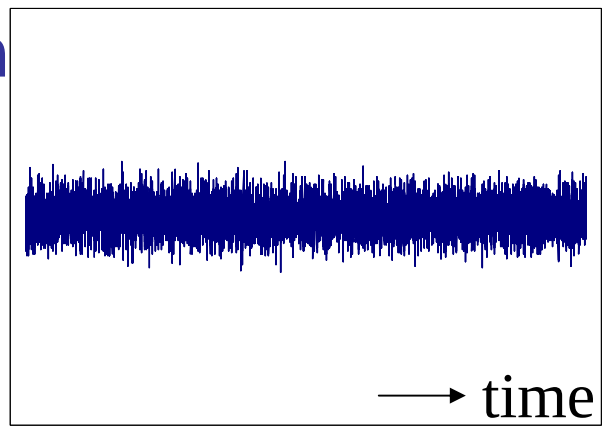


ADC Output Data





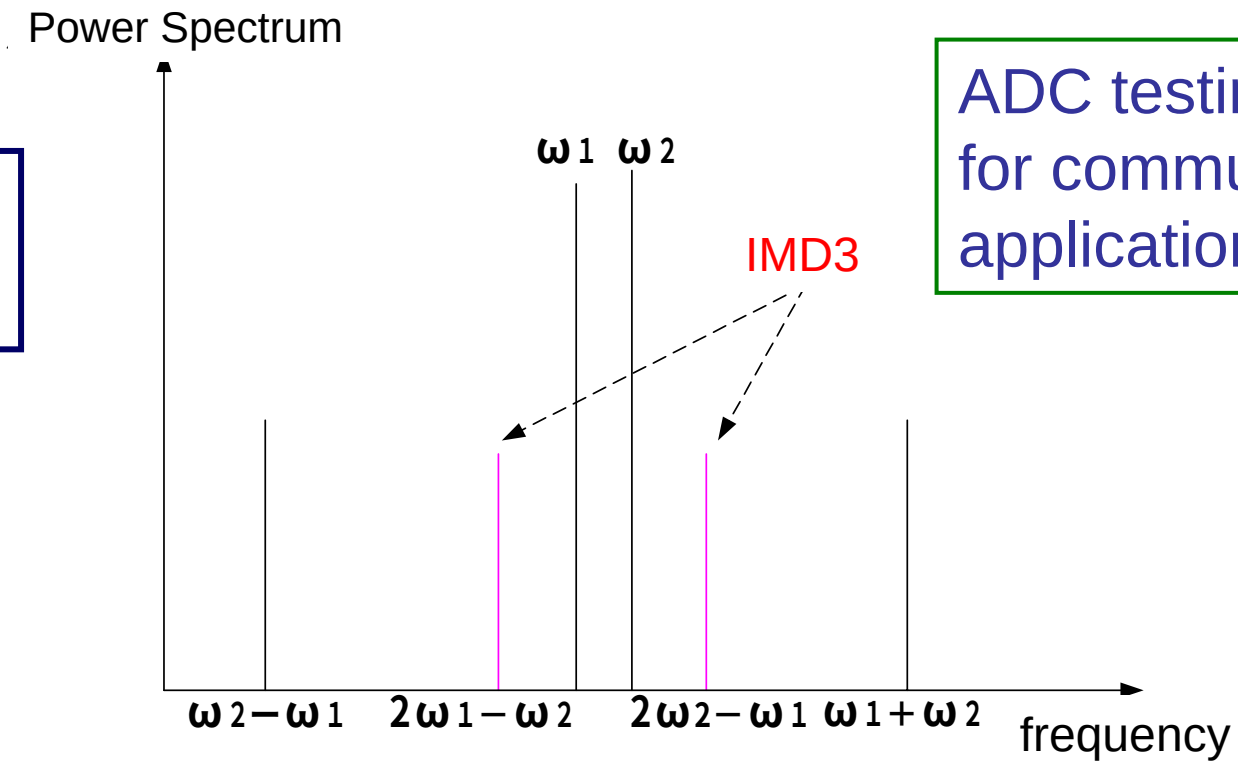
Estimated Signal



Noise, Distortion Components

Intermodulation Distortion (IMD)

Two-tone ADC testing Example 1



ADC testing item for communication applications

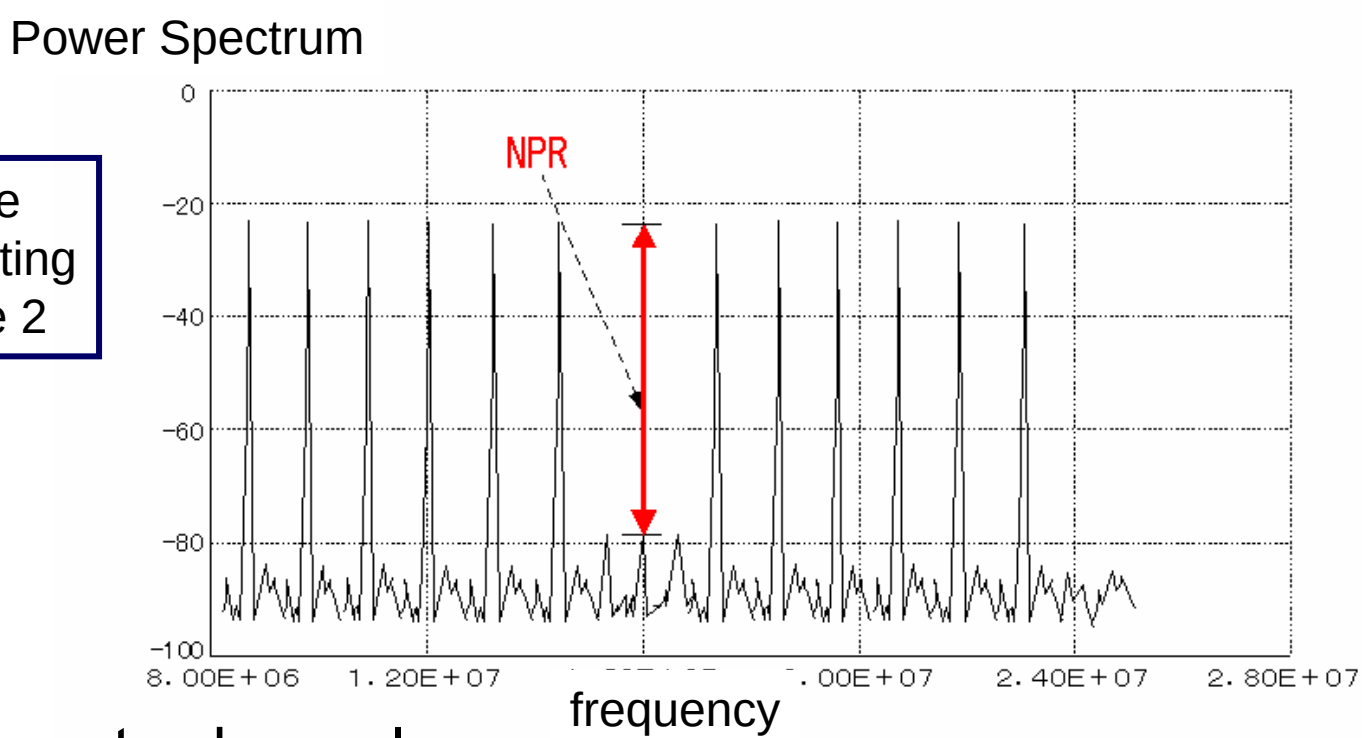
Input signal $A_1 \cos(\omega_1 t + \theta_1) + A_2 \cos(\omega_2 t + \theta_2)$

In case $\omega_1 \approx \omega_2$

IMD3 $2\omega_1 - \omega_2$, $2\omega_2 - \omega_1$ are in signal band.

Noise Power Ratio (NPR)

Two-tone
ADC testing
Example 2



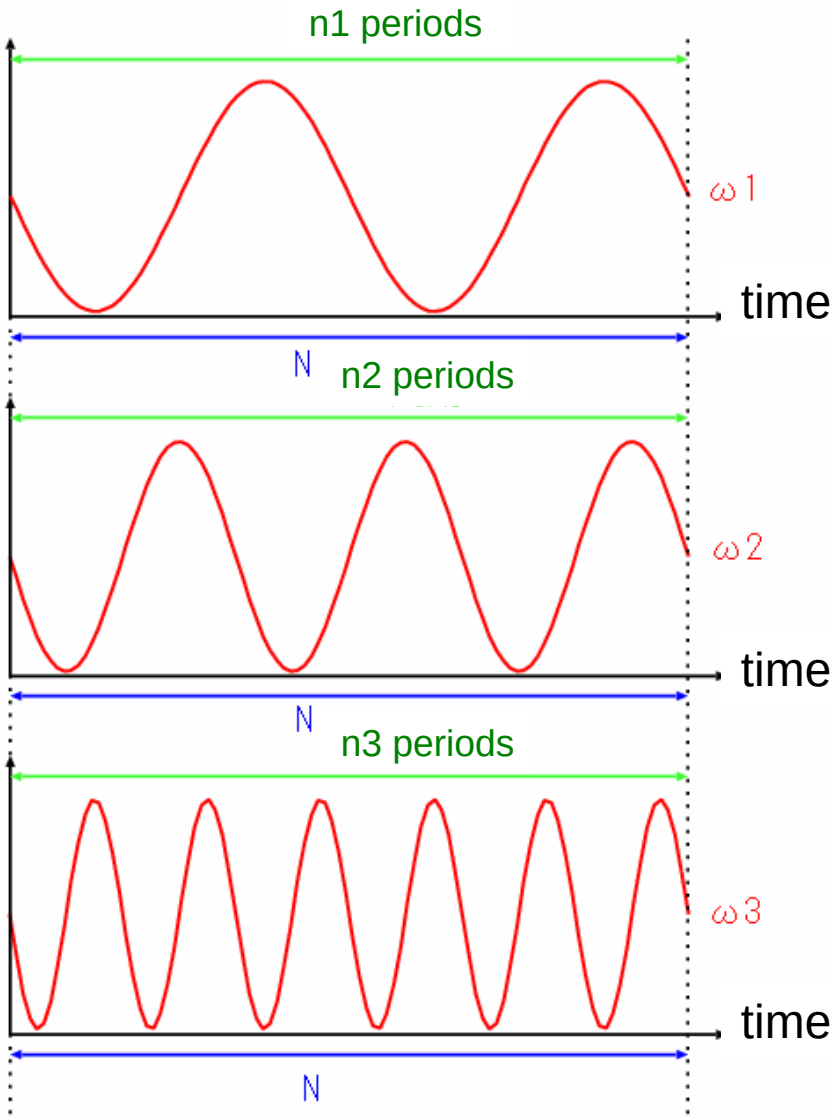
One empty channel

The other equally spaced active channels

⇨ Distortion components enter into the empty channel.

ADC testing item for ADSL

FFT Method in Multi-tone Test



N-point FFT

When $\omega_1/\omega s = n_1/N$,

$\omega_2/\omega s = n_2/N$,

$\omega_3/\omega s = n_3/N$,…

are satisfied,

window is NOT required.

↓

This condition is hard to satisfy.

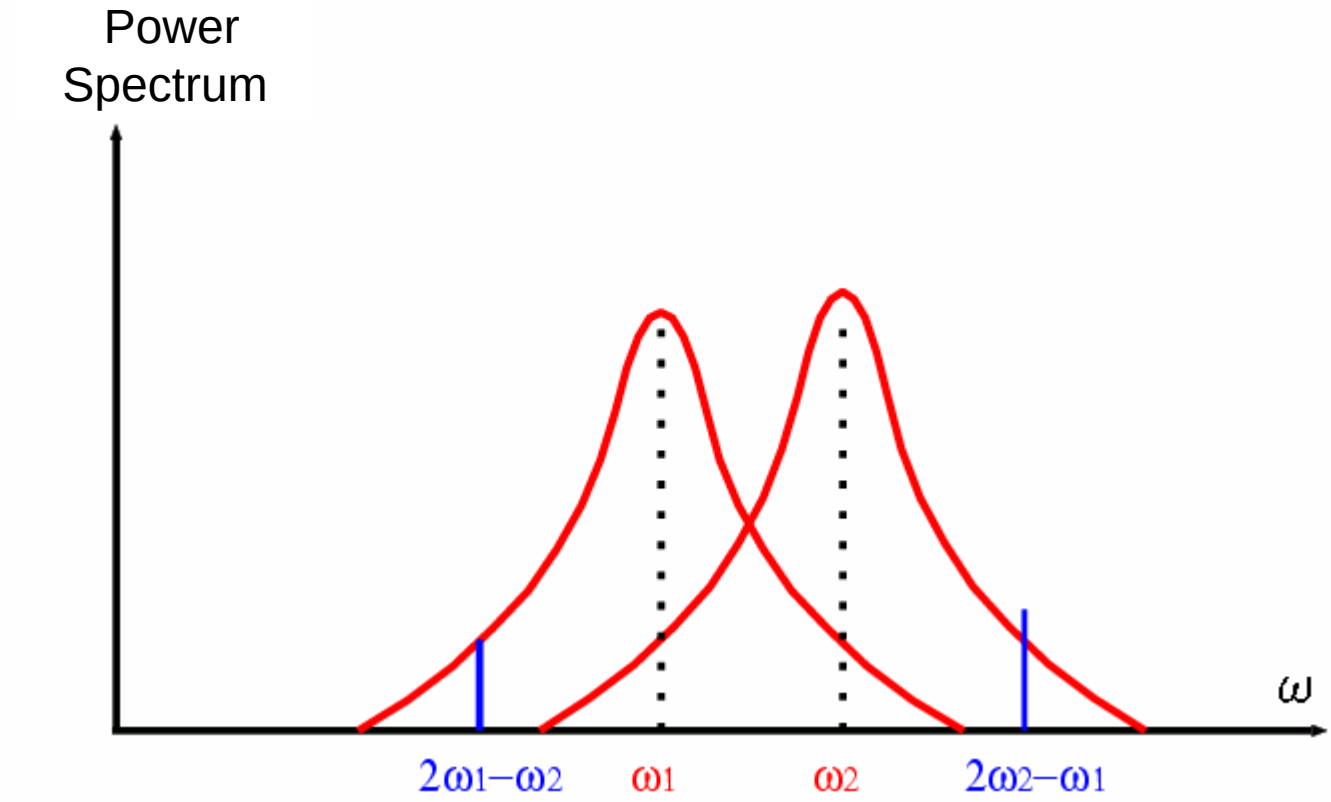
↓

Window function is required.

↓

Measurement accuracy degrades.

IMD3 Testing & Window



Spectrum has skirts when window function is used.

IMD3 testing is difficult

Two-tone Curve Fitting Algorithm

- ADC output data : $y_0, y_1, y_2, \cdots y_{N-1}$
- Least Mean Square (LMS) criterion:

  Estimate A_1, ω_1, θ_1, A_2, ω_2, θ_2, C

$$\varepsilon := \sum_{k=0}^{N-1} [y_k - m_k]^2$$

$$= \sum_{k=0}^{N-1} [y_k - A_1 \cos(\omega_1 k + \theta_1) - A_2 \cos(\omega_2 k + \theta_2) - C]^2 \rightarrow \min$$

- This cannot be solved analytically.

We have derived numerical calculation algorithm.

$$\mathbf{x}_{(n+1)} = \mathbf{x}_{(n)} + \mathbf{F}_{(n)}^{-1} \mathbf{y}_{(n)}$$

Simulation Results for [two-tone + noise] input

$$y(k) = A_1 \sin(2\pi \frac{\omega_1}{\omega_s} k + \theta_1) + A_2 \sin(2\pi \frac{\omega_2}{\omega_s} k + \theta_2) + n_a$$

N=8192

n_a: noise (σ=0.125)

	Actual value	Estimated
$\omega 1/\omega s$	2.2×10^{-4}	2.200×10^{-4}
$\omega 2/\omega s$	5.8×10^{-4}	5.798×10^{-4}
A1	1	1.0011
A2	1	1.0001
θ 1[deg]	45	44.8025
θ 2[deg]	90	90.2496

(a) Proposed algorithm

	Actual value	Estimated
$\omega 1/\omega s$	2.2×10^{-4}	2.120×10^{-4}
$\omega 2/\omega s$	5.8×10^{-4}	5.920×10^{-4}
A1	1	0.9650
A2	1	0.9663
θ 1[deg]	45	59.1427
θ 2[deg]	90	74.3681

(b) Conventional algorithm

Research Topics 4

Production Test Consideration
for Mixed-Signal IC
with Background Calibration

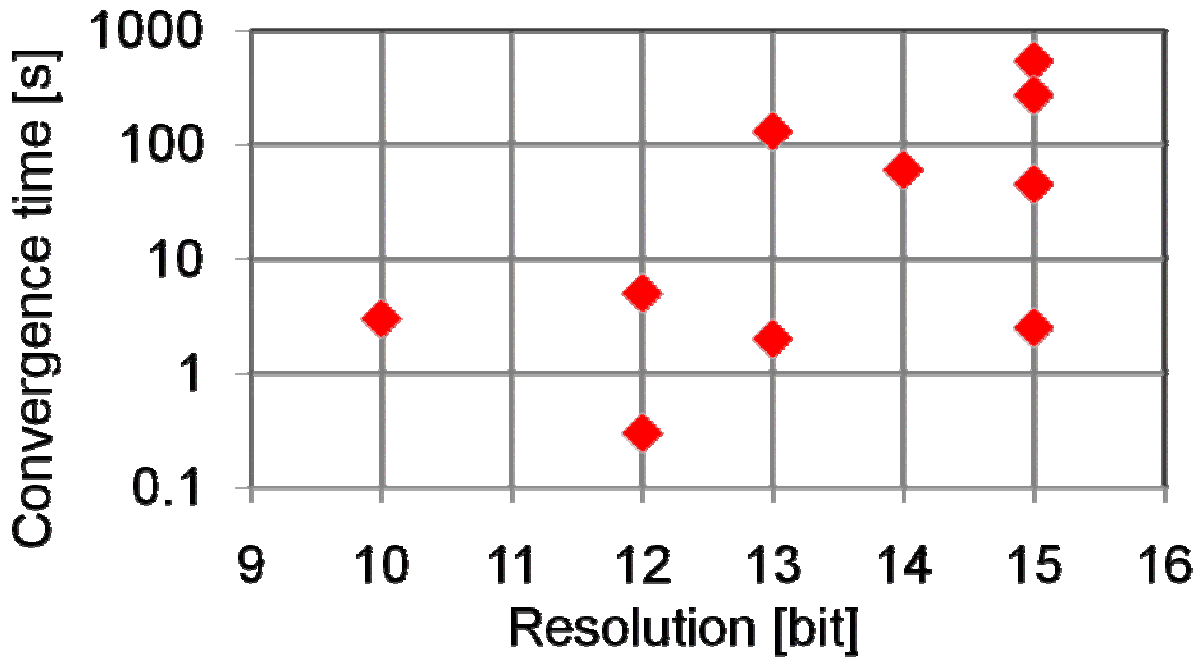
Presented at IEEJ International Analog VLSI Workshop
Chiangmai, Thailand (Nov. 2009).

Testing time reduction of background calibration IC

Digitally-Assisted Analog Circuit Test

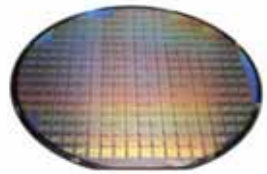
- Background calibration time → Long

[Pipelined ADC with calibration research paper in recent years]

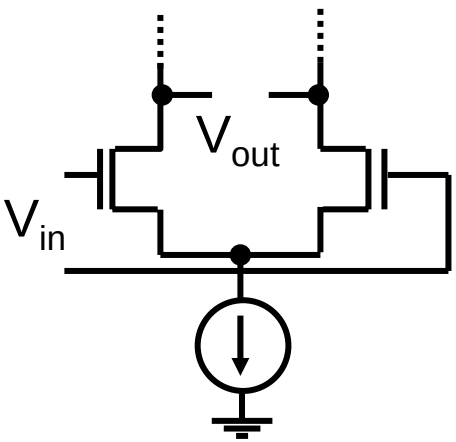


- Total testing time = Background calibration time + Functional testing time
- Long testing time → increase testing cost

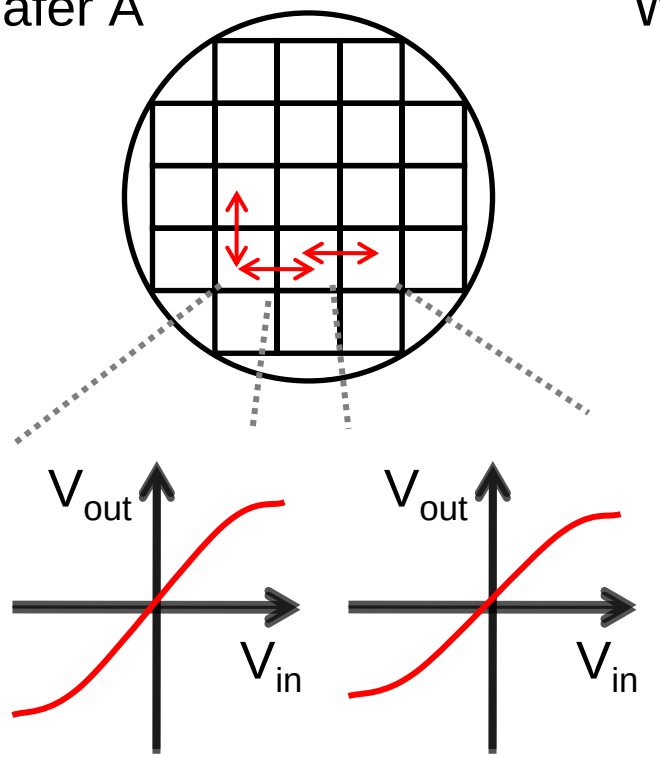
Correlation among Chips within the Same Wafer



Ex.)
Nonlinear Amplifier

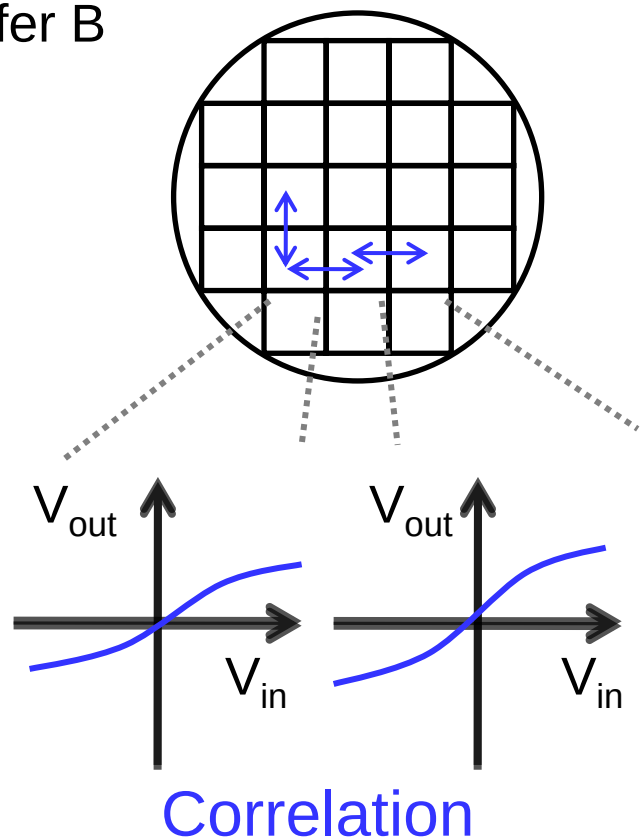


Wafer A



Correlation

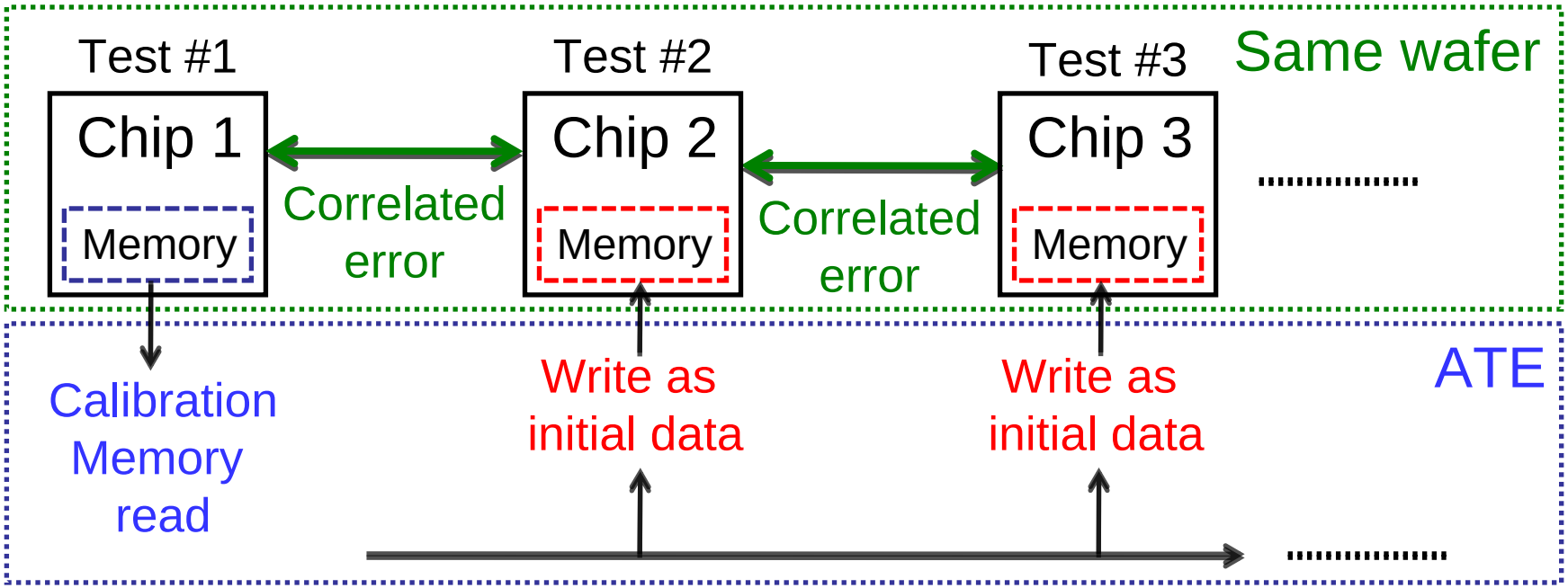
Wafer B



Correlation

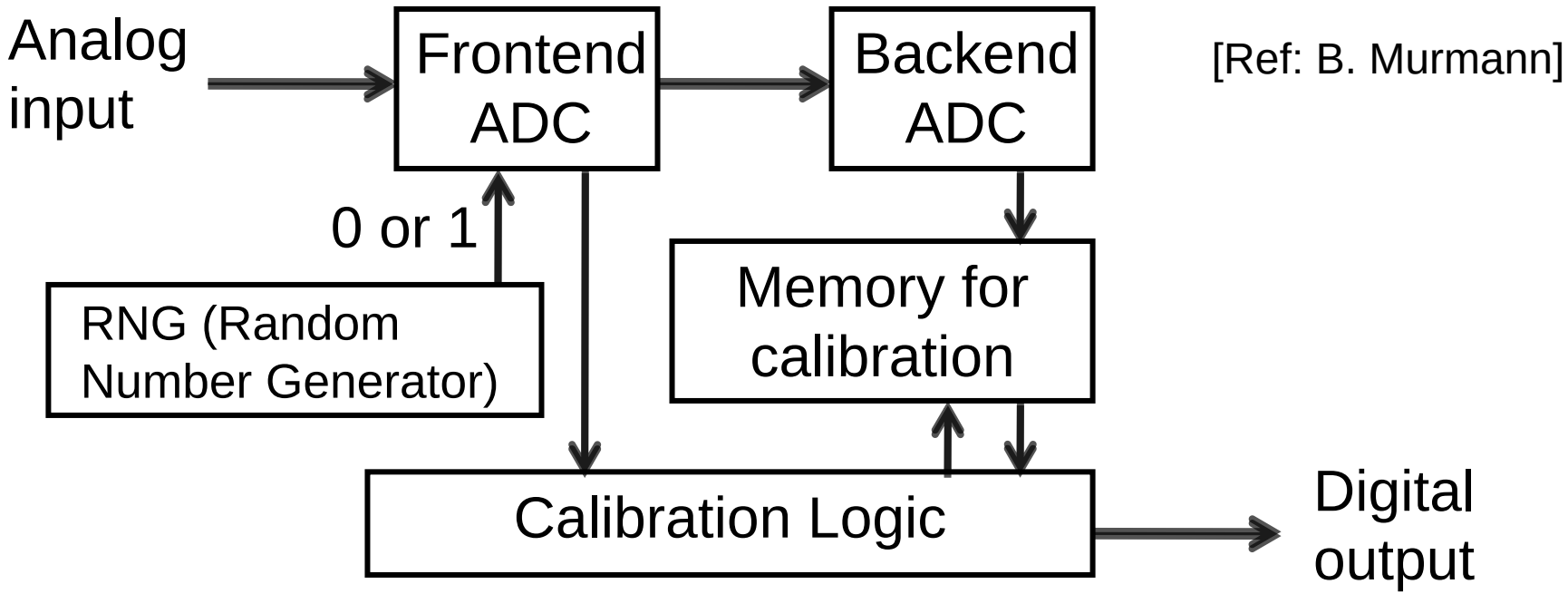
- Use strong correlation among die-to-die nonidealities
- Converged calibration parameter values would be close among chips within the same wafer

Proposed Algorithm for Calibration Time Reduction during Test



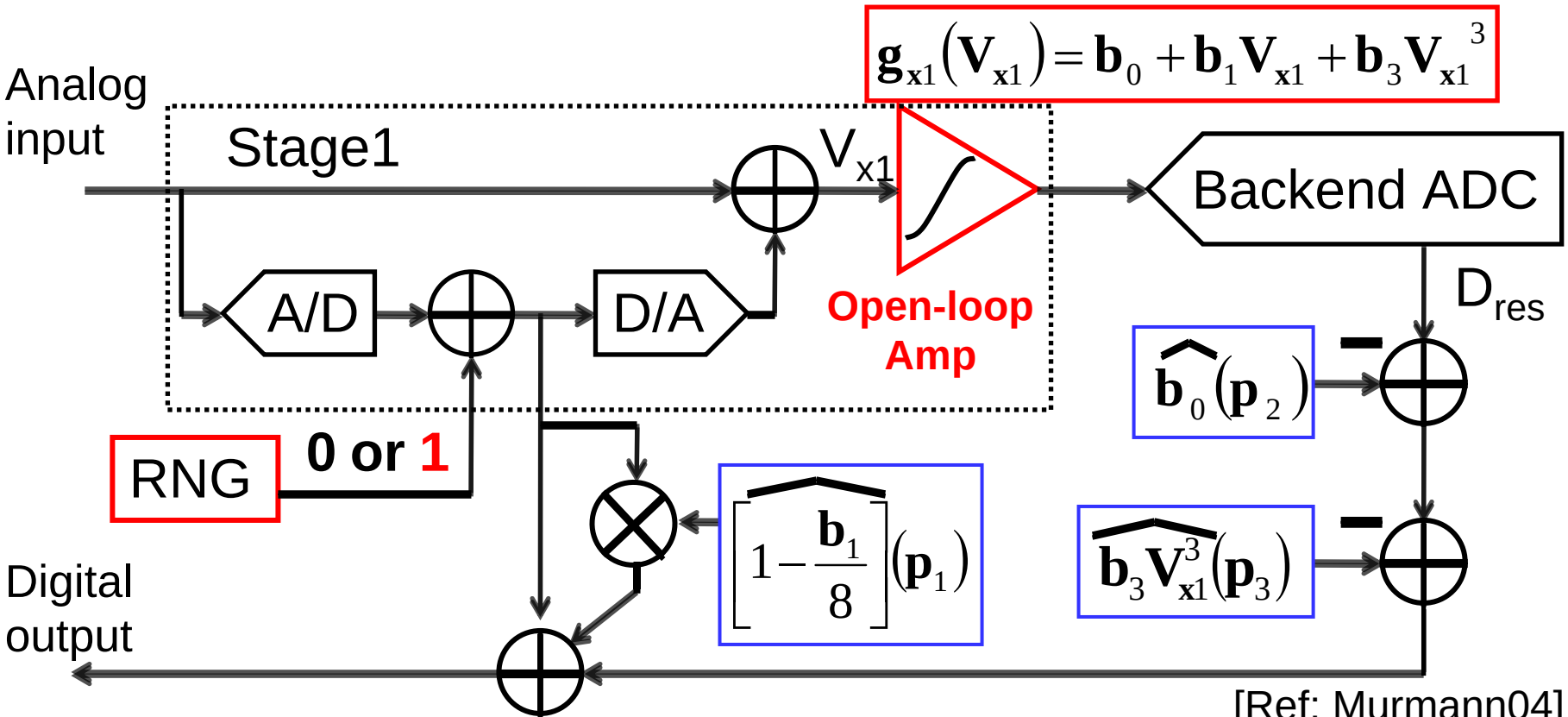
- ATE reads converged calibration data from memory of chip1
- Load them to memory of chip2, chip3 … as their initial data
- Calibration of chip2, chip3 … converges quickly

Case Study:
Pipelined ADC with Open-Loop Amplifier



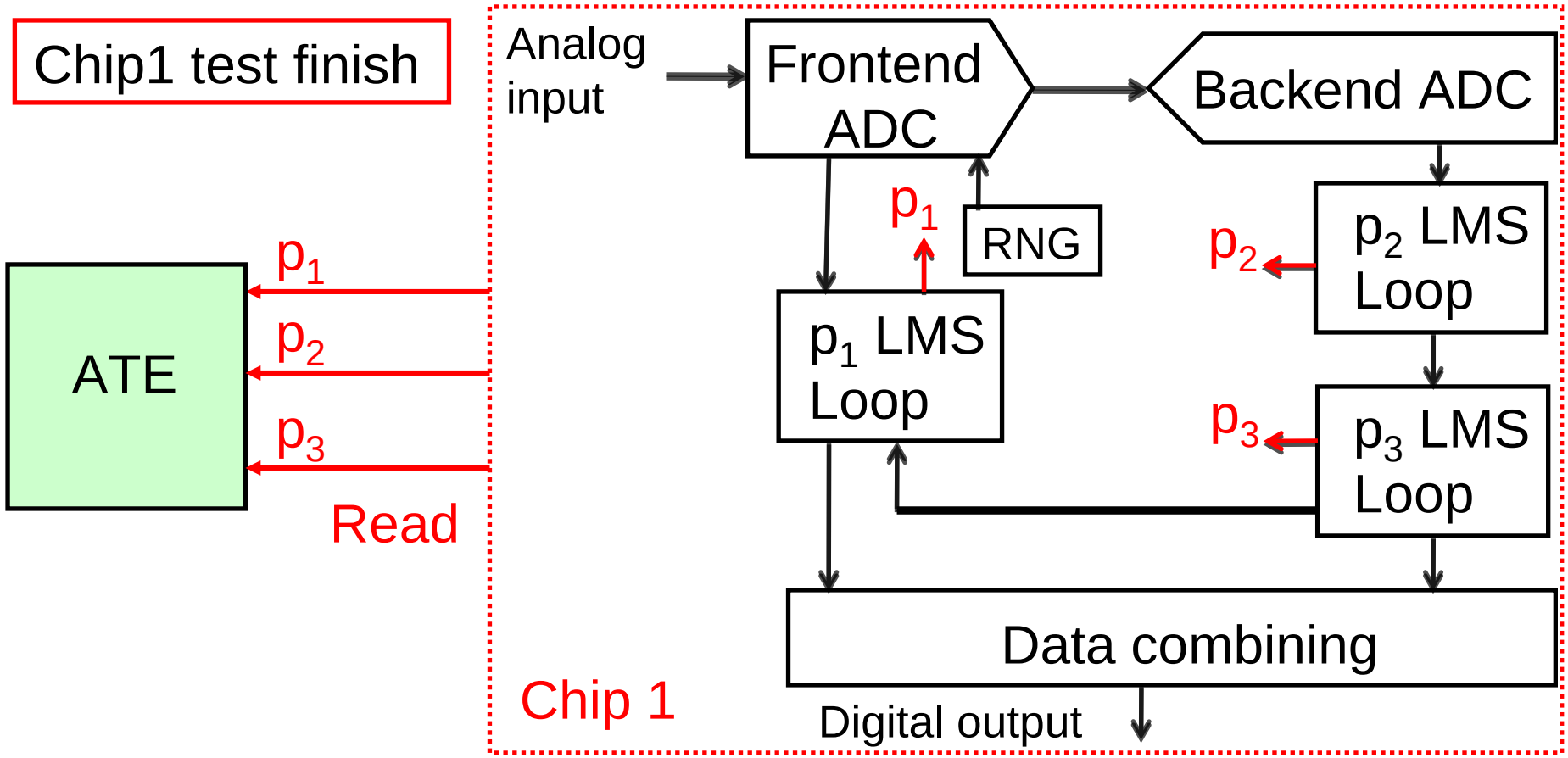
- Use open-loop amplifier in front-end ADC
  - ✓ High speed + low power
  - ✓ Amplifier Nonlinearity
    - ↳ Digital background calibration

Digital Calibration of Amp Nonlinearity



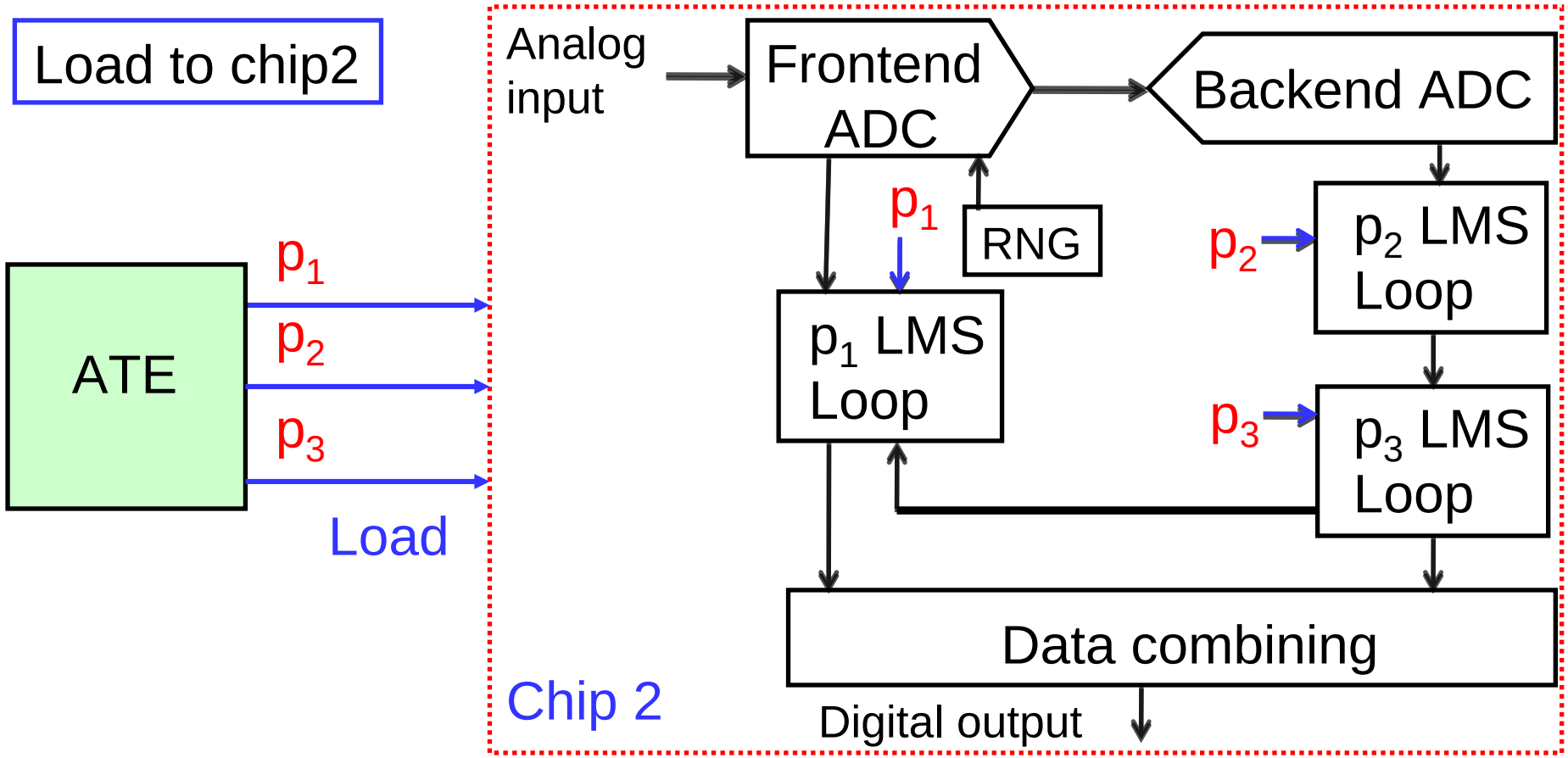
- p_1, p_2 and p_3 : 1st ,offset and 3rd order correction parameters
  - ✓ Estimated by "Distance Estimation"
  - ✓ Background calibration using LMS loop (LMS: Least Mean Square)

Apply Proposed Algorithm to Digitally-Assisted Pipelined ADC



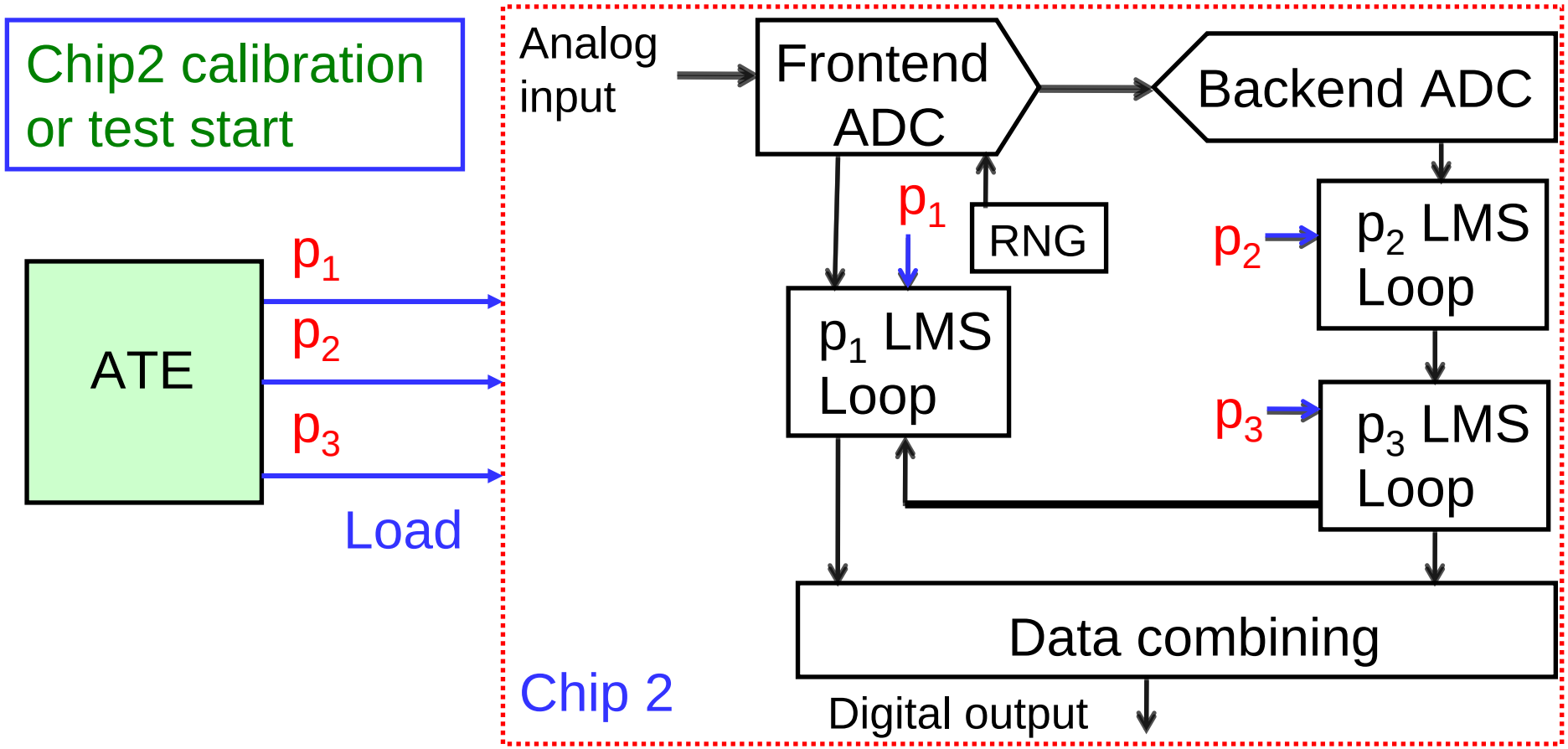
- ATE reads converged parameters p1, p2 and p3 of chip1
- Load them to registers of chip2 as their initial data

Apply Proposed Algorithm to Digitally-Assisted Pipelined ADC



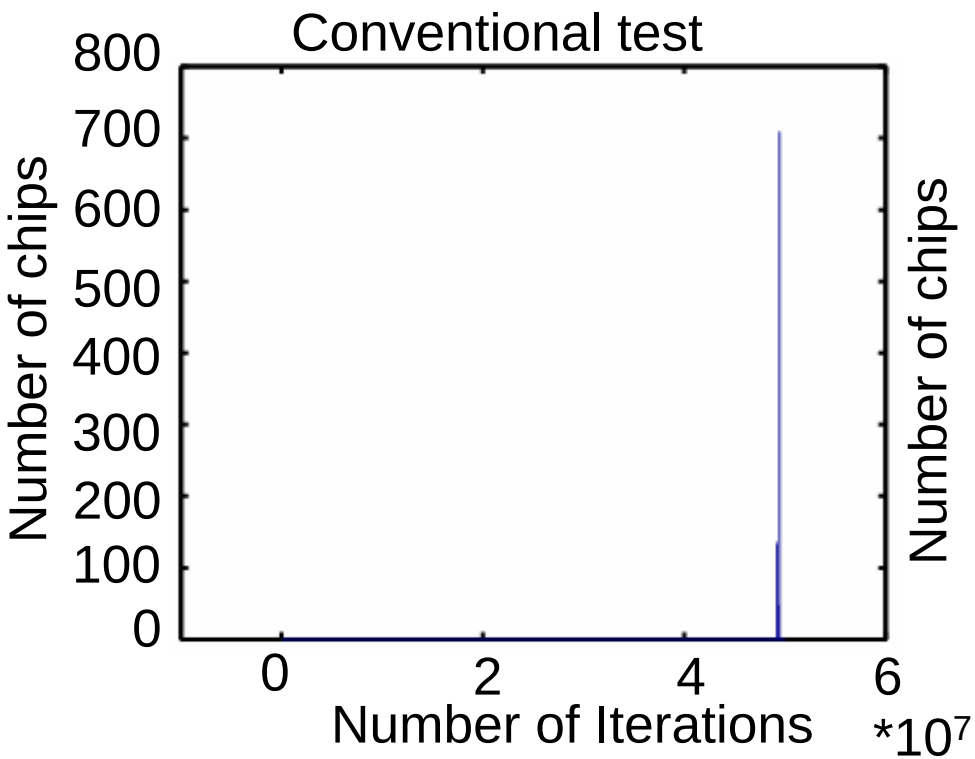
- ATE reads converged parameters p1, p2 and p3 of chip1
- Load them to registers of chip2 as their initial data

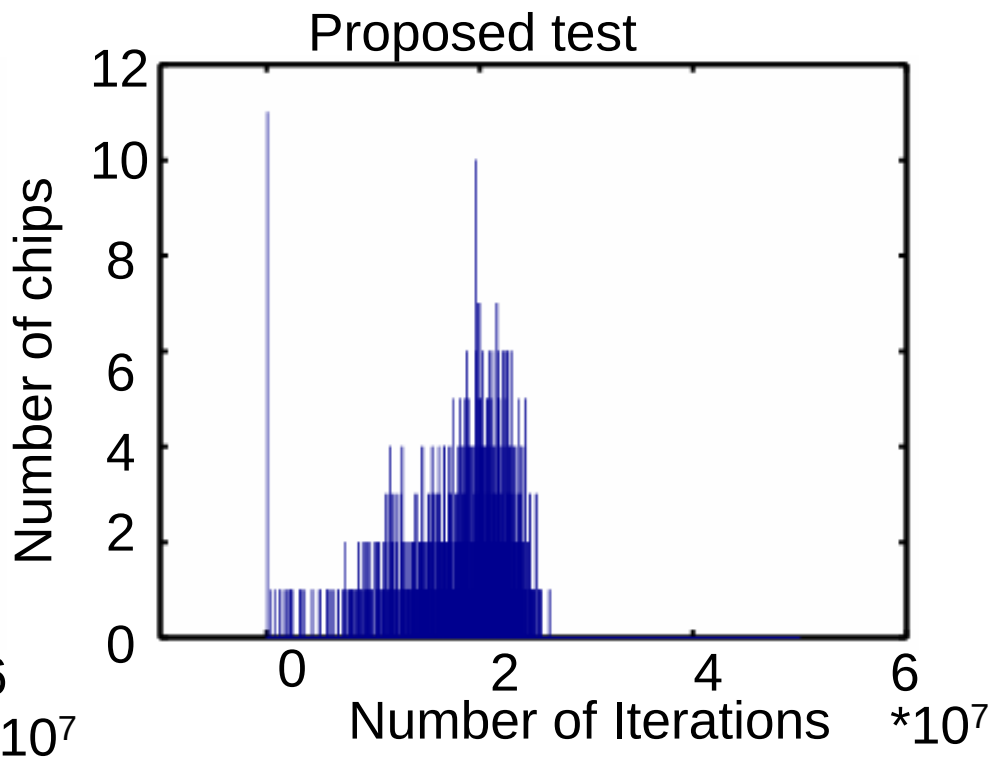
Apply Proposed Algorithm to Digitally-Assisted Pipelined ADC



- ATE reads converged parameters p1, p2 and p3 of chip1
- Load them to registers of chip2 as their initial data

Comparison of Convergence Time





- Conventional test : ~ $5*10^7$ iterations
- Proposed test : ~ $2.5*10^7$ iterations (Worst case)
  - ✓ Convergence time reduction by 1/2 during test

Contents

Challenges of Analog Testing

- Analog part testing is important
  for mixed-signal SOC cost reduction.
- Cost is the most important criterion.
- Its research is not easy.
- Analog BIST technique progress
  may be slow but it is steady.
- Solve the problems one by one.
  No general or systematic method
- Should be practical
- Use engineering sense, as well as science

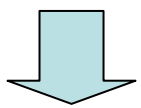
Challenges of Analog Testing

- Use all aspects of technologies
  - Circuit technique
  - Cooperation among BIST, BOST & ATE
  - Signal processing algorithm
  - Use resources in SOC

    such as μP core, memory, ADC/DAC

BOST:
Built-Out Self-Test

Especially utilization of powerful digital in SOC.



Digitally-assisted analog & RF testing projects are underway in my laboratory.

No royal road to analog testing

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