Timing Error Analysis in Digital-to-Analog Converters
- Effects of Sampling Clock Jitter and Timing Skew (Glitch) -

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Abstract

This paper describes two timing nonideality issues of Digital-to-Analog Converters (DACs); sampling clock jitter and clock skew effects. (i) A formula for the output error power due to sampling clock jitter is derived, and this has been validated by numerical simulation; spectrum characteristics of jitter-related noise are also examined. We have also found that when an analog lowpass filter follows the DAC and only the noise power inside the signal band is considered, increasing jitter and increasing input signal frequency degrade the DAC SNR. (ii) The clock timing skew inside the DAC causes glitch impulses. We try to characterize them by simulation and we have found the followings; as the input frequency increases, the effects of the glitch on the DAC SNR decrease. The effects of the glitch due to upper bits on the DAC SNR and SFDR are more significant than due to lower bits. Also glitch power is mainly located at the odd-multiple frequencies of the input signal.
Keywords: DAC, Sampling, Jitter, Clock Skew, Glitch

1 Introduction

Digital-to-Analog Converters (DACs) are essential components in communication systems (such as transceivers) and measuring instruments (such as arbitrary waveform signal generators), and higher sampling speed is being demanded of them [1, 2, 3]. For such DACs with high sampling speed, the effects of timing error may be crucial, and in this paper we have investigated two timing error issues: sampling clock jitter and clock timing skew inside the DAC. These nonidealities of DACs have not been well characterized even though those of Analog-to-Digital Converters (ADCs) and sampling circuits have been [5, 6]. In this paper we analyze these effects in theory and by numerical simulation.

2 Sampling Clock Jitter Effects

2.1 DAC Output Error Power due to Sampling Clock Jitter

A. Problem Formulation : Fig.1 shows a DAC with a digital input $V_{in}(n)$ applied, and sampling clock is CLK. Ideally the sampling clock CLK operates with a period of T_s for every cycle, however in reality its timing can fluctuate which is called clock jitter or phase noise (Fig.2) [7]. If we denote clock jitter as ϵ_n, then the n-th sampling timing of CLK is $nT_s + \epsilon_n$ instead of nT_s. Since the jitter ϵ_n is sufficiently smaller than the sampling period of T_s in most practical situations, we assume that

$$-\frac{T_s}{2} < \epsilon_n < \frac{T_s}{2}. \tag{1}$$

Also we assume that the DAC has sufficiently good resolution that quantization can be neglected, and that the DAC output $V_{out}(t)$ is zero-order hold [3]. Then Fig.3 shows the DAC outputs with an ideal clock (no jitter) and with a real clock (with jitter) while Fig.4 shows the DAC output error due to clock jitter.

B. Formula for Error Power due to Jitter : The DAC output error power P_e due to the sampling clock jitter is defined as follows:

$$P_e := \lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} e_n^2 |\epsilon_n| \tag{2}$$

Here e_n is the DAC output error due to jitter (see Fig.4). If the input signal $V_{in}(t)$ and the sampling jitter are not correlated (which is the case in general), ϵ_n and e_n are independent and we obtain

$$P_e = E[e_n^2]E[|\epsilon_n|]. \tag{3}$$

Proposition : When the input $V_{in}(n)$ to the DAC is a cosine wave $V_{in}(n) = A\cos(2\pi\frac{f_{in}}{f_s}n)$, the error power P_e due to jitter is given by

$$P_e = 2A^2 \sin^2(\pi\frac{f_{in}}{f_s}n)E[|\epsilon|].$$

Here f_{in} is the input frequency and f_s is the sampling frequency ($f_s = 1/T_s$).

Proof of Proposition : See [8].

We remark that references [9, 10] discuss nonuniform sampling effects in DACs. However, our problem formulation is different from theirs.

2.2 Numerical Simulation of DAC Output Error Power due to Sampling Clock Jitter

Example 1 : Suppose that the jitter ϵ_n follows a uniform distribution whose probability function $p(\epsilon_n)$ is as shown in Fig. 5:

$$p(\epsilon_n) = \begin{cases} \frac{1}{2a} & (-a \le \epsilon_n \le a, \text{where } 0 < a < T_s/2) \\ 0 & (\text{otherwise}). \end{cases}$$

Note that $0 < a < T_s/2$ according to eq.(1). Since $E[|\epsilon_n|] = a/2$, we obtain

$$P_e = A^2 a \sin^2(\pi\frac{f_{in}}{f_s}). \tag{4}$$

Fig.6 shows a graph of f_{in}/f_s versus P_e calculated numerically from eq.(4) and a graph obtained from a DAC simulation including jitter, where $a = T_s/4$ and $A = 2$ are used in both cases. We see that both match well.

Example 2 : Suppose that the jitter ϵ_n follows a distribution whose probability function is of cosine-squared shape as shown in Fig.7:

$$p(\epsilon_n) = \begin{cases} \frac{1}{a}\cos^2(\frac{\pi\epsilon_n}{2a}) & (-a \le \epsilon_n \le a, 0 < a < T_s/2) \\ 0 & (\text{otherwise}). \end{cases}$$

Since $E[|\epsilon_n|] = a(\pi^2 - 4)/(2\pi^2)$, we obtain

$$P_e = \frac{1}{\pi^2}(\pi^2 - 4)A^2 a^2 \sin^2(\pi\frac{f_{in}}{f_s}). \tag{5}$$

Fig.8 shows a graph of f_{in}/f_s versus P_e calculated numerically from eq.(5) and a graph obtained from a DAC simulation including jitter, with $a = T_s/4$ and $A = 2$ in both cases. We see that both match well.

Remark In general, quantization noise (which we neglected in our problem formulation), and the noise due to the sampling jitter in a DAC, are statistically independent. Hence the total error power when both the quantization and the sampling jitter exist is just the simple sum of the error power due to quantization and that due to sampling jitter.

2.3 Power Spectrum of DAC Output Error due to Sampling Clock Jitter

Next we consider the power spectrum characteristics of the DAC output error due to jitter. Suppose that the input $V_{in}(n)$ to the DAC is a cosine wave $V_{in}(n) = A\cos(2\pi(f_{in}/f_s)n)$ and the DAC suffers from uniformly-distributed sampling clock jitter (Fig.5). Fig.9 shows simulation results of the power spectrum of the error, and we see that their power has peaks at

$$kf_s \pm f_{in} \qquad (k = 1, 2, 3, ...). \tag{6}$$

2.4 Sampling Jitter Effects on DAC SNR

In this section we show that the sampling clock is very serious by analyzing their effects on DAC SNR. Fig.10 shows the power spectrum of a 10-bit ideal DAC output *without jitter* for $f_{in}/f_s = 103/512, 2048$. Note that the DAC output error due to the zero-order hold output has power spectrum peaks at $kf_s \pm f_{in}$ $(k = 1, 2, 3, ...)$ [3], and it follows from eq.(6) that the DAC output errors due to jitter and zero-order hold have power spectrum peaks at the same frequencies. On the other hand, Fig.11 shows the power spectrum of the same DAC *with jitter* (cosine-squared distribution of $a = T_s/4$ in Fig.7), and we see that the noise floor increases. Figs.12 and 13 show the SNRs of the DAC with and without jitter, where the total noise (outside as well as inside the signal band) is considered. We see that SNR degrades slightly (by a few dB). However, in practical situations, the DAC is often followed by an analog low-pass filter which sufficiently attenuates the noise components beyond $f_s/2$. In this case we consider that SNR is given by

$10log_{10}$ {signal power}/ {noise power between 0 to $f_s/2$ (total noise power in the signal band)} $[dB]$.

Figs.14 and 15 show that the DAC SNR using the above definition degrades significantly due to the sampling jitter, and these results can be interpreted as follows; the noise power due to the zero-hold output and jitter has peaks at $kf_s \pm f_{in}$ $(k = 1, 2, 3, ...)$ (which is higher than $f_s/2$ for all k). Thus if we consider the whole noise, the dominant noise peaks are located at these frequencies. The sampling clock jitter induces *spread spectrum effects* for these frequency noise peaks (as well as the signal power peak) and the power at these frequencies is widely spread out to other frequencies, and hence the noise floor increases. However, the total noise power remains almost constant. Hence, when the total noise power is considered, the DAC SNR is almost constant regardless of sampling jitter. On the other hand, when only the noise inside the signal band $f_s/2$ is taken into account, the SNR degrades significantly because the noise floor inside the signal band is raised by the jitter.

3 Clock Timing Skew Effects

3.1 Glitch and Clock Timing Skew

Glitch is one of the important performance specification of DACs [3], and it is caused by the clock timing skew inside the DAC. Consider a binary-weighted current steering DAC in Fig.16, where the digital input changes from code 7 to code 8. When the digital input is 7, switches $D3$, $D2$ and $D1$ are ON and the output voltage is $7IR$. When the digital output is 8, switches $D4$ is ON and the output voltage is $8RI$. Suppose that during the input transition from 7 to 8, the the switch $D4$ turns on slightly before the switches $D1$, $D2$ and $D3$ turn off; in a transition moment, all of the switches $D1$, $D2$, $D3$ and $D4$ are ON, which outputs an impulse voltage of $15IR$, and this is called "glitch". The switch timing difference among $D1$, $D2$, $D3$ and $D4$ are caused by the skew among the clocks inside the DAC which control on and off of the current switches. The glitch degrades SNR and SFDR of the DAC, and also an amplifier circuit following the DAC often can

not respond to the impulse. Note that this glitch impulse is caused and problematic even when the input frequency is low. To our knowledge, the glitch characteristics itself has not been well-investigated theoretically, and in this paper we will try to clarify it. On the other hand, several DAC architecture and circuit techniques have been proposed to reduce the glitch as follows:
(i) In many high-speed DACs, segmented configuration for the upper bits is used for the glitch reduction while binary-weighted configuration for the lower bits is used for the hardware and power reduction [4].
(ii) A track-and-hold (T/H) circuit sometimes follows the DAC output for the glitch effect reduction, and such a T/H circuit is called as "deglitcher circuit" [4]. However it is very difficult to design such a T/H circuit to meet the specification requirements of very high performance DACs.
(iii) Recently a track-and-attenuation (T/A) circuit is proposed to replace the T/H circuit as a deglitcher [11]. The T/A circuit is relatively easy to design though it reduces the signal power of the DAC output by a factor of 2.
(iv) Note that in principle the glitch can not be reduced even if the differential output is used [4].

3.2 Glitch Simulation

We have simulated the DAC glitch effects using C programs. In the simulation, we assume that the DAC employs an 8-bit binary-weighted current steering architecture and its output is zero-hold. The DAC output is analog and it is continuous in time, and hence for our digital simulation we have "subsampled" the sampling period T_s by a factor of M (here $M = 64$). In our simulation, the data of N sampling prediods (here $N = 128$) were collected and hence we have performed $N \times M$-point discrete Fourier transform to obtain the DAC output power spectrum. Figs.17-20 show the simulation results of the DAC output waveforms and its power spectrum with some timing skews. Fig.21 shows the simulation results for the DAC SNR versus timing skew.

From these results, we have obtained the following observations:
(i) Effects of the glitch due to upper bits on the DAC SNR and SFDR are more significant than due to lower bits.
(ii) As the timing skew increases, its effects on the DAC SNR and SFDR become more serious.
(iii) As the input frequency increases, the effects of the glitch on the DAC SNR decreases.
(iv) The glitch power spectrum has peaks at odd-multiple frequencies of f_{in} and it does not have much power at its even-multiples. This corresponding the fact that "the glitch can not be reduced even if the differential output is used".
Remark However, in our experiences, the glitch power spectrum of actual DACs often has a finite (nonzero) value at even-multiples of f_{in} as well as its odd-multiples; this would be probably because the propagation delay time of t_{pdON} for a current switch to turn on and that of t_{pdOFF} to turn off are different. We are trying to incorporate this effect in our simulation.

4 Concluding Remarks

As an on-going project, we are investigating the following:
(i) Quantitative analysis of the glitch in the segmented (for upper bits) + binary-weighted (for lower bits) DAC architecture, as well as in the binary-weighted (for all bits) DAC architecture.
(ii) Quantitative clarification of the relationships between the input frequency and the glitch energy.

(iii) Confirmation of the results here by SPICE simulation.

By considering the timing error analysis in this paper, we have desinged and laid-out a 10bit CMOS DAC and it is now under fabrication (Figs.22, 23, 24), and its design contents may be also reported at the conference.

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We would like to thank H. Okano, M. Iwasaki and K. Wilkinson for valuable discussions.

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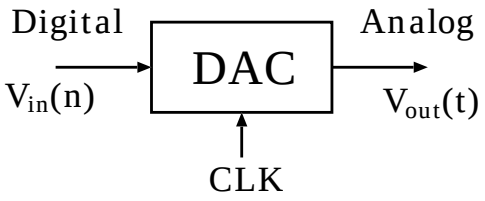

Figure 1: A DAC with digital input signal, sampling clock and analog output signal.

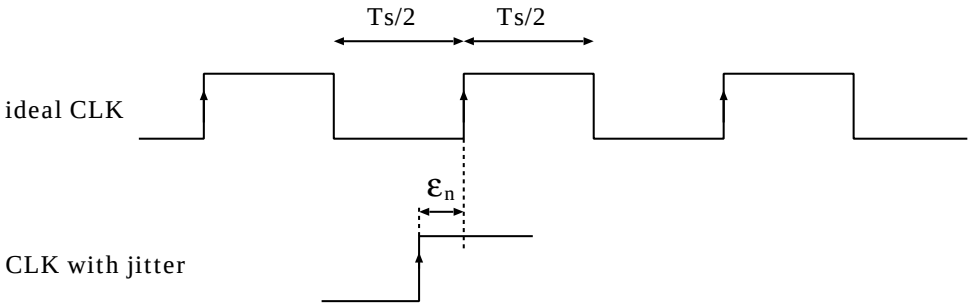

Figure 2: Ideal sampling clock (without jitter) and actual sampling clock (with jitter ϵ_n) provided to a DAC.

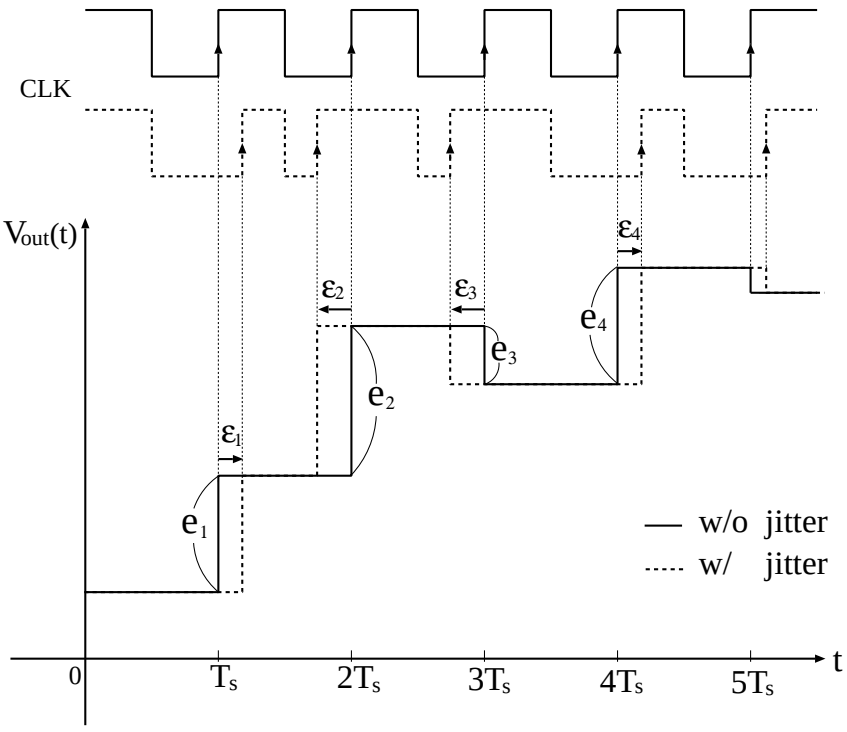

Figure 3: DAC output waveforms with ideal sampling clock (without jitter) and actual sampling clock (with jitter ϵ_n).

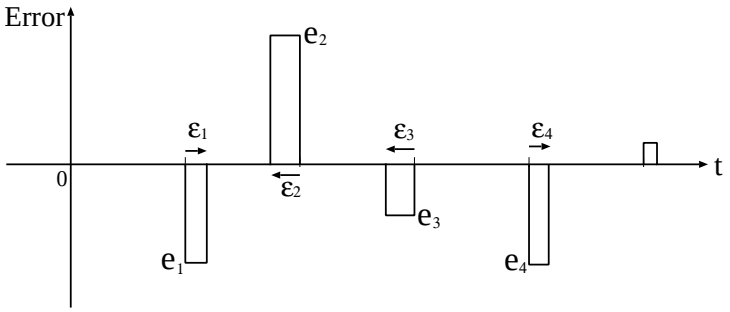

Figure 4: DAC output error due to sampling clock jitter ϵ_n.

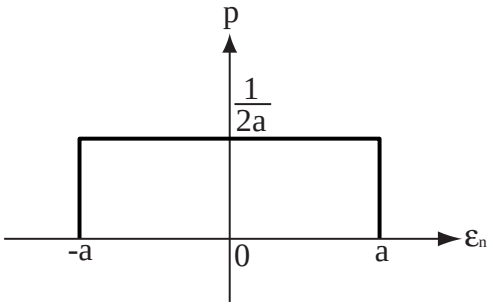

Figure 5: Probability distribution of the jitter ϵ_n (uniform distribution, $0 < a < T_s/2$).

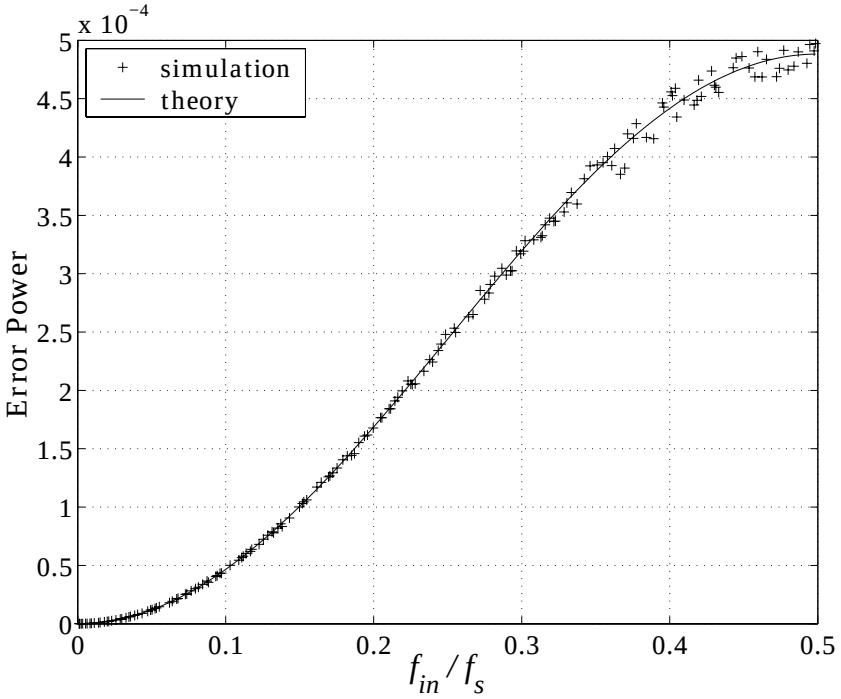

Figure 6: f_{in}/f_s versus P_e characteristics for the cosine wave input of amplitude $A = 2$ and the jitter of the uniform distribution with $a = T_s/4$ (Fig.5). The solid line shows numerical calculation results from eq.(4) while + indicates DAC simulation results including jitter.

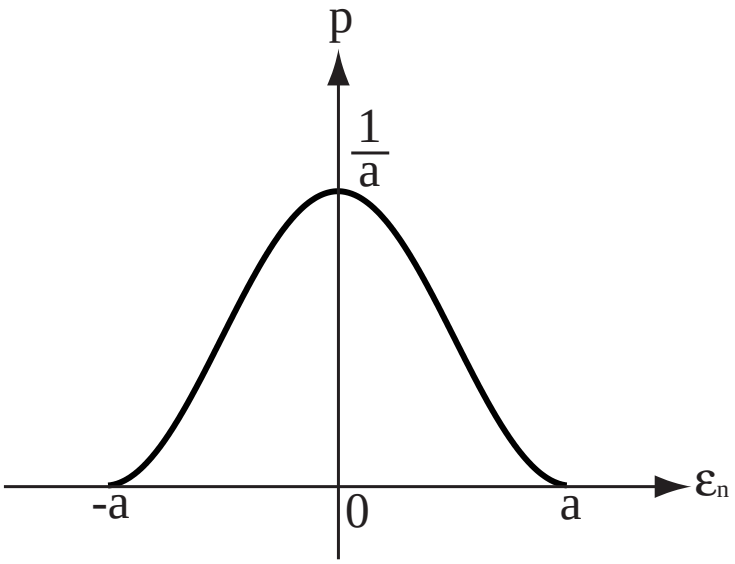

Figure 7: Probability distribution of the jitter ϵ_n (cosine squared distribution, $0 < a < T_s/2$).

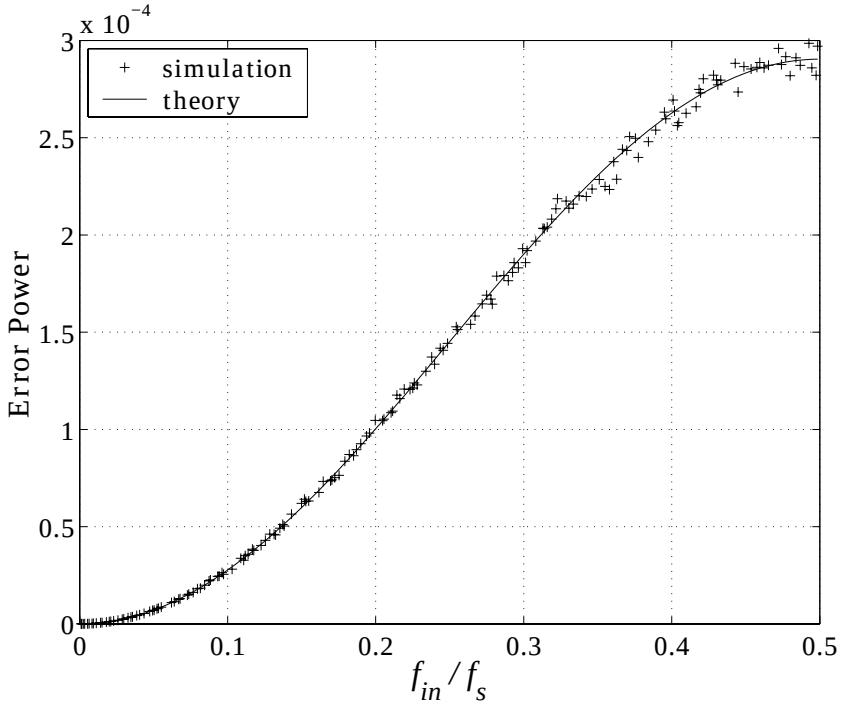

Figure 8: f_{in}/f_s versus P_e characteristics for the cosine wave input of amplitude $A = 2$ and the jitter of the cosine squared distribution (Fig.7) with $a = T_s/4$. The solid line showsnumerical calculation results from eq.(5) while + indicates DAC simulation results including jitter.

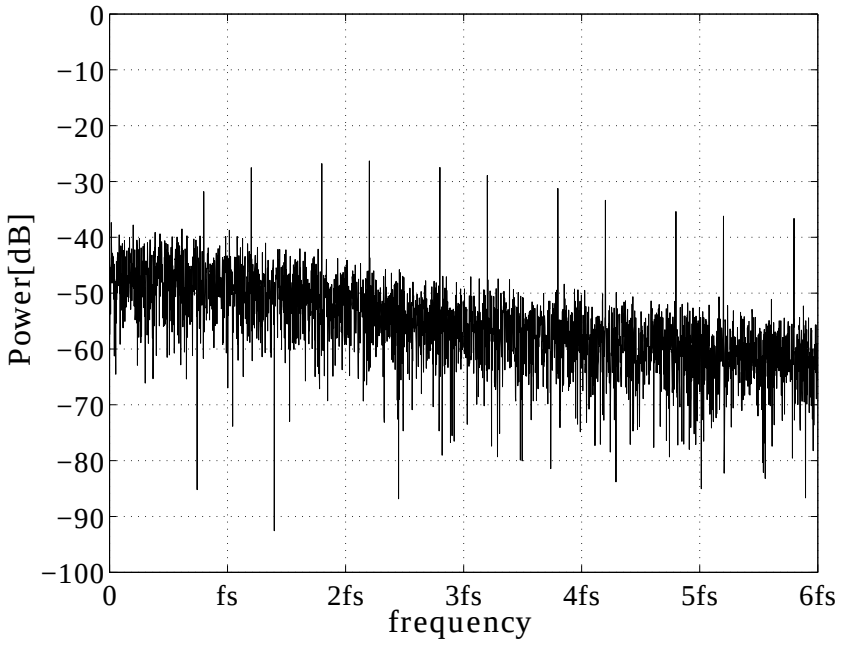

Figure 9: The power spectrum of DAC output error power due to jitter (whose distribution is shown in Fig.5 with $a = T_s/4$) for the input $V_{in}(n) = \cos(2\pi(f_{in}/f_s)n)$ with $f_{in}/f_s = 103/512$. The peaks are located at $f_s k \pm f_{in}$ where $k = 1, 2, 3, ..$

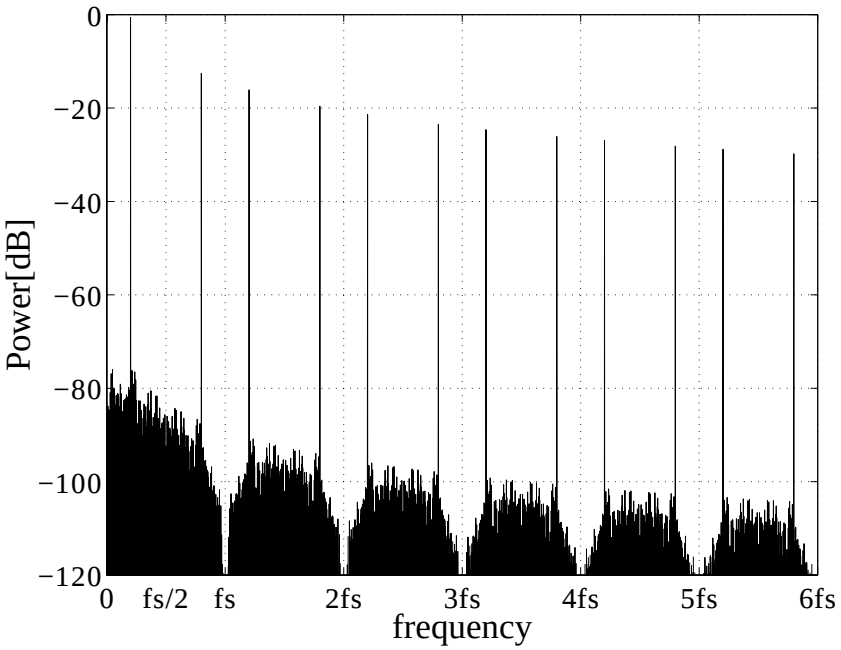

Figure 10: The power spectrum of a 10-bit DAC zero-hold output without the sampling clock jitter for $f_{in}/f_s = 103/512$.

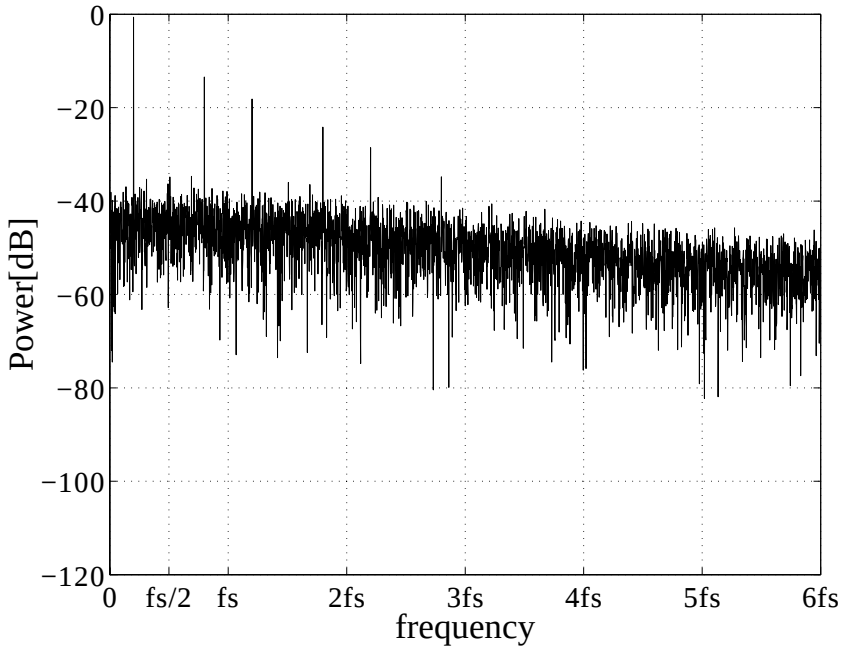

Figure 11: The power spectrum of a 10-bit DAC zero-hold output with the sampling clock jitter of cosine squared distribution of $a = T_s/4$ (Fig.7), for $f_{in}/f_s = 103/512$.

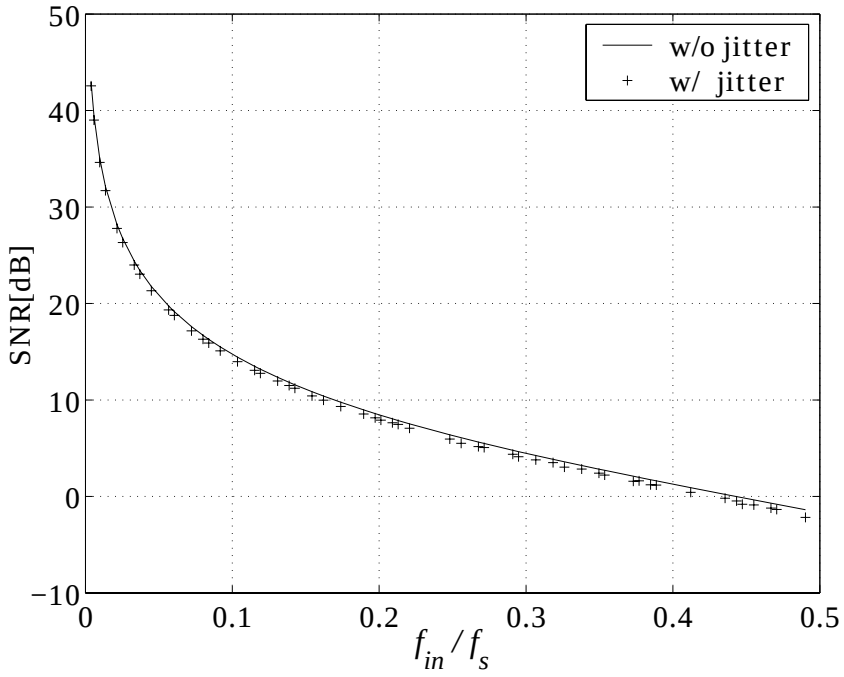

Figure 12: Simulation result of SNR versus f_{in}/f_s of a 10-bit DAC with and without jitter of cosine squared distribution of $a = T_s/4$ (Fig.7). Here the total noise power outside as well as inside the signal band is considered.

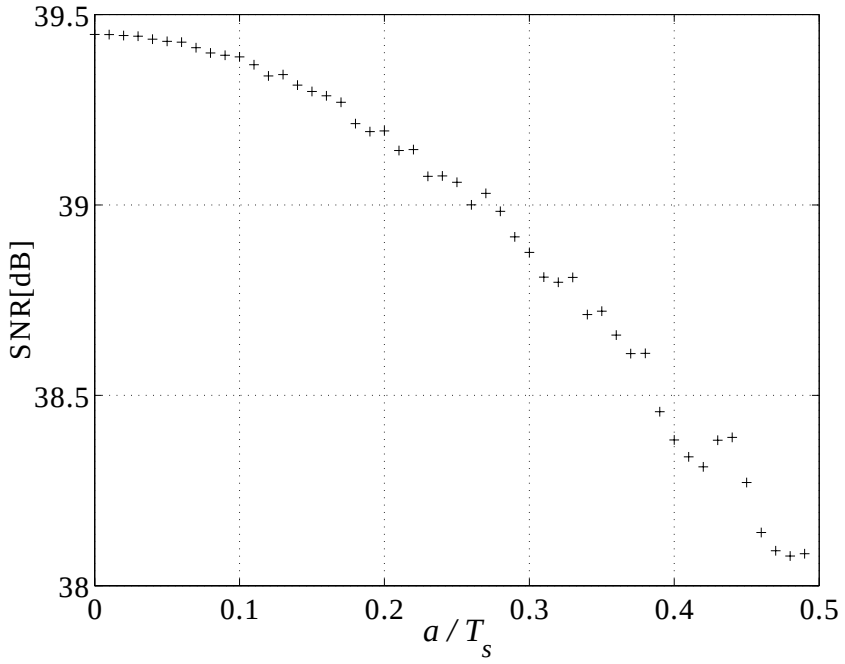

Figure 13: Simulation result of SNR versus the jitter a/T_s of a 10-bit DAC with jitter of cosine squared distribution (Fig.7) for $f_{in}/f_s = 3/512$. Here the total noise power outside as well as inside the signal band is considered.

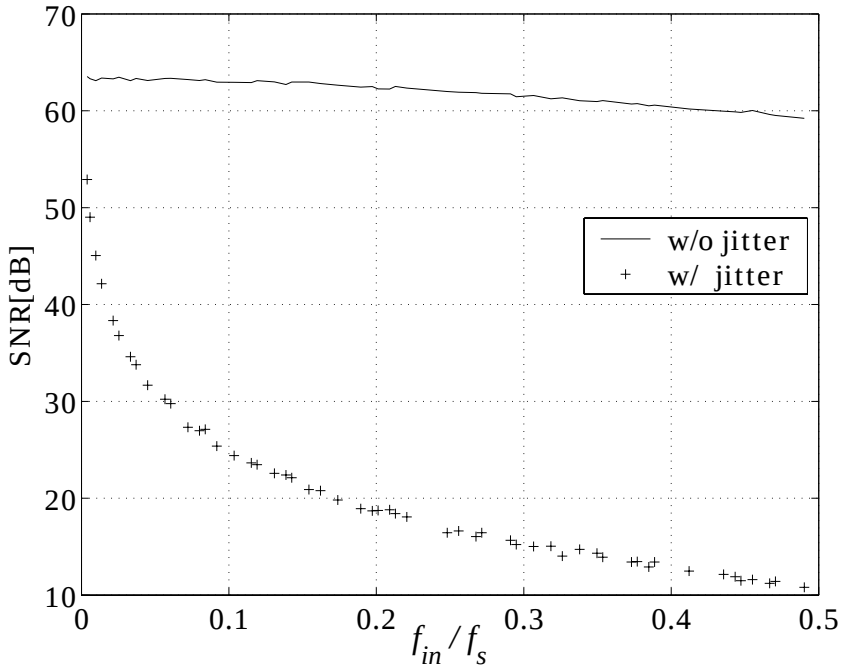

Figure 14: Simulation result of SNR versus f_{in}/f_s of a 10-bit DAC with and without jitter of cosine squared distribution of $a = T_s/4$ (Fig.7). Here only the noise power inside the signal band $f_s/2$ is considered.

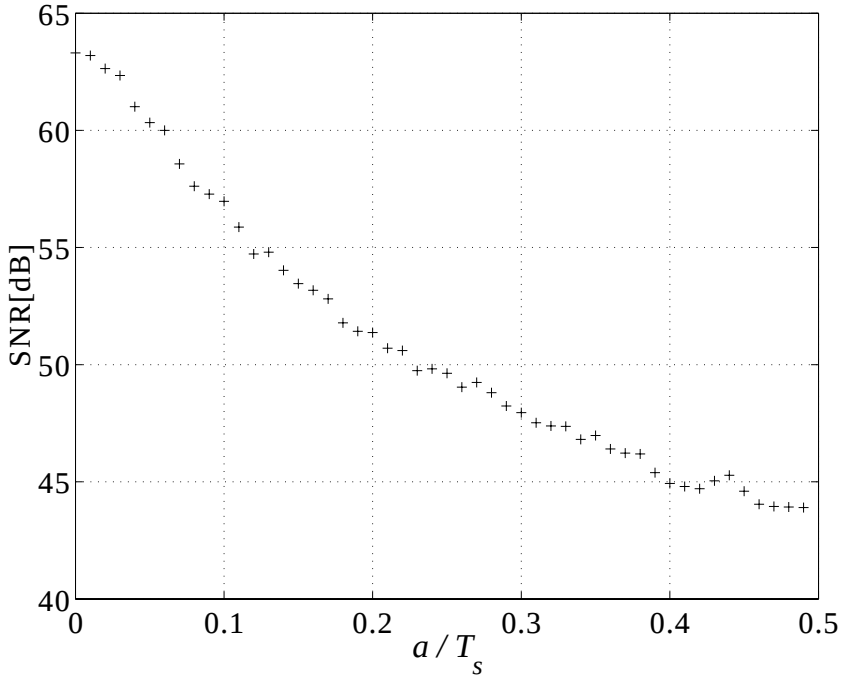

Figure 15: Simulation result of SNR versus the jitter a/T of a 10-bit DAC with jitter of cosine squared distribution (Fig.7) for $f_{in}/f_s = 3/512$. Here only the noise power inside the signal band $f_s/2$ is considered.

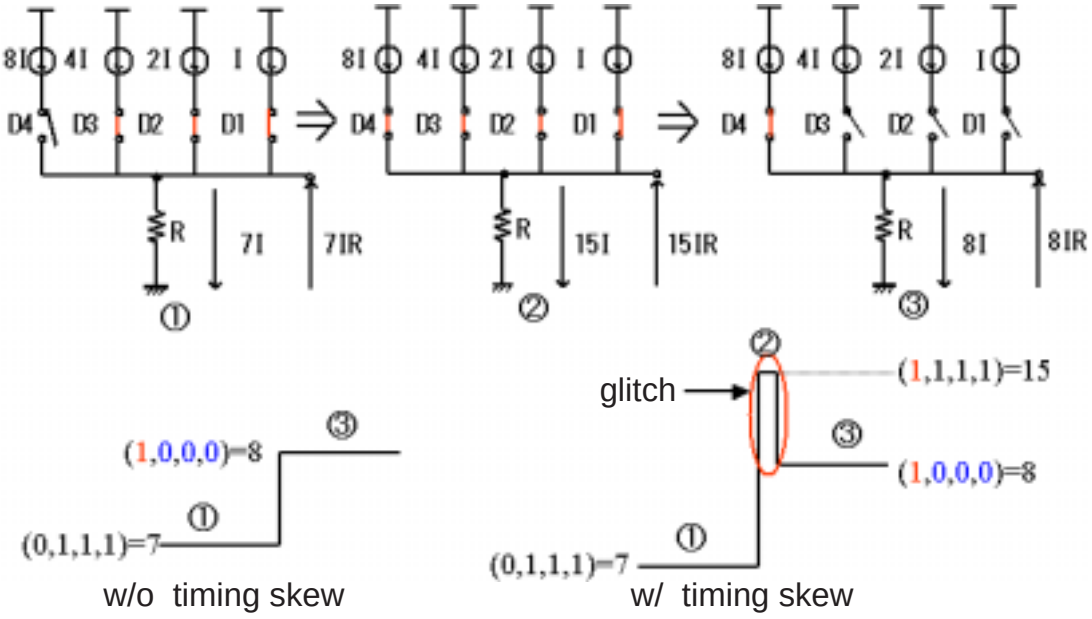

Figure 16: Glitch causing mechanism in a current steering DAC. Suppose that the switch $D4$ turns on before the other switches turn off (due to clock timing skew) when the input changes from code 7 to code 8. Then a glitch impulse of $15IR$ is caused during the transition.

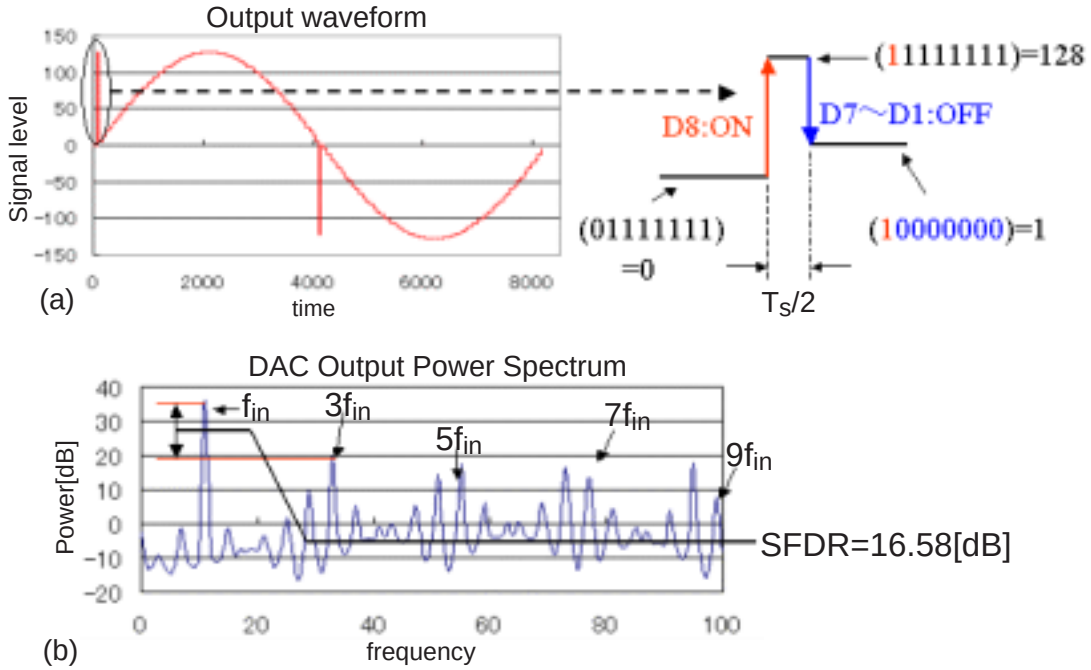

Figure 17: Simulation results for a sinusoidal input in case that the switch for MSB ($D8$) changes faster by $T_s/2$ than those for the other bits. (a) DAC output waveform for $f_{in} = f_s/128$. (b) DAC output power spectrum for $f_{in} = (11/128)f_s$.

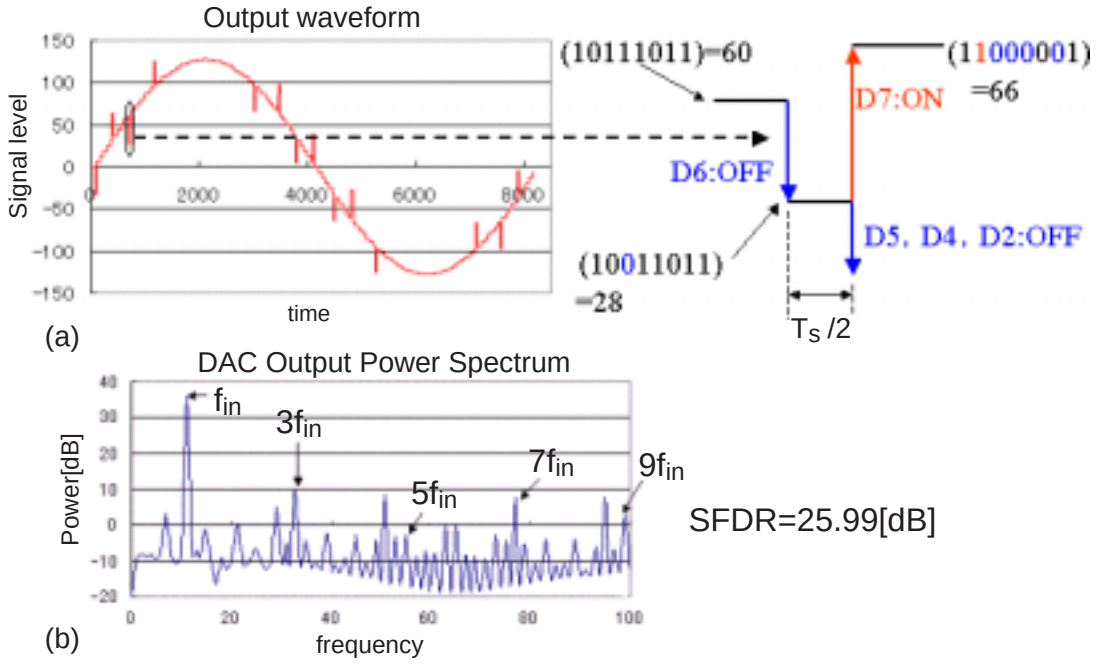

Figure 18: Simulation results for a sinusoidal input in case that the switch for MSB-2 ($D6$) changes faster by $T_s/2$ than those for the other bits. (a) DAC output waveform for $f_{in} = f_s/128$. (b) DAC output power spectrum for $f_{in} = (11/128)f_s$.

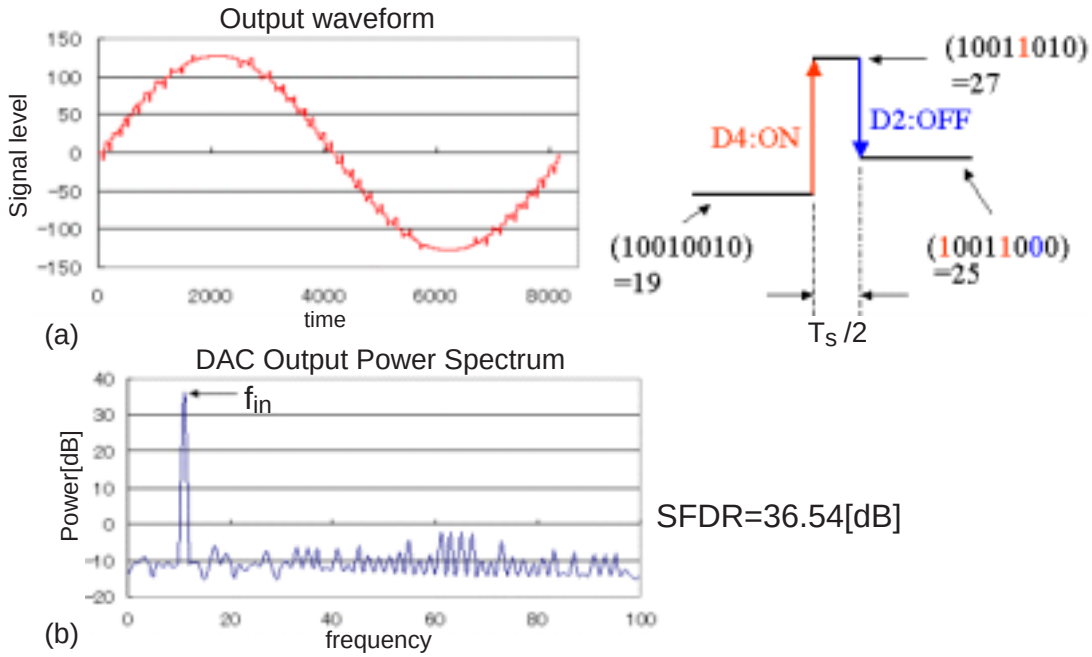

Figure 19: Simulation results for a sinusoidal input in case that the switch for MSB-4 ($D4$) changes faster by $T_s/2$ than those for the other bits. (a) DAC output waveform for $f_{in} = f_s/128$. (b) DAC output power spectrum for $f_{in} = (11/128)f_s$.

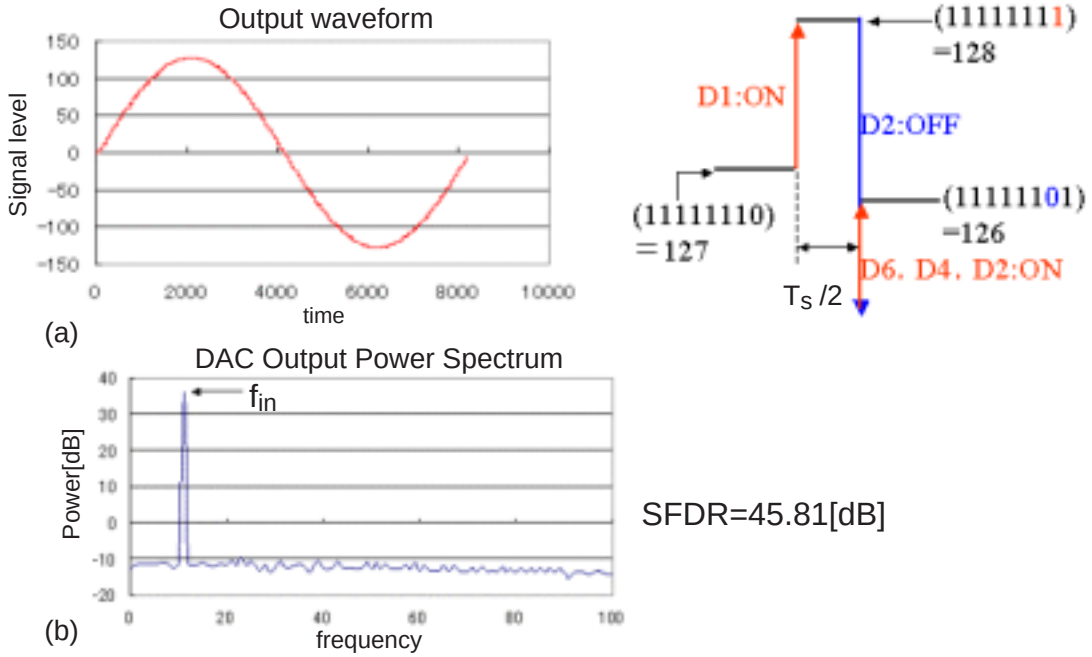

Figure 20: Simulation results for a sinusoidal input in case that the switch for LSB ($D1$) changes faster by $T_s/2$ than those for the other bits. (a) DAC output waveform for $f_{in} = f_s/128$. (b) DAC output power spectrum for $f_{in} = (11/128)f_s$.

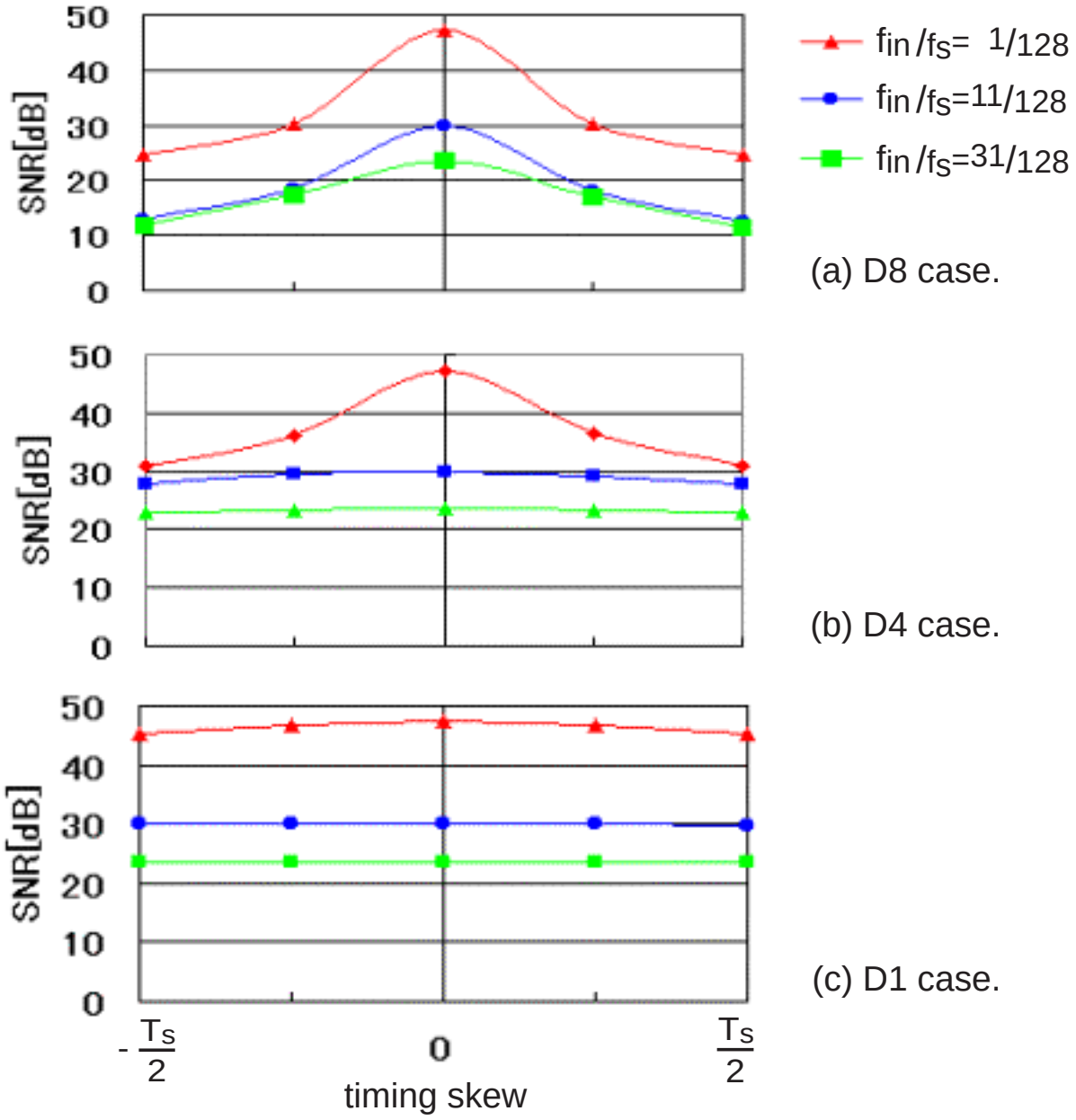

Figure 21: Timing skew (of $D8$, $D4$, $D1$) versus SNR for $f_{in}/f_s = 1/128$, $11/128$ and $31/128$.

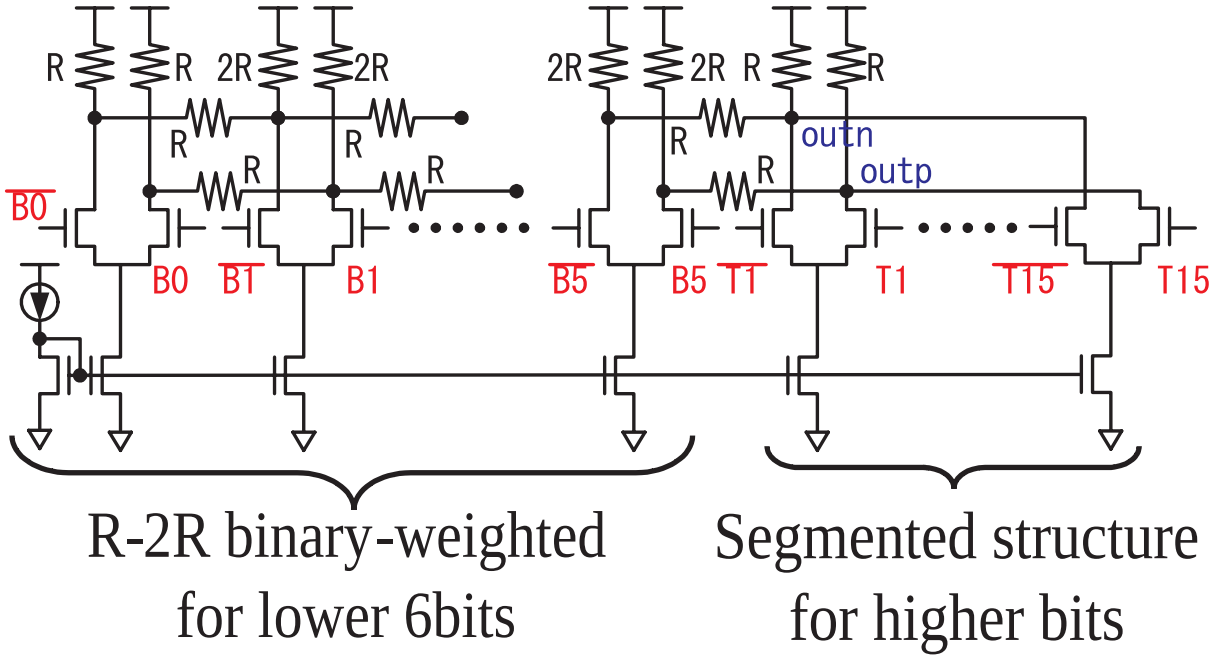

Figure 22: Analog part of our designed 10bit CMOS DAC, where segmented structure (for higher bits) + R-2R binary-weighted strucuture (for lower bits) is used.

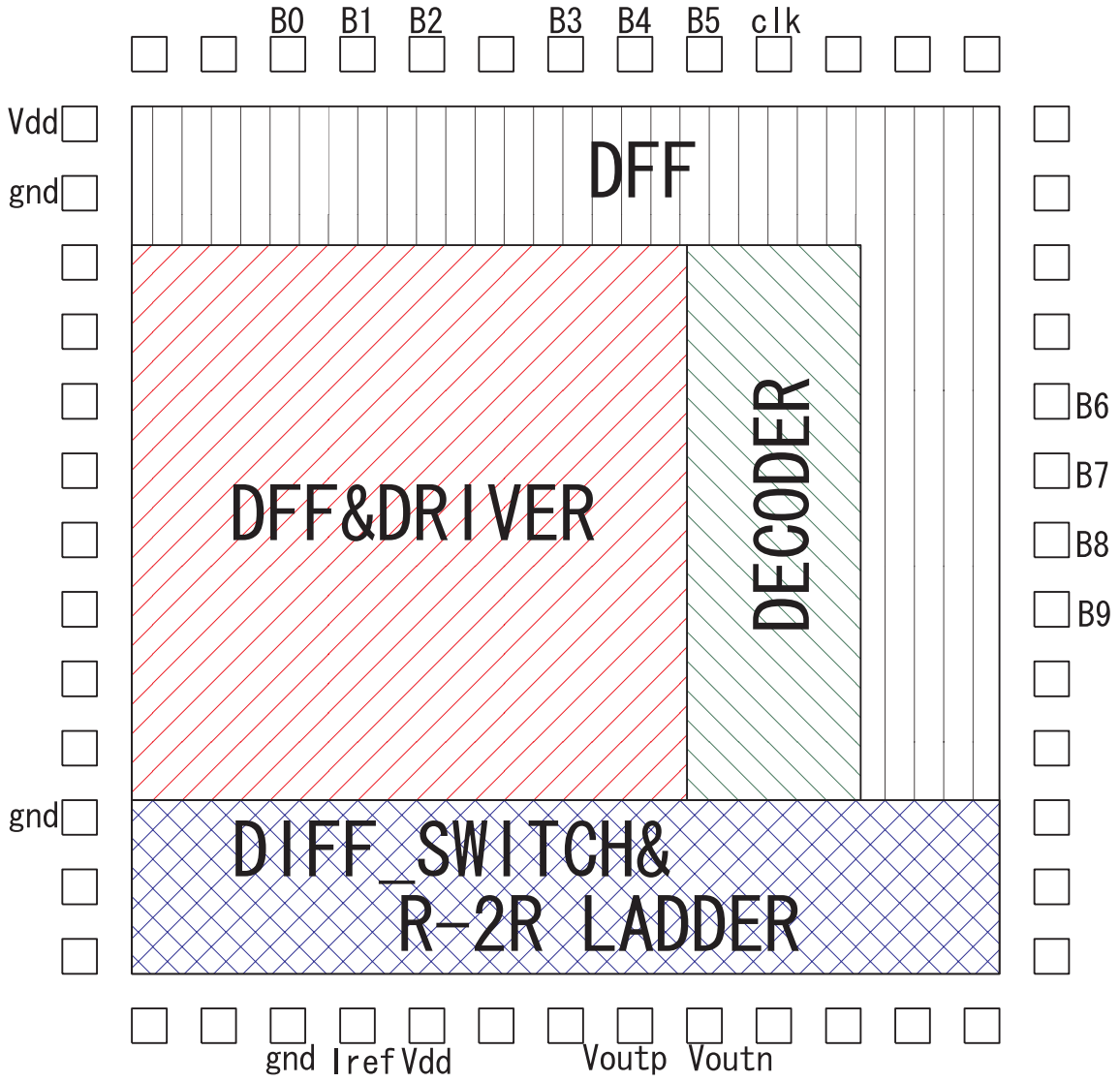

Figure 23: Floor plan of our designed 10bit CMOS DAC.

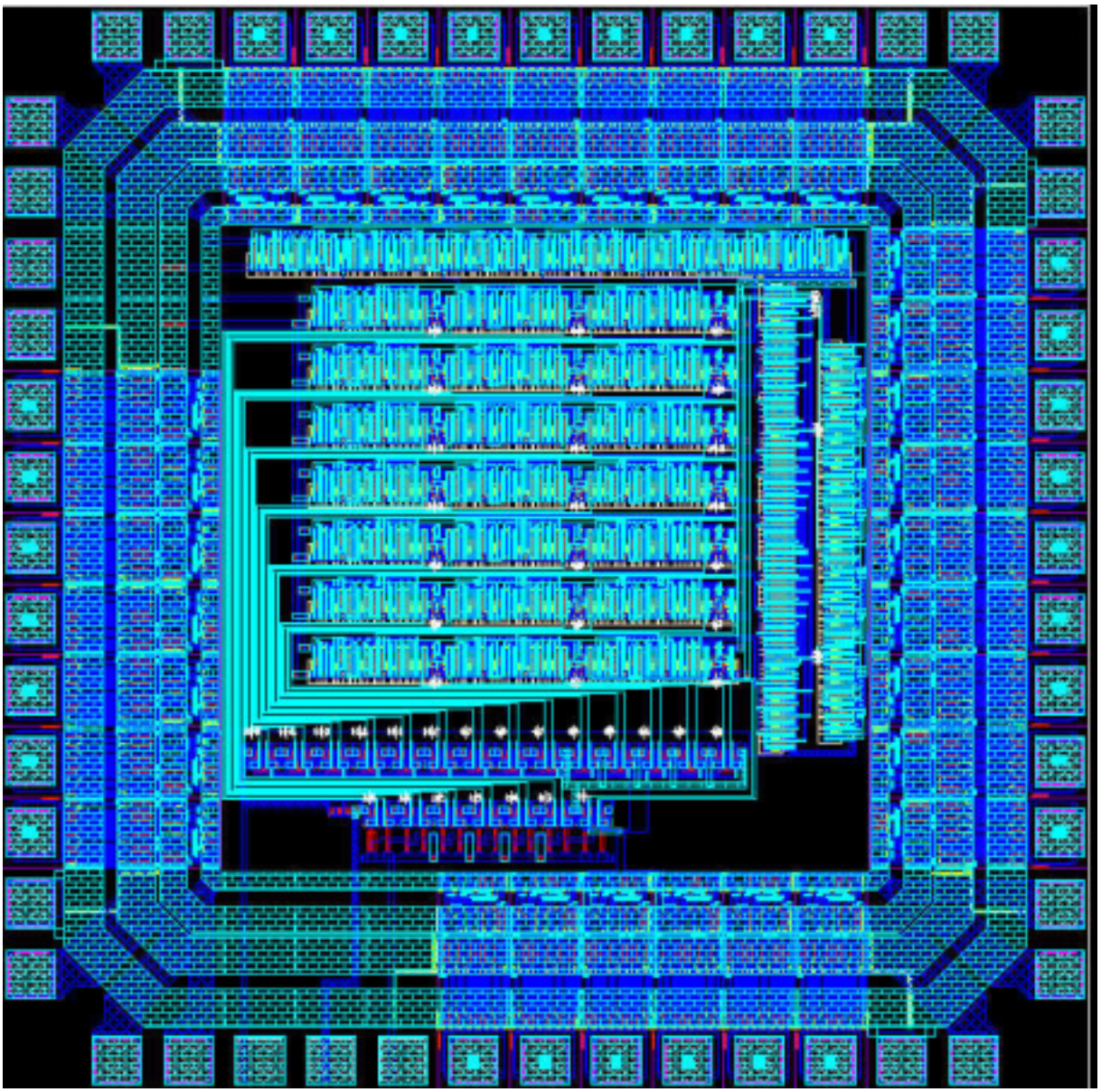

Figure 24: Layout of our designed 10bit CMOS DAC, whose die size is 2.6mm x 2.6mm in 1.2μm CMOS process.