Non-binary SAR ADC with Digital Error Correction for Low Power Applications

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***Abstract*— This paper describes techniques for creating a low-power SAR ADC with an error-correcting non-binary successive approximation algorithm; it is suitable for low power applications, performs digital error correction, and does not require analog calibration. Two techniques have been proposed for implementing low-power SAR ADCs: use of two comparators, and a charge-sharing architecture. However these techniques would normally require analog calibration of comparator offsets. Here we propose a non-binary SA algorithm that compensates for comparator offset effects in the digital domain, and so eliminates the need for analog calibration. Results of our Matlab simulation validate the effectiveness of this approach.**

Keywords : SAR ADC, Comparator, Low power, Redundancy, Non-binary, Digitally-assisted analog technology

I. Introduction

Low-power SAR ADCs with small chip area are widely used for high-resolution (10-16bit) and medium-sampling-speed applications, such as automotive, factory automation, and pen digitizer applications [1]-[6], and there is continuing demand for SAR ADCs with higher power efficiency.

This paper describes techniques for creating a low-power SAR ADC that uses an error-correcting non-binary successive approximation algorithm. By digitally correcting for the comparator offset and comparator decision errors inherent in two low power techniques proposed in [1], [2], it eliminates the need for analog calibration, which is suitable for fine CMOS implementation.

(1) To realize low power consumption, two dynamic comparators can be used: a low-power high-noise comparator for the early conversion stages, and a second comparator with lower noise but higher power consumption for the later stages (Fig.2). We propose using an error-correcting non-binary SAR ADC algorithm to digitally correct comparator decision errors – caused by the high noise of the first conversion stages, and by offset mismatch between the two comparators – and eliminate the need for analog calibration.

(2) To realize low power consumption, a charge-sharing SAR ADC using a binary successive approximation algorithm also seems attractive Fig.3. However comparator offset in the charge-sharing ADC degrades ADC linearity; [2] proposes that this offset be calibrated by an analog method. Here we propose using such a charge-sharing SAR ADC with a non-binary algorithm that digitally corrects for comparator offset, thus eliminating the need for analog calibration.

II. Binary search algorithm

SAR ADCs consist of a sample and hold circuit, comparator, DAC, SAR logic circuit and timing generator (Fig.1), and conventional SAR ADCs use a multi-step binary search algorithm (Fig.4). This section explains the binary search algorithm which realizes N-bit resolution SAR ADC with N steps, and we assume that the analog input range is normalized from 0 to $2^N - 1$. The comparator compares the analog input (V_{in}) and the reference voltage (DAC output), and its output $s(k)$ at k-th step is defined by

$$s(k) = \begin{cases} 1 & \text{(when } V_{in} > V_{ref}(k)\text{)} \\ -1 & \text{(otherwise).} \end{cases}$$

The reference voltage in the k-th step ($V_{ref}(k)$) is given by

$$V_{ref}(k) \quad = \quad 2^N \cdot \big(2^{-1} + \sum_{i=2}^{k} s(i-1)2^{-i}\big).$$

Also the ADC output D_{out} is given by

$$D_{out} \quad = \quad 2^{N-1} + \big(\sum_{i=2}^{N} s(i-1)2^{N-i}\big) + \frac{1}{2}(s(N)-1).$$

III. Generalized Non-binary Algorithm

We describe here our generalized non-binary algorithm which realizes N-bit resolution SAR ADC in M steps (N $\leq$ M) (Fig.4) [5], [6]. We give the reference voltage in k-th step($V_{ref}(k)$) as follows:

$$V_{ref}(k) \quad = \quad 2^{N-1} + \sum_{i=2}^{k} s(i-1)p(i). \qquad (1)$$

Here $k = 1, 2, .., M$, and $p(k)$ is the value for addition to (or subtraction from) the reference voltage in the previous step. Then we have the following ADC digital output :

$$D_{out} \quad = \quad 2^{N-1} + \sum_{i=2}^{M} s(i-1)p(i) + \frac{1}{2}(s(M)-1). \quad (2)$$

We have derived that $p(i)$ must satisfy the following:

$$p(1) \quad = \quad 2^{N-1}, \quad \sum_{i=1}^{M} p(i) = 2^N - 1 + 2 \cdot \text{(over-range)}.$$

For the non-binary search algorithm using eq.(2), we see that there are 2^M comparison patterns (possible comparator output combination of all M steps) and 2^N output patterns (output codes in binary format), and since M is bigger than N, 2^M is bigger than 2^N. In other words, for a given output level D_{out}, there can be multiple comparison patterns, which means that there is some redundancy. Thus even if the comparator decision in a given step is wrong, correct ADC output may be obtained in the following step.

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IV. Low Power Non-binary SAR ADC with Two Comparators

A conventional SAR ADC uses one comparator with low noise and relatively high power in all steps. To implement a low-power SAR ADC, it has been proposed to use a high-noise low-power comparator in earlier successive- approximation steps, followed by a low-noise high-power comparator for the final binary step(s) (Fig.2, [1]), (Fig.5). The comparison errors of the high-noise low-power comparator in the earlier stages is corrected by the low-noise high-power comparator at the last step.

However, offset mismatch between the two comparators causes SAR ADC nonlinearity (Fig.6), and analog calibration for the offsets is used [1].

We propose using a non-binary SAR ADC algorithm with these two comparators (a high-noise low-power comparator for early stages, and a low-noise high-power comparator for later stages). The non-binary algorithm *digitally* compensates for comparison errors due to noise in early stages, and nonlinearity due to comparator offset mismatch. We can design a generalized non-binary SAR algorithm, based on the method in [5], [6], to obtain the correct output data – in spite of comparison errors due to noise in early stages, and offset mismatch.

Example : 10-bit SAR ADC. A high-noise low-power comparator : offset=+4LSB, input-referred noise $6\sigma = 1LSB$. A low-noise low-power comparator : offset -2LSB, input-referred noise $6\sigma = 0.2LSB$.

Table I (left) shows the algorithm for the conventional case, and Fig.9 shows DNL simulation results for a ramp input (without analog calibration of the comparator mismatch). We observe that DNL errors are large.

Table I (right) shows the algorithm for the proposed case, and Fig.10 shows DNL simulation results for a ramp input with digital correction. We see that DNL errors are suppressed.

Comparator mismatch allowance and power consumption are trade-offs in the proposed SAR ADC. If the comparator offset mismatch is large in the worst case, we have to design so that the high-noise low-power comparator is switched to the low-noise high-power comparator in an earlier successive-approximation step, and there is less reduction in power consumption. (Fig.8).

V. Charge-Sharing SAR ADC

A charge-sharing ADC has been proposed for high efficiency [1], [2] (Fig.3), and its signal processing is performed in the charge domain while that of a conventional charge distribution SAR ADC is in the voltage domain.

The charge-sharing SAR ADC samples V_{in} and charges it to C_s, and also charges V_{ref} to the binary weighted capacitors $C_1 \sim C_{M-1}$. Then in each step, a comparator examines the polarity of the charge in C_s: at the first step, if its output is "1", C_1 is connected so that the charge in C_s is subtracted, and if it is "0", it is connected in an opposite way. This procedure is repeated from C_1 to C_{M-1}.

However, the linearity of this charge-sharing SAR ADC suffers due to comparator offset. (For a conventional SAR ADC (such as a charge distribution SAR ADC), the comparator offset becomes just the whole ADC offset and does not degrade its linearity [7].) This is because the comparator input-referred offset is in the voltage domain and its corresponding charge domain offset changes as the step proceeds and the connected capacitors change (Fig.13). To solve this problem, analog calibration is performed so that the comparator offset is within ± (1/2)LSB [1], [2].

TABLE I
10b SAR ADC algorithm with two comparators. Left: conventional. Right: proposed.

	step k	weight p_k
Low power high noise comparator	1	512
	2	256
	3	128
	4	64
	5	32
	6	16
	7	8
	8	4
	9	2
High power low noise comparator	10	1
	11	1

	step k	weight p_k
Low power high noise comparator	1	512
	2	256
	3	128
	4	64
	5	32
	6	16
High power low noise comparator	7	8
	8	8
	9	4
	10	2
	11	1

We propose here a charge-sharing non-binary SAR ADC which compensates for comparator offset effects using digital error correction, to eliminate the need for analog calibration (Fig.14). We design a generalized non-binary algorithm based on [5], [6] so that the comparator offset effects are cancelled out.

Example : 10bit charge-sharing SAR ADC, V_{in} : -1 - +1V V_{ref}=1V, $C_s = 512C$, Comparator offset V_{os}=55mV.

In a conventional binary case, we show its capacitor array weighting in Table II (left) and Matlab simulation results in Fig.11. In our proposed non-binary case, we designed its capacitor array weighting in Table II (right) as 10-bit, 11-step, and the Matlab simulation result is shown in Fig.12. We see that our proposed method can compensate for comparator offset effects.

VI. Conclusion

We have proposed using a non-binary SAR ADC algorithm to eliminate the need for analog calibration by compensating in the digital domain for comparator offset effects inherent in two low-power techniques: the use of two comparators (low-power high-noise for the first successive-approximaton steps, and low-noise higher-power for the final steps), and the use of a charge-sharing SAR ADC architecture. Our Matlab simulation demonstrates the effectiveness of this approach.

We acknowledge K. Mashiko, M. Kondo and K. Wilkinson.

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TABLE II

10BIT SAR ADC ALGORITHM FOR A CHARGE-SHARING SAR ADC. LEFT: BINARY. RIGHT: NONBINARY (11-STEP).

step k	size C_k
1	256
2	128
3	64
4	32
5	16
6	8
7	4
8	2
9	1
10	0

step k	size C_k
1	237
2	127
3	69
4	37
5	20
6	11
7	6
8	3
9	2
10	1
11	0

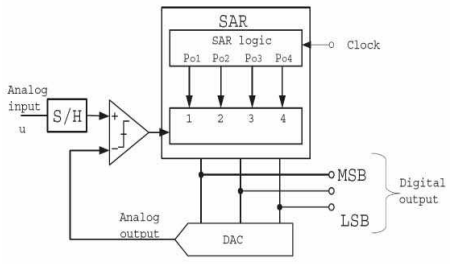

Fig. 1. SAR ADC block diagram.

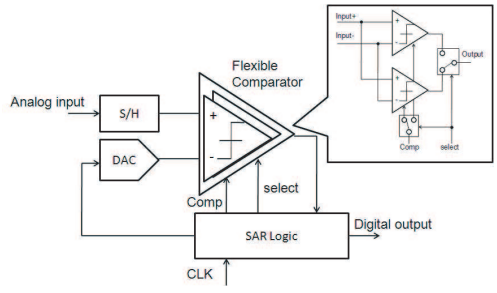

Fig. 2. Block diagram of an SAR ADC with two comparators.

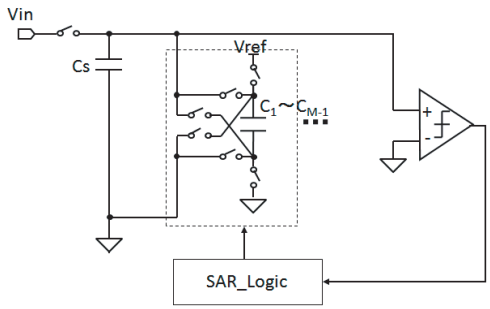

Fig. 3. Block diagram of a charge-sharing SAR ADC.

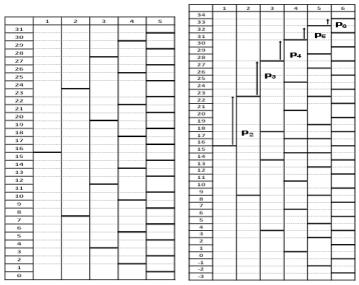

Fig. 4. Binary search algorithm of a 5-bit SAR ADC with 5 steps (Left). Non-binary search algorithm of a 5-bit SAR ADC with 6 steps (Right).

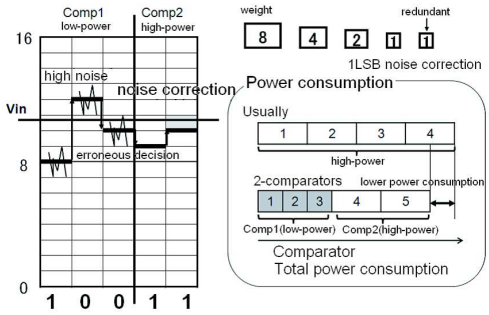

Fig. 5. SAR ADC with two comparators for low power.

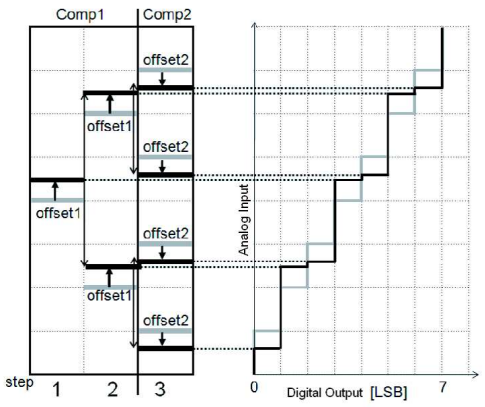

Fig. 6. Non-linearity caused by the comparator offset mismatch in an SAR ADC with two comparators.

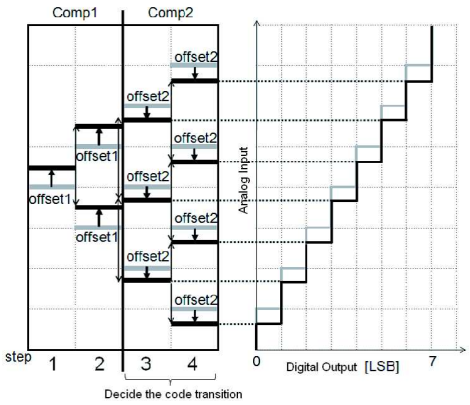

Fig. 7. Digital error correction of the comparator offset mismatch effects by the non-binary algorithm in an SAR ADC with two comparators.

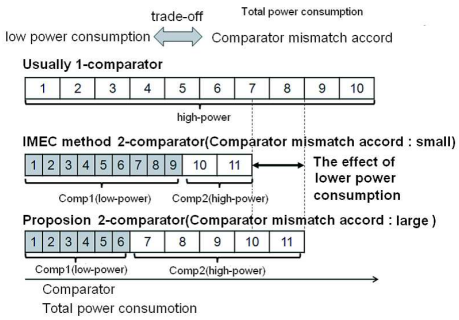

Fig. 8. Trade-off between power consumption and comparator offset mismatch allowance.

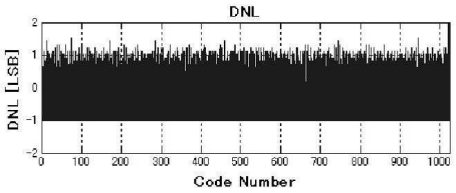

Fig. 9. Simulation result of the conventional SAR AD with two comparators (in case of no analog calibration of comparator offset).

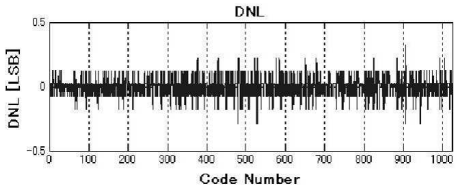

Fig. 10. Simulation result of the proposed SAR ADC with two comparators and using the non-binary algorithm.

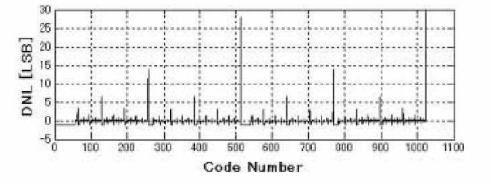

Fig. 11. Simulation result of the conventional charge-sharing SAR ADC with the binary algorithm (in case of no analog calibration of comparator offset).

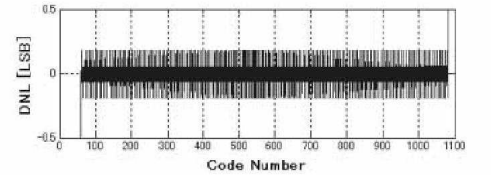

Fig. 12. Simulation result of the proposed charge-sharing SAR ADC with the non-binary algorithm.

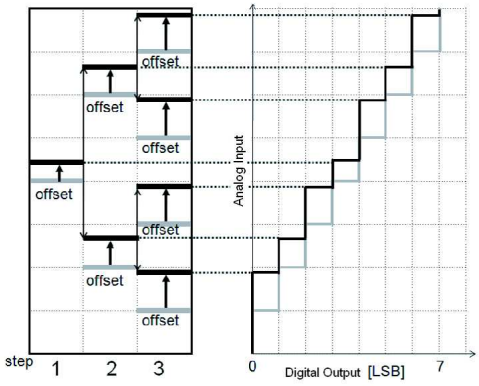

Fig. 13. Non-linearity caused by the comparator offset in the charge-sharing SAR ADC.

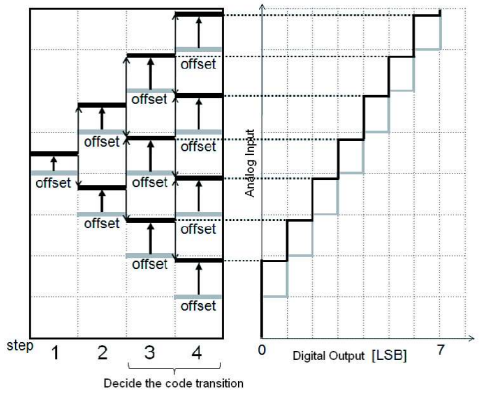

Fig. 14. Digital error correction by the non-binary algorithm for the comparator offset effects in the charge-sharing SAR ADC.