ADC Linearity Test Signal Generation Algorithm

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***Abstract*— This paper describes an algorithm for generating test signals to efficiently test the linearity of ADCs. Linearity is an important testing item for ADCs, and it takes a long time (hence is costly) to test low-sampling-rate, high-resolution ADCs. We here propose to generate a test signal consisting of multiple sine waves, to precisely test the linearity for specific important codes (such as around the center of the output codes), using an arbitrary waveform generator (AWG) and an analog filter. We have performed MATLAB simulation to validate our algorithm, and the results show that in some cases the testing time can be reduced to half that for conventional sine wave histogram testing.**

Keywords: ADC, Testing, Linearity, Histogram, AWG, ATE

I. Introduction

LSI production testing is becoming important in the semiconductor industry because testing cost is increasing while the cost of silicon is decreasing (Fig.1). ADCs/DACs are key components of mixed-signal SOCs, so their testing is important [1]-[5]; for high-resolution, slow-sampling-rate ADCs (such as SAR ADCs embedded in micro-controller chips), their DC linearity testing is very important but very time consuming, and hence costly.

This paper describes a novel method to shorten the time required to test the DC linearity of ADCs, while maintaining the required testing quality. We use a test input signal consisting of multiple sine waves generated by an AWG. We clarify its algorithm, show Matlab simulation results and estimate the testing time reduction with our proposed method.

II. Linearity Test of ADC

There are two widely-used linearity testing methods for ADCs using their histogram [1], [2], [6]; the ramp signal input method and the single-sine-wave input method (Fig.2).

(1) The ramp input method is moderately effective for reducing testing time, because the ADC output histograms for all bins are equal if the ADC is ideally linear (Fig.2 (a)). However highly-linear ramp signal generation is difficult, and hence its testing with ramp signals is likely to be limited to ADCs whose resolution is 12 bits or less.

(2) The single-sine-wave method can be applied to high resolution ADCs because high-accuracy sine waves can be generated using an analog filter which removes high-order harmonics (Fig.2 (b)). However, the histogram or the number of samples is small around the center of output codes, and hence longer testing time (by x $\pi/2$) is required to test these codes than the ramp input method for specified DNL resolution.

In some cases, the input signal for ADCs in SoC is mainly in the vicinity of the center of the input range, and is not evenly distributed over its full range. In this case, high resolution linearity testing in the vicinity of the center codes, as well as short testing time, are important; the sine wave method is not suitable because the frequency of samples in the vicinity of the center code is small; an input signal whose corresponding ADC output histogram is large around the center is more suitable (Fig.3) [8].

Also, depending on the ADC architecture, some codes and their vicinities may have to be tested to high resolution [3].

Based on these considerations, we propose here to design a test input signal that increases the frequency of samples in the vicinity of specific ADC codes that require high resolution linearity testing.

III. Proposed Test Signal Generation Method

A. Signal Generation Algorithm

We describe the design algorithm for generating the proposed test signal. First we approximate a triangular wave with multiple sine waves.

$$V_{in} = \frac{4}{\pi}\sum_{n=1}^{\infty} V_n \quad (1)$$

$$V_n = \frac{\cos(2\pi\cdot(2n-1)\cdot f\cdot t)}{(2n-1)^2}. \quad (2)$$

To generate a test input that increases the frequency for specific codes, we select and add terms V_n with adjusted coefficients (Fig.4).

Next, we describe the method for selecting the terms V_n to be added and for deciding their coefficients. By considering a quarter cycle (T/4) of the first term (Fig.4 (a)), we can understand the influence on the histogram of the first, second, third, fourth terms etc. (Fig.4 (b)); and we can estimate which terms are necessary to increase the frequency near the target codes. Fig.5 shows the input signals and their histograms when synthesizing them sequentially from the first to fourth terms. We see from the Fig.5 that the number of regions where the number of samples increases and the approximate code is obtained by the following expressions:

$$\text{Number of regions} = N-1$$
$$\text{Code} = \left(2^{bit}-1\right)/N.$$

N is the number of terms V_n added sequentially, and 2^{bit} is the ADC resolution. We found in Fig.4 (b) that the influence on the histogram of each term V_n is different. Because the

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frequency with respect to V_{in} is high for the high-order terms ($V_n,\ n >> 1$), their influence on the histogram is in several fine ranges. As a result, the samples increases like the peak. Therefore, the second term V_2 and the third term V_3 are used for expanding the range of the histogram increase.

B. Implementation Method

We use an AWG to digitally generate the synthesized signal, then use a DAC to output the corresponding analog signal, and use an analog low-pass filter or bandpass filter to remove spurious components (Fig.6). Consider the case that the resolution of the ADC under test is 14 bits and the linearity of a reasonable AWG is limited to 12-bit. Even in such a case, the analog filter can remove spurious components and provide multiple pure sine waves; so the analog filter circuit is also a key design item for the proposed method (and suitable designs are under investigation).

IV. Simulation Results

We have simulated the proposed algorithm with Matlab.

A. Increase of number of samples in vicinity of center code

Fig.7 (a) shows an generated test signal with our algorithm, and Fig.7 (b) shows the histogram when it is applied to a 12-bit ADC. We use the following to generate the test signal:

$$V_{in} = \frac{4}{\pi}\{V_1 + 2.6 \cdot V_2 + 1.8 \cdot V_3 + 1.4 \cdot V_6 + 1.2 \cdot V_7\} \quad (3)$$

We have adjusted the coefficient of each term heuristically, and also we have developed a systematic method of the coefficient adjustment using a genetic algorithm [7] which works well.

Fig.8 zooms the ADC output histogram in Fig.7 for the single sine wave and the proposed test signal inputs. We see that there are only about 12 samples per bin in the vicinity of the center code for the single sine wave input, but there are 32 samples for the proposed test signal input: about three times the number of samples enter bins of the center code with the proposed test signal input.

B. Increase in number of samples at codes other than center

The codes to be tested accurately are not necessarily in the vicinity of the center; this may depend on the ADC architecture under test. We can generate a suitable test signal input even in such cases.

For example, Fig.9 (a) shows several input waveforms that increase the number of samples at two codes with the proposed method, and Fig.9 (b) shows their corresponding histograms. The codes whose number of samples increases are selected to be at $14/32$, $12/32$, and $8/12$ of full scale. The histograms are symmetric with respect to half of the full scale code $(2^{bit} - 1)/2$. We see from Fig.9 (b) that about three or four times more samples enter bins in the vicinity of the selected codes; this is useful to test code transitions where the ADC operation mode changes [6]. Therefore, one code range where the number of samples is increased can be selected arbitrarily with the proposed method. Table I shows minimum and maximum numbers of samples at code ranges of $700 \sim 960$, $960 \sim 3130$ and $3130 \sim 3400$ for several input signals with the proposed method, and we see that the number of samples can be increased in the specified code region with the proposed method.

In addition, it is also possible to increase the number of samples in two or more code ranges. However, in such cases the range selection may be restricted to some extent; arbitrarily selecting all possible ranges is difficult.

V. Estimation of ADC Test Time

We estimate the test time for a 12-bit 100 kS/s SAR ADC under test with automatic test equipment (ATE), based on Table II.

(1) Setup time for measurement module and settling time for DUT : 10 msec
(2) DC linearity testing time: $2^{12} \times 40 \times 10\mu$ sec= 1600 msec
(3) SINAD testing time: $2^{12} \times 4 \times 10\mu$ sec =160 msec
(4) The time for data transfer and operation: 10 msec

Here we assume in the above (2) that the single sine wave input histogram method is used for DC linearity testing, and we see that the DC linearity testing time is dominant. If a testing time of 1 sec. for a one-dollar chip is reasonable, we see that this total test time (about 1.8 sec) is too long.

Next we estimate the test time reduction by our proposed method. We compare the testing times for both the single sine wave and our proposed signal inputs with the condition of at least 5 samples in each bin, and 10 samples or more in a bin in the vicinity of the center code (Fig.8). Our simulation shows that 65,536 samples are required for the single sine wave input and 32,768 samples for the proposed method.

We see from the above observations that the total test time can be reduced by about half with our proposed method.

VI. Conclusions

We have proposed a novel method for efficiently testing the DC linearity of ADCs with the histogram method, using a test input signal consistign of multiple sine waves, and described the generation algorithm. Our Matlab simulation has validated our algorithm, and we estimate that our proposed method can reduce the testing time by half in some cases. Our method can be implemented with an AWG and an analog filter.

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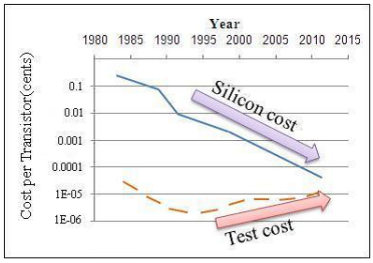

Fig. 1. Silicon and production test cost trends for LSIs.

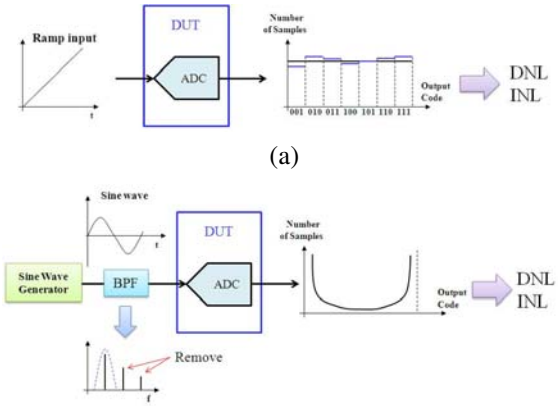

Fig. 2. Conventional ADC test signals and histograms for linearity testing. (a) Ramp input case. (b) Single sine wave input case.

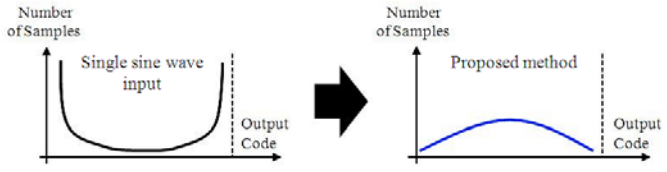

Fig. 3. ADC output histograms in the single sine wave case and in the proposed method case.

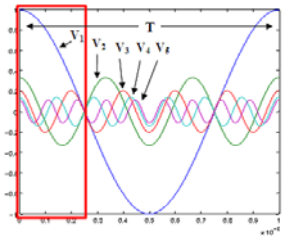

Fig. 4. Influence of sine waves on the histogram. (a) Sine waves. (b) Their influence on the histogram (the number of samples).

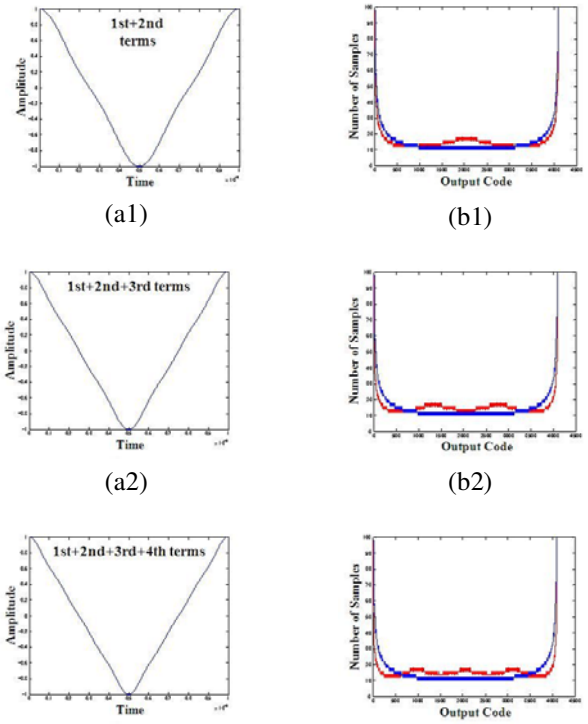

Fig. 5. Synthesized waveforms with multiple sine waves and the corresponding histograms. (a1), (a2), (a3) Input waveforms. (b1), (b2), (b3) Corresponding histograms.

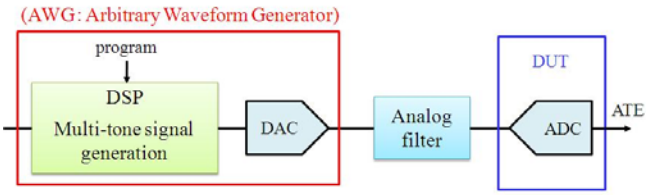

Fig. 6. System for generating the proposed test signal.

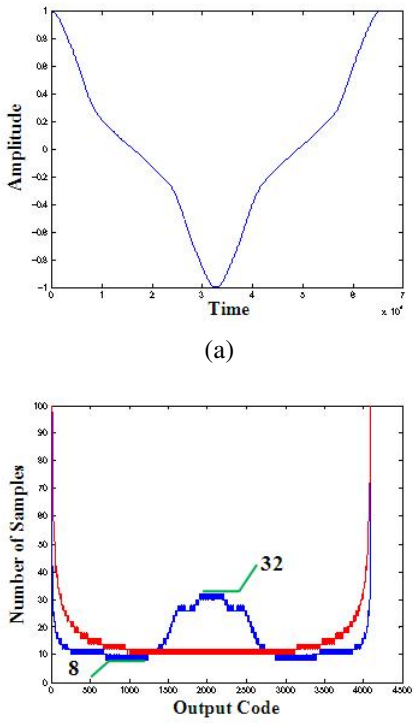

Fig. 7. Simulation result of the proposed method which increases the number of samples at center codes. (a) Input waveform. (b) Corresponding histogram is shown in blue, and the one in red is for the conventional sine wave input.

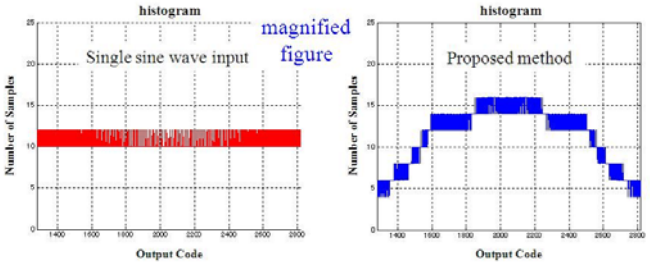

Fig. 8. Zoom of the histograms in Fig.7 (b).

TABLE I

COMPARISON OF NUMBER OF SAMPLES BETWEEN THE CONVENTIONAL SINE WAVE SIGNAL METHOD AND THE PROPOSED METHOD

Output Code	700 ∼ 960	
	Conventional	Proposed
Samples (Minimum)	12	30
Samples (Maximum)	14	52

Output Code	960 ∼ 3130	
	Conventional	Proposed
Samples (minimum)	10	32
Samples (maximum)	12	66

Output Code	3130 ∼ 3400	
	Conventional	Proposed
Samples (minimum)	12	30
Samples (maximum)	14	52

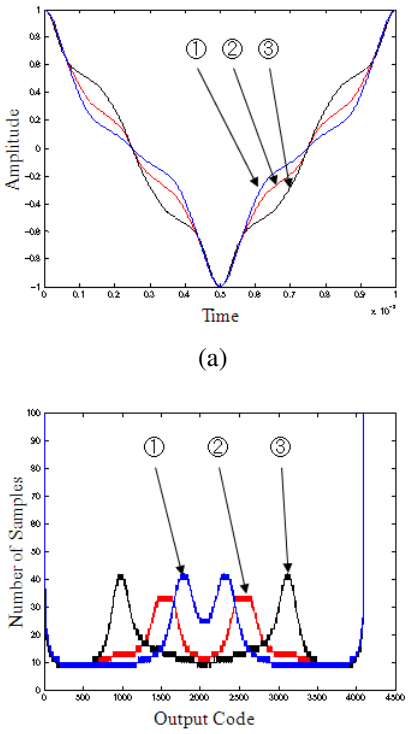

Fig. 9. Simulation results of the proposed method which increases the number of samples at other than the center codes. (a) Input waveforms. (b) Corresponding histograms.

TABLE II

TYPICAL ADC TESTING TIME WITH ATE

	Content	Time
1)	Setup time for module	less than 1 msec
2)	Settling time for module and DUT	several msec
3)	DC linearity testing time	$2^{bit} \times (16 \sim 64) \times$ (ADC conversion time)
4)	SINAD testing time	$2^{bit} \times (1 \sim 4) \times$ (ADC conversion time)
5)	Time for data transfer and operation	several msec
6)	Other test time	several msec