SAR ADC That is Configurable to Optimize Yield

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***Abstract*— This paper describes a non-binary SAR ADC architecture that is reconfigurable at production testing time to increase the number of chips that meet a given sampling speed specification, i.e. to improve yield. A non-binary SAR ADC can realize higher sampling rates than a comparable conventional binary SAR ADC, by using overlapping SA ranges so that any errors due to incomplete settling of the internal DAC can be corrected in later steps of the successive approximation. In general, using more of the overlapping successive- approximation (SA) steps (and faster steps) permits faster SAR ADC sampling rates but increases power consumption. Thus this power-speed tradeoff can be utilized to compensate for CMOS process variations of each ADC chip; if the chip is slow, we can use more-rapid SA steps and more overlapping steps to satisfy the sampling speed specification (at the cost of increasing power consumption); if the chip is fast, we can use fewer (and slower) steps to satisfy the sampling speed specification and also achieve lower power consumption. We use automatic test equipment (ATE) for production testing and to store the appropriate algorithm data that enables the sampling rate specification to be met in flash memory on the chip. The DAC output settling margin is determined by checking comparator output at each step and confirming that ADC final output is correct. Our measurements demonstrate the effectiveness of this approach.**

Keywords: SAR ADC, Redundancy, Reconfigurable, Yield, Low Power, ADC Testing

I. Introduction

This paper describes a non-binary SAR ADC architecture whose successive-approximation algorithm can be configured at production testing time to optimize both yield and power consumption. The proposed architecture enables a too-slow SAR ADC chip to be reconfigured as a faster in-spec chip that uses relatively high power; a fast SAR ADC chip can be reconfigured to use lower power yet still meet the sampling rate specification [1], [2]. Our proposed architecture uses this trade-off between power and speed to choose the optimal algorithm that compensates for CMOS process variations between chips. An ATE is used to determine speed margin and set the optimal algorithm. DAC output settling margin is determined by checking comparator output at each step and confirming that ADC final output is correct.

We present these principles and algorithms in the following sections, and show measurement and simulation data that validates this approach.

II. Successive Approximation Algorithm

A. Binary search algorithm

We here describe the conventional binary search algorithm that realizes an N-bit resolution SAR ADC with N steps (Fig.1), and we assume that the analog input range is normalized from 0 to $2^N - 1$. The comparator compares the analog input (V_{in}) and the reference voltage (DAC output), and its output $s(k)$ at k-th step is defined by

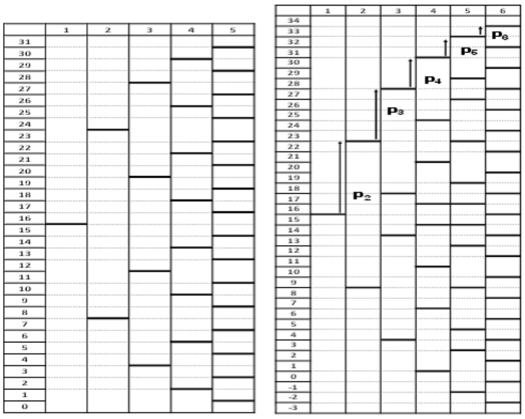

Fig. 1. Binary search algorithm of a 5-bit SAR ADC with 5 steps (Left). Non-binary search algorithm of a 5-bit SAR ADC with 6 steps (Right).

$$s(k) = \left[\begin{array}{ll} 1 & \text{(when } V_{in} > V_{ref}(k)) \\ -1 & \text{(otherwise).} \end{array} \right.$$

The reference voltage in the k-th step ($V_{ref}(k)$) is given by

$$V_{ref}(k) \quad = \quad 2^N \cdot \left(2^{-1} + \sum_{i=2}^{k} s(i-1)2^{-i}\right).$$

Also the ADC output D_{out} is given by

$$D_{out} \quad = \quad 2^{N-1} + \left(\sum_{i=2}^{N} s(i-1)2^{N-i}\right) + \frac{1}{2}(s(N)-1).$$

B. Non-binary Algorithm

We here describe our generalized non-binary algorithm that realizes N-bit resolution SAR ADC in M steps (N $\leq$ M) (Fig.1) [1], [2]. We give the reference voltage in k-th step($V_{ref}(k)$) as follows:

$$V_{ref}(k) \quad = \quad 2^{N-1} + \sum_{i=2}^{k} s(i-1)p(i). \tag{1}$$

Here $k = 1, 2, .., M$, and $p(k)$ is the value for addition to (or subtraction from) the reference voltage in the previous step. Then we have the following ADC digital output :

$$D_{out} \quad = \quad 2^{N-1} + \sum_{i=2}^{M} s(i-1)p(i) + \frac{1}{2}(s(M)-1). \tag{2}$$

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We have derived that $p(i)$ must satisfy the following:

$$p(1) \;=\; 2^{N-1}, \quad \sum_{i=1}^{M} p(i) = 2^N - 1 + 2 \cdot (\text{over-range}).$$

For the non-binary search algorithm using eq.(2), we see that there are 2^M comparison patterns (possible comparator output combinations for all M steps) and 2^N output patterns (output codes in binary format), and since M is bigger than N, 2^M is bigger than 2^N. In other words, for a given output level D_{out}, there can be multiple comparison patterns, which means that there is some redundancy. Thus even if the comparator decision in a given step is wrong, correct ADC output may be obtained in the following step.

III. DAC Incomplete Settling

A. SAR ADC Sampling Speed & DAC Incomplete Settling

We consider the incomplete settling effects of the DAC for generating the reference voltage inside the SAR ADC. We assume that the DAC is a first-order system with a time constant of τ, and the actual reference voltage (DAC output) $V_{ref}^{act}(k)$ at k-th step is given by

$$V_{ref}^{act}(k) =$$
$$V_{ref}^{act}(k-1) \;\;+\;\; [V_{ref}(k) - V_{ref}^{act}(k)][1 - e^{-\frac{T_{step}}{\tau}}]. \quad (3)$$

Here T_{step} is the time slot for each step, The reference voltage error at k-th step due to the DAC output incomplete settling is given by

$$V_{ref,er}(k) = V_{ref}^{act}(k) - V_{ref}(k).$$

If time slot "T_{step}" is long enough, the error becomes small. Note also that the error is smaller in later steps because the change in the reference voltage between steps is smaller, and that the SAR ADC with the binary algorithm has to wait for the DAC to settle within 1/2 LSB in each step (Fig.2 (a)). The non-binary search algorithm can correct for error due to incomplete DAC settling in the previous step, and we do not have to wait for the DAC to settle within 1/2 LSB (Fig.2 (b)).

B. Estimating DAC output settling value

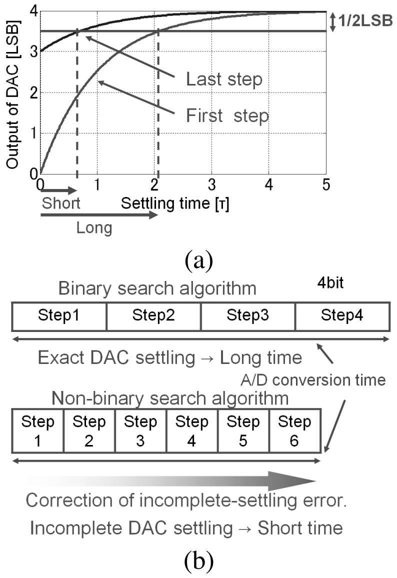
Now we discuss the algorithm for estimating the DAC output settling value at each SA conversion step. Let us consider two values of the ADC input V_{in1}, V_{in2}. The DAC output settling value $V_{DAC}(k)$ at the k-th step is between V_{in1} and V_{in2} when, for the inputs V_{in1} and V_{in2}, the comparator decision results are the same from the first to the k-th steps but they are different at the (k+1)-th step.

In other words, we can determine the DAC output settling value $V_{DAC}(k)$ at the k-th step from the measured values V_{in1} and V_{in2} in this case（Fig.3 (a)）.

$$V_{in1} \leq V_{DAC}(k) \leq V_{in2}.$$

Now we have the following algorithm for estimating DAC output settling value from the above observation:

1) We apply a ramp input signal to the SAR ADC during its test and obtain the comparator decision results for all steps, as well as the final ADC output.



(a)

(b)

Fig. 2. (a) Settling of the DAC output to generate a reference voltage at each stage. (b) AD conversion-time explanation for the binary and non-binary algorithms.

2) At the early steps (where comparator decision errors are allowable to some extent, due to overlapping steps), we find the values of V_{in1} and V_{in2} for which comparator decisions are different.
3) Let the ADC output for V_{in1} be ADC_{out1} and that for V_{in2} be ADC_{out2}. If ADC_{out1} and ADC_{out2} are equal, then the DAC output settling value is the reference voltage multiplied by ADC_{out1} (= ADC_{out2}). Else if they are different, the DAC output settling value is between the reference voltage multiplied by ADC_{out1} and that multiplied by ADC_{out2} (Fig.3 (b)).

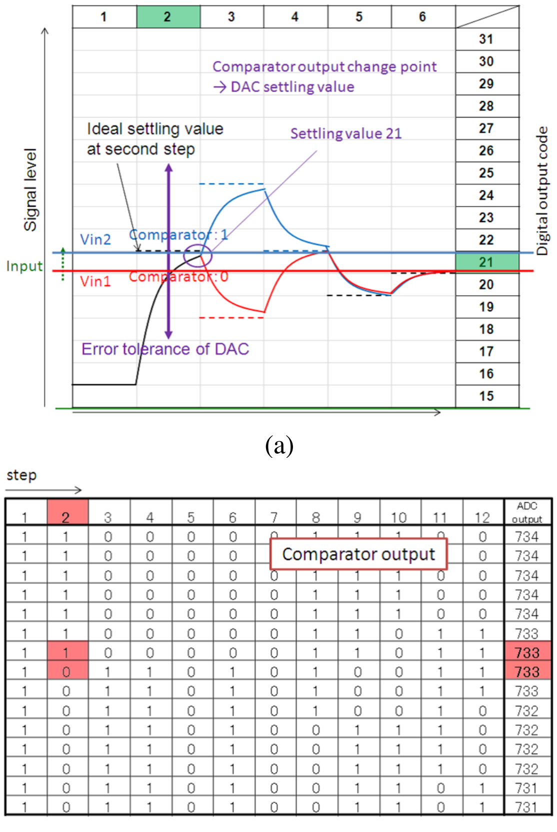
IV. SA Algorithm Selection

After estimating the DAC settling value, we can estimate the DAC time constant τ using eq.(3). As an example, we have derived the SA algorithms using simulation to meet 10b 10MS/s specification in cases of DAC time constant $\tau = 3.5ns, 4.0ns, 4.5ns$, as shown in Tables I, II, III. The number of SA steps is minimized for low power. We see that even the slow chip ($\tau = 4.5ns$) can operate at 10MS/s with appropriate choice of non-binary algorithm; if a binary algorithm is used, a slow chip cannot operate at 10MS/s and is rejected at production testing time.

In general, using more of the overlapping SA steps (and faster steps) permits faster SAR ADC sampling rates but increases power consumption.

V. Configurable Non-binary Algorithm SAR ADC

Fig.4 shows a block diagram of our proposed configurable SAR ADC; it consists of a clock generator, a timing generator (a ring counter and associated logic circuits), a comparator, a DAC for the reference voltage generation and SAR logic with a coefficient RAM (an array of DFFs) and an adder/subtracter. The coefficient RAM stores the non-binary (or binary) steps to choose the next reference level. When the comparator output is



(a)

1	2	3	4	5	6	7	8	9	10	11	12	ADC output
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	0	1	1	733
1	1	0	0	0	0	0	1	1	0	1	1	733
1	0	1	1	0	1	0	1	0	0	1	1	733
1	0	1	1	0	1	0	1	0	0	1	1	733
1	0	1	1	0	1	0	1	0	0	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	0	1	731
1	0	1	1	0	1	0	0	1	1	0	1	731

Comparator output

(b)

Fig. 3. DAC settling estimation algorithm. (a) DAC output waveform. (b) Comparator output pattern.

”1”, the RAM data is read and added to the current reference level with the adder; when it is ”0”, the data is subtracted with the subtracter. The result is applied to the DAC as its digital input.

The clock generator and timing generator are programmable so that we can select the number of steps. This configurable SAR ADC architecture allows us to set a binary or non-binary search algorithm by changing the algorithm in RAM and choosing the number of steps. .

VI. Production-time Configuration of SAR ADC

We here assume the following (Fig.5 (a)):

- The ADC output at the final step is observable from an ATE.
- The comparator output at each step is observable from an ATE.
- DAC settling time is the speed bottleneck of the SAR ADC.

During production testing (Fig.5 (b)):,

- the ATE applies a ramp input to the SAR ADC, and estimates the DAC settling time (time constant) by observing the comparator output at each step and the final ADC output.
- Based on the estimated DAC settling value, we use the ATE to calculate the optimal non-binary SA algorithm and store its parameters in flash memory. (Fig.5).

TABLE I
Fast chip (estimated DAC time constant τ = 3.5ns), 10-bit 11-step (Low power)

step	p(k)
1	512
2	256
3	115
4	63
5	35
6	19
7	11
8	6
9	3
10	2
11	1

TABLE II
Middle speed chip (τ=4.0ns), 10-bit 12-step (middle power)

step	p(k)
1	512
2	256
3	109
4	62
5	36
6	21
7	12
8	7
9	4
10	2
11	1
12	1

TABLE III
Slow chip (τ=4.5ns), 10-bit 13-step (large power)

step	p(k)
1	512
2	256
3	102
4	61
5	37
6	22
7	13
8	8
9	5
10	3
11	2
12	1
13	1

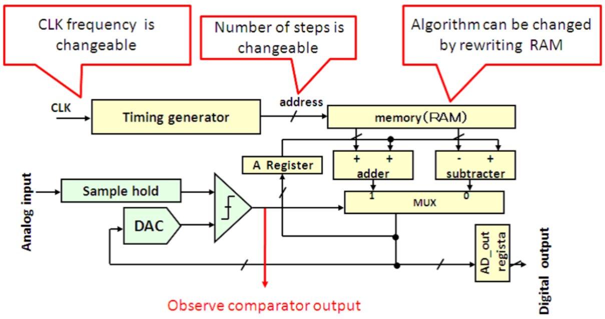


Fig. 4. Block diagram of the reconfigurable nonbinary SAR ADC.

As described above, we estimate the DAC output settling value (and hence the DAC time constant) in the non-binary-algorithm SAR ADC. Settling values may vary among chips due to CMOS process variations, hence the optimal non-binary algorithm can differ from chip to chip; the algorithm is selected to correct for error due to incomplete settling of DAC output.

The choice of optimal non-binary SA algorithm is a trade-off between power and speed: if the chip is slow, we can use more-rapid SA steps and more overlapping steps to satisfy the sampling speed specification (at the cost of increasing power consumption); if the chip is fast, we can use fewer (and slower) steps to satisfy the sampling speed specification and also achieve lower power consumption.

VII. Measurement Results

We have implemented our 10-bit reconfigurable SAR ADCs two times with a TSMC 0.18μm CMOS process to validate the effectiveness of our proposed architecture.

A. DAC Settling Estimation

Fig.6 shows ideal DAC output values (in the completely settled case) and the estimated values (in actual incomplete settled case) for the first, second, third and fourth SA conversion steps.

The first prototype SAR ADC did not have good SNDR, and we consider that this was due to DAC output ringing,

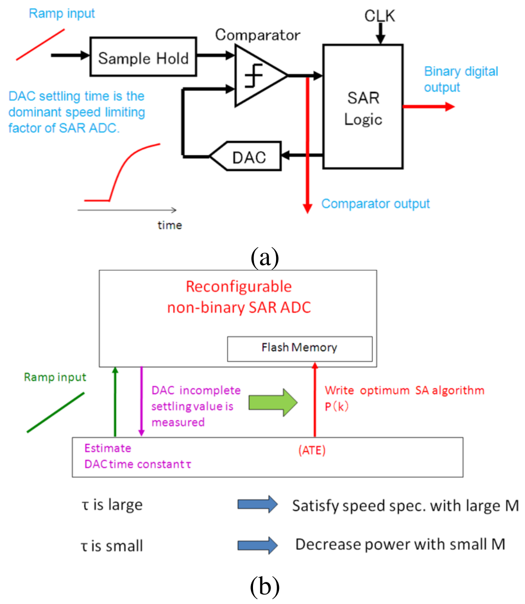


Fig. 5. Reconfiguration of the non-binary SAR ADC. (a) Test of the reconfigurable nonbinary SAR ADC. (b) Cooperation with ATE.

with overshoot and undershoot. The problem was fixed in the second prototype SAR ADC.

Fig.6 (a) shows measurement results from the first prototype chip. We see that the estimated DAC output shows overshoot/undershoot, which is probably due to DAC output ringing.

Fig.6 (b) shows measurement results for the second prototype chip which fixes the DAC output ringing problem. We see that the estimated DAC output shows the incomplete settling of a first-order system approximation, and this SAR ADC shows better performance.

We see from these measurements that our DAC settling estimation method is effective.

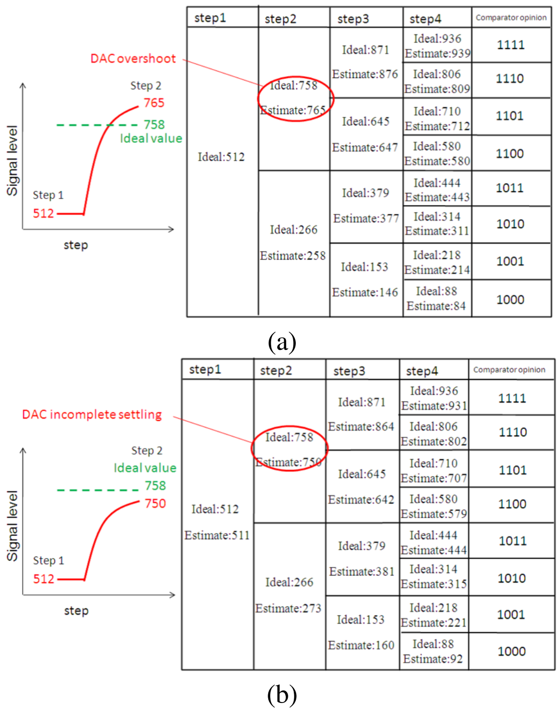
B. Speed Improvement by using faster SA Algorithm

Fig.7 shows a SNDR comparison of 10-step (binary) and 12-step (non-binary), algorithms for an input frequency of 100kHz, using the second prototype. We see that the 12-step non-binary algorithm achieves better speed performance than the 10-step binary algorithm.

VIII. Conclusion

We have proposed a non-binary SAR ADC whose algorithm can be configured at production test time to compensate for CMOS process variation between ADC chips and thus to improve yield (number of chips that satisfy the sampling-rate specification). An ATE is used to determine estimated speed margin and set the optimal algorithm. We have shown measurements and simulations of our SAR ADC design that validate the effectiveness of the proposed architecture.

We conclude this paper by remarking that most of the reconfigurable ADCs proposed by several researchers are reconfigurable to satisfy different specifications, but our reconfigurable ADC proposed here is reconfigurable to meet one sampling-rate specification and save slow chips that would otherwise be rejected – a new concept, we believe.



step1	step2	step3	step4	Comparator opinion
Ideal:512	Ideal:758 Estimate:765	Ideal:871 Estimate:876	Ideal:936 Estimate:939	1111
			Ideal:806 Estimate:809	1110
		Ideal:645 Estimate:647	Ideal:710 Estimate:712	1101
			Ideal:580 Estimate:580	1100
	Ideal:266 Estimate:258	Ideal:379 Estimate:377	Ideal:444 Estimate:443	1011
			Ideal:314 Estimate:311	1010
		Ideal:153 Estimate:146	Ideal:218 Estimate:214	1001
			Ideal:88 Estimate:84	1000

(a)

step1	step2	step3	step4	Comparator opinion
Ideal:512 Estimate:511	Ideal:758 Estimate:750	Ideal:871 Estimate:864	Ideal:936 Estimate:931	1111
			Ideal:806 Estimate:802	1110
		Ideal:645 Estimate:642	Ideal:710 Estimate:707	1101
			Ideal:580 Estimate:579	1100
	Ideal:266 Estimate:273	Ideal:379 Estimate:381	Ideal:444 Estimate:444	1011
			Ideal:314 Estimate:315	1010
		Ideal:153 Estimate:160	Ideal:218 Estimate:221	1001
			Ideal:88 Estimate:92	1000

(b)

Fig. 6. Measurement result of 10bit 12step SAR ADC. (a) DAC output ringing case. (b) No ringing case.

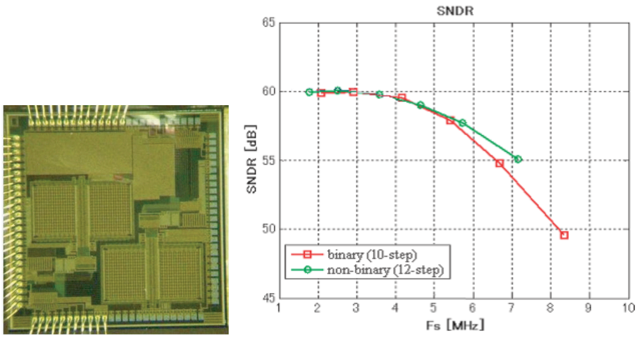


Fig. 7. (Left) Photo of the second chip (2.5mm x 2.5mm) with two SAR ADCs. (Right) SNDR comparison of 10-step (binary) and 12-step (non-binary), with respect to sampling frequency F_s.

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