Fast Testing of Linearity and Comparator Error Tolerance of SAR ADCs

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***Abstract*— This paper describes techniques, and built-in-self-test circuitry, that reduce the cost of testing SAR ADCs by enabling reduced testing time. The first technique targets DC linearity testing, and the second targets testing of nonbinary-algorithm comparator-error-tolerant SAR ADCs. Here we describe the basic concepts, and show results of some experiments. The techniques involve adding very little digital circuitry to the SAR ADCs, and they significantly improve testability and reduce testing time, so are practicable.**

Keywords : ATE, SAR ADC, Testing, DC Linearity

I. Introduction

Successive Approximation Register (SAR) ADCs embedded in microcontroller chips are now widely used in applications, such as automotive electronics, that require low cost, low power, medium speed, high accuracy and high reliability. Such ADC chips need to be production-tested using automatic test equipment (ATE).

This paper describes two techniques that enable testing time of SAR ADCs to be reduced, and thus reduce testing costs. The first technique targets DC linearity testing, and the second targets testing of non-binary-algorithm comparator-error-tolerant SAR ADCs.

Section II below provides an overview of SAR ADCs, Section III describes the technique for reducing time for testing DC linearity, and Section IV describes the technique for testing non-binary-algorithm comparator-error-tolerant SAR ADCs. Section V provides conclusions.

II. SAR ADC Overview

SAR ADC Characteristics : Low-power SAR ADCs with small chip area are widely used for high-resolution (10-14bit) and medium-sampling-speed applications, such as automotive, factory automation, and pen digitizer applications [1]- [12].

SAR ADC Configuration: An SAR ADC consists of a sample and hold circuit, comparator, DAC, SAR logic circuit and timing generator (Fig.2).

SAR ADC Binary-Search Algorithm : Conventional SAR ADCs use a multi-step binary search algorithm that realizes N-bit resolution with N steps(Fig.2).

This section explains the binary search algorithm which realizes N-bit resolution SAR ADC with N steps, and we assume that the analog input range is normalized from 0 to $2^N - 1$. The comparator compares the analog input (V_{in}) and the reference voltage (DAC output), and its output $d(k)$ at k-th step is defined by

$$d(k) = \begin{cases} 1 & (\text{when } V_{in} > V_{ref}(k)) \\ 0 & (\text{otherwise}). \end{cases}$$

We also introduce a variable $s(k)$ defined by

$$s(k) = \begin{cases} 1 & (\text{when } d(k) = 1) \\ -1 & (\text{when } d(k) = 0). \end{cases}$$

The reference voltage in the first step ($V_{ref}(1)$) is given by

$$V_{ref}(1) = 2^{N-1}.$$

If the output of the comparator in (k-1)-th step ($d(k-1)$) is "1", the reference voltage in k-th step ($V_{ref}(k)$) is given by

$$V_{ref}(k) = V_{ref}(k-1) + 2^{N-k}.$$

If the output of the comparator in (k-1)-th step($d(k-1)$) is "0", $V_{ref}(k)$ is given by

$$V_{ref}(k) = V_{ref}(k-1) - 2^{N-k}.$$

Thus

$$V_{ref}(k) = 2^N \cdot \big(2^{-1} + \sum_{i=2}^{k} s(i-1)2^{-i}\big).$$

Then, the ADC output D_{out} is given by

$$\begin{aligned} D_{out} &= d(1)2^{N-1} + d(2)2^{N-2} + ... \\ &\quad .. + d(N-1)2 + d(N) \\ &= 2^{N-1} + \big(\sum_{i=2}^{N} s(i-1)2^{N-i}\big) + \frac{1}{2}(s(N)-1). \end{aligned}$$

We see that if any comparator decision errors occur, D_{out} cannot be corrected because there is no redundancy.

Nonbinary SAR ADC Algorithm : Recently, a nonbinary search algorithm has been used to improve reliability, realizing SAR ADC N-bit resolution with M steps (M > N) using the radix $2^{N/M}$ (Fig.3) [1], [2]. In this algorithm, the reference voltages (which are different from those with the binary search algorithm) are given by

$$V_{ref}(k) = 2^{N-1} + \big(\sum_{i=2}^{k} s(i-1)\gamma^{M-i}\big).$$

Here $\gamma = 2^{N/M}$. The SAR ADC digital output is given by

$$D_{out} = 2^{N-1} + \big(\sum_{i=2}^{M} s(i-1)\gamma^{M-i}\big). + \frac{1}{2}(s(M)-1)$$

This non-binary algorithm is restricted to the radix $\gamma = 2^{N/M}$. We propose a generalized non-binary algorithm which is not restricted to the radix $2^{N/M}$ [9]-[12]

III. Faster SAR ADC DC Linearity Testing

When testing high-resolution ADCs, DC linearity is one of the most important test items, and any method of reducing testing time while maintaining test accuracy can reduce testing cost [13], [14].

When testing the SAR ADC, we know (that is, we can control) the analog input value at each sampling time, so we can reduce the number of SAR conversion steps (and hence the SAR ADC DC linearity testing time) by preadjusting the reference voltages accordingly. We here describe circuitry that can be built into the SAR ADC IC to enable such adjustment of the reference voltage to be performed during testing.

As shown in Fig.4, the reference voltage levels that correspond to testing-time DAC inputs are stored in the RAM of our SAR ADC. For DC linearity testing, suppose that the SAR ADC is supplied with a staircase ramp input with very slow slope so that the value of the ramp input is controlled (known) at each sampling time, and suppose that the SAR ADC (5-bit, 5-step in this example) would normally use a 4-step binary search algorithm during testing to confirm that linearity is acceptable. Since we know the input value at each test point, if we preadjust the corresponding comparator reference voltages to values close to the input voltages, then we do not need a 4-step algorithm; fewer steps (say, 2 steps) will be sufficient, as illustrated in Fig.5.

This reference voltage adjustment can be implemented with a small test-mode RAM and multiplexer plus a digital controller (Fig.6). In test mode, the ATE can play the role of the digital controller, hence little added circuitry is required – just the test mode RAM and multiplexer.

For an actual 10-bit binary search SAR ADC whose INL may be expected to be within $\pm$ 8 LSBs [2], we found that the number of SAR ADC steps required at each test voltage could be reduced from 10 to 4. In our experience with ATE, approximately 20% overhead time is required to set up the ADC during such DC linearity testing. Hence we can obtain (6/10) x 80% =46% testing time reduction by using the above testing methodology.

So far we have done a brief validation of this methodology using an SAR ADC chip implementation that includes the additional testing-specific circuitry. Our measurement results in Fig.7 show that the ADC output after 3 steps in testing mode is comparable to that after 10 steps of normal binary operation, which seems to validate the basic concepts of this testing methodology.

We close this section by remarking that testing and measurement are similar but different technologies. When measuring, the analog input value is uncontrollable and unknown. However, when testing, it is controllable and known.

IV. Testing comparator-error tolerance in Nonbinary SAR ADC

Nonbinary SAR ADCs that use one comparator and require M steps for N-bit resolution, where M > N – in other words, using overlapping steps – are now widely used [1], [2], [9], [10], [11], [12]. SAR ADCs using these algorithms can be more reliable and also faster than those using binary search algorithms, since the latter have to allow for settling time of the DAC inside the ADC [9], [12].

In a nonbinary SAR ADC, even if the comparator makes a wrong decision, this can be corrected in the next step due to range-overlap redundancy [9], [10], [11], [12]. However it is difficult to test and verify this comparator-error tolerance (ideally we would test this by forcing a comparator decision error and confirming that the final output is still correct)

BIST for Nonbinary SAR ADC ; We here propose simple built-in circuitry – MUX4 and associated circuits in Fig.8 – to allow us to verify comparator-error tolerance. With SEL signals in MUX4, the SAR ADC operation can be controlled;
(i) When SEL=0, MUX4 output is normal comparator output (normal operation).
(ii) When SEL=1, MUX4 output is inverted – in other words, we can force a comparator decision error.
(iii) When SEL=3, MUX4 output is forced to 0.
(iv) In case SEL=4, MUX4 output is forced to 1.

Fig.9 shows SAR ADC operation with this built-in ciruitry; in the upper path, SEL=0 (normal operation) or SEL=3 (output=1) is selected at the second stage, while in the lower path, SEL=1 (comparator decision error) or SEL=0 (output=0) is selected. The digital controller function can be part of an ATE, and hence the added digital circuitry required in the SAR ADC is minimal, so this concept is practicable.

Speed Test of Nonbinary SAR ADC ; We also propose to estimate the speed of an nonbinary SAR ADC. We assume that the nonbinary SAR ADC uses a capacitor-array DAC, and the its output behaves as a first-order system with a time constant of RC, where R is a MOS switch on-resistance and C is unit capaticitor of the DAC; Fig.10 shows the DAC output waveform at the second and third steps, where the DAC output transient starts after the DAC input decoding at the second step. For the analog input signal just below the correct reference level of the second step, the second step comparison decision may be wrong due to the DAC output incomplete settling, and from this testing we can we can estimate the decoding time (MOSFETs speed) and the RC time constant.

V. Conclusions

We have described how adding a little circuitry to SAR ADCs can reduce time for testing DC linearity, and also allow comparator-error tolerance in nonbinary SAR ADCs to be verified. Since little additional digital circuitry is required, and digital controller functions can be provided by an ATE, these concepts are practicable. Prototype chip testing has validated the basic concepts.

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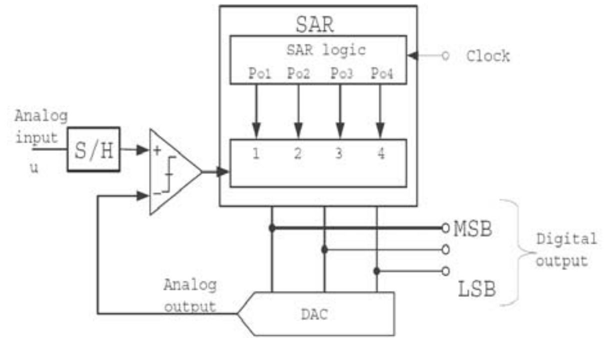

Fig. 1. Block diagram of an SAR ADC.

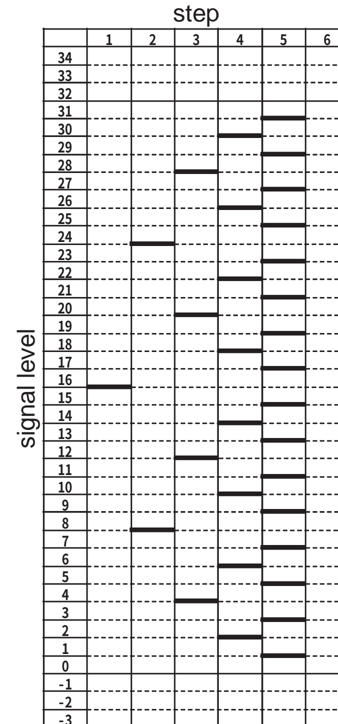

Fig. 2. Binary search algorithm of a 5-bit 5-step SAR ADC.

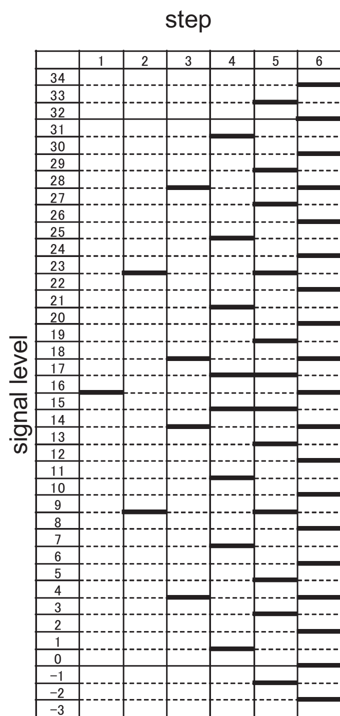

Fig. 3. Redundant search algorithm of a 5-bit 6-step SAR ADC.

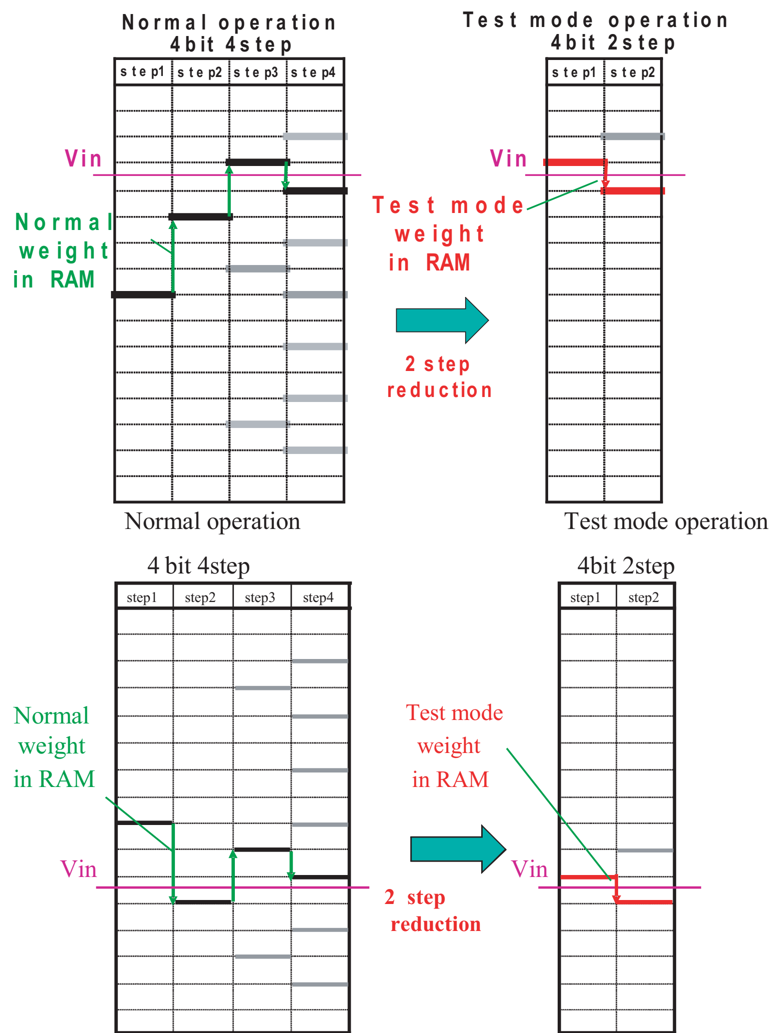

Fig. 5. Operation of SAR ADC with built-in test circuitry – the number of SAR ADC steps can be reduced from 4 to 2 in DC linearity test mode by presetting Vref corresponding to known value of analog input Vin.

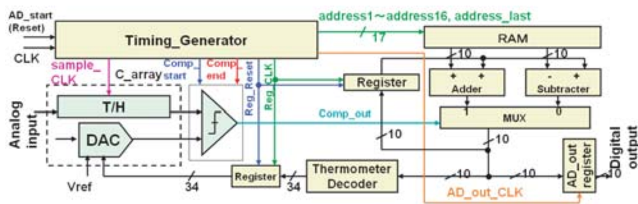

Fig. 4. Block diagram of our SAR ADC prototype with weighting coefficients RAM.

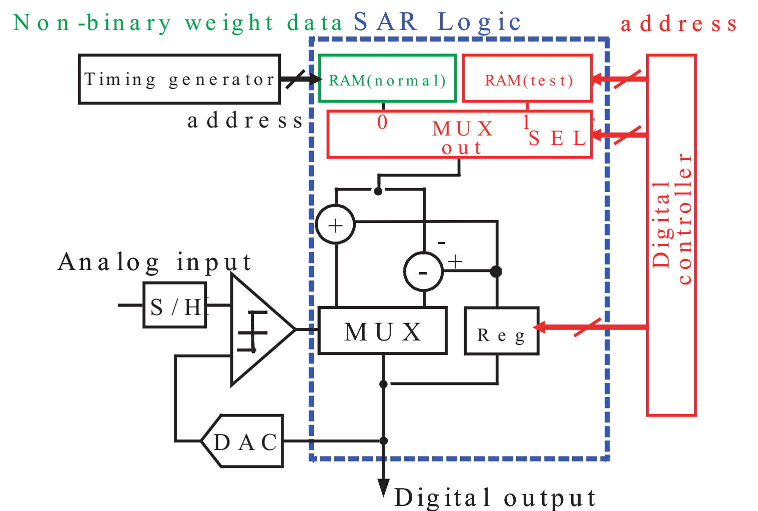

Fig. 6. SAR ADC with built-in circuitry to reduce DC-linearity testing time. The digital controller can be in an ATE.

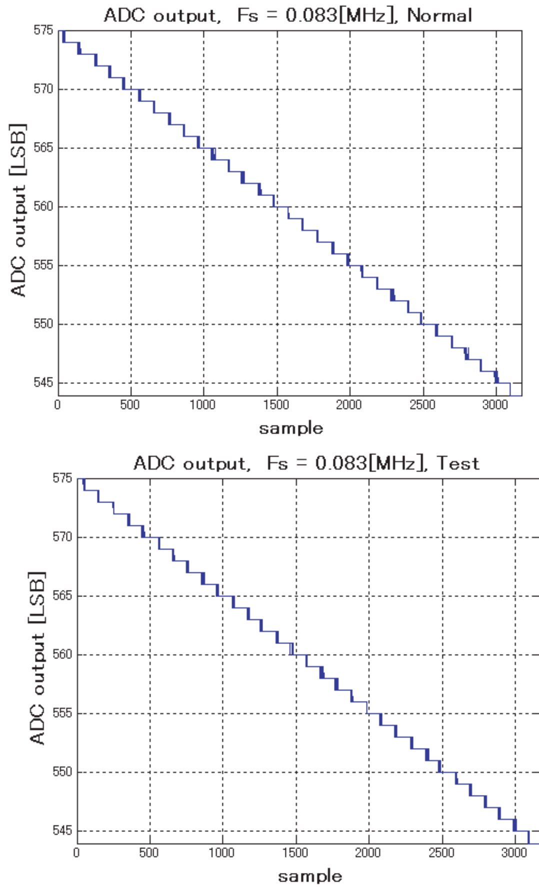

Fig. 7. Measurement results of 10bit SAR ADC chip with built-in circuitry for reducing DC linearity testing time. (a) Normal mode (10 steps). (b) Proposed test mode (4 steps).

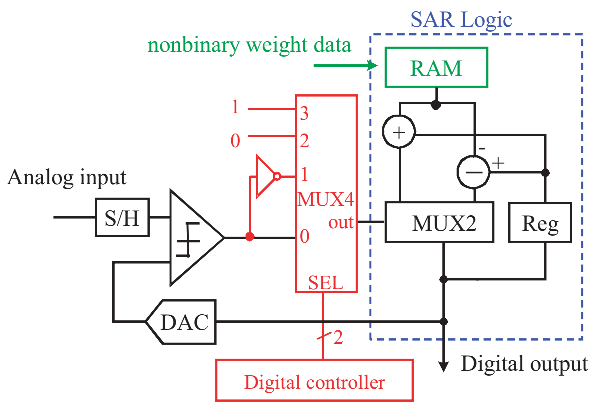

Fig. 8. Using built-in circuitry to test error tolerance in nonbinary SAR ADC.

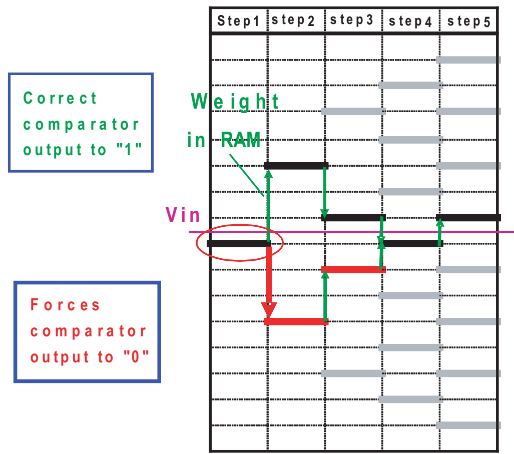

Fig. 9. Operation of built-in circuitry to test error tolerance in nonbinary SAR ADC.

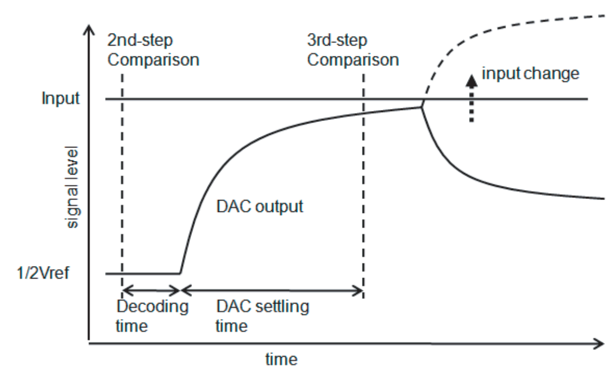

Fig. 10. DAC output settling speed testing.