Fast Testing of Linearity and Comparator Error Tolerance of SAR ADCs

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Outline

- Research purpose
- SAR ADC
- Fast testing of SAR ADC DC linearity
- Testing of comparator-error tolerance in non-binary SAR ADC
- Conclusion

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Research purpose

- Successive Approximation Register (SAR) ADCs
  - · Widely used
  - · low sampling rate, high resolution
  - · Testing time is long ⇒ Costly

⇓

- BIST for fast DC linearity testing
- BIST for SAR ADC redundancy check in cooperation with ATE

ATE : Automatic Test Equipment

BIST : Built-In-Self -Test

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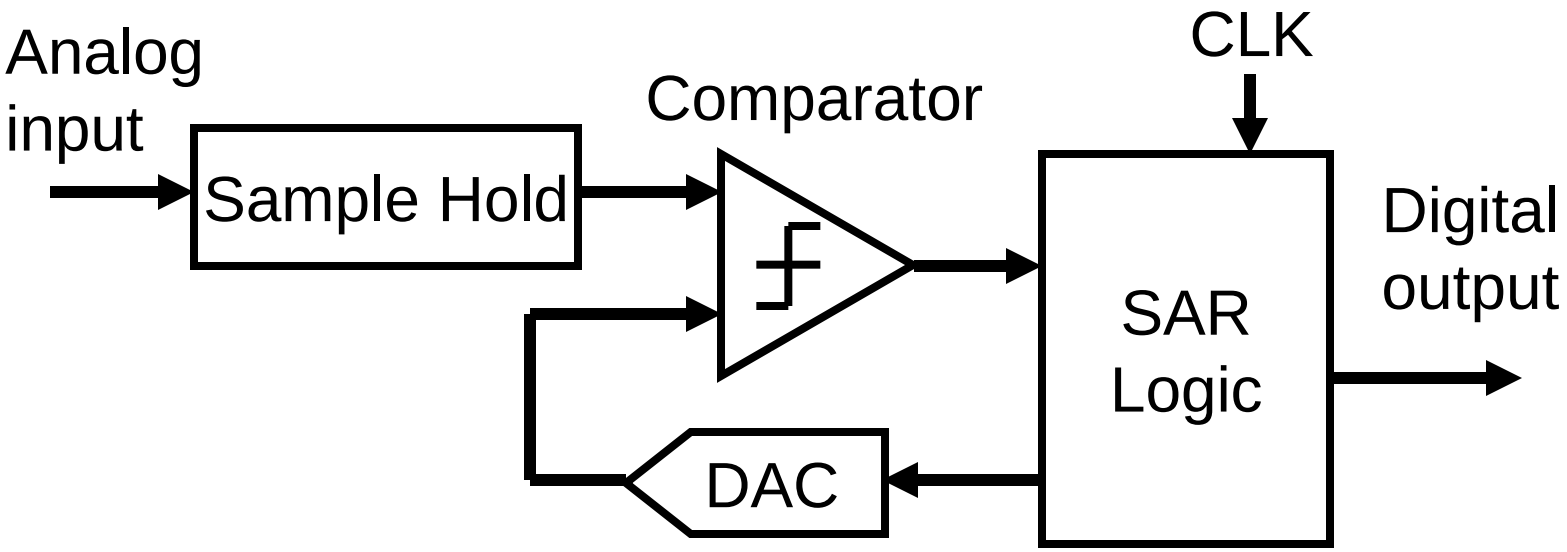
SAR ADC Block

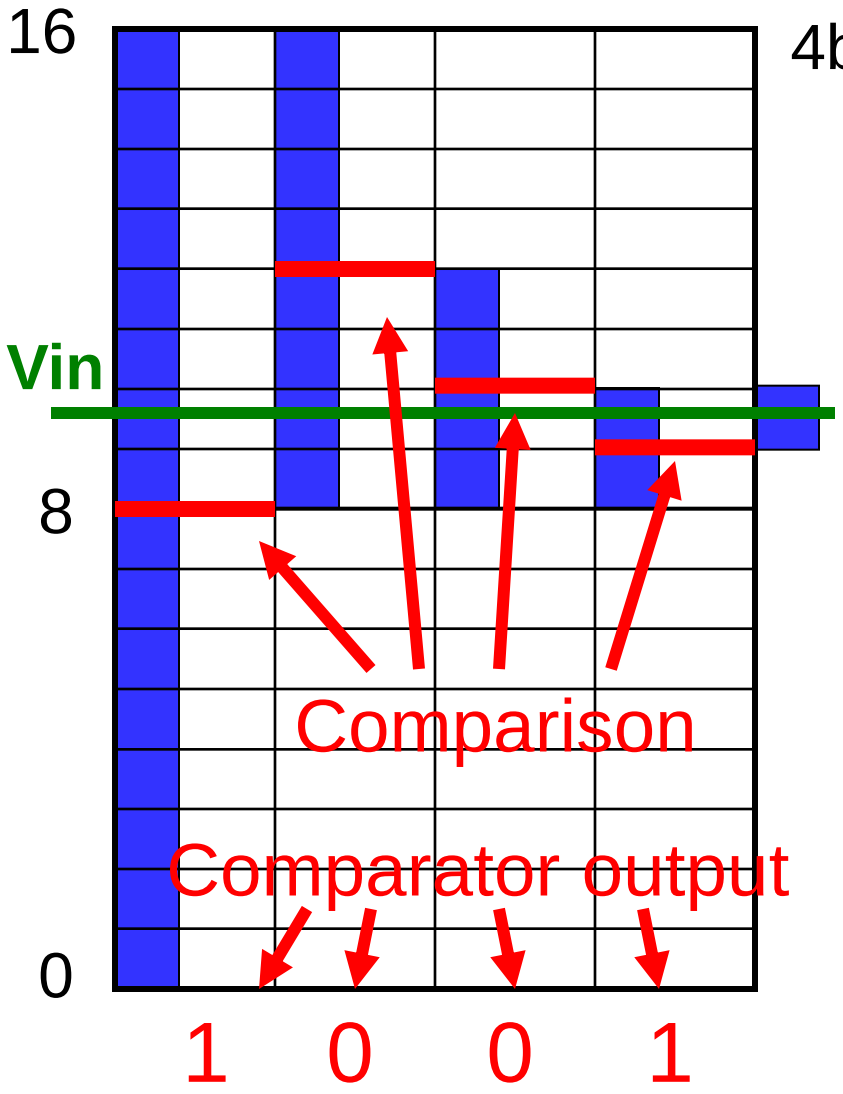


SAR ADC is digital centric.

→ Suitable for fine CMOS implementation.

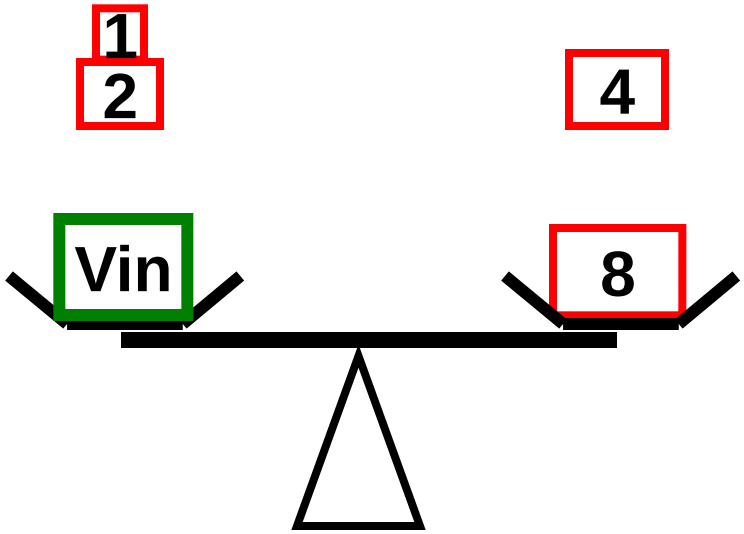
- Small chip area
- Low power
- Not use OP-amp

SAR ADC Principle Operation
- Binary search case -



4bit 4step

“Principle of a balance”



$$Vin = 8 - 2 + 1 = 9$$

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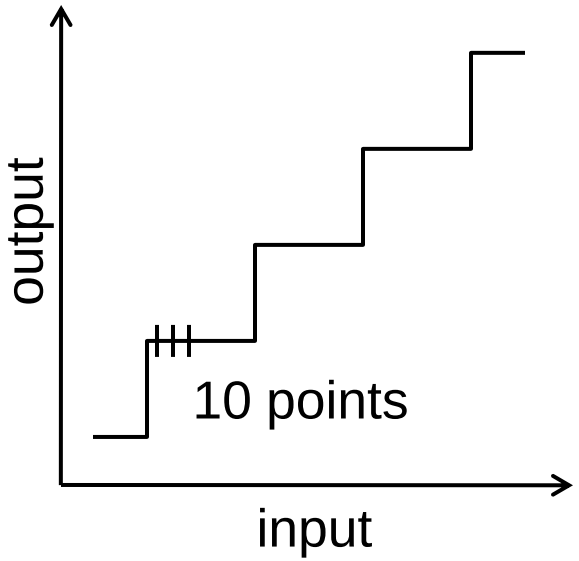
Testing time of SAR ADC

- High resolution (10bit)
- Low sampling speed (1MS/s)
- DC linearity testing time



10 bit → 1024 LSBs

10 points / 1LSB

10240 points x 1us = 10 msec

x3 Vdd change

x3 Temperature change

→ 90 msec

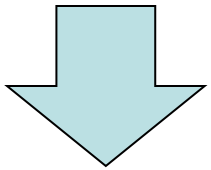
1$ chip → 1sec testing time is reasonable.

Mass volume → Even 1msec testing time reduction is significant cost reduction.

Fast testing of SAR ADC DC linearity

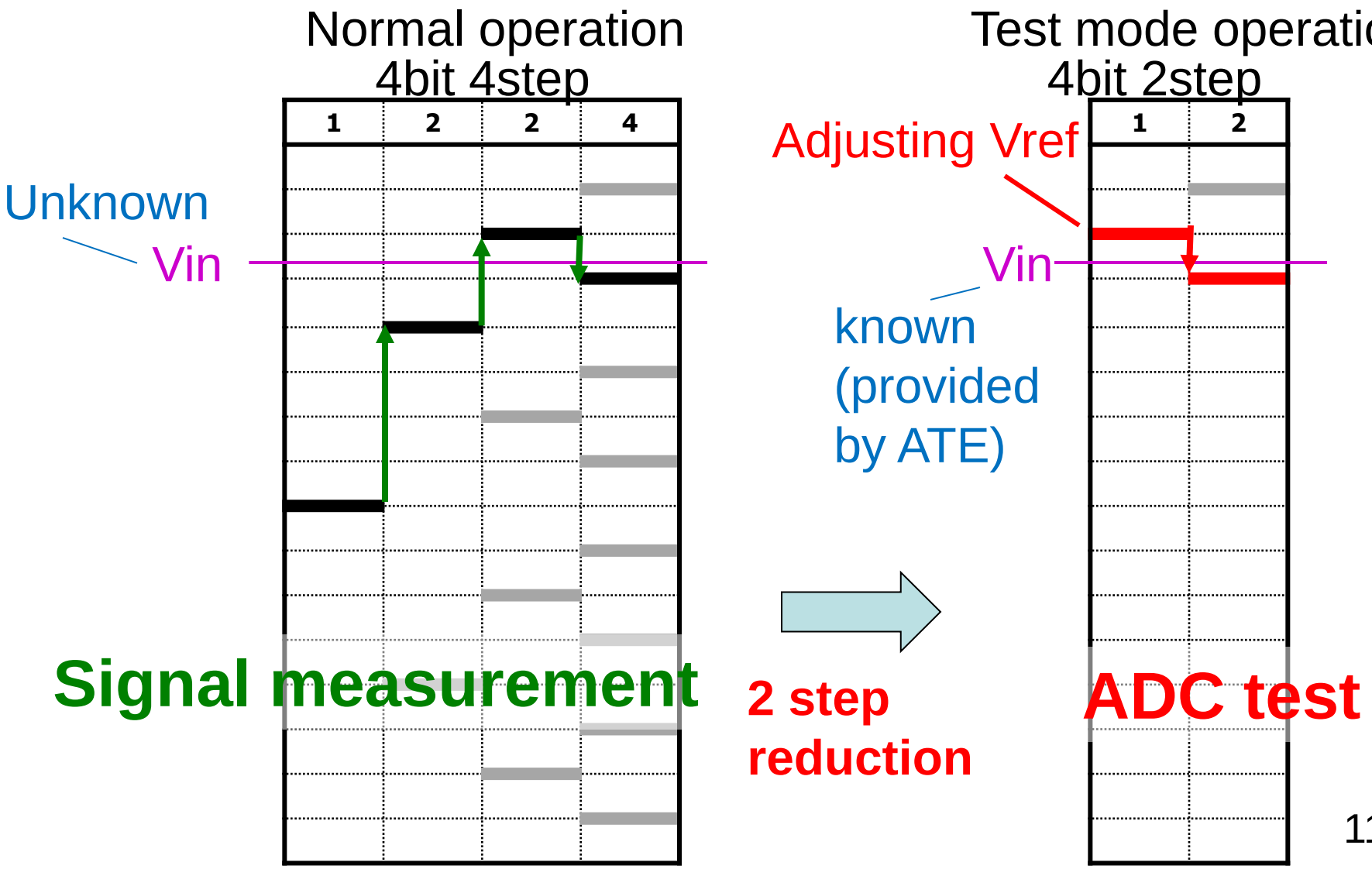
- DC linearity is the important testing item.
- Testing time reduction

  ⇨ cost reduction

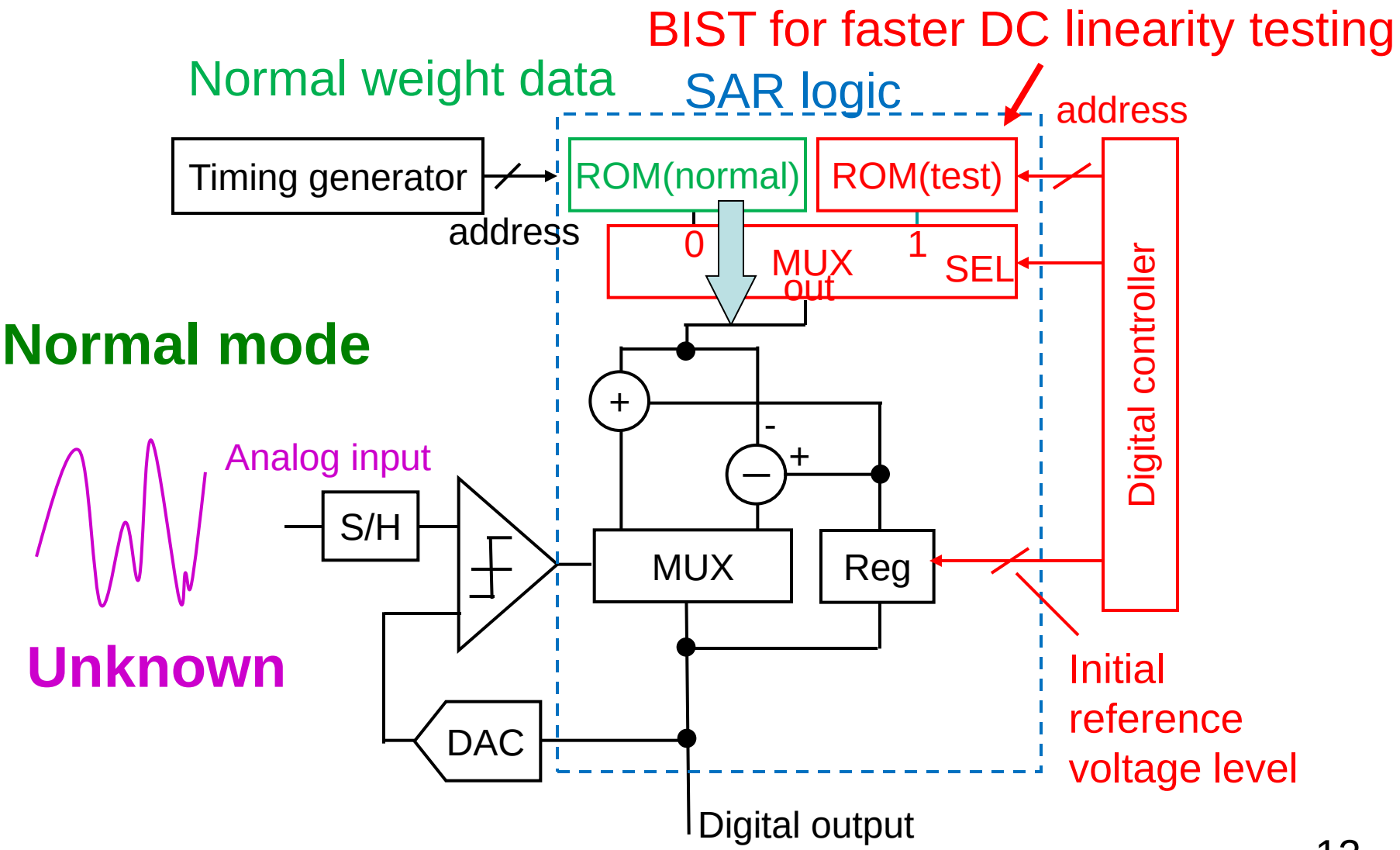


- The number of SAR conversion steps reduction during DC linearity testing.

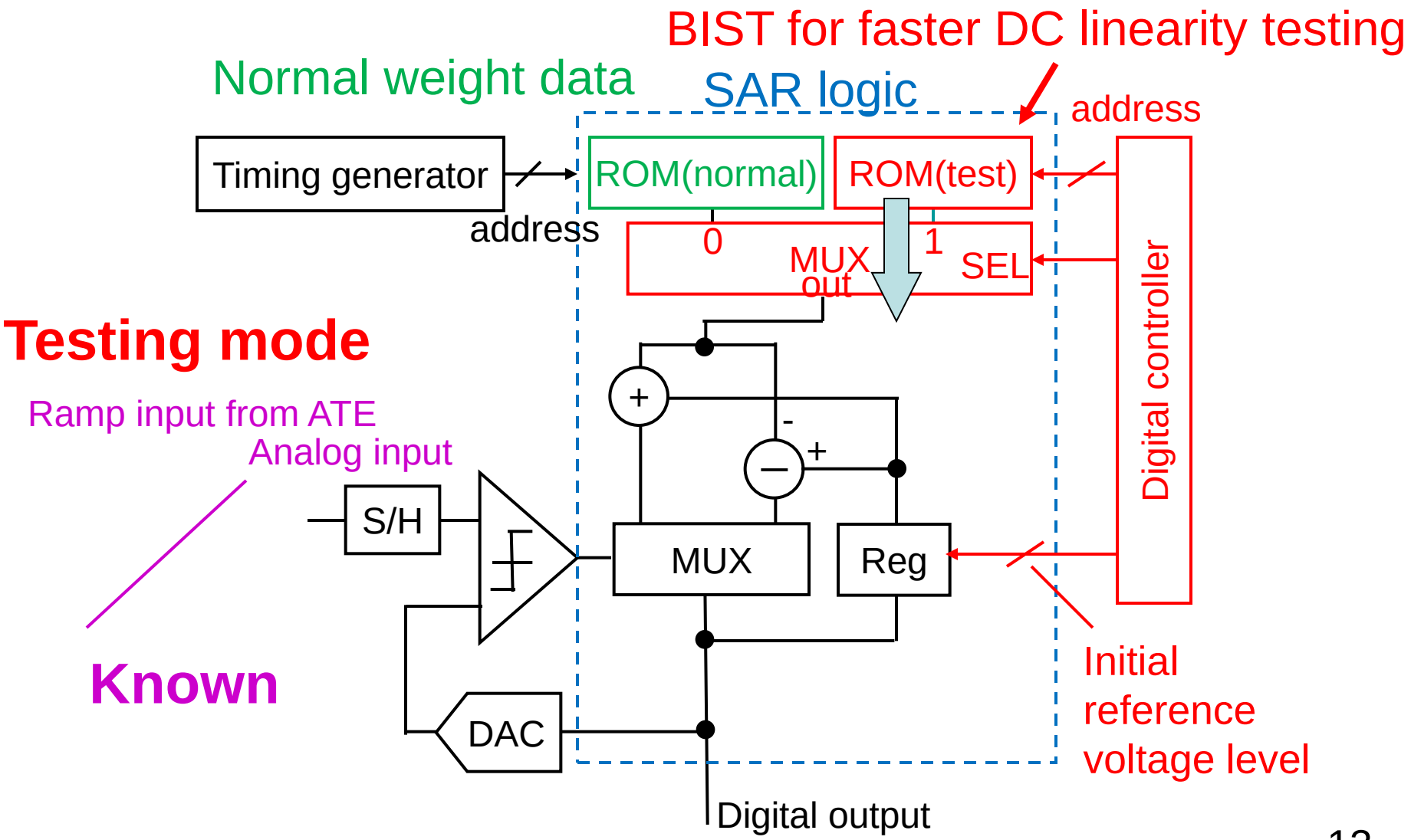
Operation of SAR ADC with BIST



SAR ADC Implementation with BIST

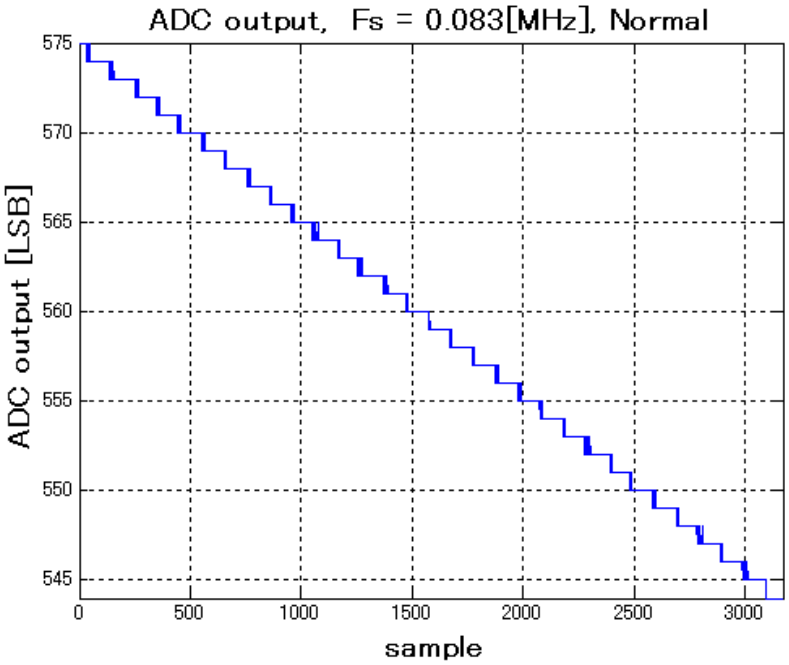


SAR ADC Implementation with BIST

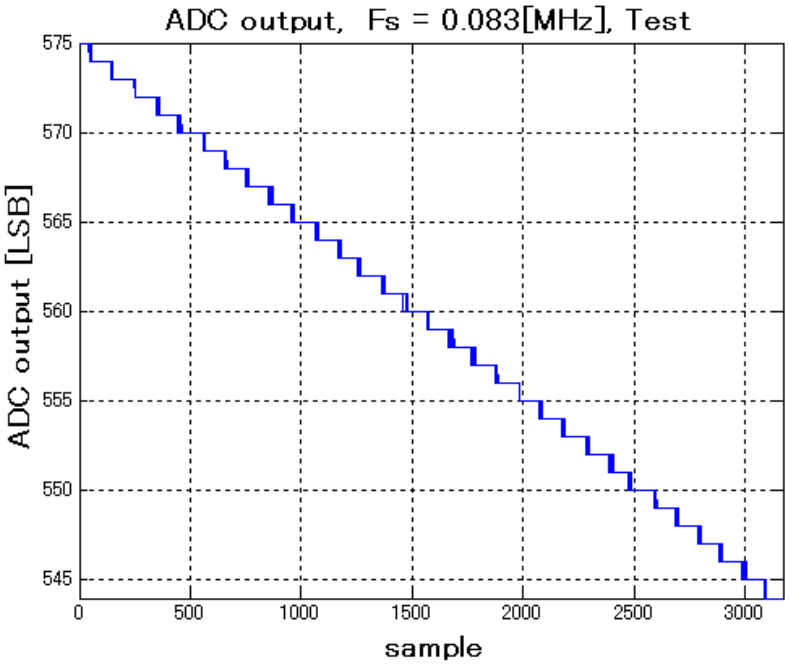


Measurement results of 10bit SAR ADC chip

10 steps normal binary operation



5 steps testing mode operation

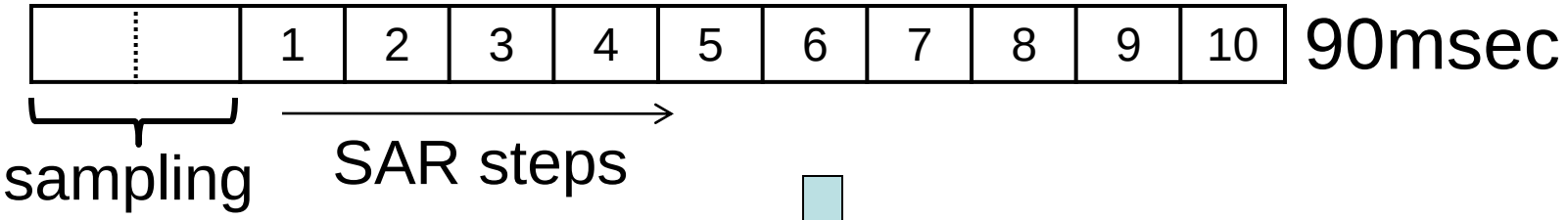


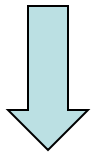
Results are equivalent.

The basic concept is validated.

Testing time reduction

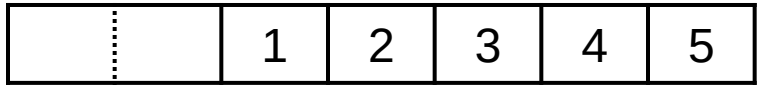
- Time of setup, settling : 10 msec
- Normal





5step reduction

- Proposed testing



- Data transfer and processing : 10 msec

Conventional : 110 msec

Proposed : 73 msec

33% reduction

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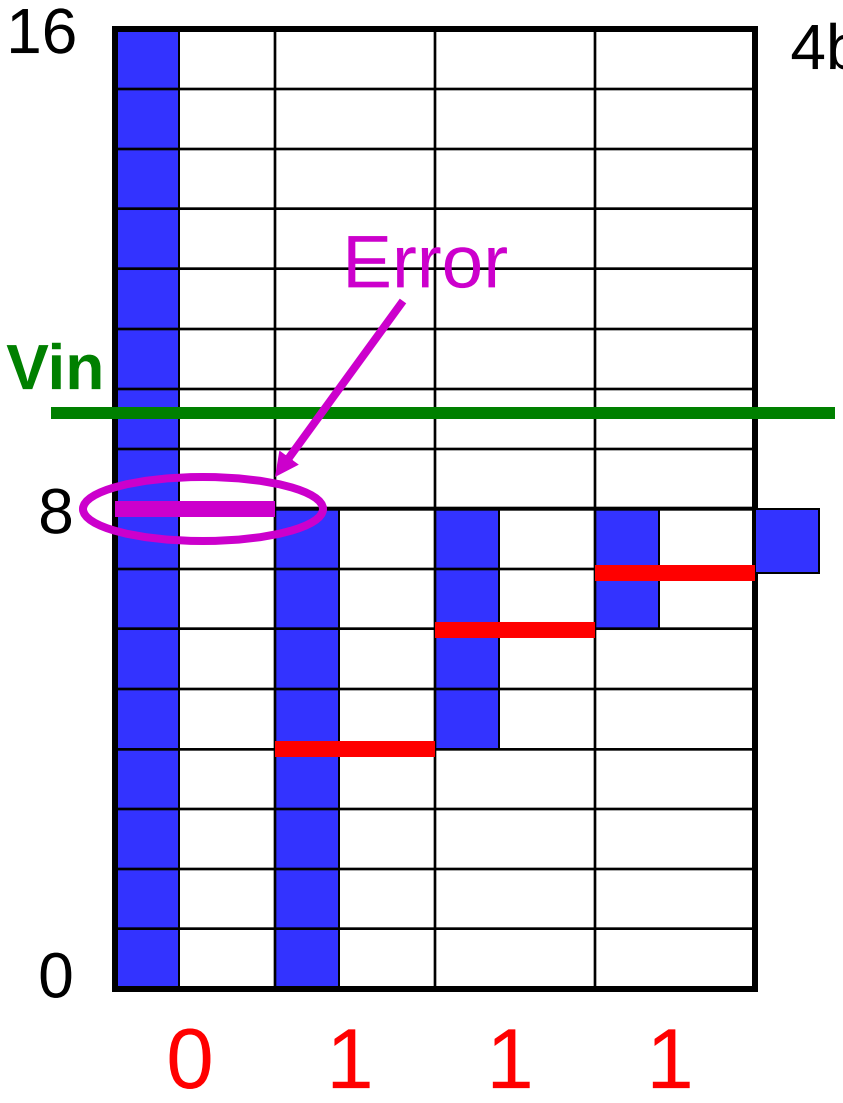
Problem of binary search algorithm



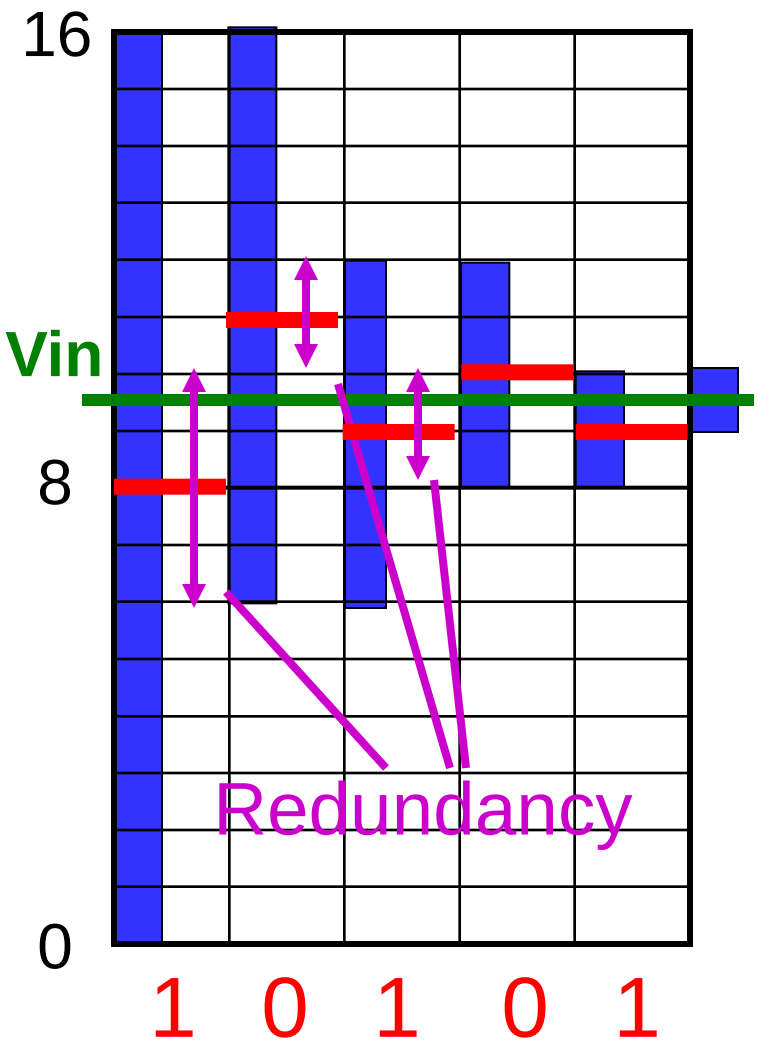
4bit 4step

No redundancy

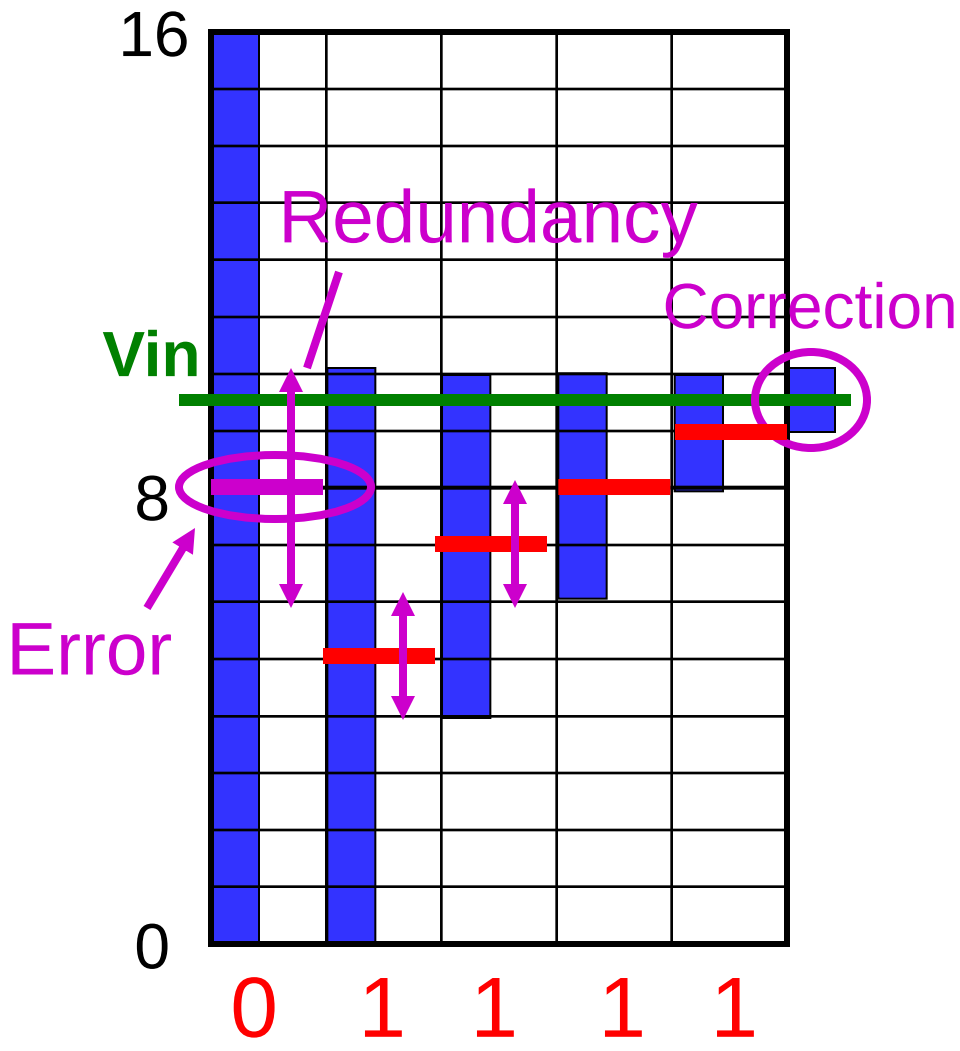
Search result has error.

Digital output has error.

Non-binary search algorithm



4bit 5step



1step redundancy

Principle of error correction

Expression of “9”

Binary search algorithm

No error correction

Comparator output : **1 0 0 1** ← Only one

Dout = 8 + 4 – 2 – 1 + 0.5 – 0.5 = 9

Non-binary search algorithm

error correction

Comparator output : **1 0 1 0 1** ← Multiple

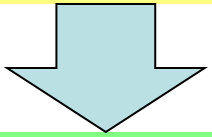
Dout = 8 + 3 – 2 + 1 – 1 + 0.5 – 0.5 = 9

Comparator output : **0 1 1 1 1**

Dout = 8 – 3 + 2 + 1 + 1 + 0.5 – 0.5 = 9

Comparator-error tolerance testing in non-binary SAR ADC

- In a non-binary SAR ADC, this comparator-error tolerance testing is difficult.



- Proposed simple BIST can check comparator-error tolerance.

  - Output patterns are multiple.

    Expression of “9”

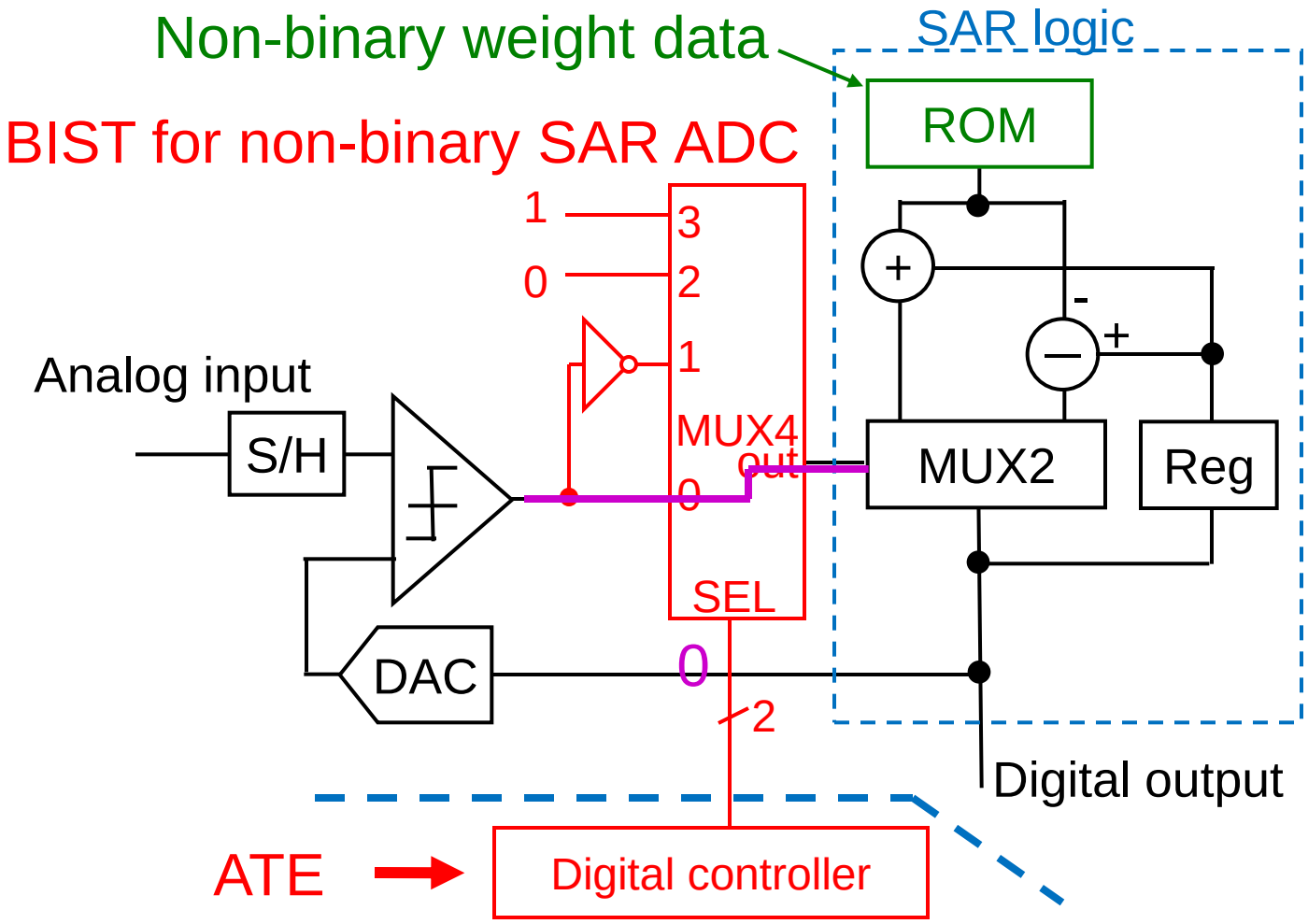
Error

0 1 1 1 1 : Comparator error path

1 0 1 0 1 : Correct path

Not controllable.

Non-binary SAR ADC with BIST



- Small additional digital circuitry.
- ATE provides digital controller functions.

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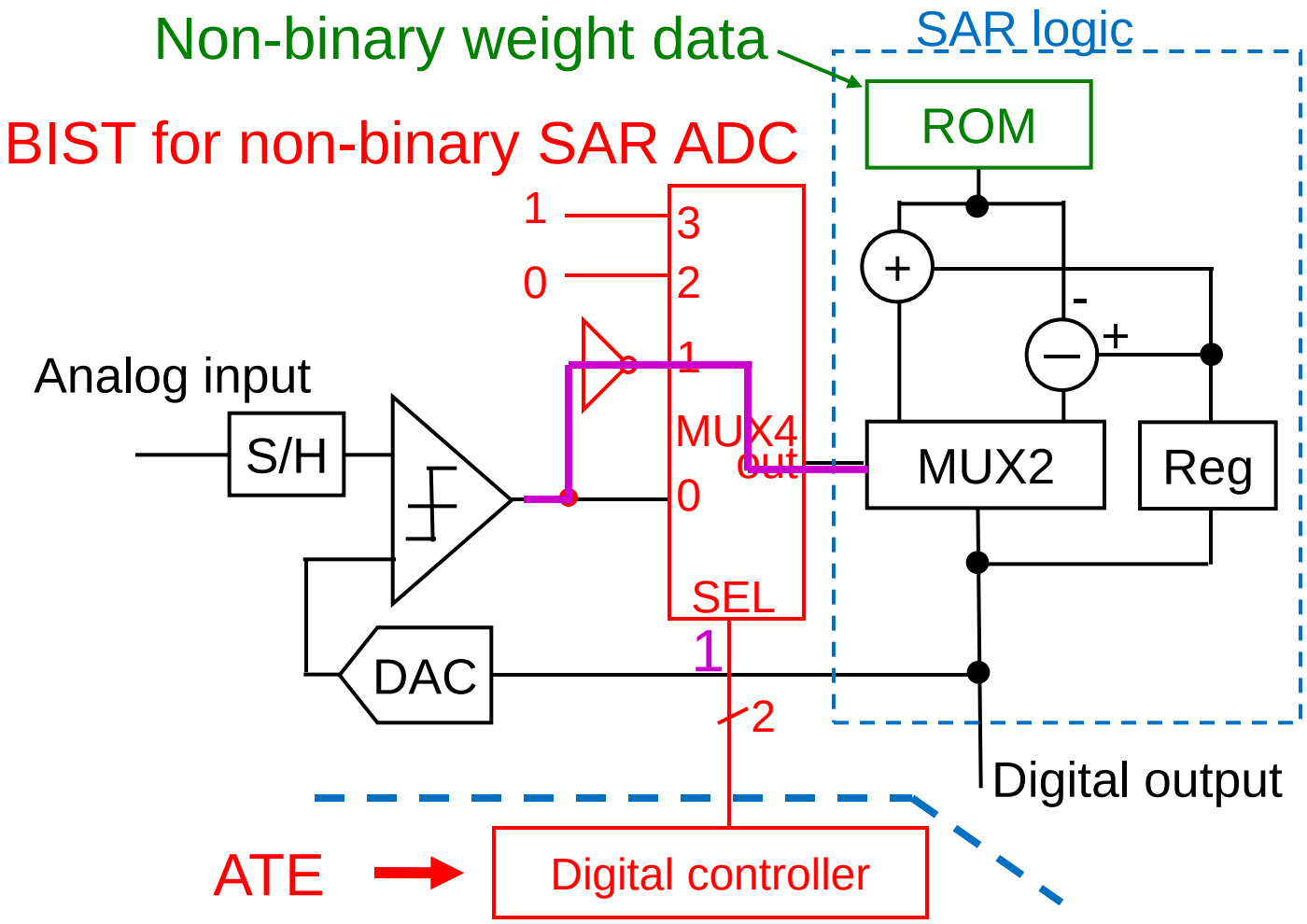

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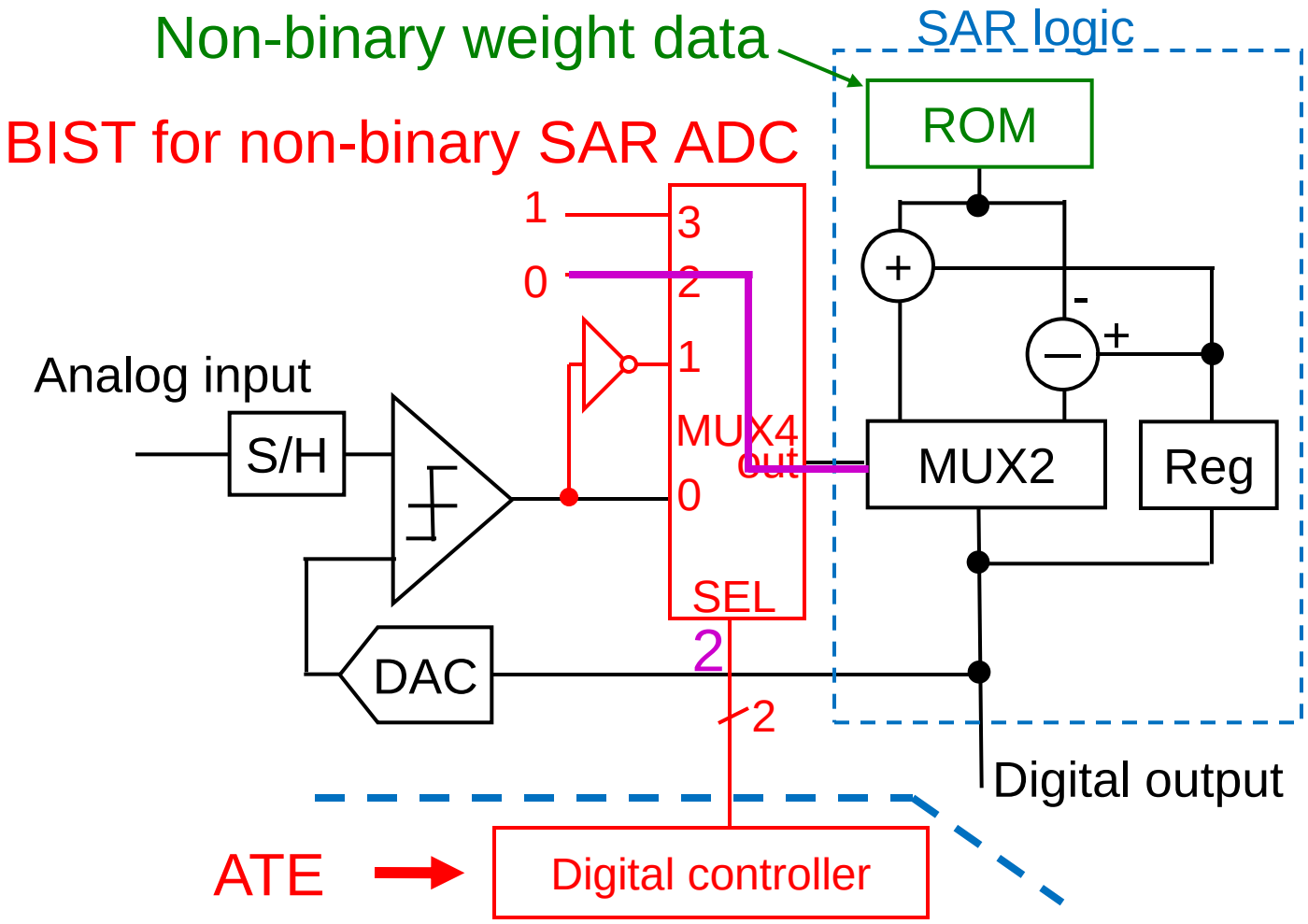

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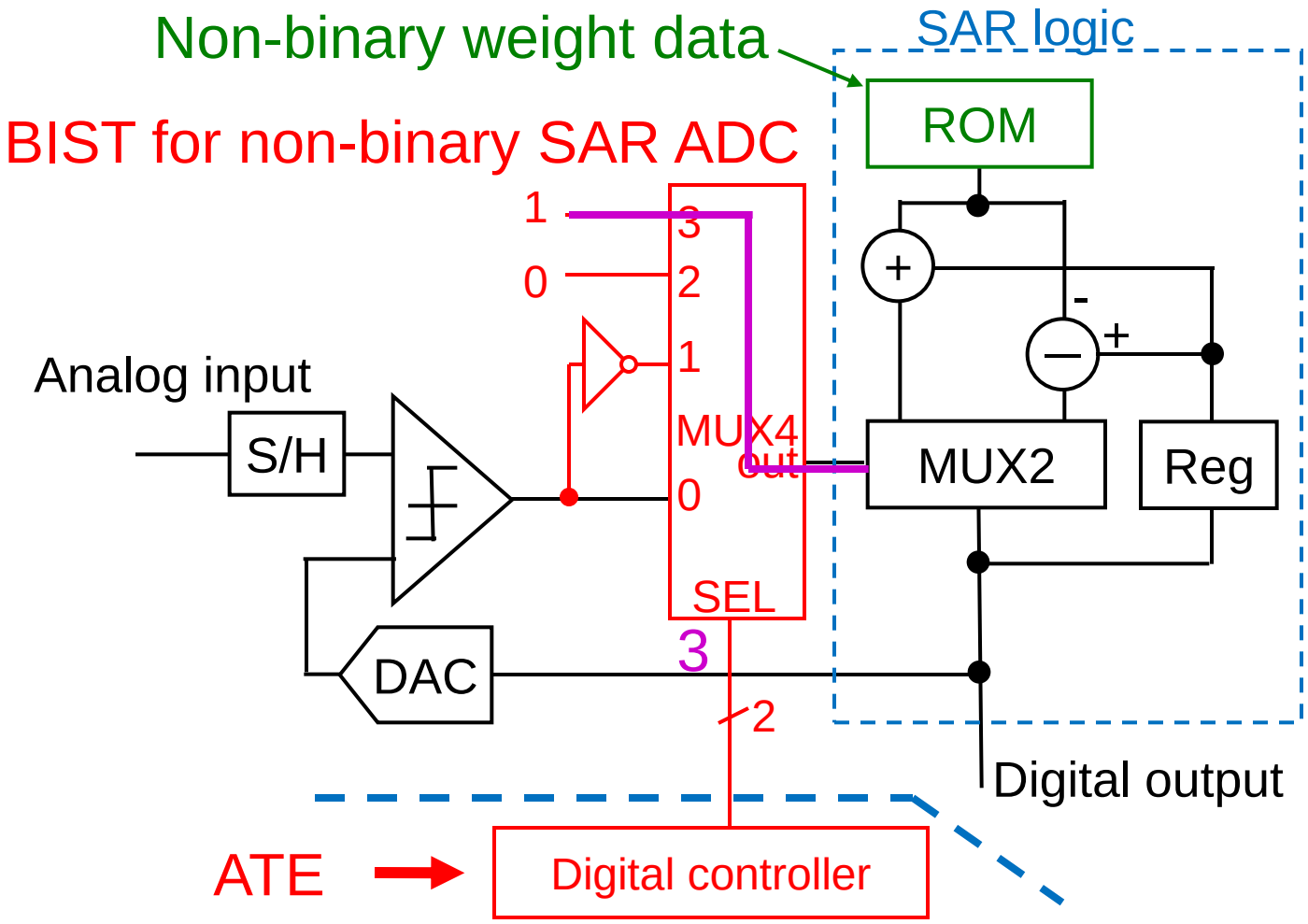

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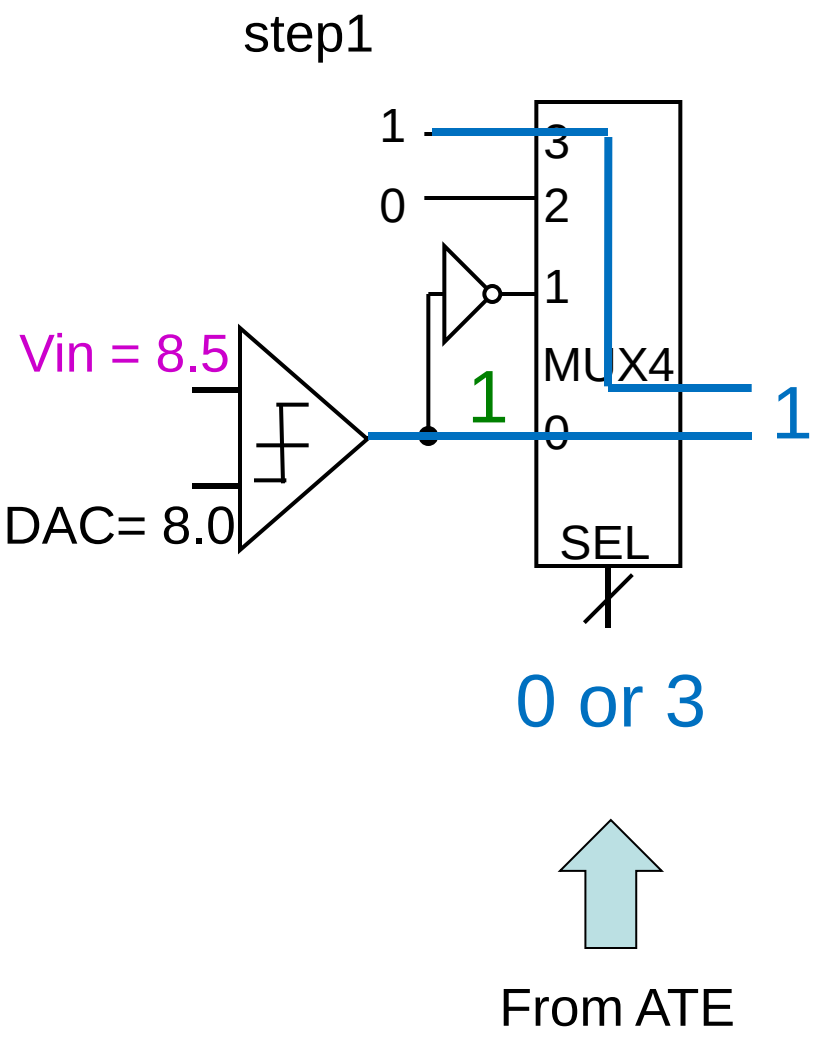
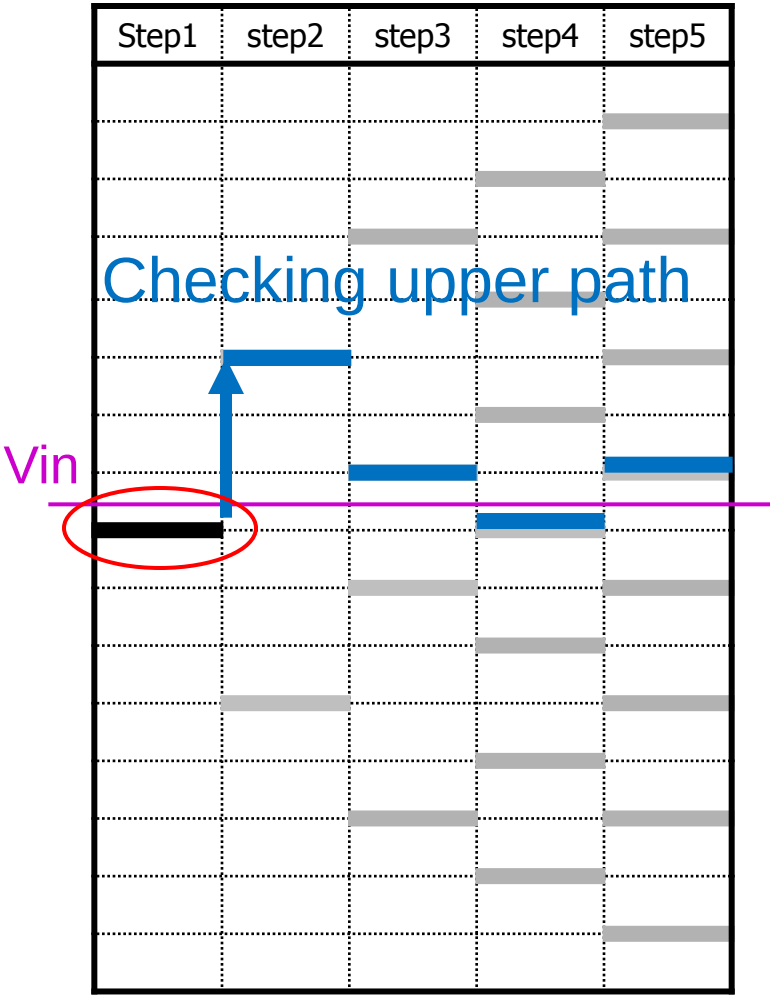
Operation of BIST to test error-tolerance in non-binary SAR ADC





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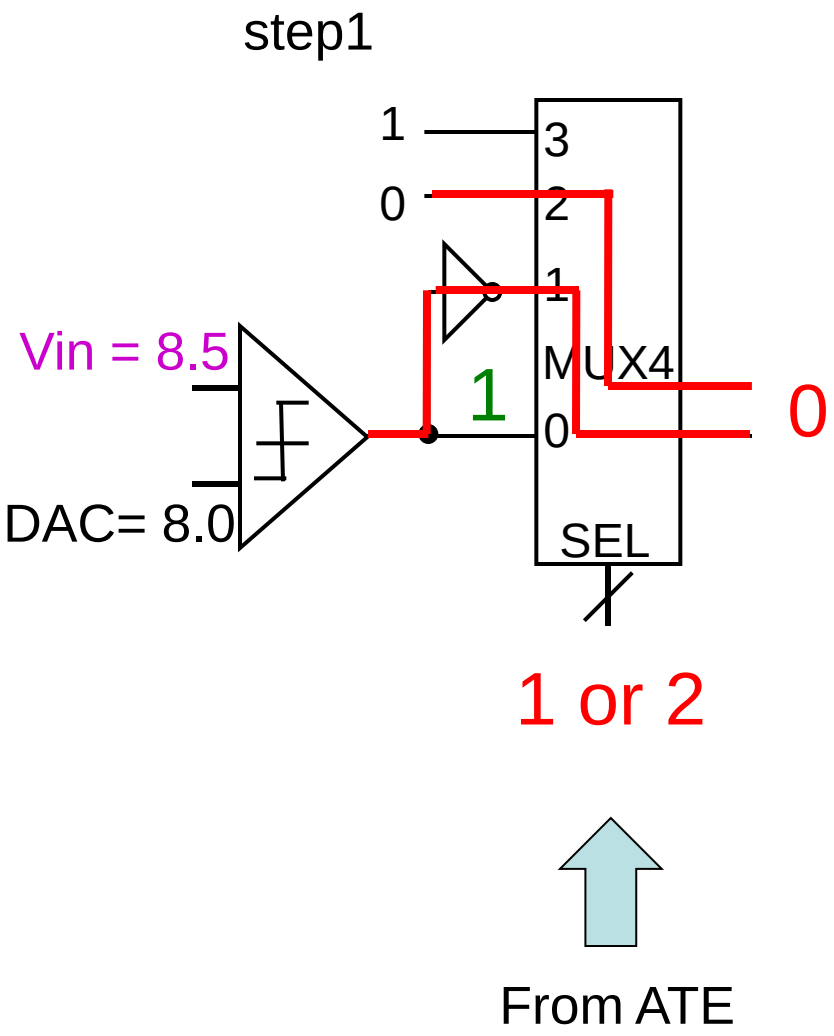

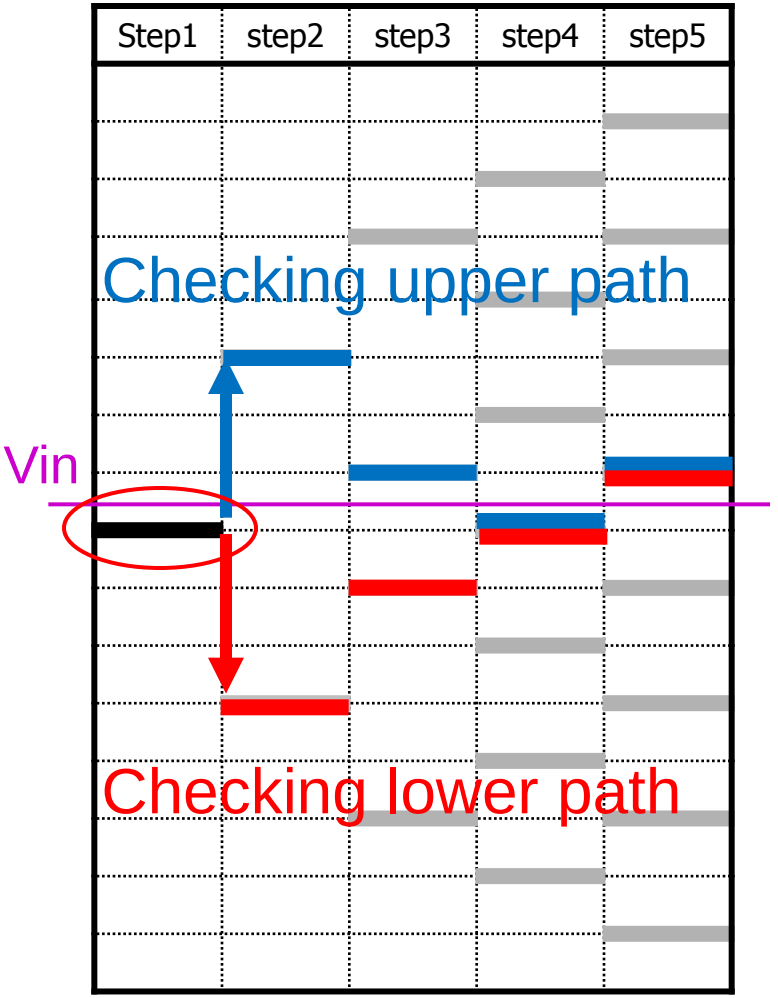

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Conclusion

We have proposed BIST for testing SAR ADCs.

- SAR ADC DC linearity testing time reduction.
  - ⇨ Measurement results validate the basic concept.
- Comparator-error tolerance check BIST in non-binary SAR ADCs.
  - ⇨ Small additional circuitry in cooperation with ATE.