

Finite Aperture Time and Sampling Bandwidth

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1. Research Objective

Sampling is an important technique for waveform acquisition, but high-frequency sampling is adversely affected by sampling circuit non-idealities such as finite aperture time [1][2]. This paper discusses the effect of finite aperture time, the lowpass action of an RC sampling circuit modeled by a switch with non-zero turn-off time τ (Fig.1). We have derived the explicit formula for the bandwidth-limiting effects of such a circuit, and show that SPICE simulation results agree well with our derived theoretical results.

2. Theoretical Results

We have derived the following rigorous transfer function for the sampling circuit with aperture time τ in Fig.1:

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{sinc(\omega\tau)}{sinc(\omega\tau) + j\omega RC} \quad (1)$$

Eq.(1) shows a lowpass action in track mode imposed by the RC pole, and another lowpass action given by a *sinc* function whose null lies at a frequency equal to the inverse of τ . The lower of the two cutoffs dominates.

3. SPICE Simulation Results

We show results of SPICE simulation using an NMOS switch with TSMC 0.18um CMOS in Fig.1. Fig.2 shows a comparison between the theoretical and simulation results for 3dB bandwidth; Fig.2 (a) shows a large discrepancy, but when the aperture time is multiplied by 1/6 in simulation as in Fig.2 (b), there is good agreement. This is because the sampling FET transitions from ON to OFF over 1/6th of the fall time of the gate voltage, which swings between V_{dd} and 0 (Figs. 3, 4). This fraction will change with FET dimensions.

4. Conclusion

We have derived a simple formula for finite aperture time effect in a sampling circuit, and confirmed its accuracy with SPICE simulation.

References

- [1] H. Kobayashi, et. al., "Sampling Jitter and Finite Aperture Time Effects in Wideband Data Acquisition Systems", IEICE Trans. Fundamentals, volE85-A, no.2, pp.335-346 (Feb. 2001).
- [2] S. Lindfors, et. al., "A 3-V 230-MHz CMOS Decimation Sub-sampler," TCAS-II, vol.50, no.30, pp.105-117 (March 2003).

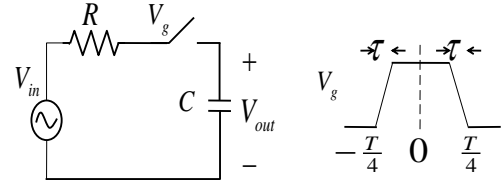
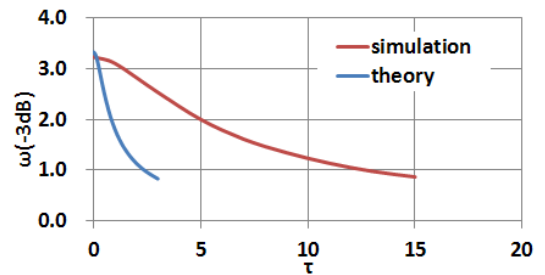
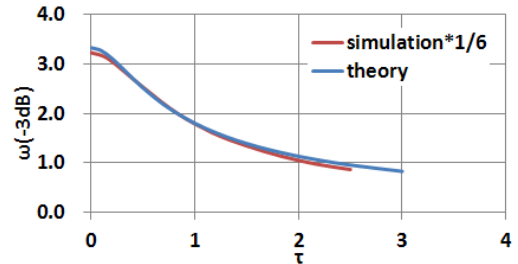


Fig.1 Sampling circuit with aperture time τ .



(a) 3dB bandwidth comparison



(b) 1/6th aperture time in simulation.

Fig.2 Simulation result with NMOS switch.

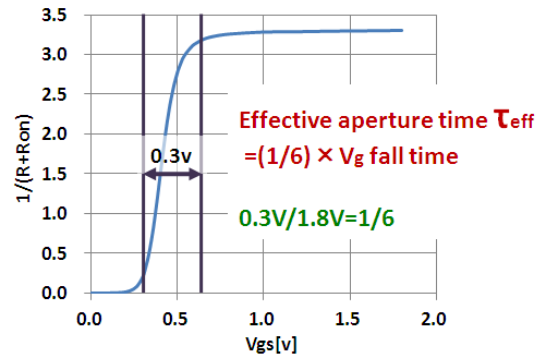


Fig.3 On-resistance with respect to V_g .

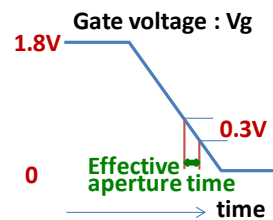


Fig.4 Effective aperture time.