APCCAS 2010

Session : Sentral Ballroom B(Hilton Kuala Lumpur)
Analog Signal Processing V
Paper ID : 1569325505

Stochastic TDC Architecture with Self-Calibration

S. Ito, S. Nishimura, H. Kobayashi, S. Uemori,
Y. Tan, N. Takai, T. J. Yamaguchi, K. Niitsu

Gunma University, Japan

Supported by STARC

12/9/2010

Outline

- Introduction
- Time to Digital Converter（TDC）
- Encoder Circuit
- Self-Calibration
- Stochastic TDC Structure
- Self-Testing Function
- Conclusions

Outline

- Introduction
- Time to Digital Converter（TDC）
- Encoder Circuit
- Self-Calibration
- Stochastic TDC Structure
- Self-Testing Function
- Conclusions

Introduction

“Fine time resolution” and “high linearity” TDC (Time to Digital Converter) is essential for jitter BIST & ADPLLs

- High linearity TDC

  →Self-Calibration circuit
- Fine time resolution TDC

  →Stochastic architecture
- High reliability TDC

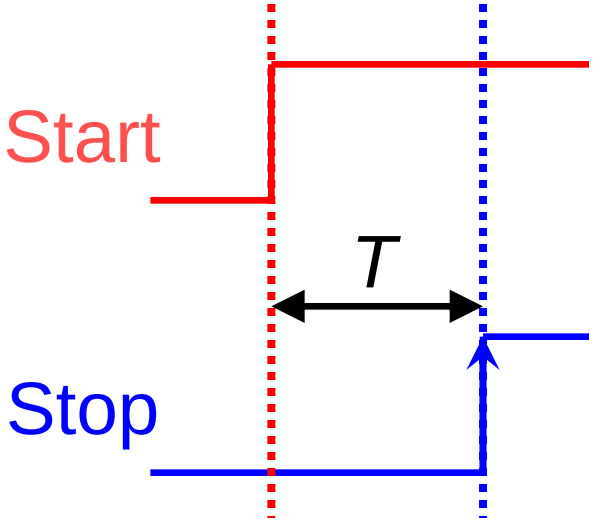
  →Self-testing capability

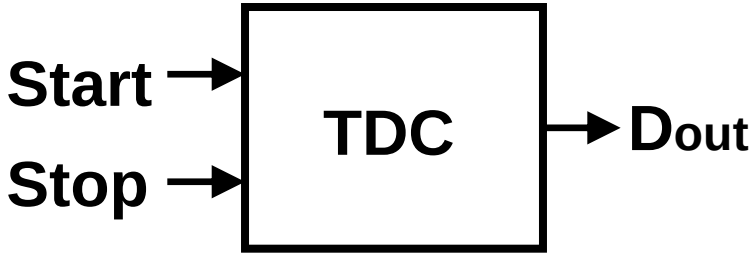
Outline

- Introduction
- Time to Digital Converter（TDC）
- Encoder Circuit
- Self-Calibration
- Stochastic TDC Structure
- Self-Testing Function
- Conclusions

Time to Digital Converter（TDC）

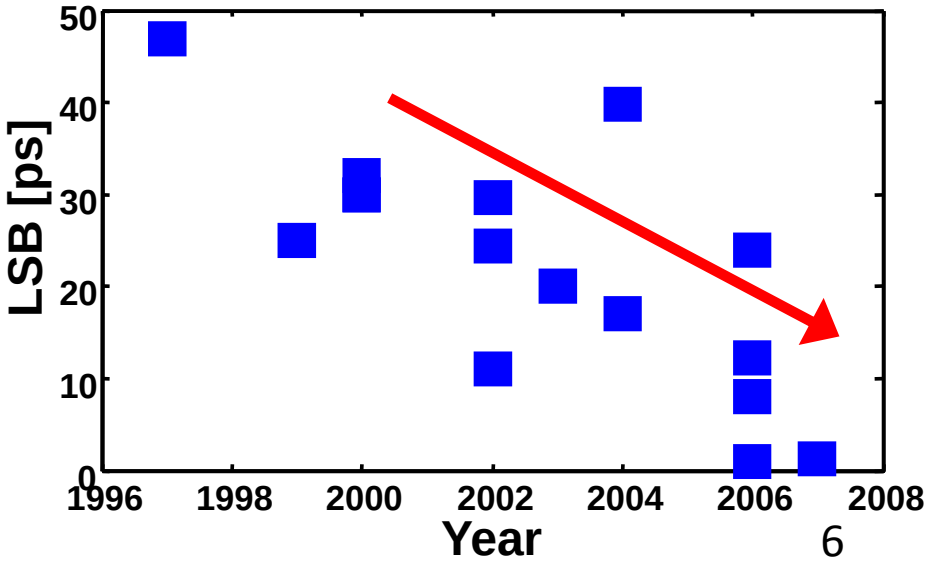
- time interval → Measurement → Digital value



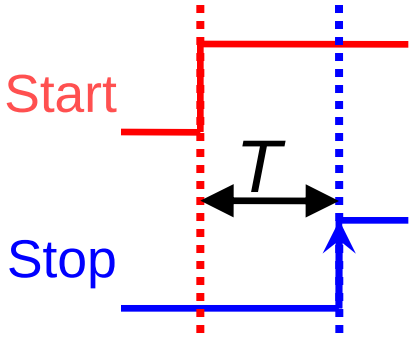


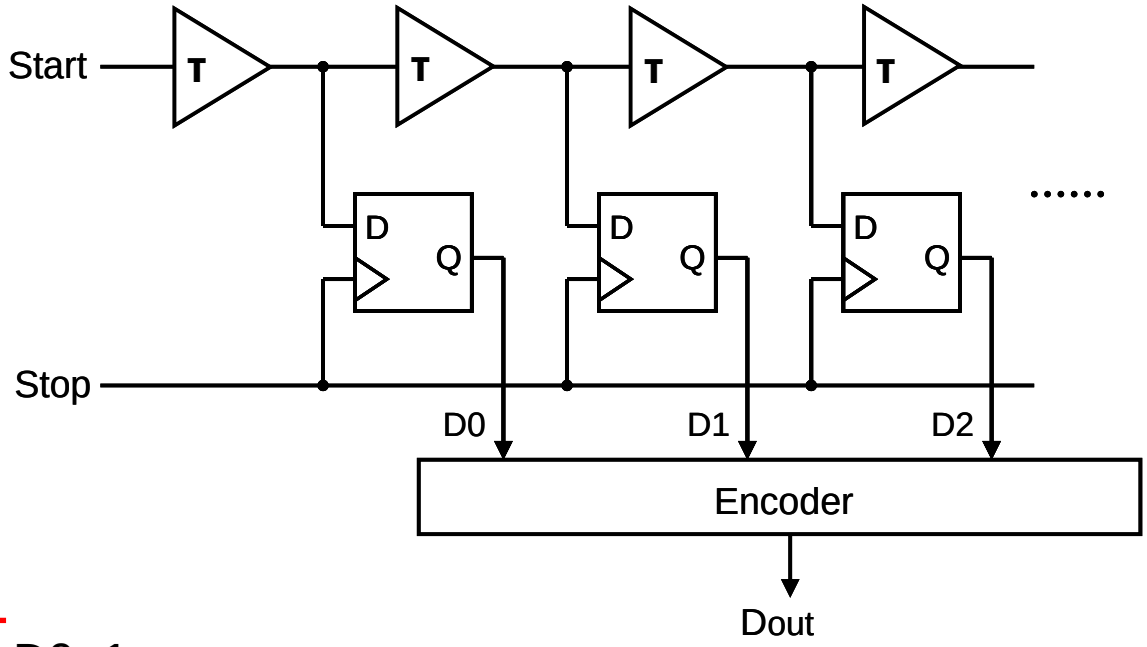
- Key component of Time-domain analog circuit
- Higher resolution can be obtained with scaled CMOS

Higher resolution with CMOS scaling

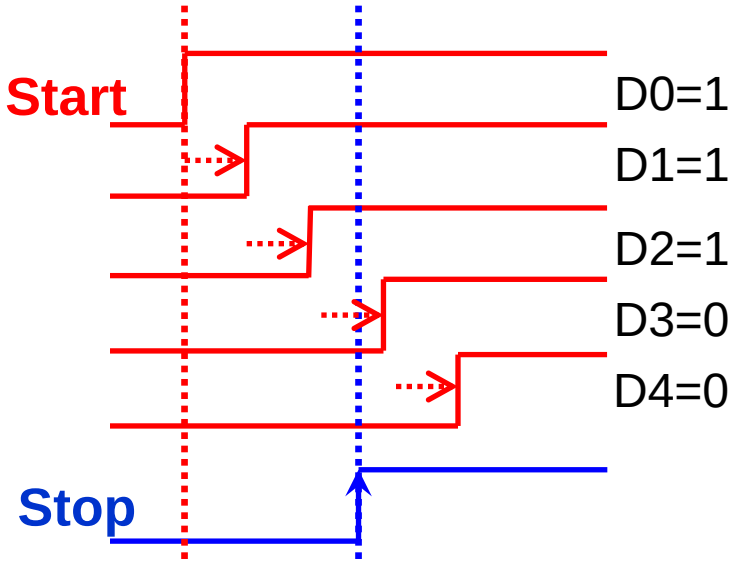


Time to Digital Converter（TDC）





Timing chart



Encoder

Thermometer code

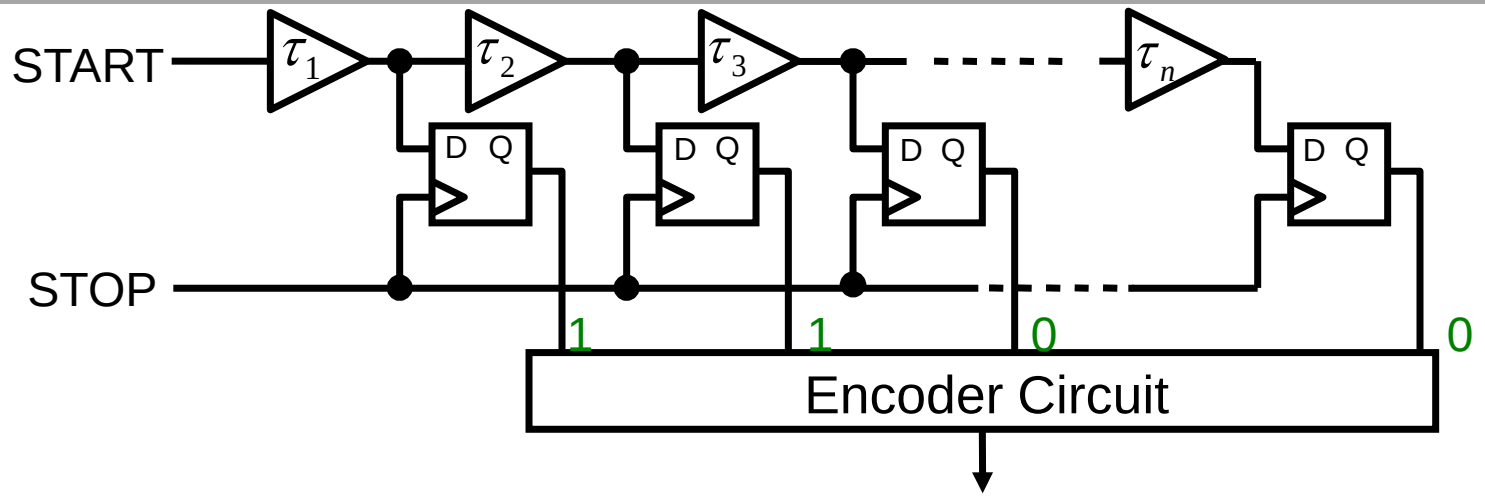
▼

binary code

Outline

- Introduction
- Time to Digital Converter（TDC）
- Encoder Circuit
- Self-Calibration
- Stochastic TDC Structure
- Self-Testing Function
- Conclusions

Encoder Circuit

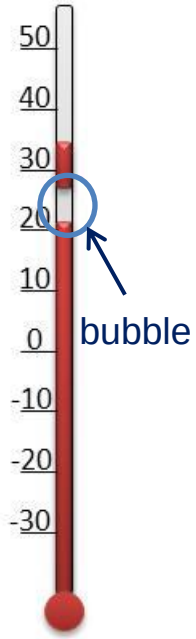


DFF outputs	Dout
0 0 0 0 0 0 0 0	0
1 0 0 0 0 0 0 0	1
1 1 0 0 0 0 0 0	2
1 1 1 0 0 0 0 0	3
1 1 1 1 0 0 0 0	4
1 1 1 1 1 0 0 0	5
1 1 1 1 1 1 0 0	6
1 1 1 1 1 1 1 0	7
1 1 1 1 1 1 1 1	8

1 0 1 0 0 0 0 0	2
1 1 1 0 0 0 0 0	3
1 1 1 0 1 0 0 0	4
1 1 1 0 1 0 1 0	5
1 1 1 0 1 0 1 1	6

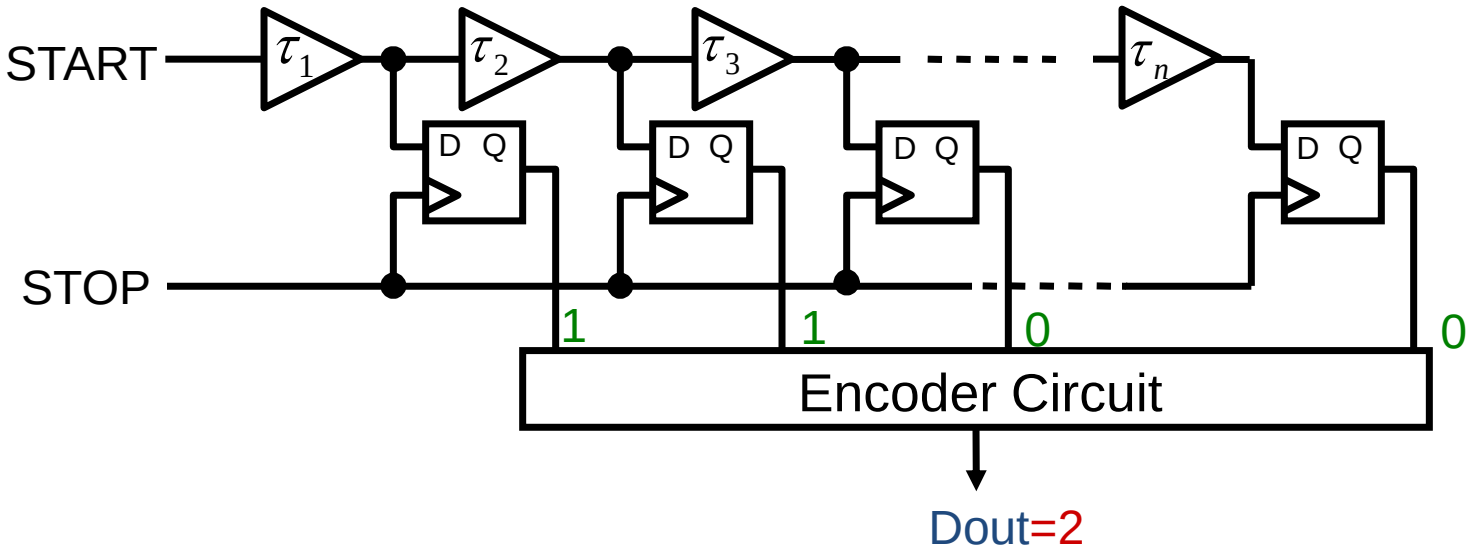
Buffer delay
DFF offset mismatch

Bubble error



thermometer

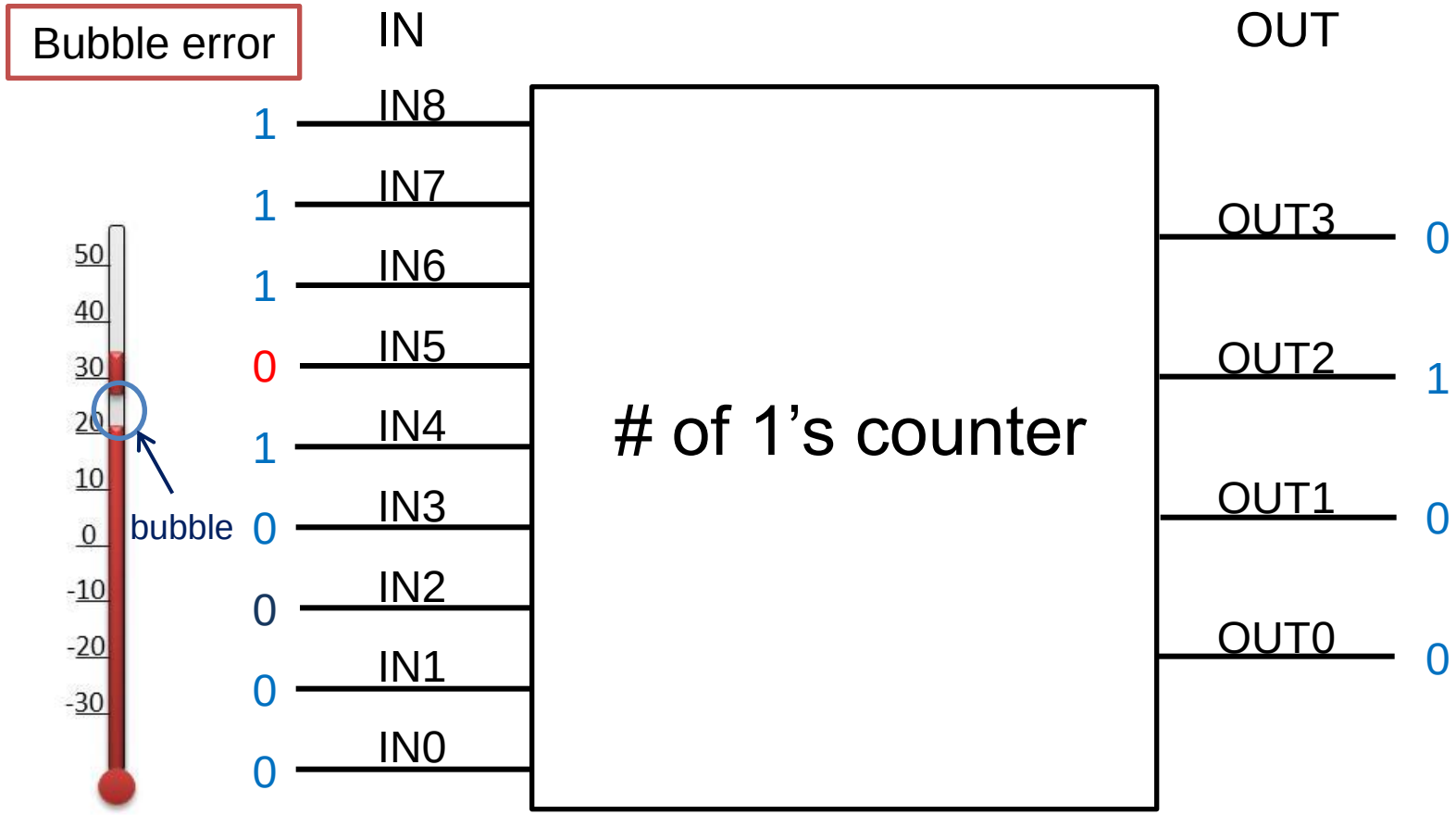
Encoder Circuit



Count the number of “1” outputs from DFFs

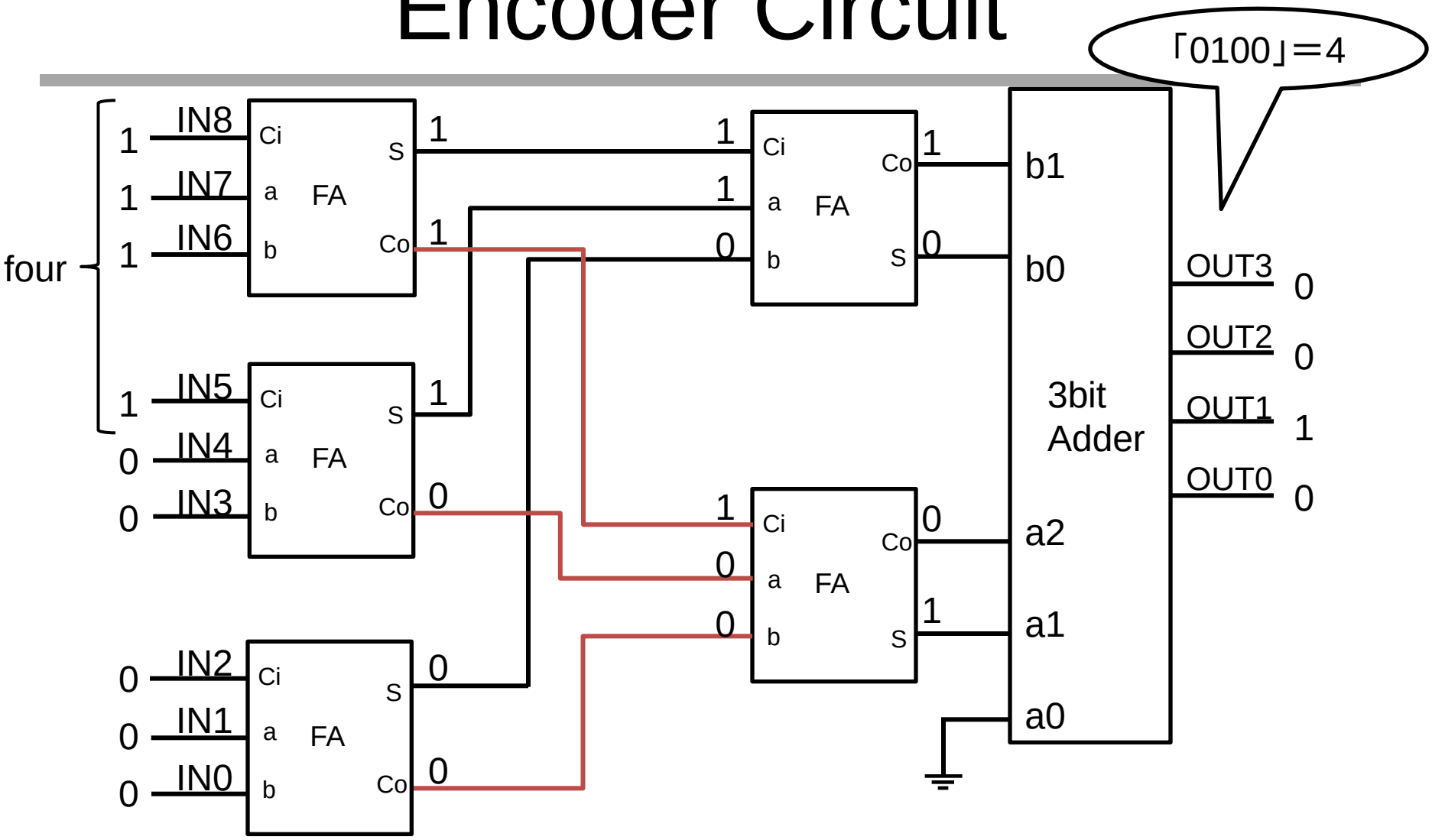
To ensure monotonicity of the TDC

Encoder Circuit



Bubble error effects are suppressed.

Encoder Circuit

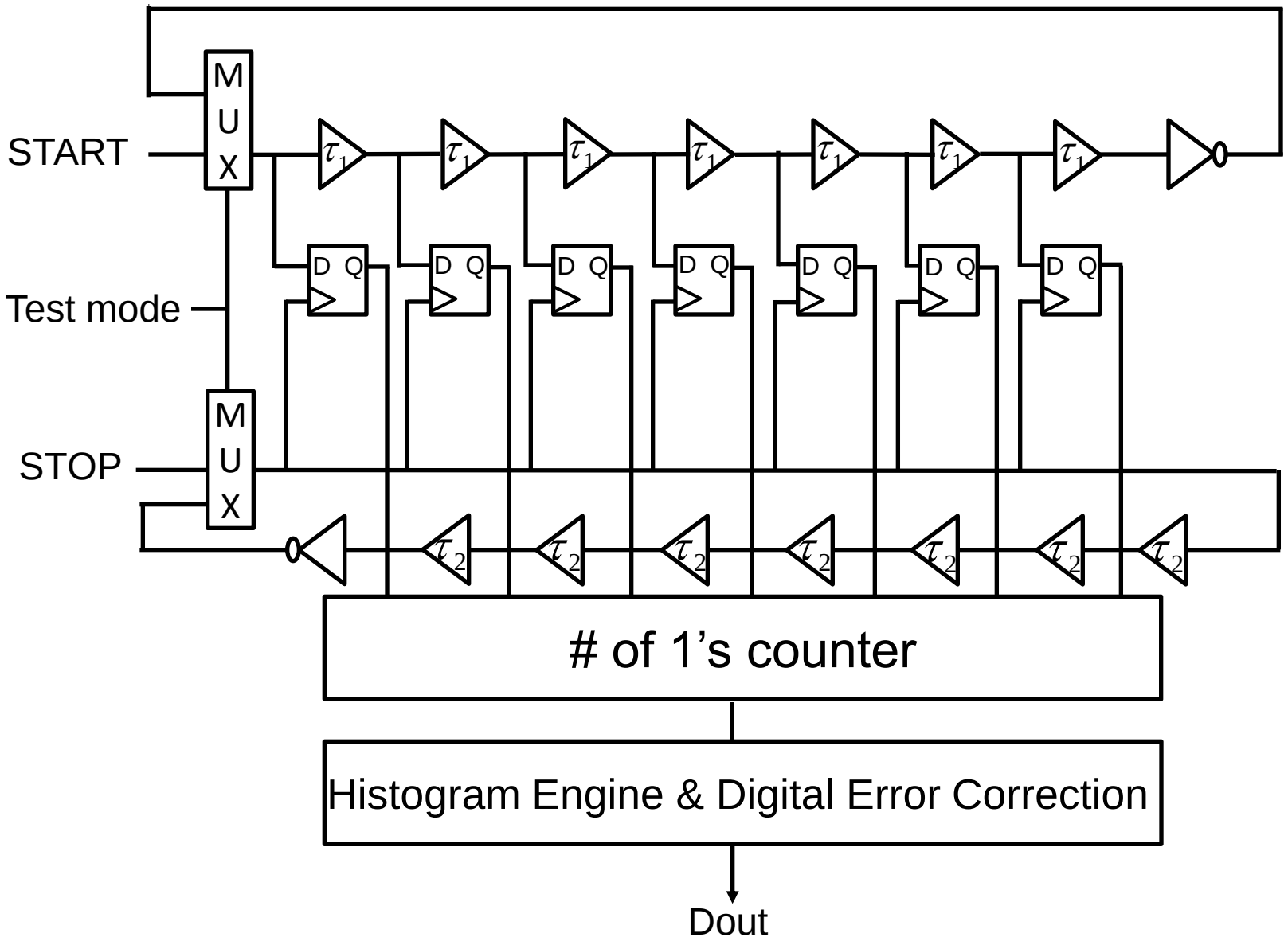


Designed the encoder using an array of full adders

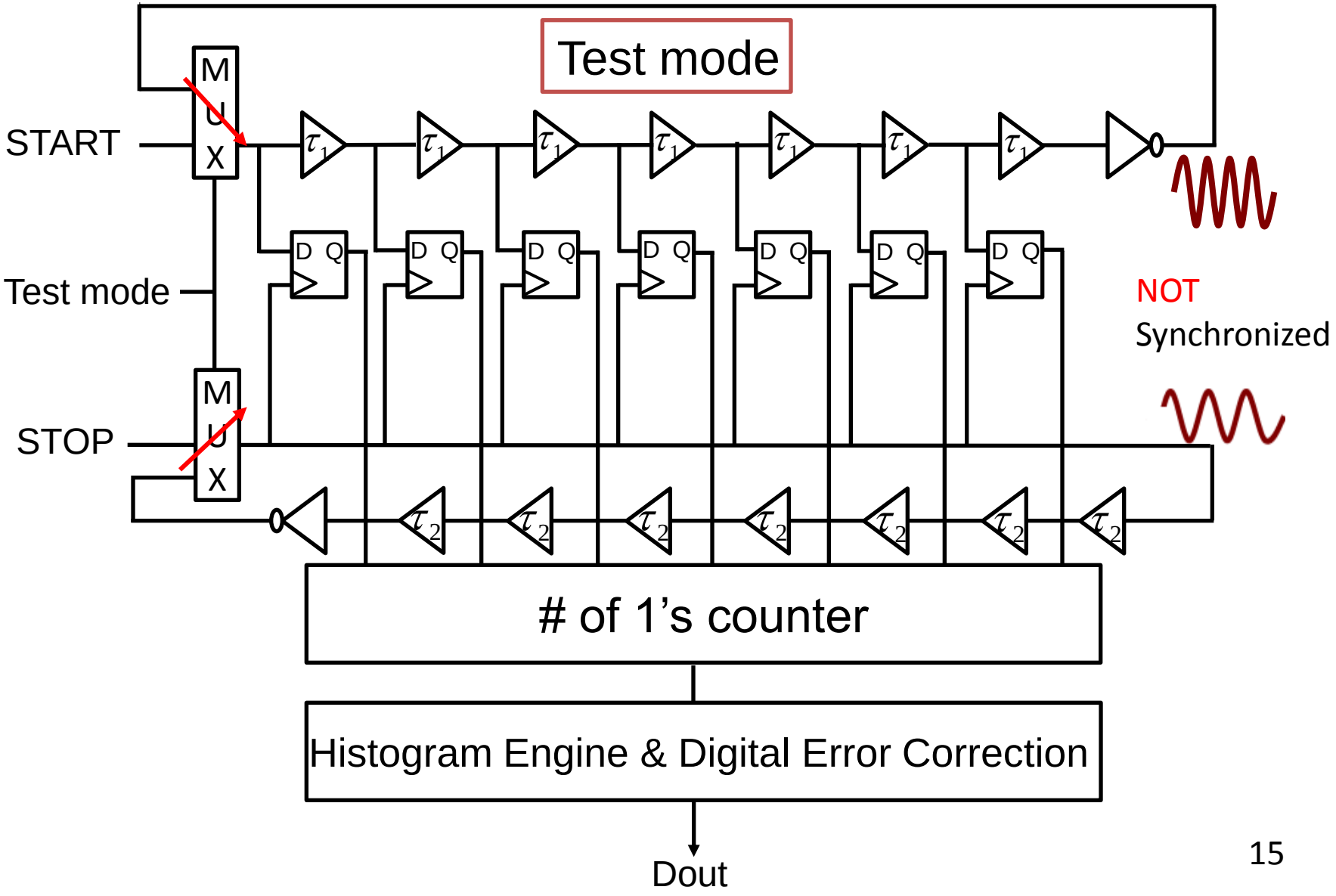
Outline

- Introduction
- Time to Digital Converter（TDC）
- Encoder Circuit
- Self-Calibration
- Stochastic TDC Structure
- Self-Testing Function
- Conclusions

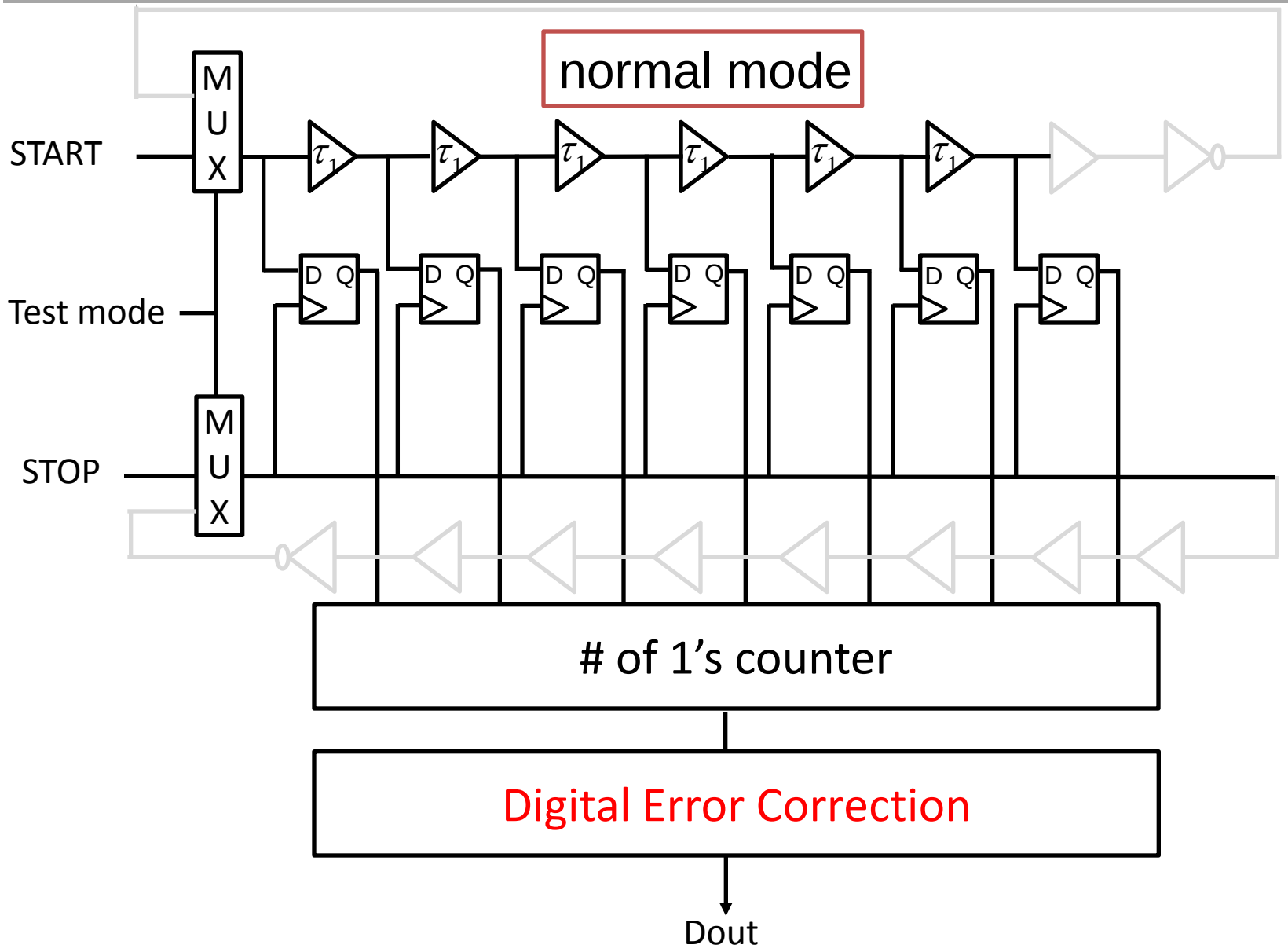
Proposed TDC Architecture with Self-Calibration



Self-Calibration Mode



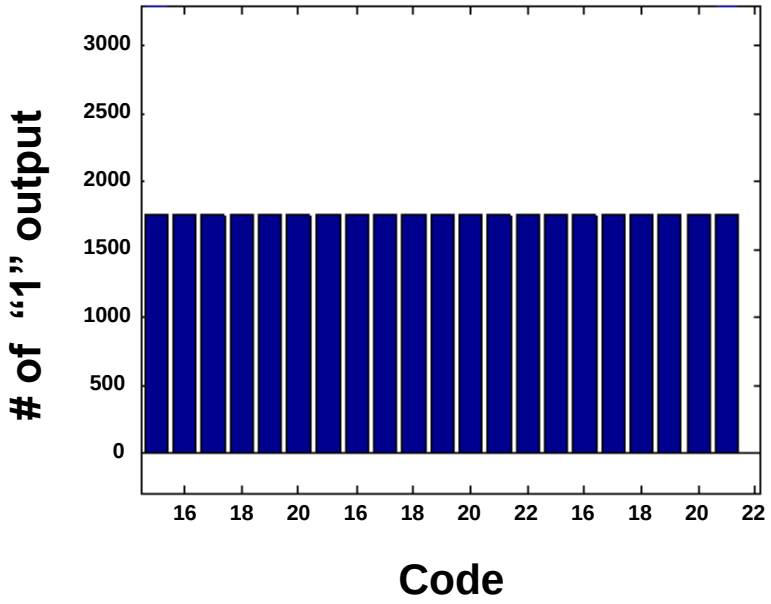
Normal Operation Mode



Self-Calibration

Test mode

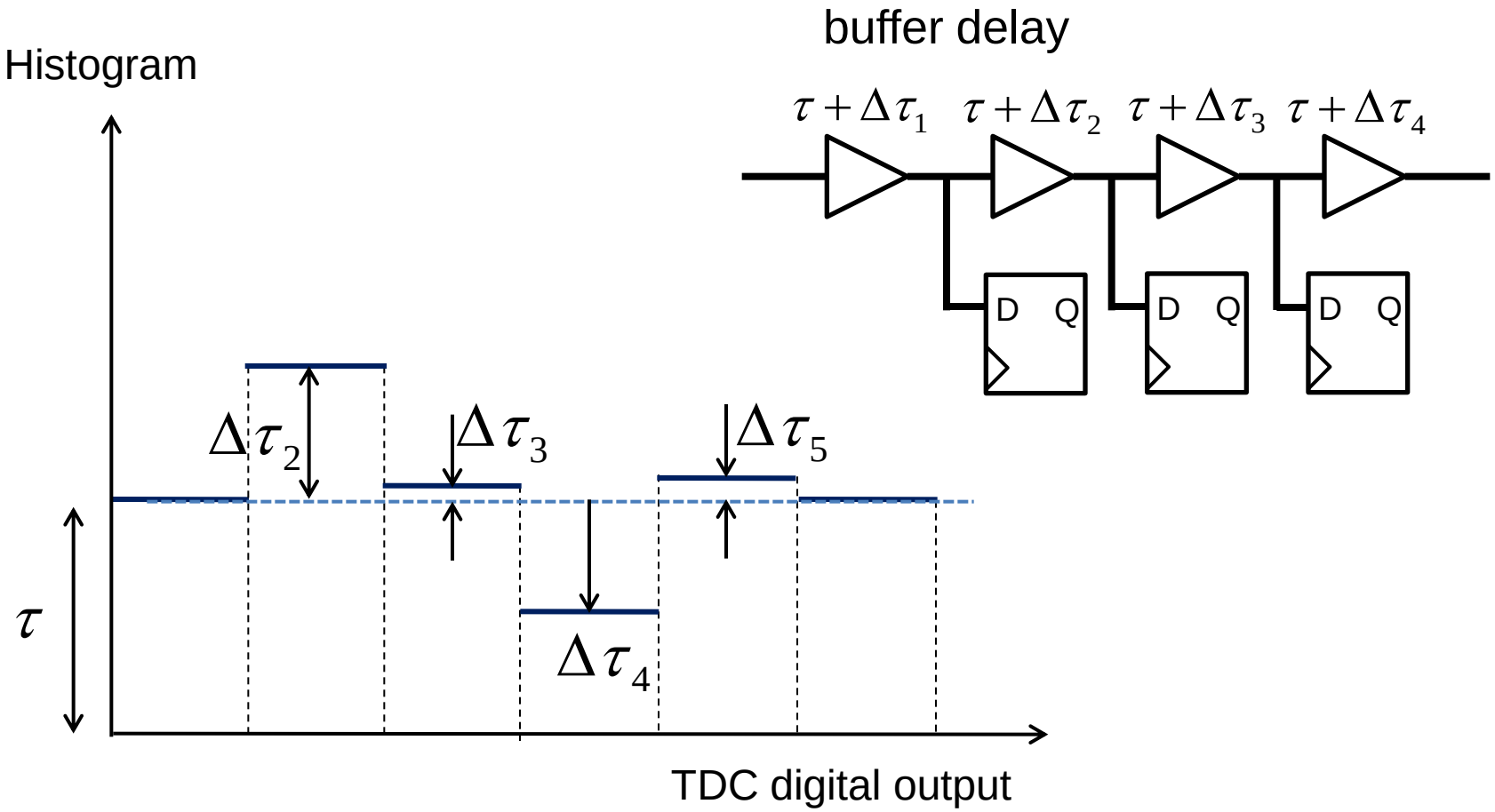
The two oscillators are different from each other and not synchronized



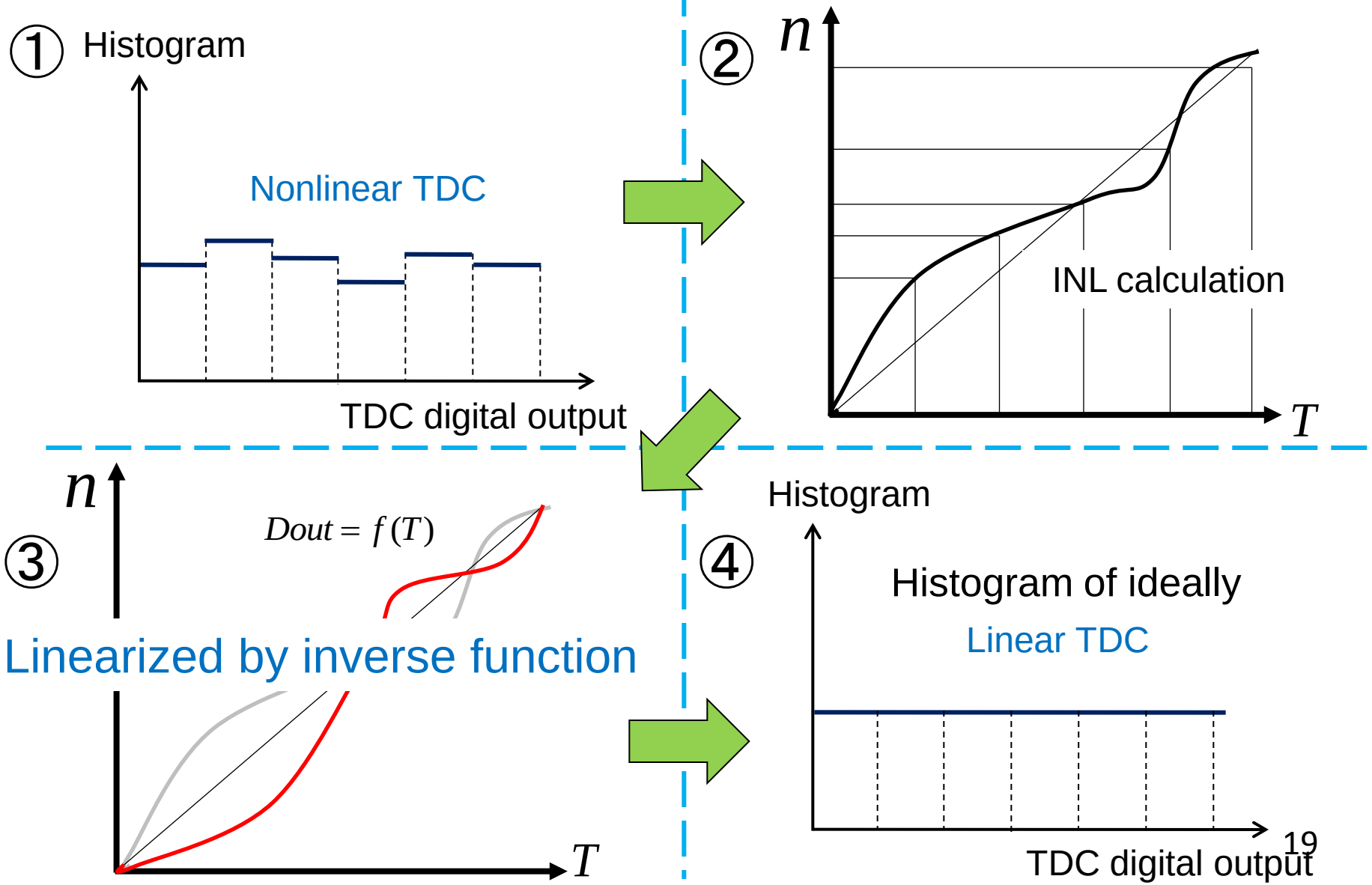
The histograms in all bins will be equal, after collection of a sufficiently large number of data, if the TDC has perfect linearity

Self-Calibration

TDC is non-linear



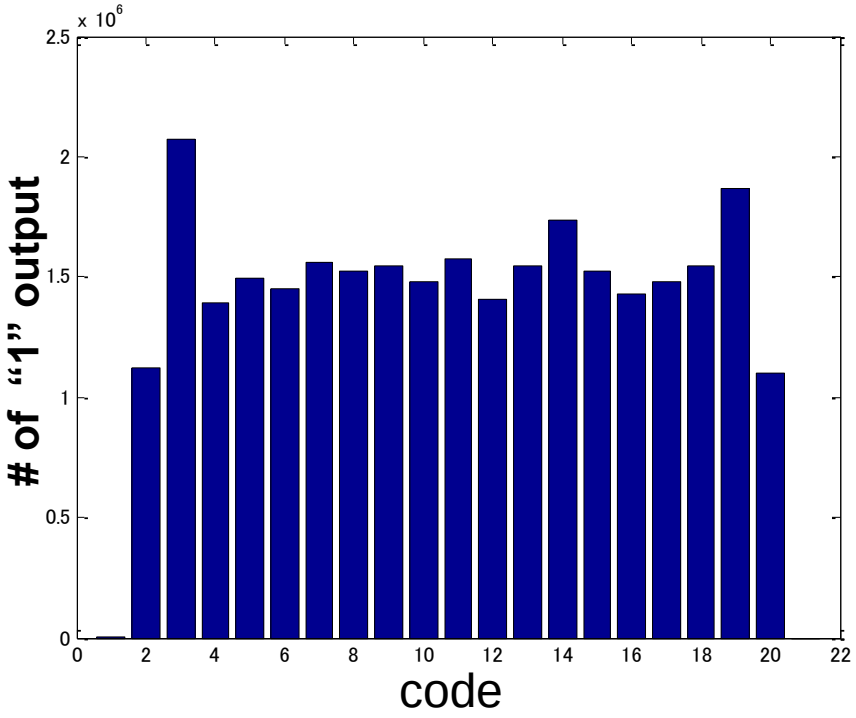
Principle of Self-Calibration



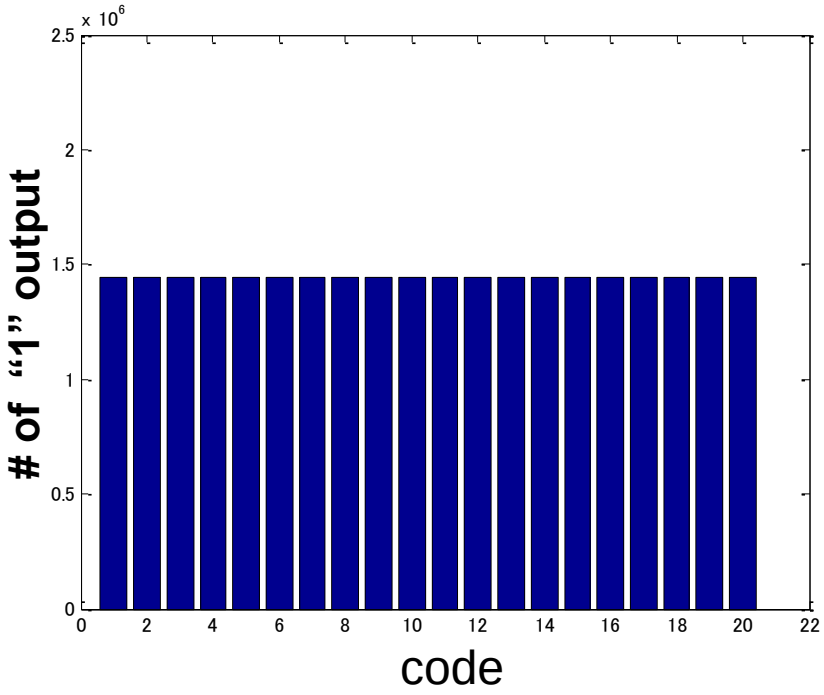
Simulation Result of Self-Calibration

MATLAB

before calibration



after calibration



Sampling points 28,848,432

$\tau_1 = 60 \sim 69\,ps$

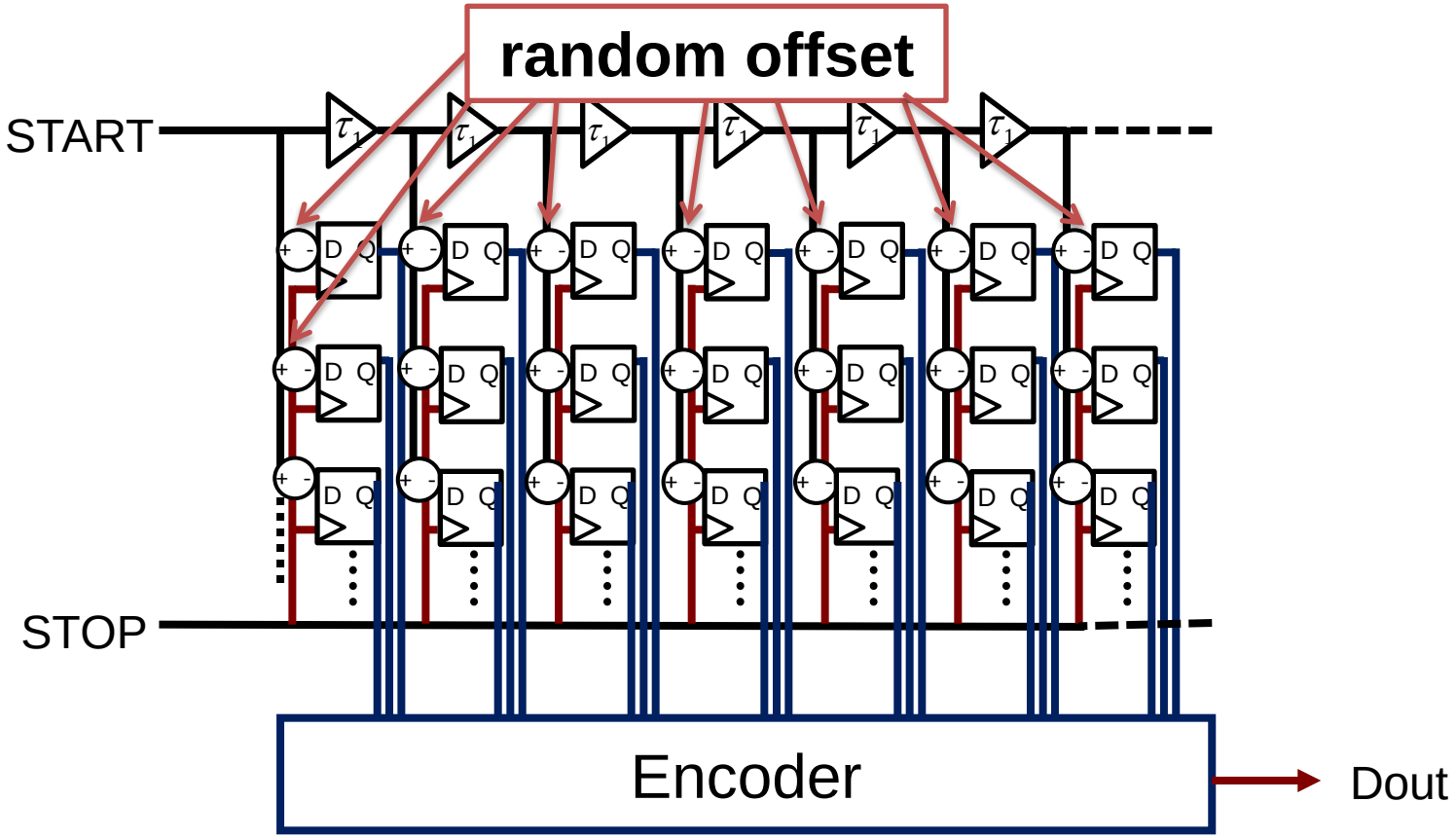
$\tau_2 = 10ns$

Histogram for each bin is the same when the TDC is linear.

Outline

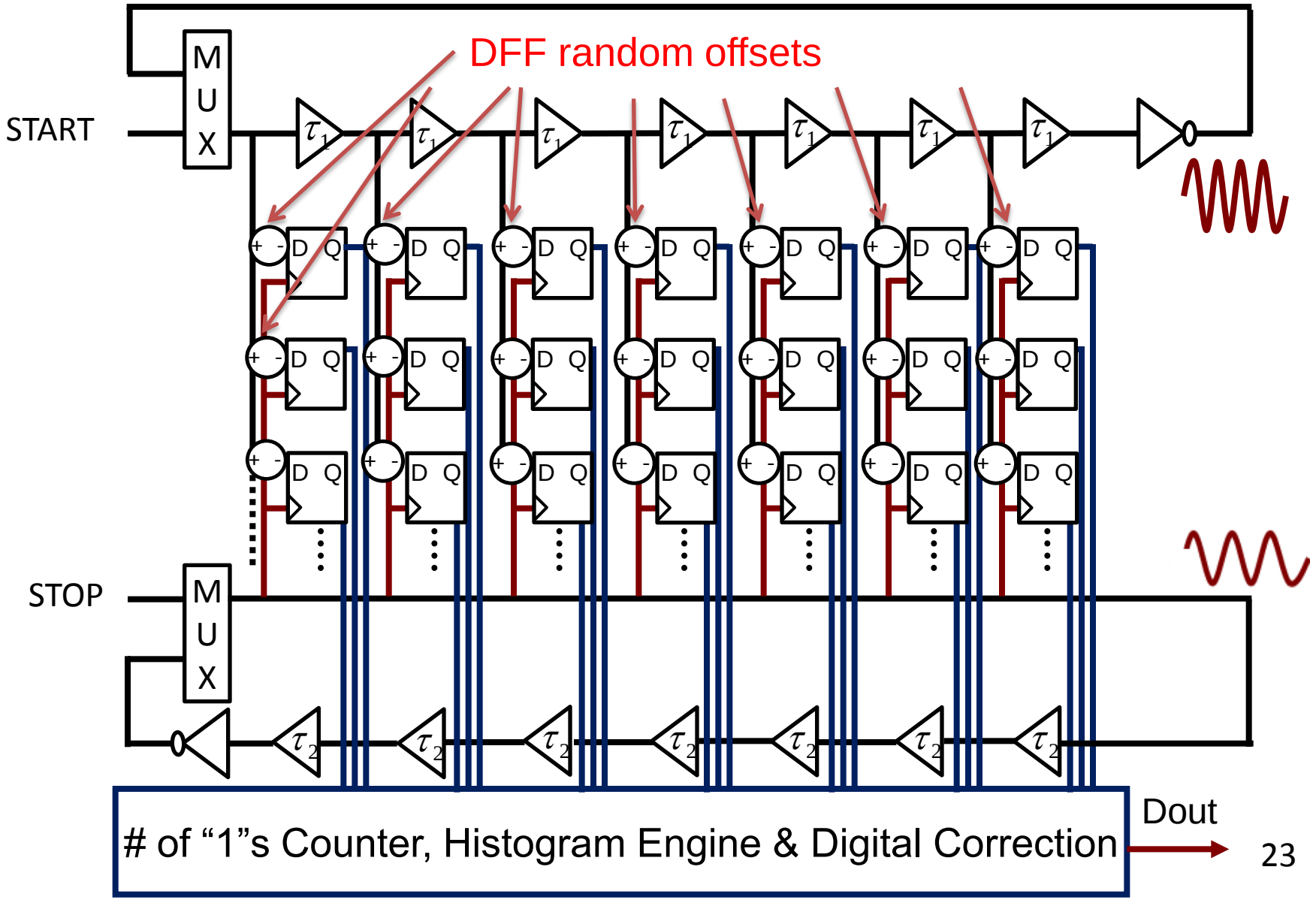
- Introduction
- Time to Digital Converter（TDC）
- Encoder Circuit
- Self-Calibration
- Stochastic TDC Structure
- Self-Testing Function
- Conclusions

Stochastic TDC Structure

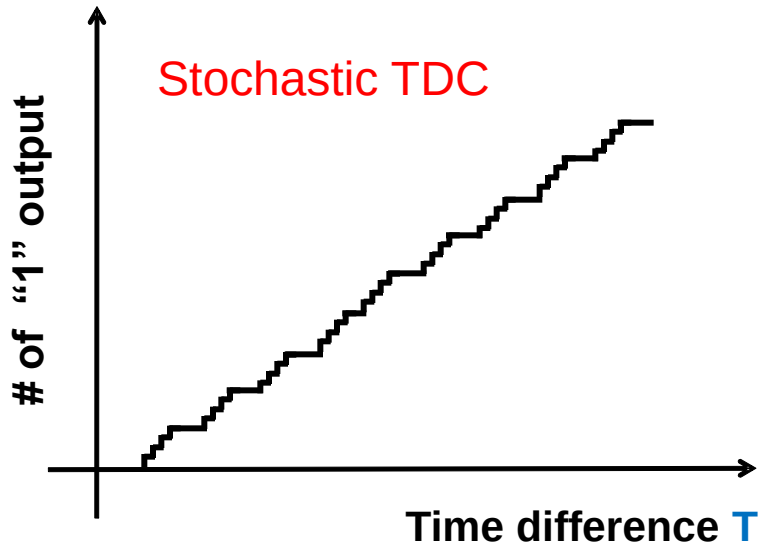


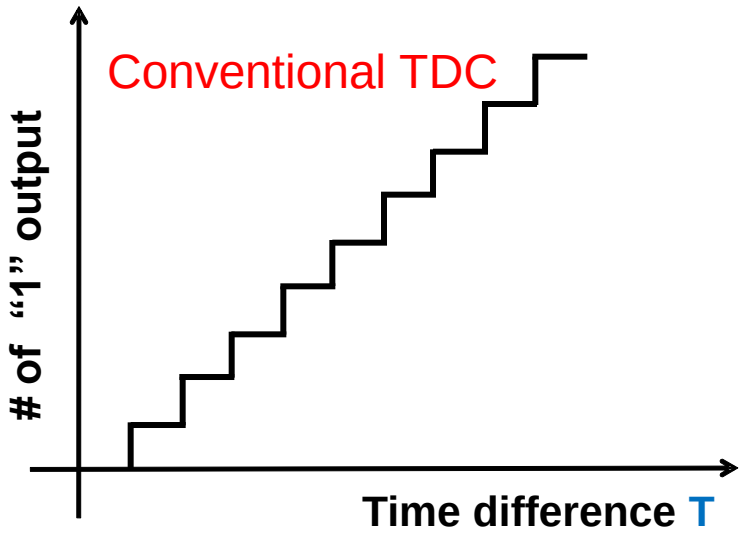
Use the random offset proactively

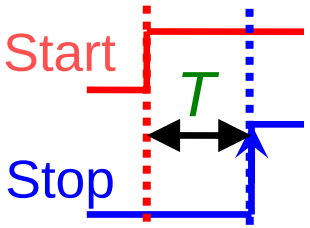
Stochastic TDC for Fine Time Resolution



Fine Time Resolution of Stochastic TDC





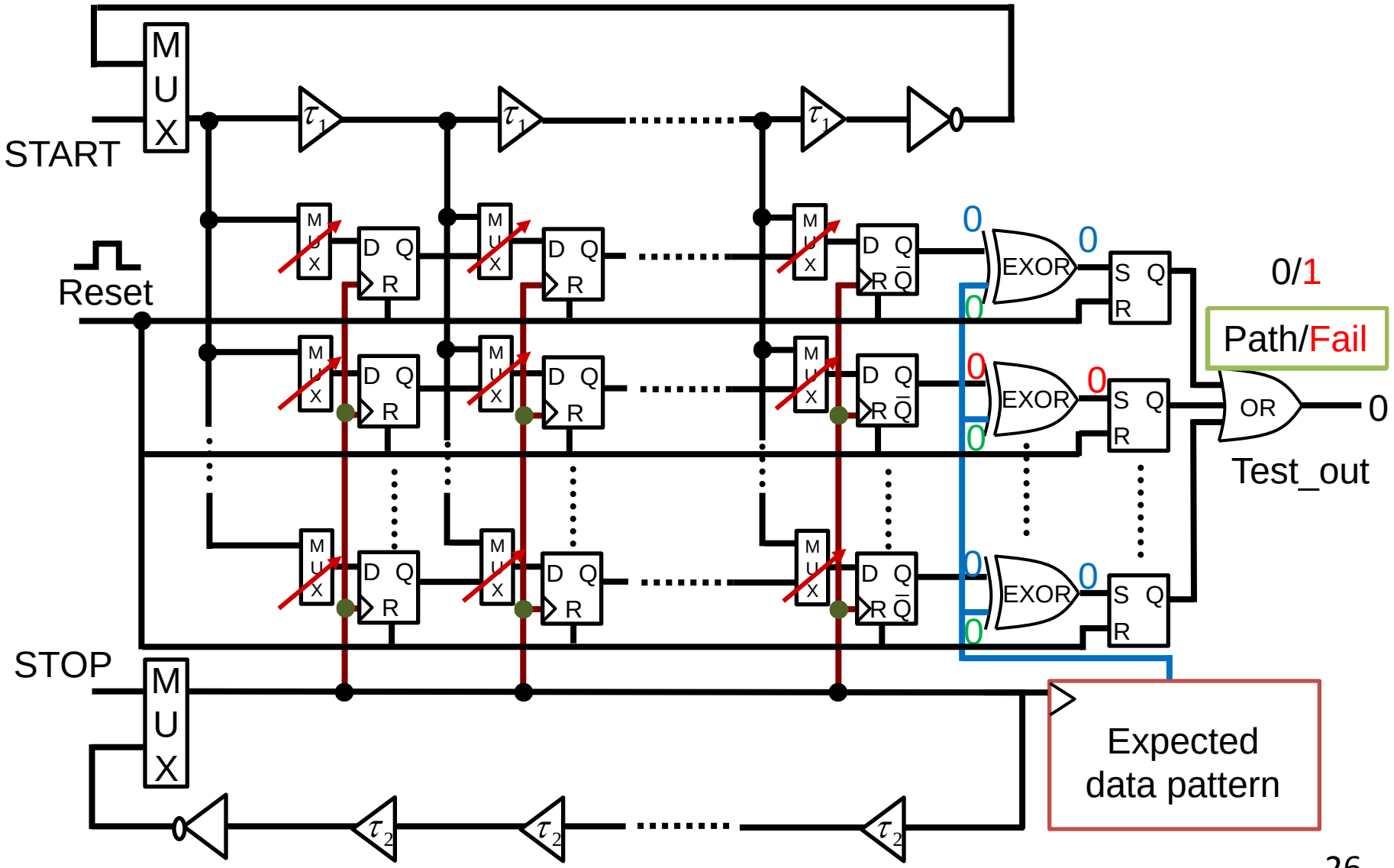


Encoder (# of 1's counter) and self-calibration make the stochastic TDC practical.

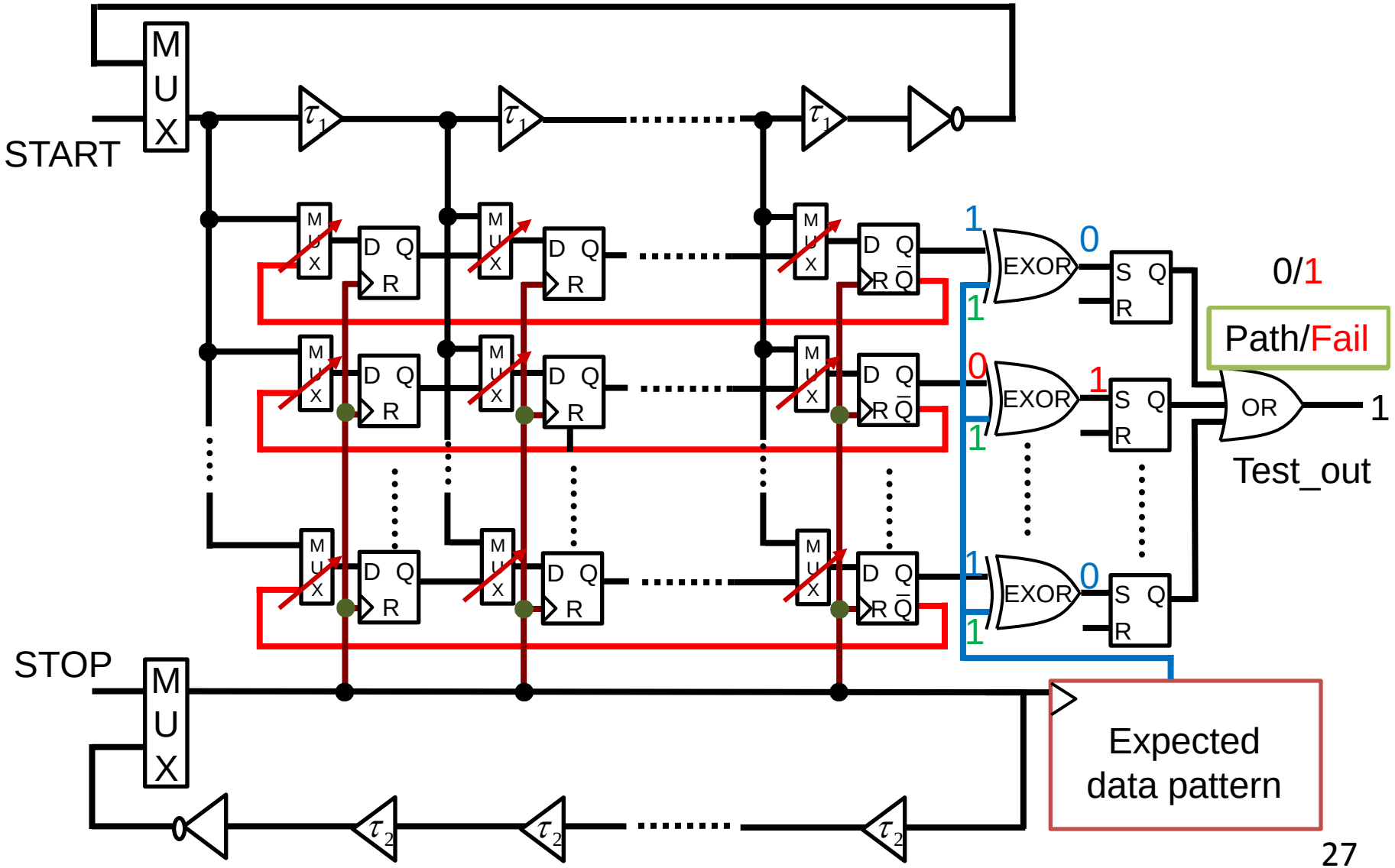
Outline

- Introduction
- Time to Digital Converter（TDC）
- Encoder Circuit
- Self-Calibration
- Stochastic TDC Structure
- Self-Testing Function
- Conclusions

Self-Testing Function



Self-Testing Function



Outline

- Introduction
- Time to Digital Converter（TDC）
- Encoder Circuit
- Self-Calibration
- Stochastic TDC Structure
- Self-Testing Function
- Conclusions

Conclusions

- High linearity TDC
  →Self-Calibration circuit
- Fine time resolution TDC
  →Stochastic architecture
- High reliability TDC
  →Self-testing capability

■ Fine digital CMOS implementation

- Verification
- Self-calibration
- Testability
- Consists of digital standard cells
  (hence even FPGA implementation is possible)