APCCAS 2010

Session : **ADC / DAC I**

Tuesday, 7th December 2010
14:20-14:40

1569326283

Non-Binary SAR ADC with Digital Error Correction for Low Power Applications

T. Ogawa, T. Matsuura, H. Kobayashi

N. Takai, M. Hotta, H. San

A. Abe, K. Yagi, T. Mori

Gunma University

STARC, Tokyo City University

Outline

- Research goal
- SAR ADC characteristics
- Proposed non-binary SAR ADC
  - Two-comparator architecture
  - Charge-sharing architecture
  - Combined two-comparator & charge-sharing architecture
- Conclusions

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- Research goal
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Research Goal

IMEC (Inter-university Microelectronics Center) proposed development of power-efficient SAR ADCs with

- Two-comparator architecture
- Charge-sharing architecture

Problem: They require analog tuning.

- Our Research Goal
  - Eliminate analog tuning -- use non-binary SA algorithm with digital compensation instead.

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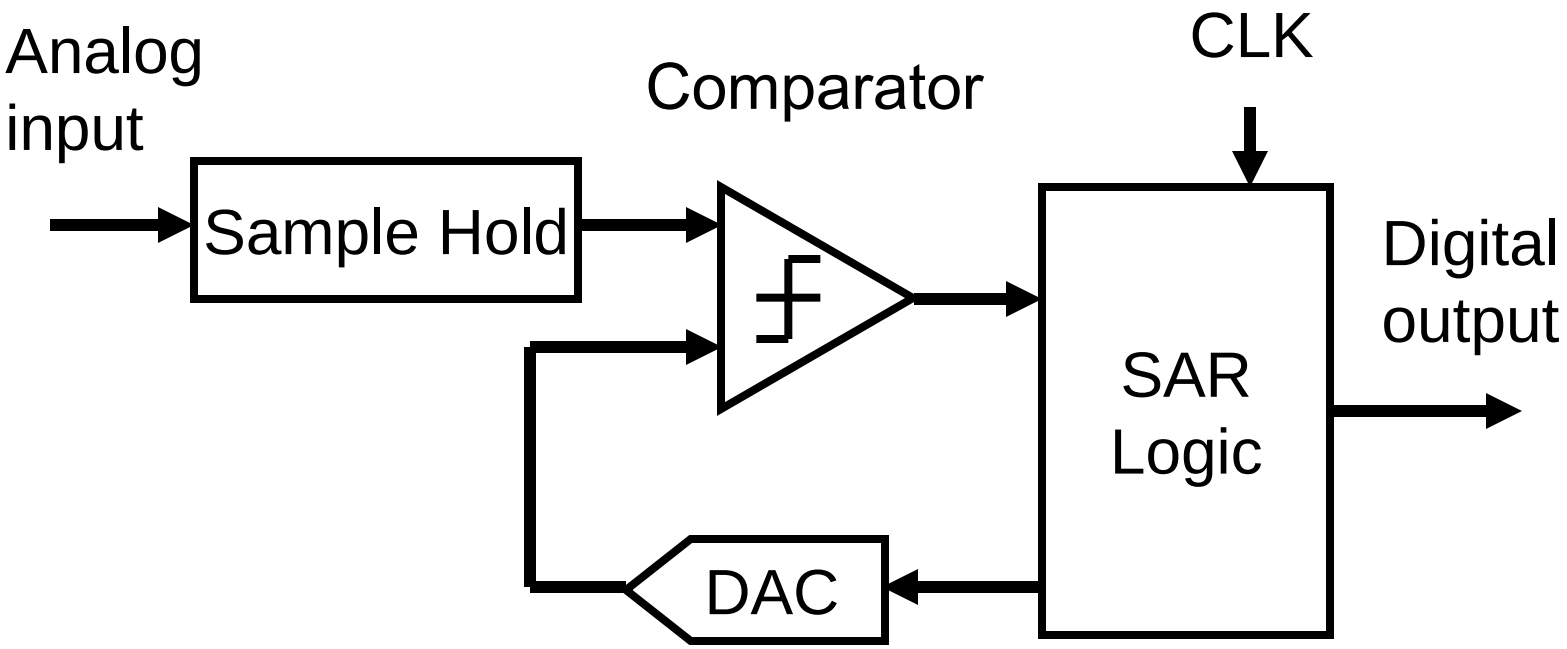
SAR ADC Block Diagram



SAR ADC is digital centric.

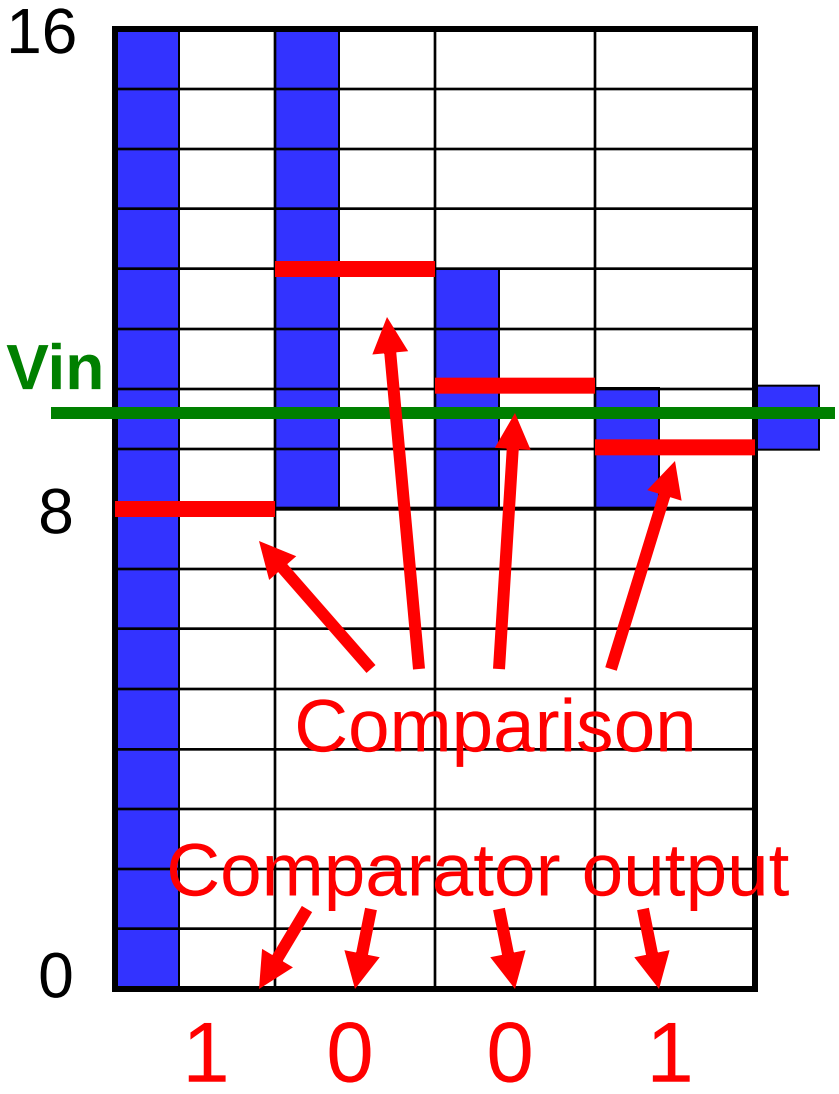
→ Suitable for fine CMOS implementation.

SAR ADC Characteristics

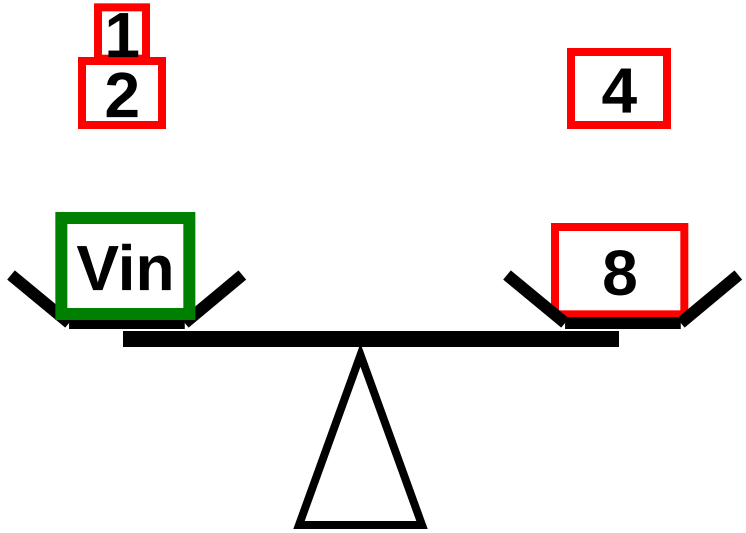
- High resolution (10-16bit)
- Medium sampling speed (10-40 MS/s)
- Small die area
- Low power (a few mW)
- Doesn’t require an OP-amp
- Application examples:

  automotive, factory automation

Binary search algorithm

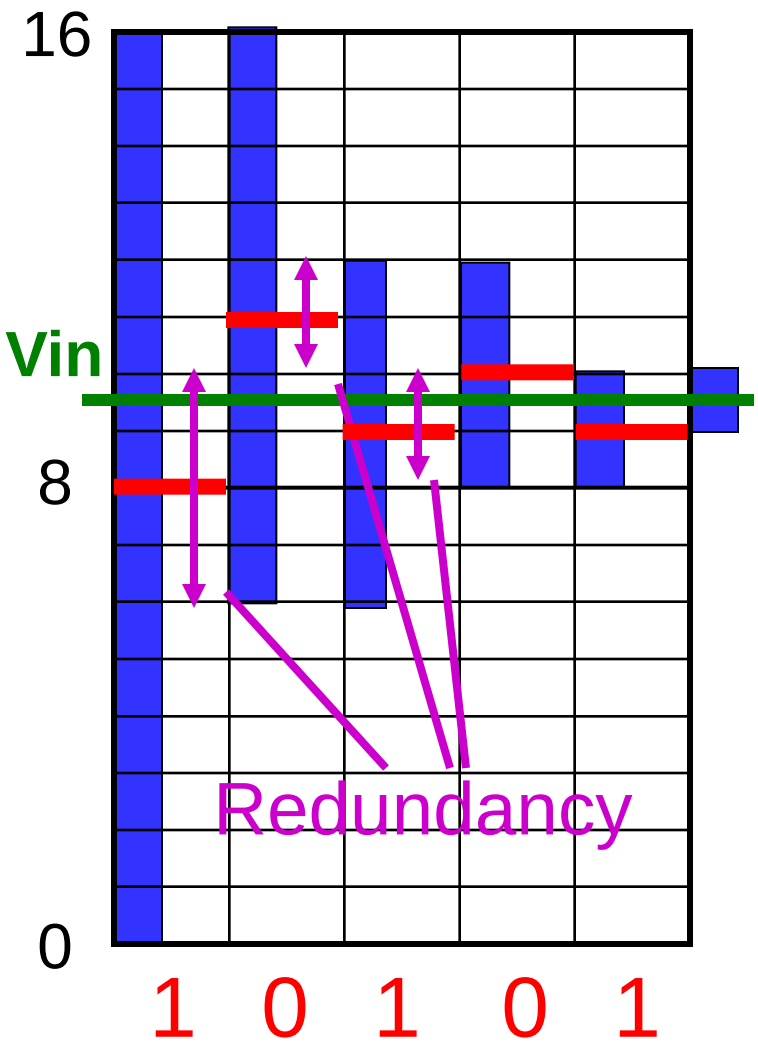


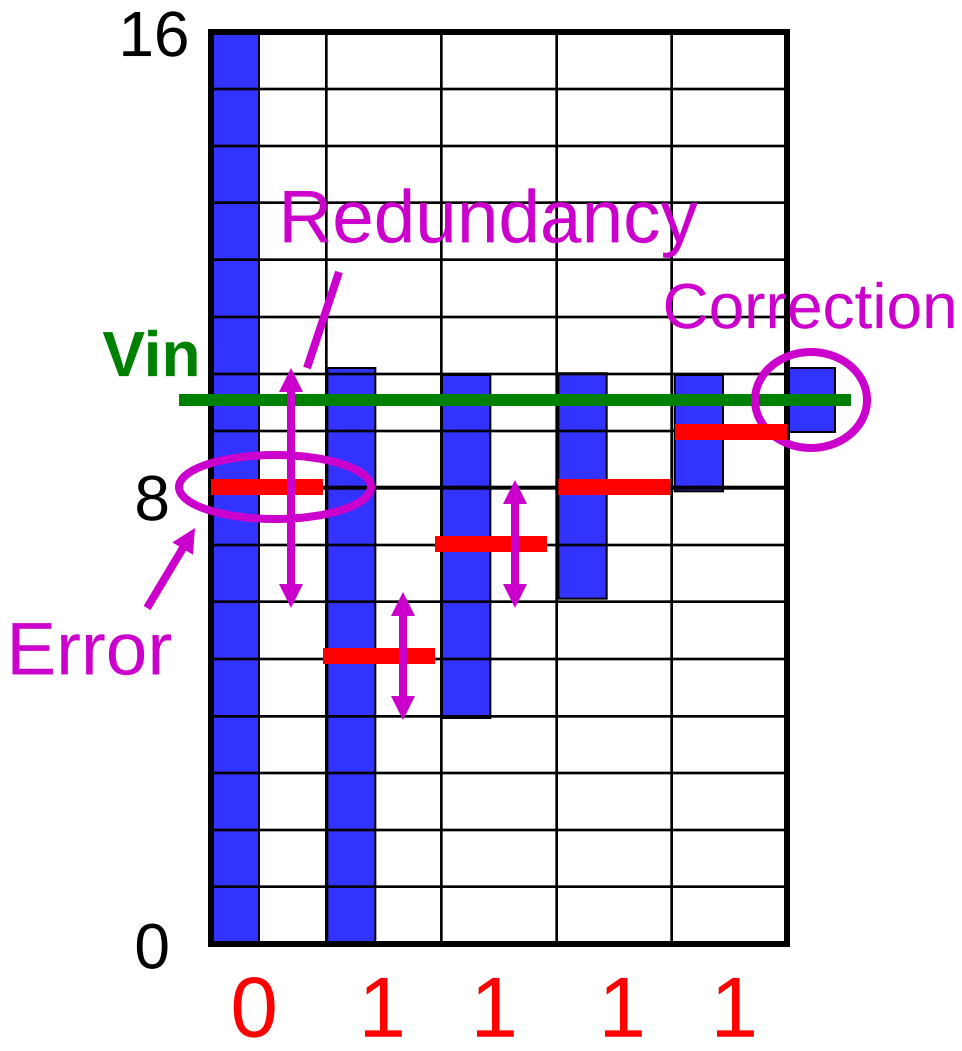
“Principle of a balance”



Vin = 4 + 8 − 1 + 2 = 9

Non-binary search algorithm





4-bit 5-step case

Principle of digital error correction

Binary search algorithm

Comparator output : **1 0 0 1** ← Only one

Dout = 8 + 4 – 2 – 1 + 0.5 – 0.5 = 9

Non-binary search algorithm

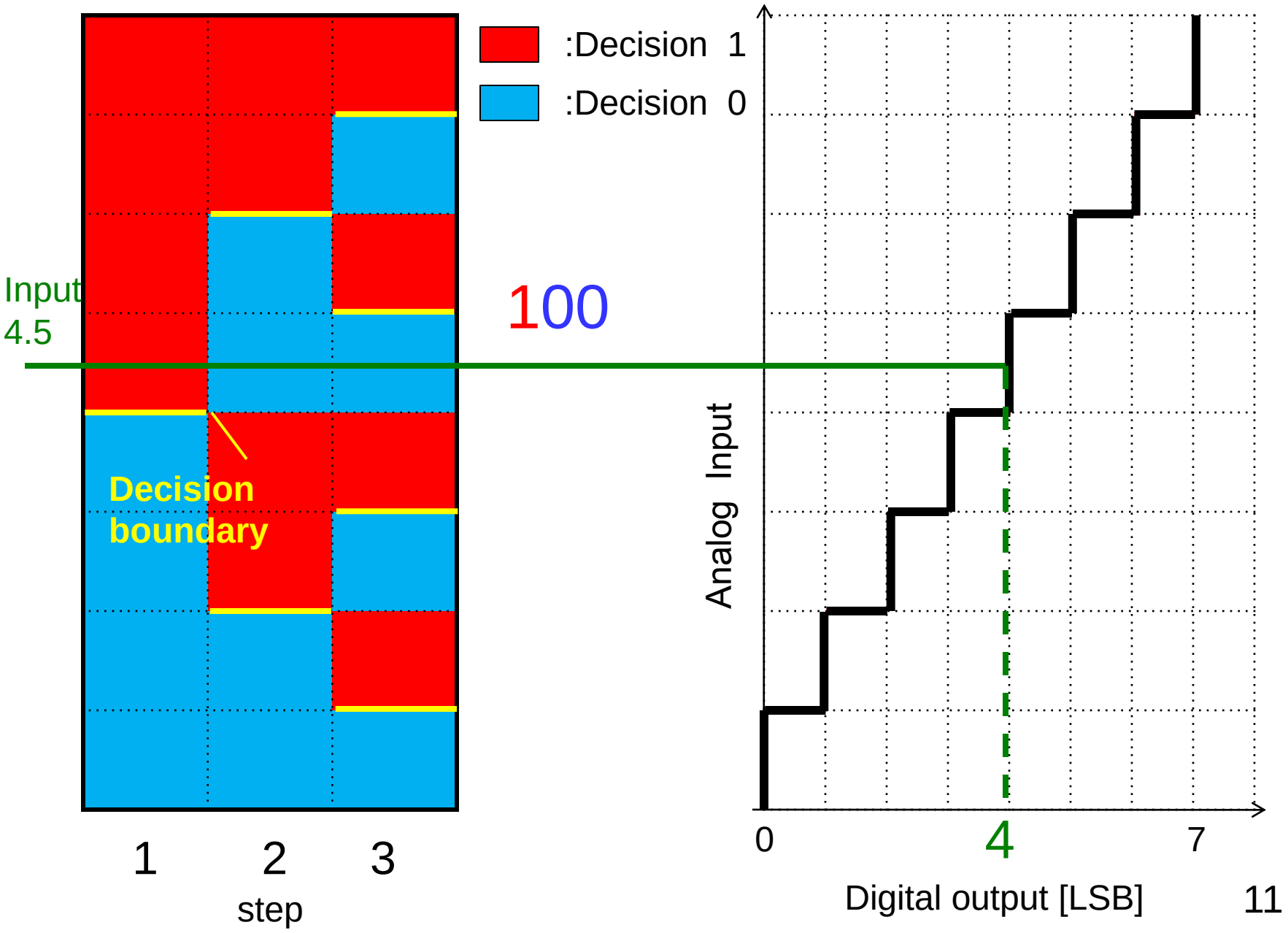
Comparator output : **1 0 1 0 1** ← Multiple

Dout = 8 + 3 – 2 + 1 – 1 + 0.5 – 0.5 = 9

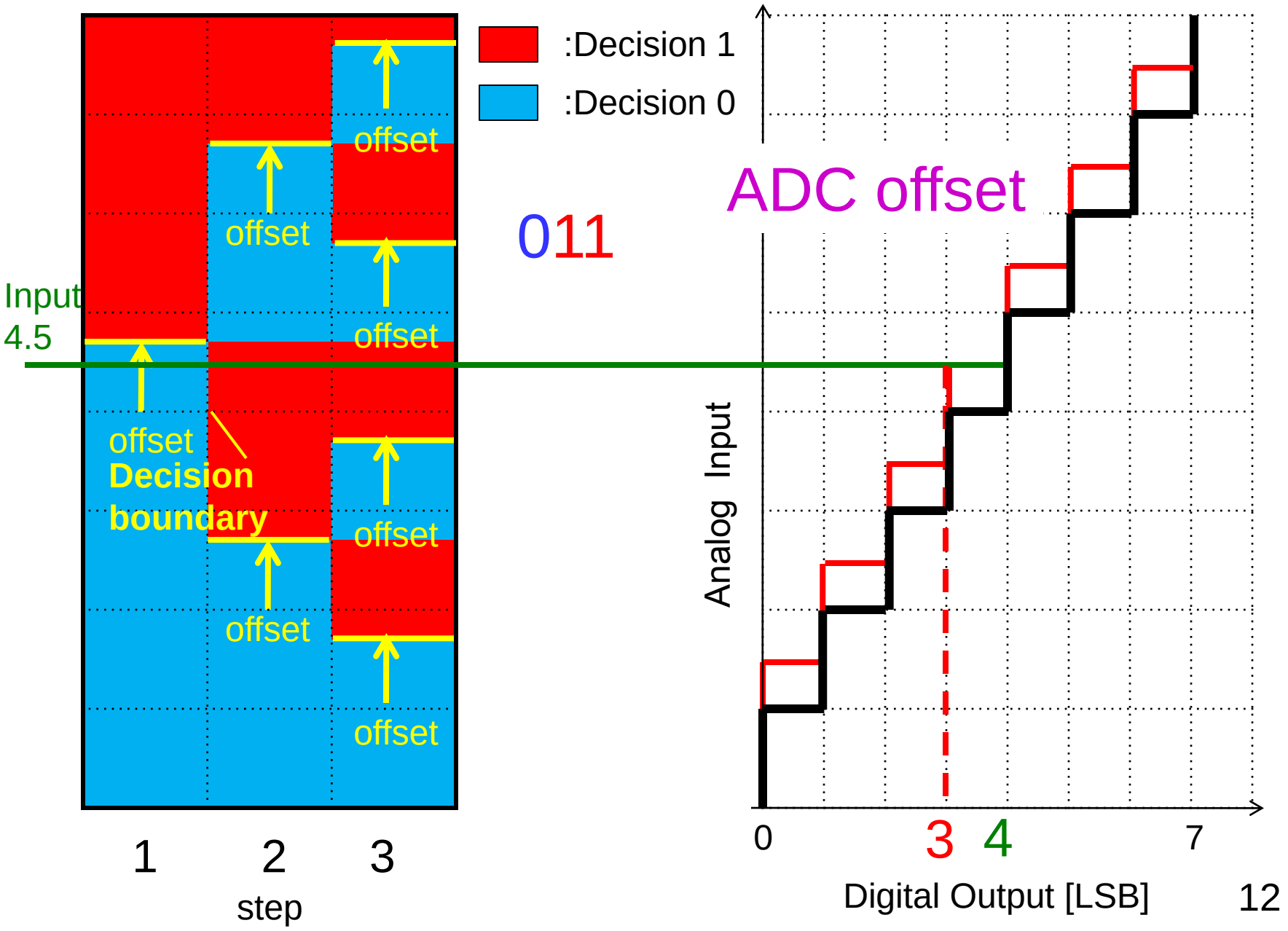
Comparator output : **0 1 1 1 1**

Dout = 8 – 3 + 2 + 1 + 1 + 0.5 – 0.5 = 9

Comparator Offset Effects in Conventional SAR ADC



Comparator Offset Effects in Conventional SAR ADC



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- Research purpose
- SAR ADC
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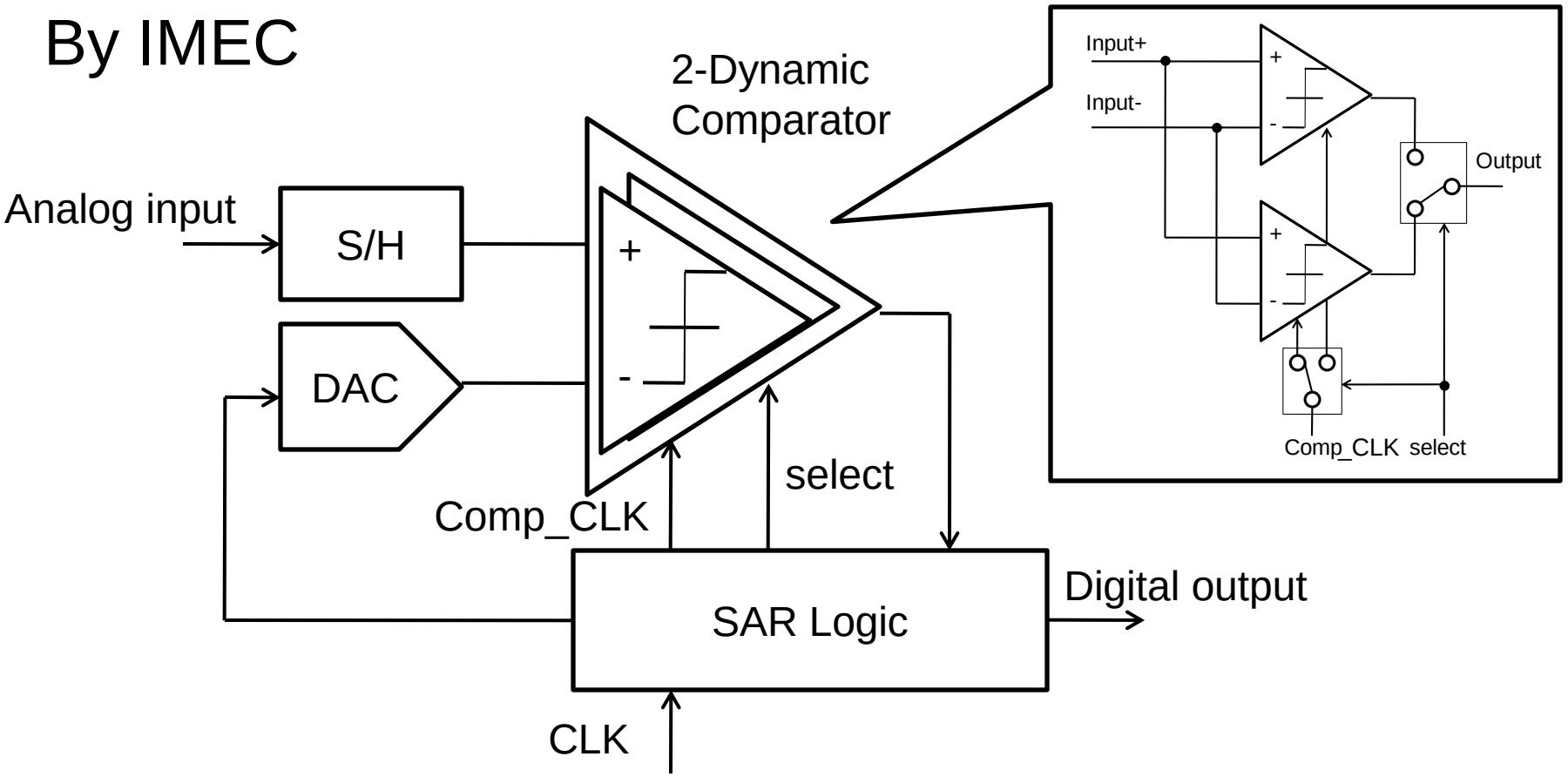
Two-Comparator SAR ADC

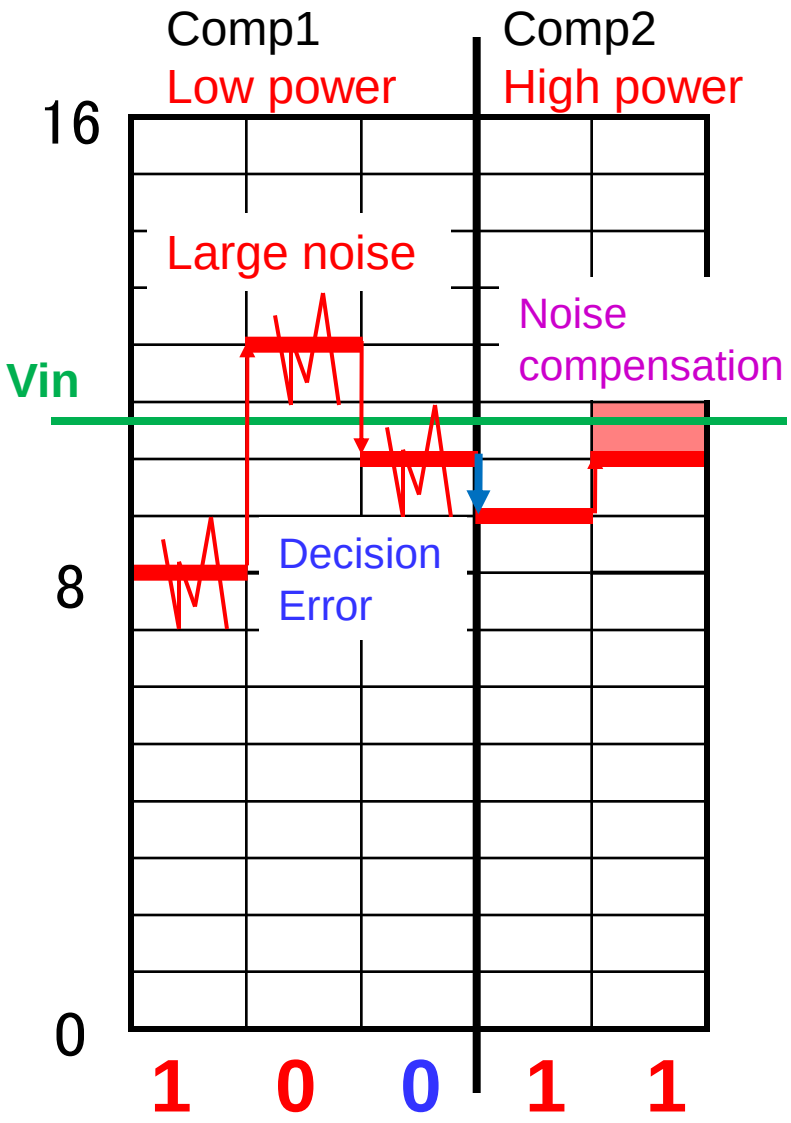
By IMEC

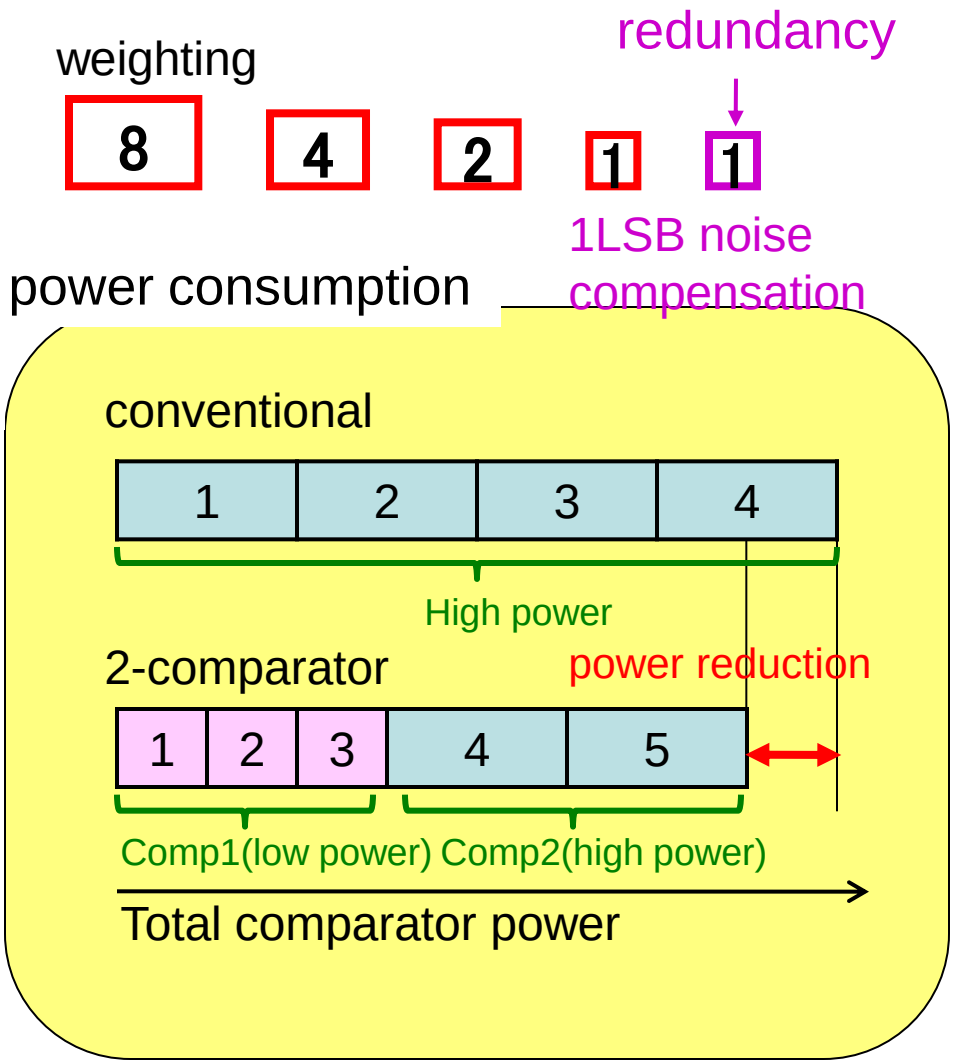


Reference

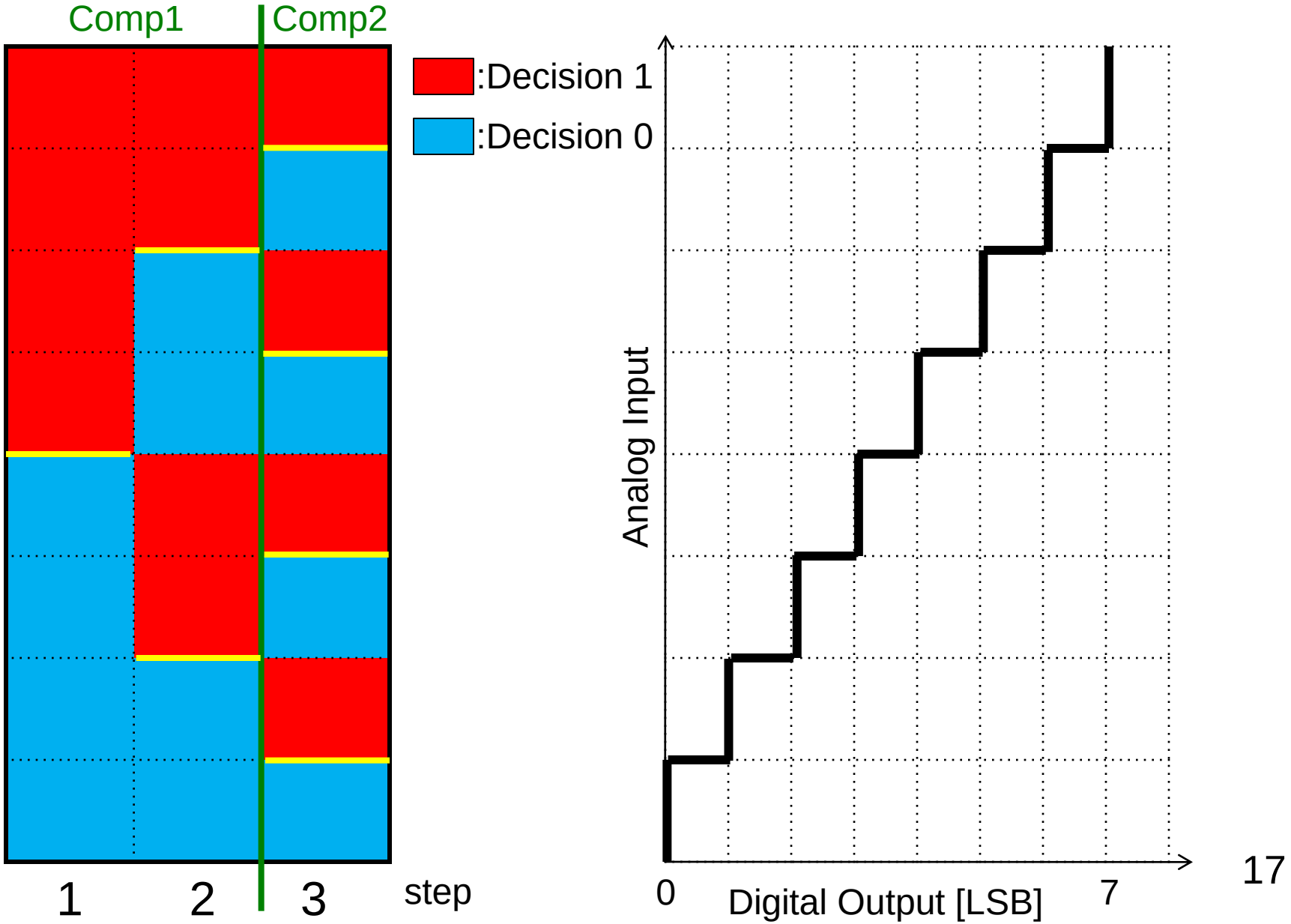
[1] V. Giannini, P. Nuzzo, V.Chironi, A.Baschirotto, G. V. Plas, J. Craninckx
" An 820 μ W 9b 40MS/s Noise-Tolerant Dynamic-SAR ADC in 90nm Digital CMOS "
ISSCC (Feb.2008).

2-Comparator SAR ADC
（Proposed by IMEC）

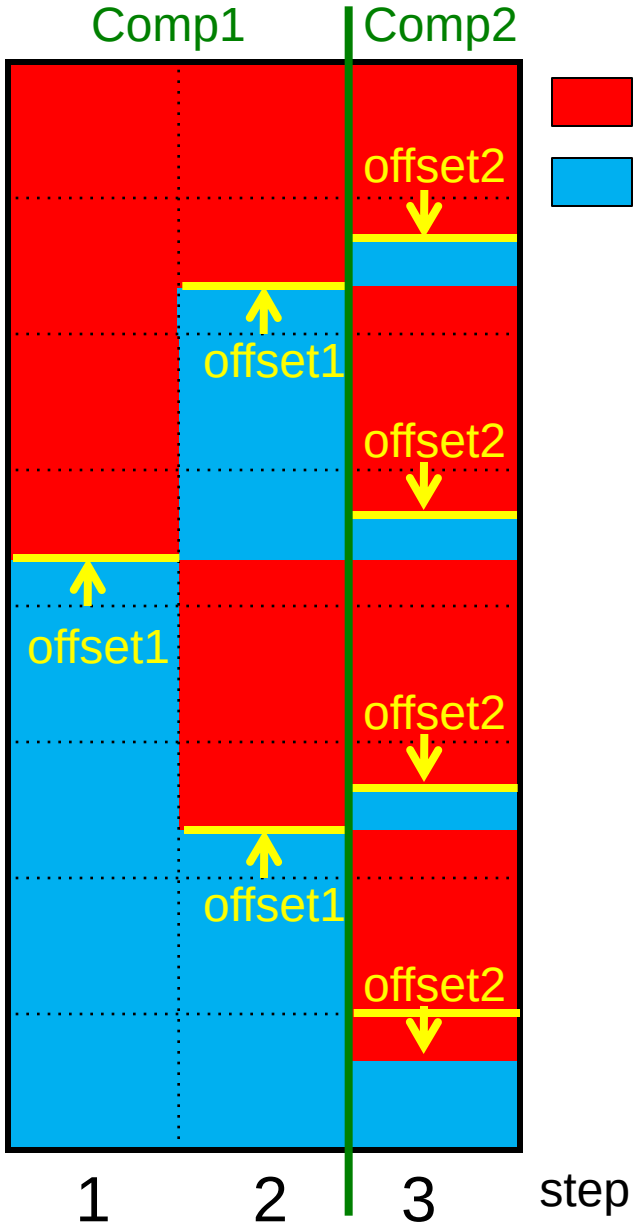




Comparator Offset Effects of Two-Comparator SAR ADC

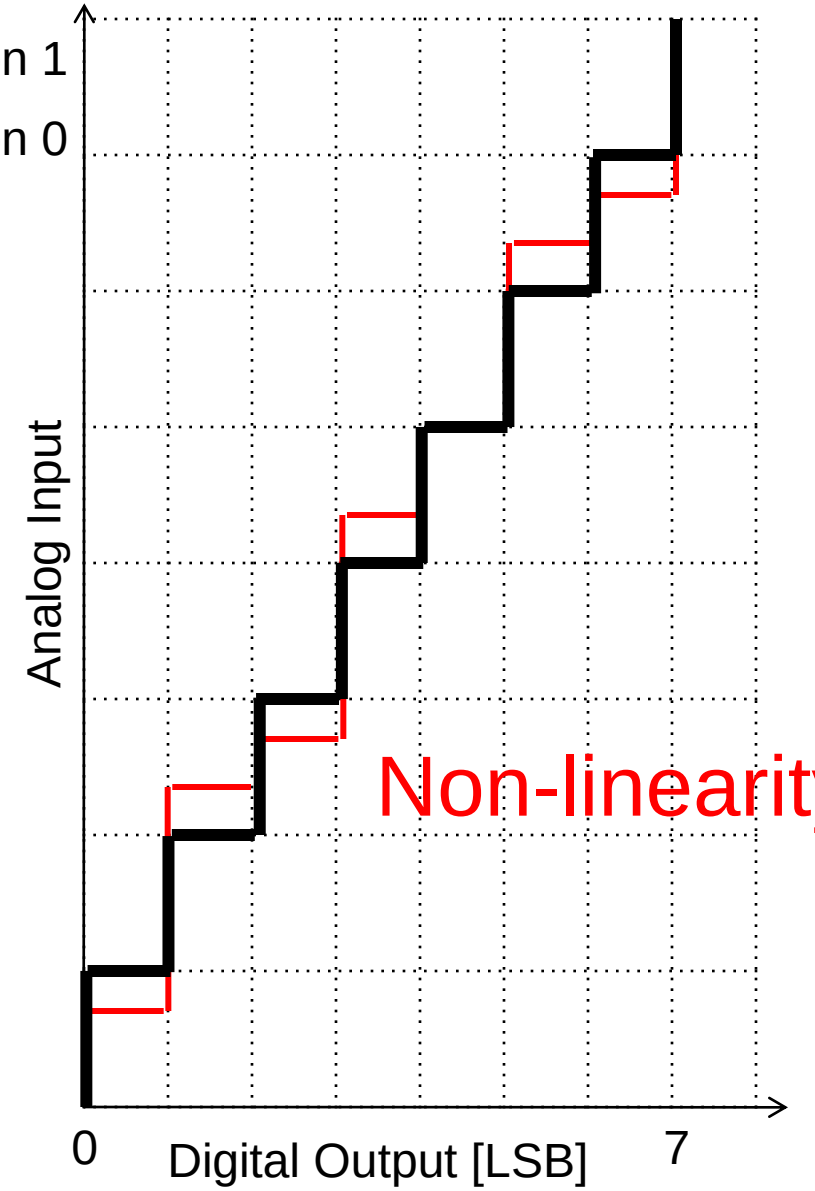


Comparator Offset Effects of Two-Comparator SAR ADC

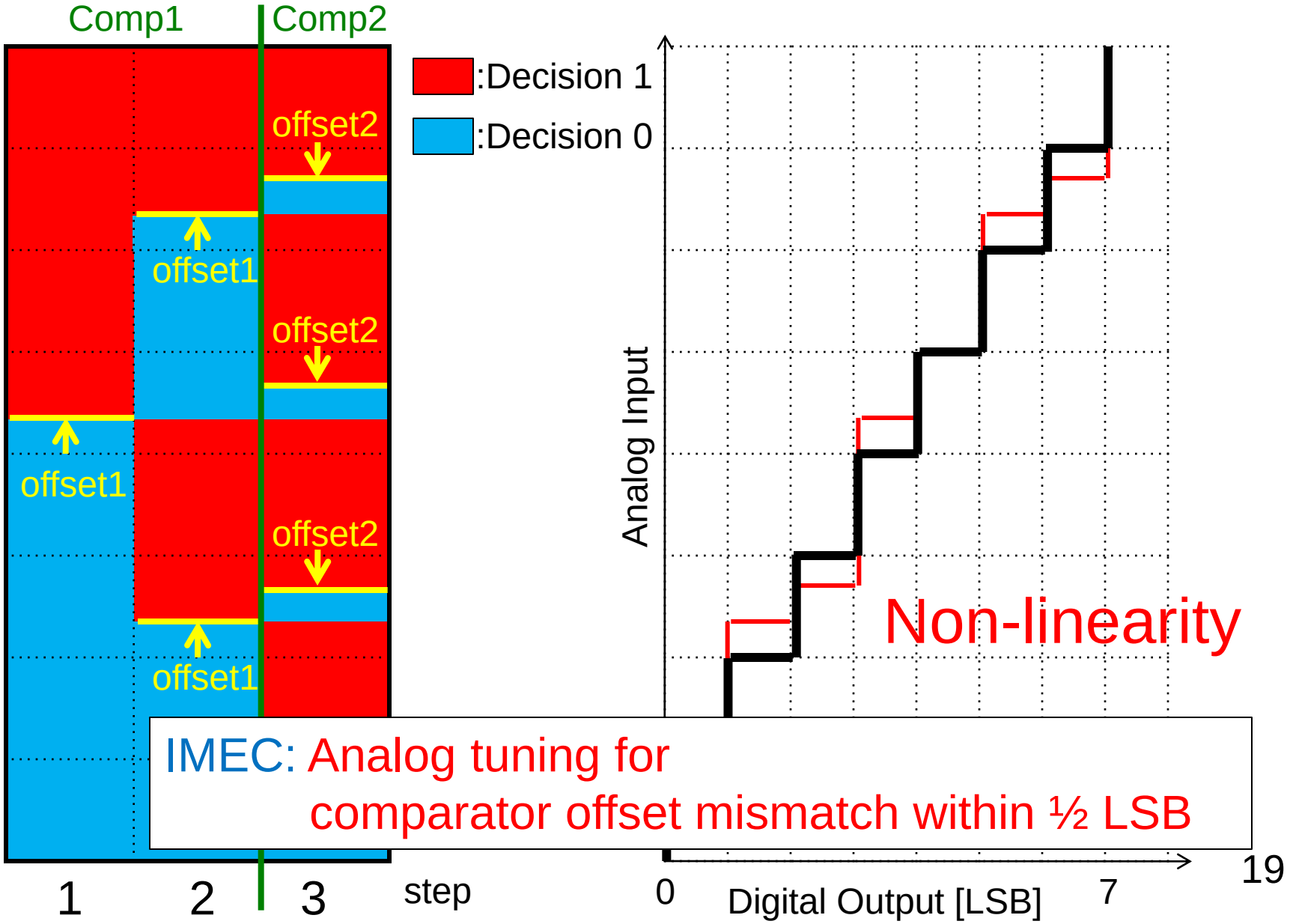


:Decision 1

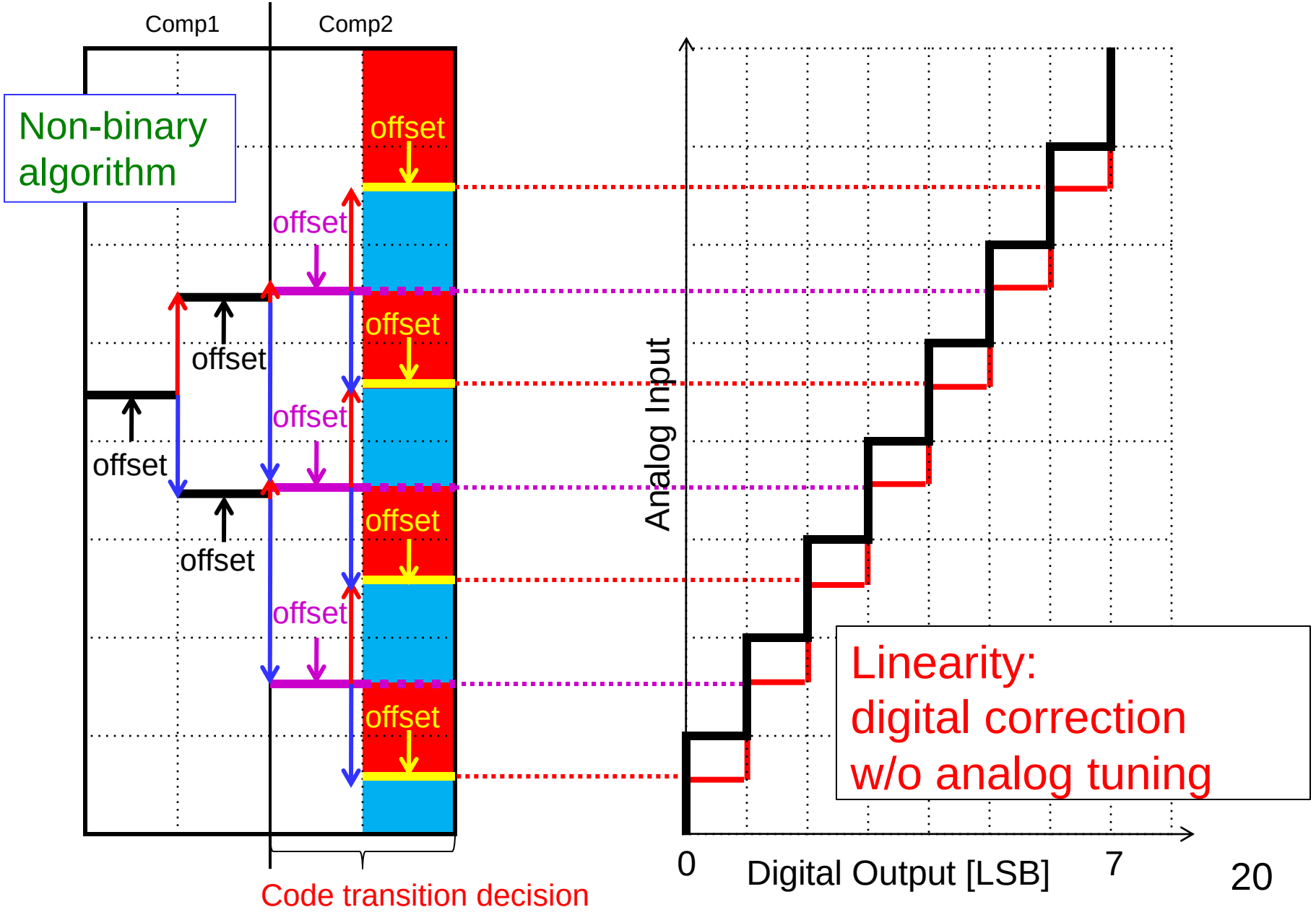
:Decision 0



Comparator Offset Effects of 2-Comparator SAR ADC



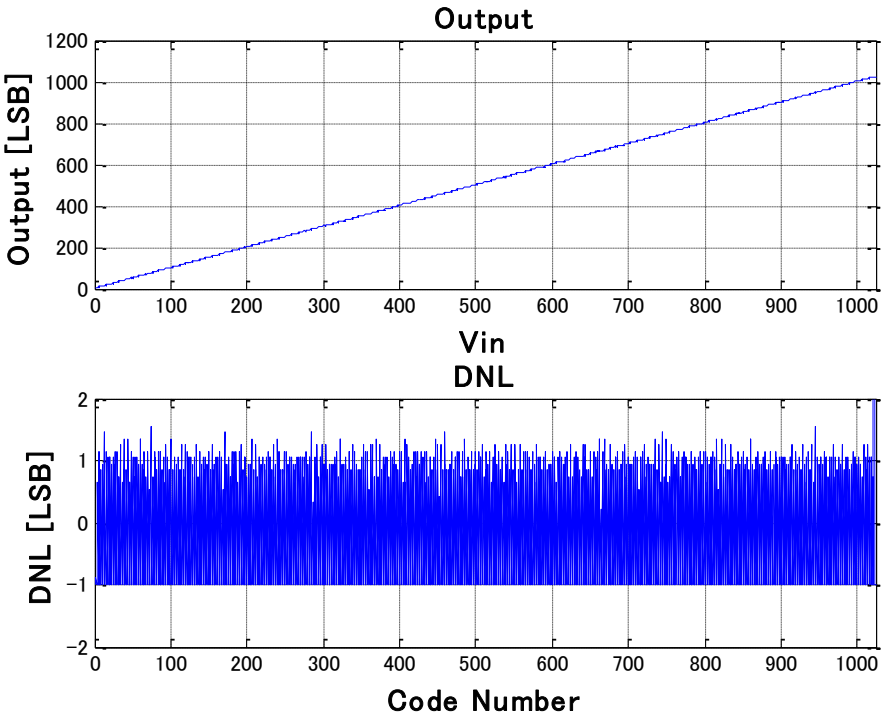
Our Proposal: Digital Correction by Redundancy



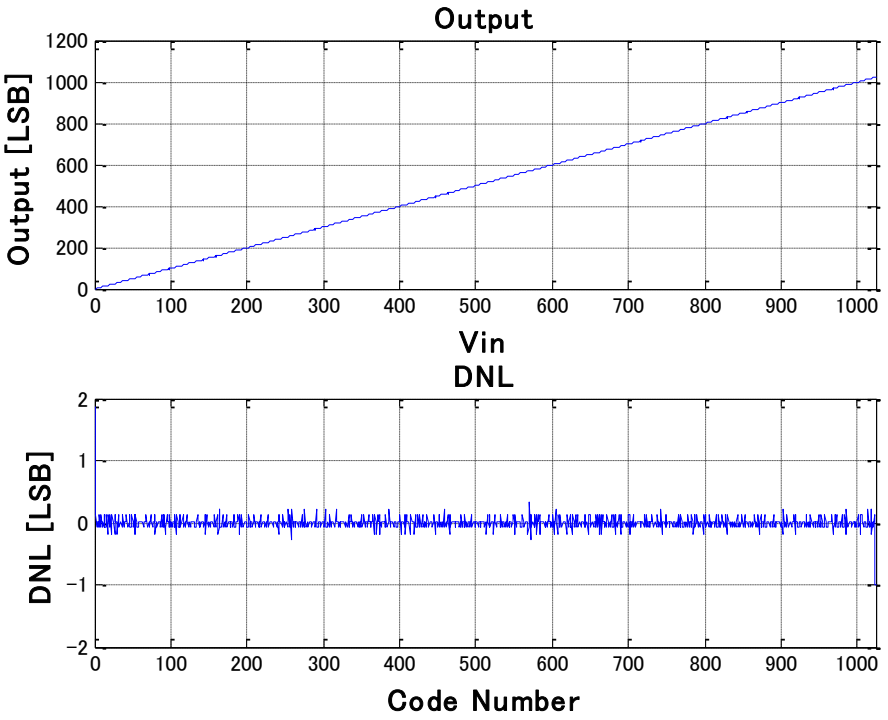
MATLAB Simulation（Ramp Input）

Comp1（low power）　offset：＋4.0 LSB　noise：1.0 LSB
Comp2（high power）　offset：－2.0 LSB　noise：0.2 LSB
W/O analog tuning of comparator offsets

IMEC method (binary)



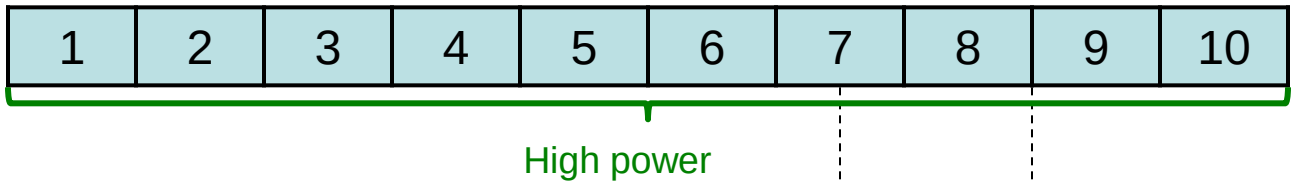
Proposed method (non-binary)



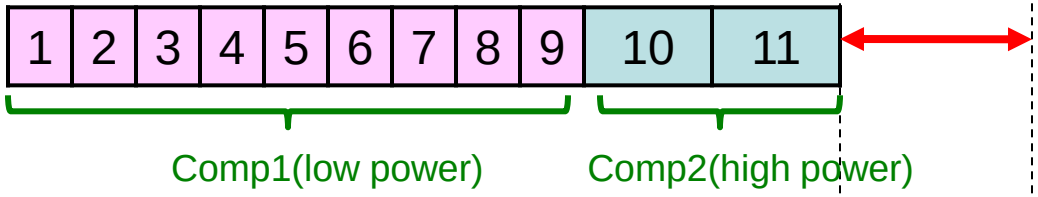
Trade-off of power and comparator offset mismatch allowance

Smaller mismatch ⇨ More power reduction

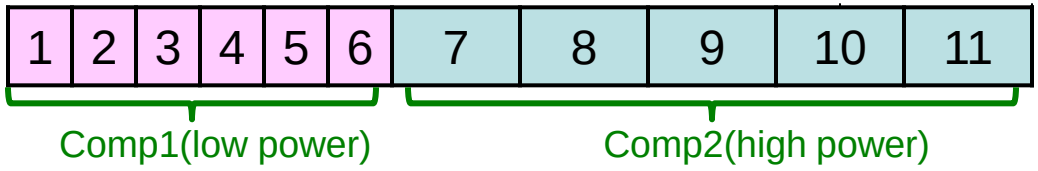
1-comparator SAR ADC



IMEC method 2-comparator (offset mismatch allowance : small)



Proposed 2-comparator (offset mismatch allowance: large)



Total comparator power

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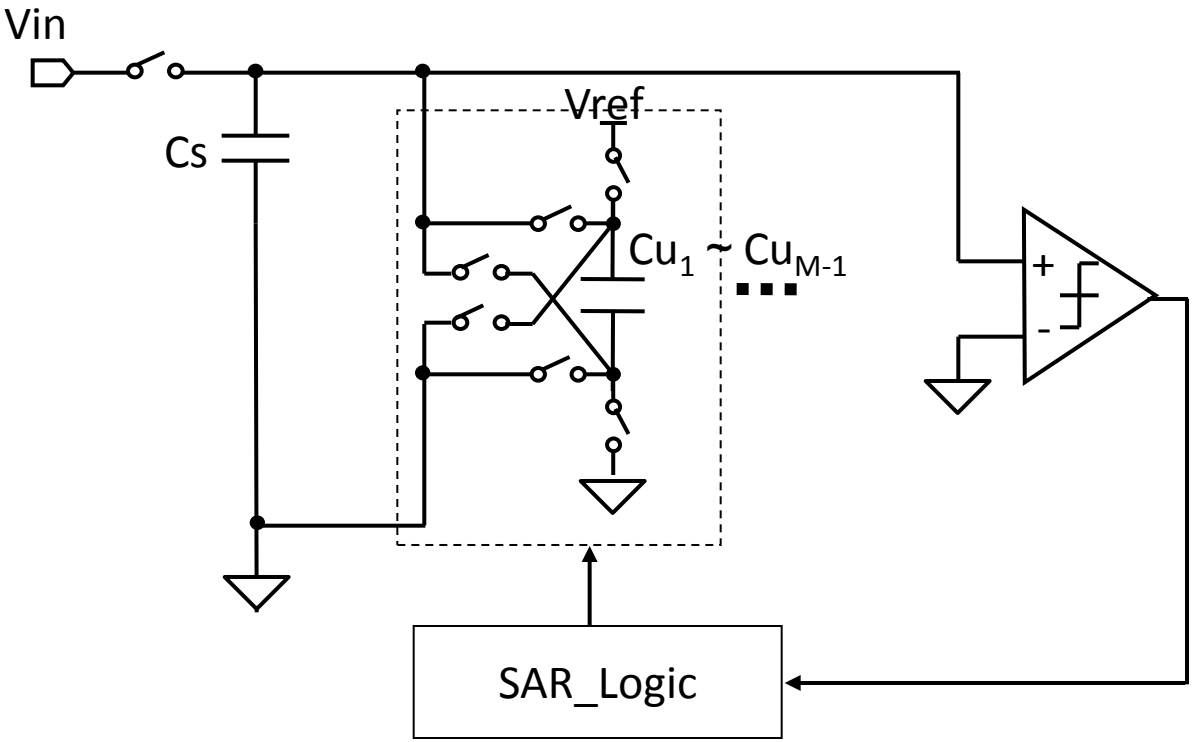
Charge-Sharing Binary SAR ADC

Proposed by IMEC

Low power SAR ADC

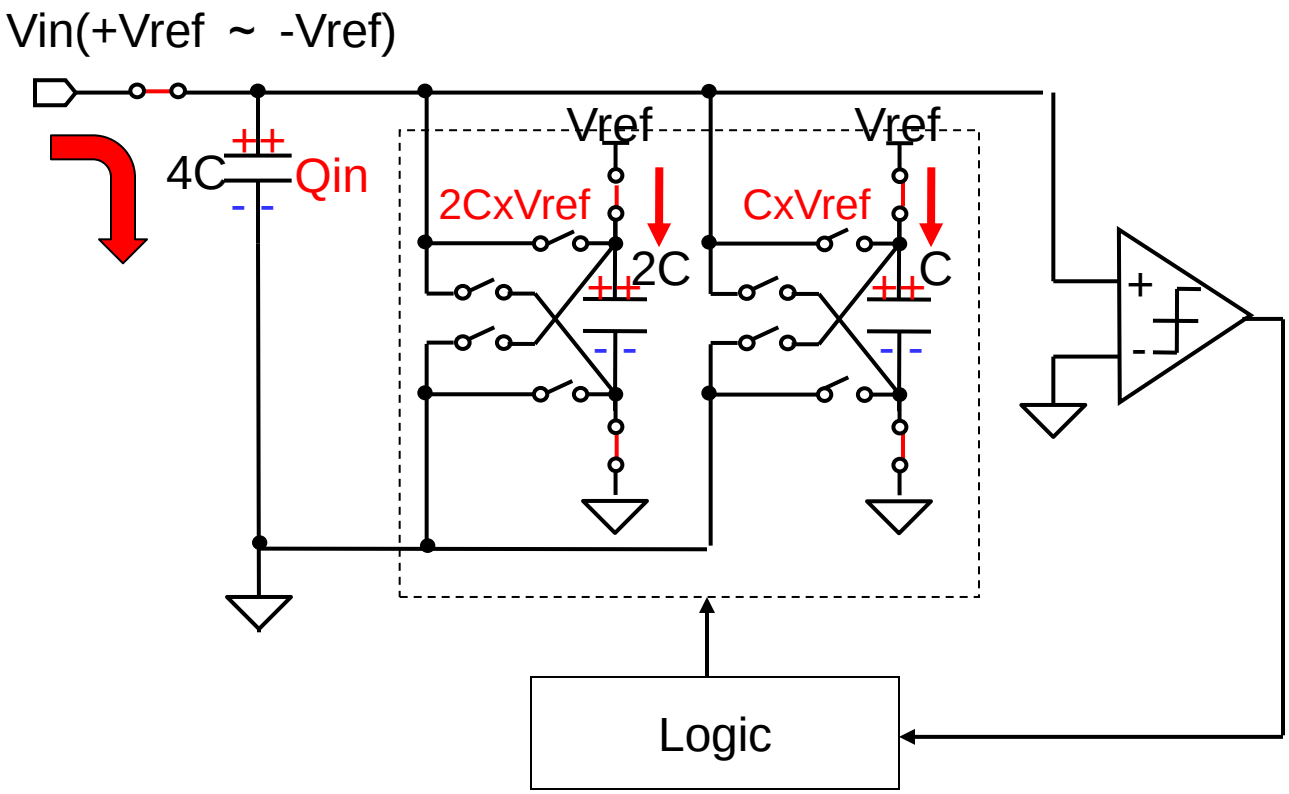


References

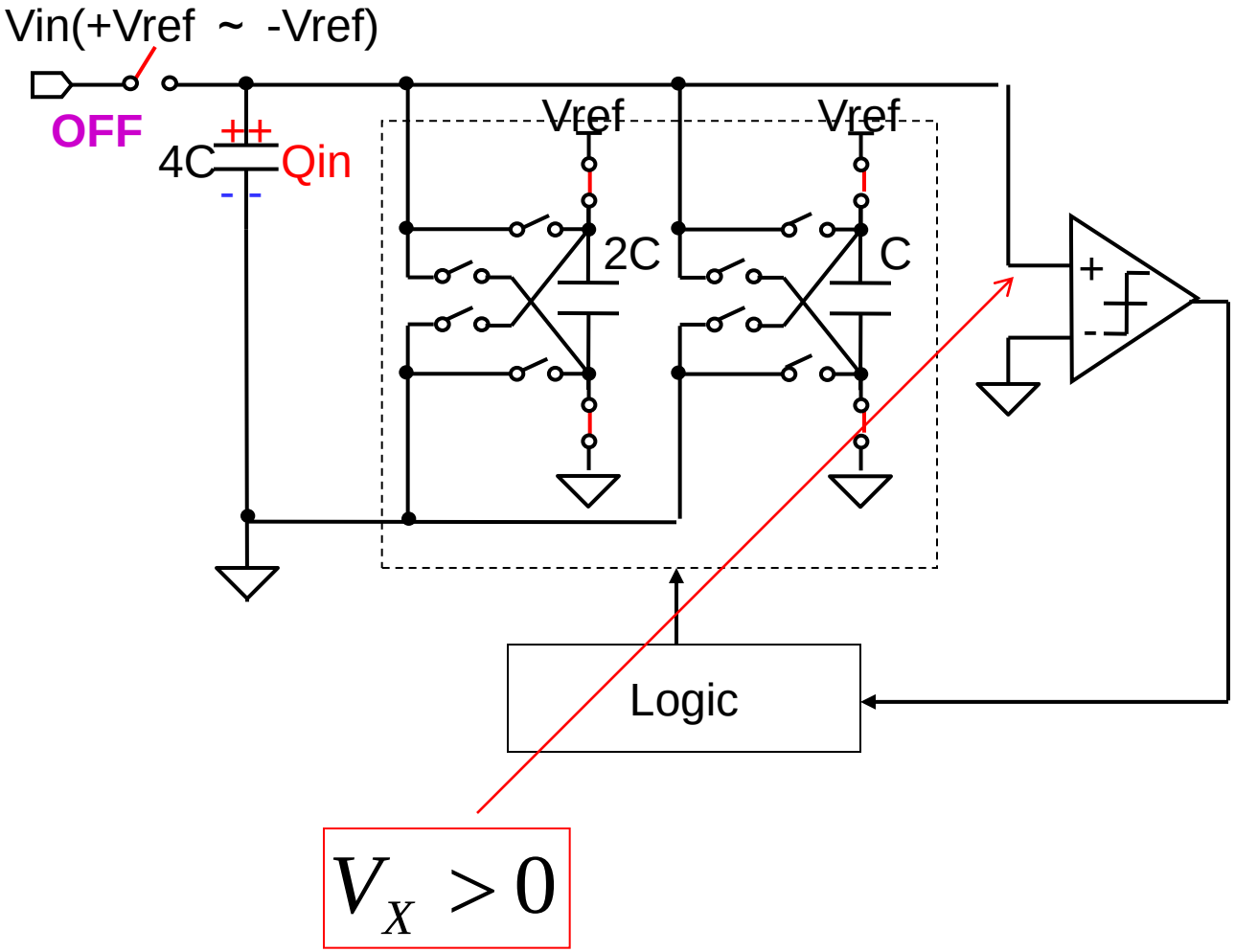
[1] J. Craninckx and G. Van der Plas,
“A 65fJ/Conversion-Step 0-to-50Ms/s 0-to-0.7mW 9b Charge-Sharing SAR ADC in 90nm Digital CMOS ”,
ISSCC Dig. Tech. Papers, pp. 246-247, Feb. 2007.

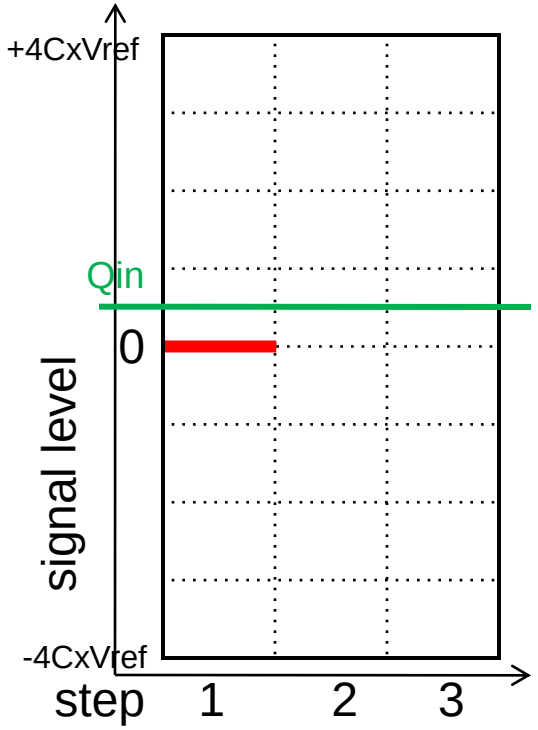
[2] V.Giannini, P.Nuzzo, V.Chironi,A.Baschirotto, G.V.Plas,J.Craninckx
“ An 820 μ W 9b 40MS/s Noise-Tolerant Dynamic-SARADC in 90nm Digital CMOS ”
ISSCC (Feb.2008).

Operation (sampling)



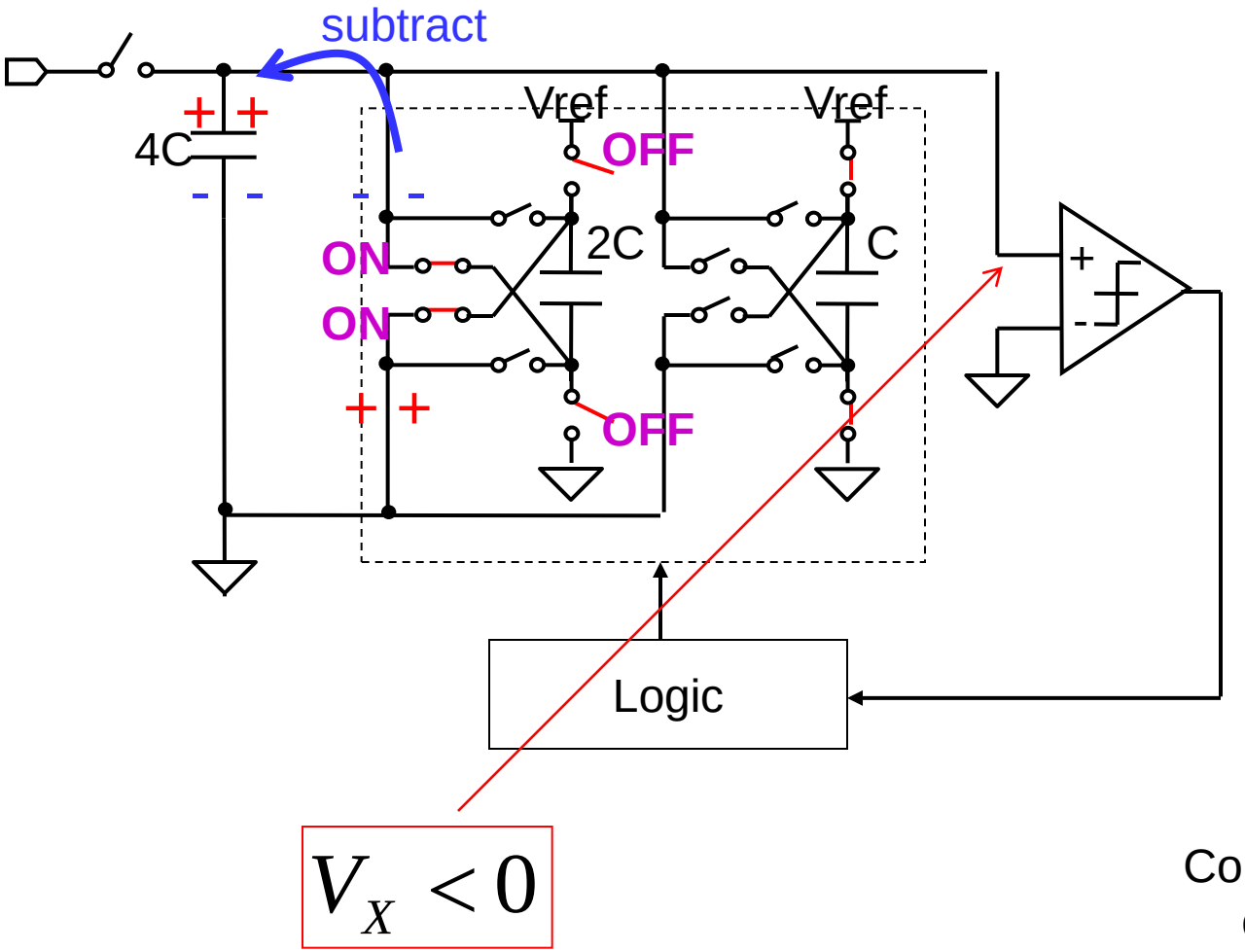
Operation (step1)

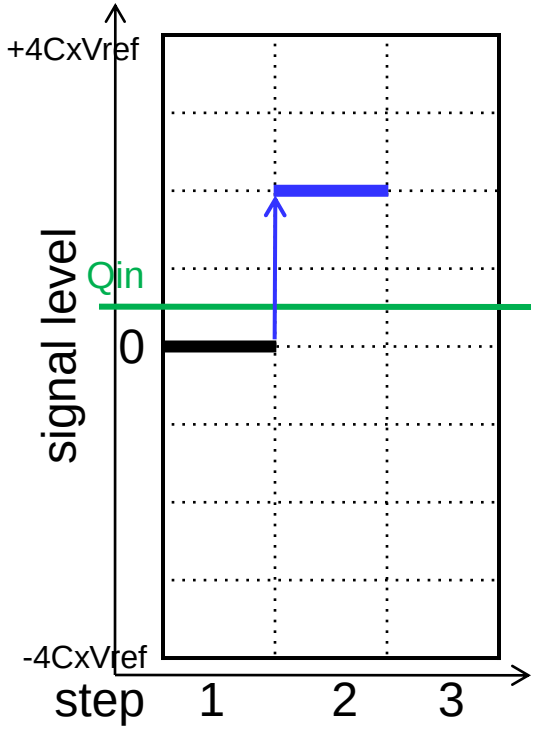




Comparator output : 1

Operation (step2)



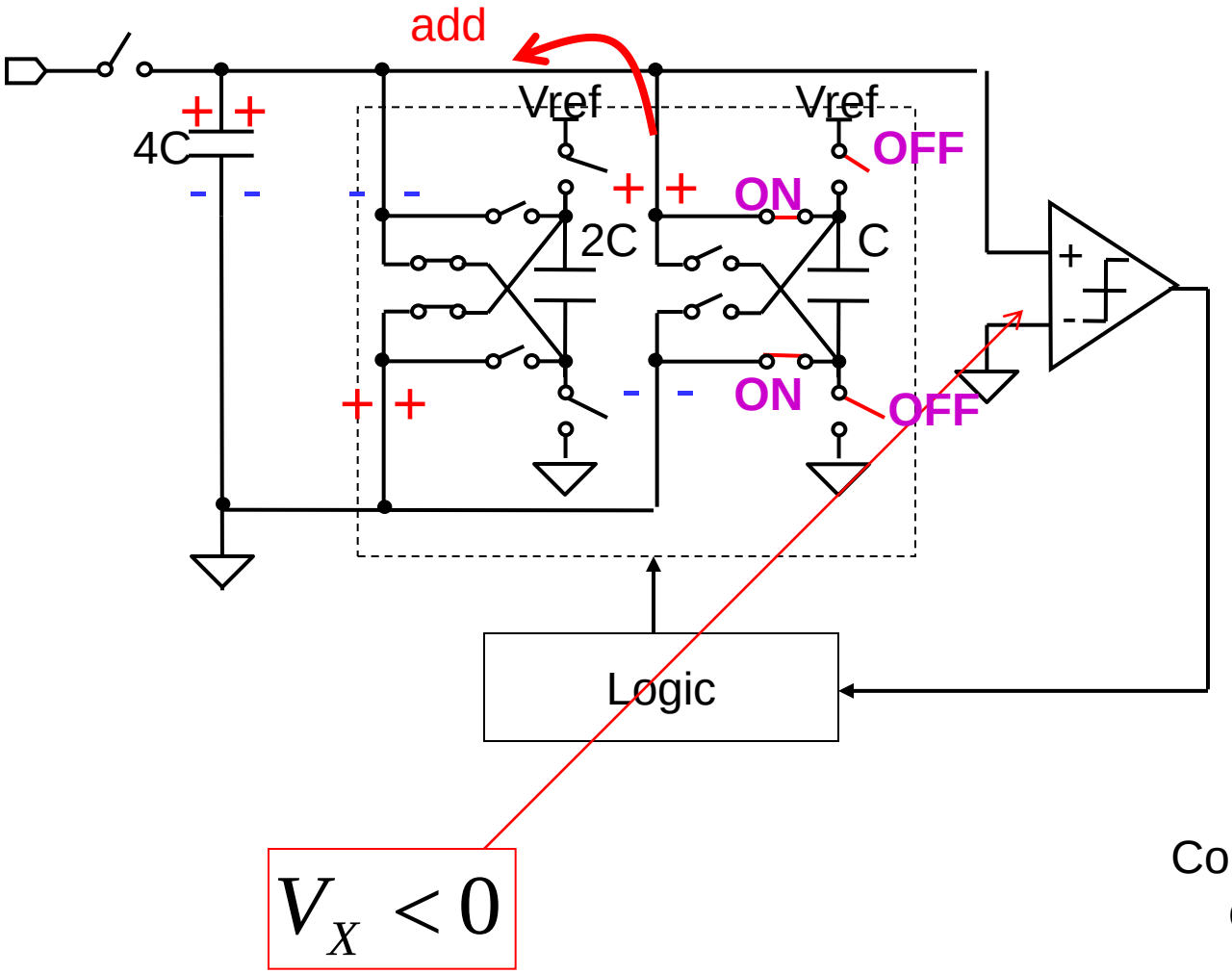


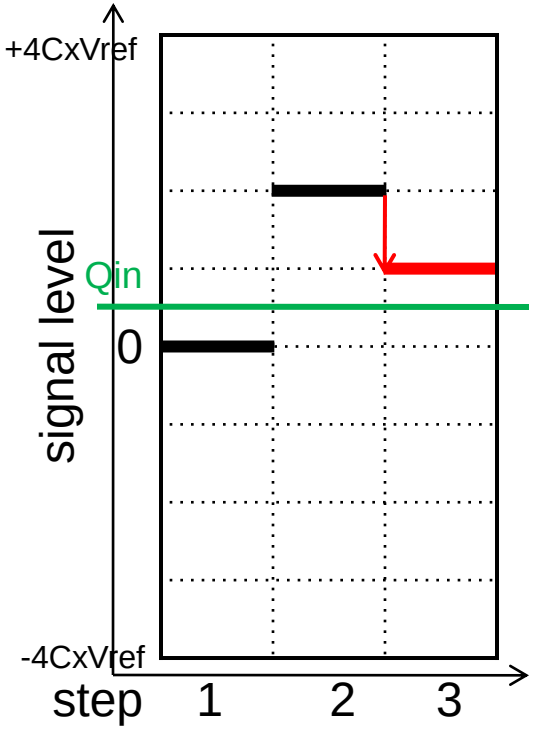
$V_X < 0$

Comparator output **1** **0**

Comparator output : 0

Operation (step3)





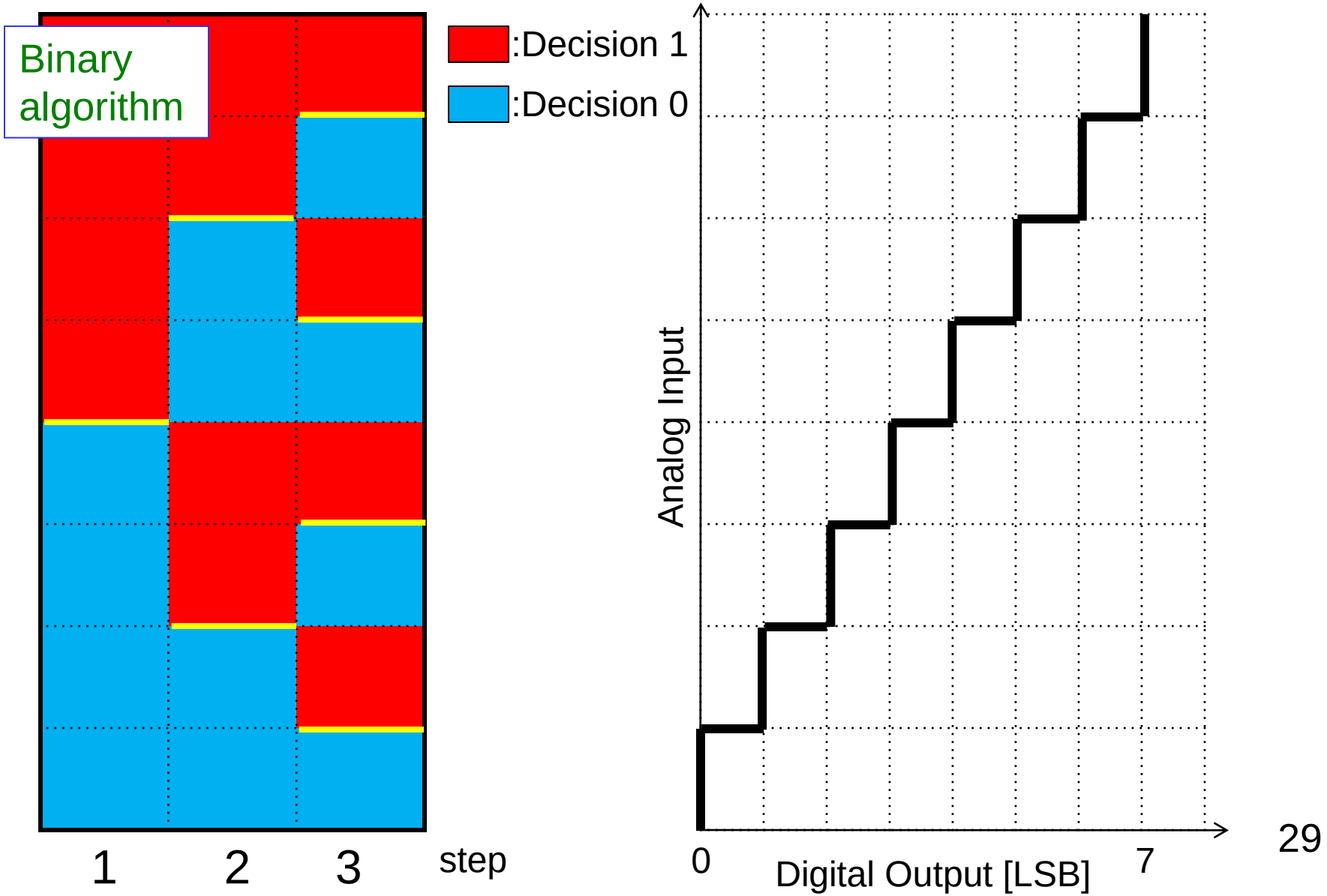
$V_X < 0$

Comparator output : 0

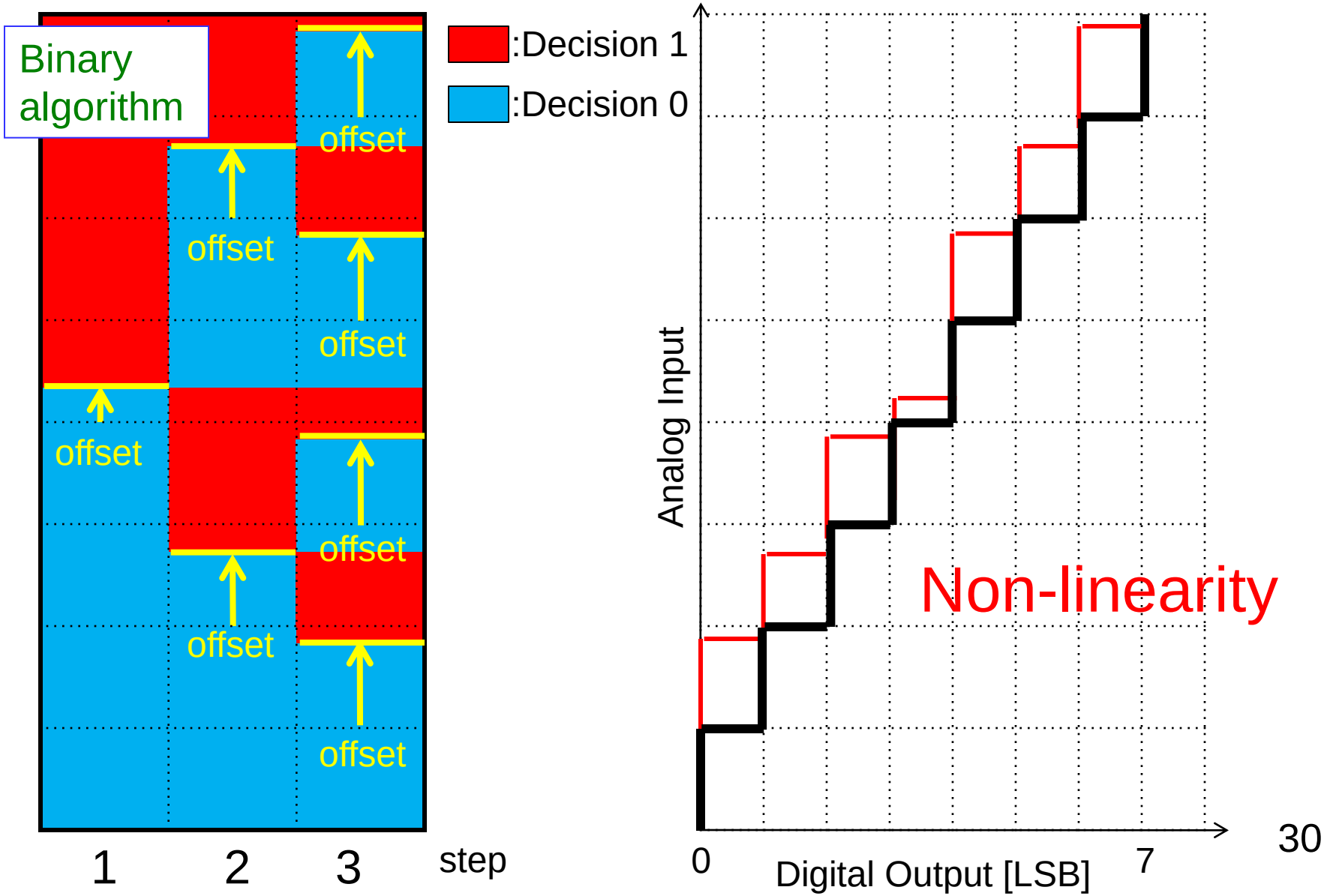
Comparator output **1 0 0**

Digital output : 4

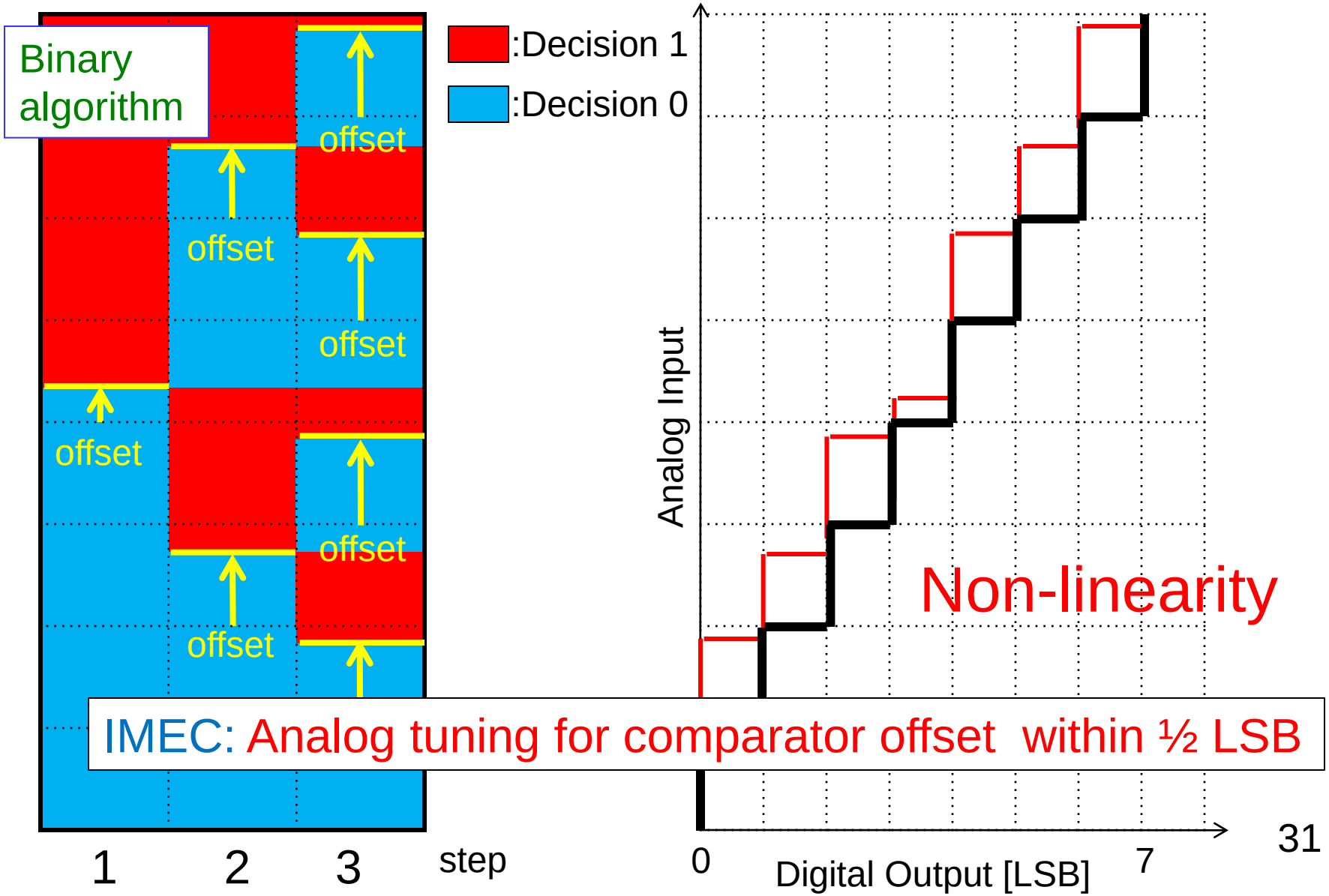
Charge-Sharing SAR ADC
Comparator Offset Effects



Charge-Sharing SAR ADC
Comparator Offset Effects



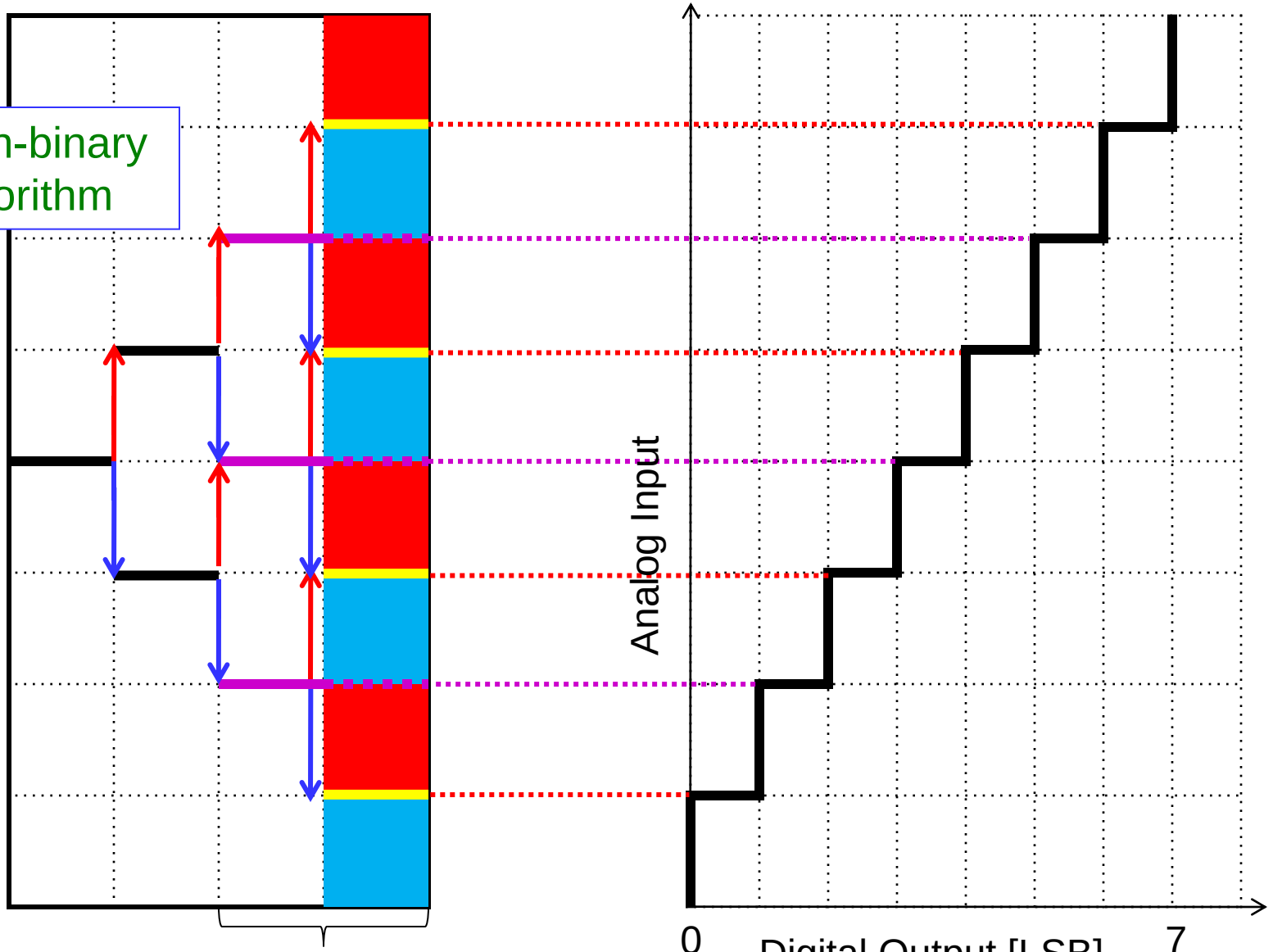
Charge-Sharing SAR ADC
Comparator Offset Effects



IMEC: Analog tuning for comparator offset within ½ LSB

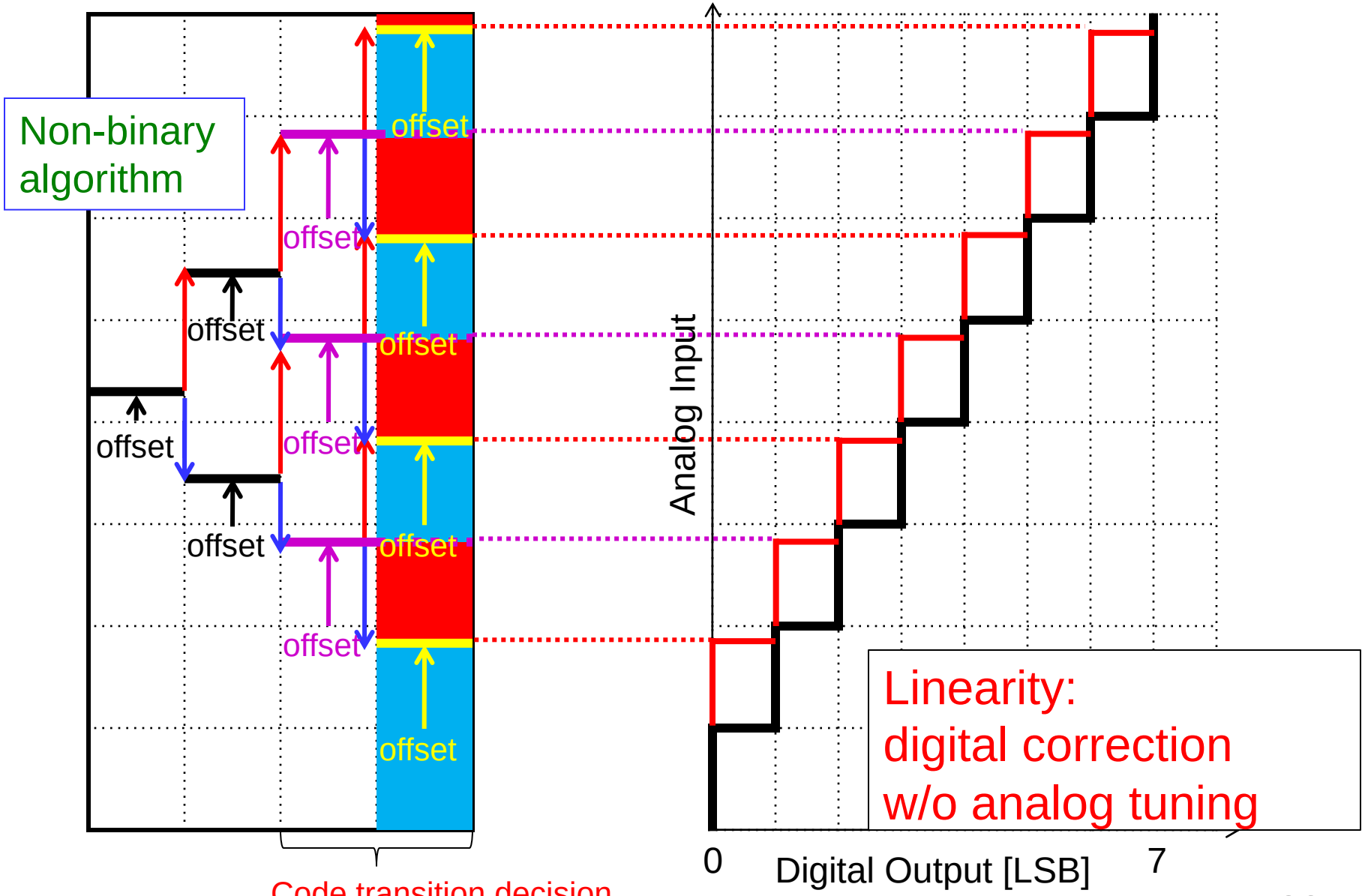
Our Proposal : Digital Correction by Redundancy

Non-binary algorithm



Offset changes are small at latter stages

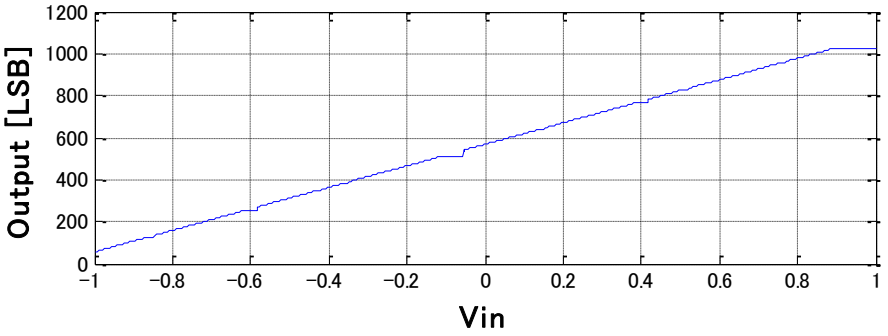
Proposed : Digital Correction by Redundancy

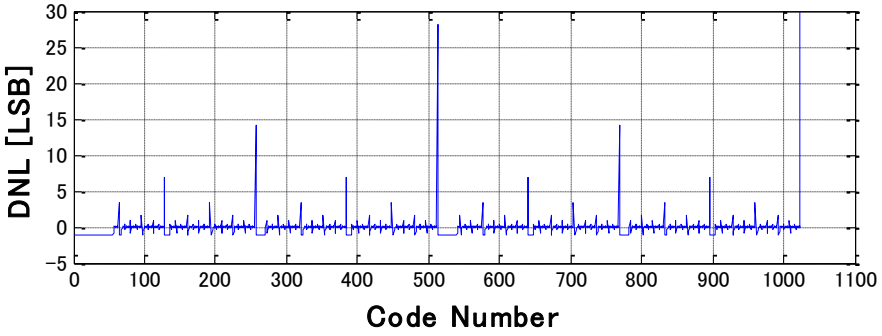


MATLAB Simulation（Ramp Input）

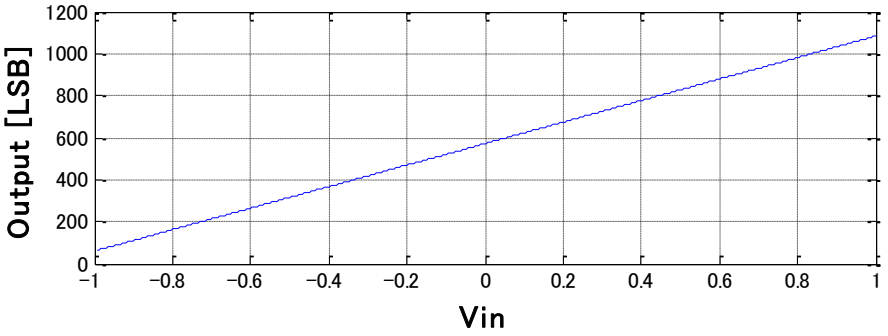
Vin: - 1 ~ +1 , Vref = 1 V , Cs = 512 C
Vos = 55 m V
W/O analog tuning for comparator offset

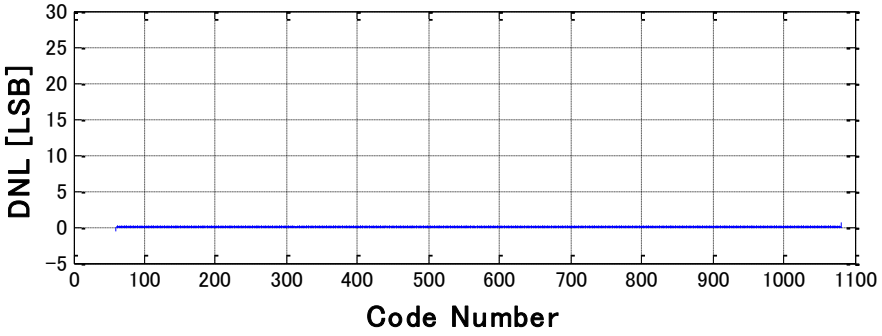
IMEC method (binary)





Proposed method (non-binary)





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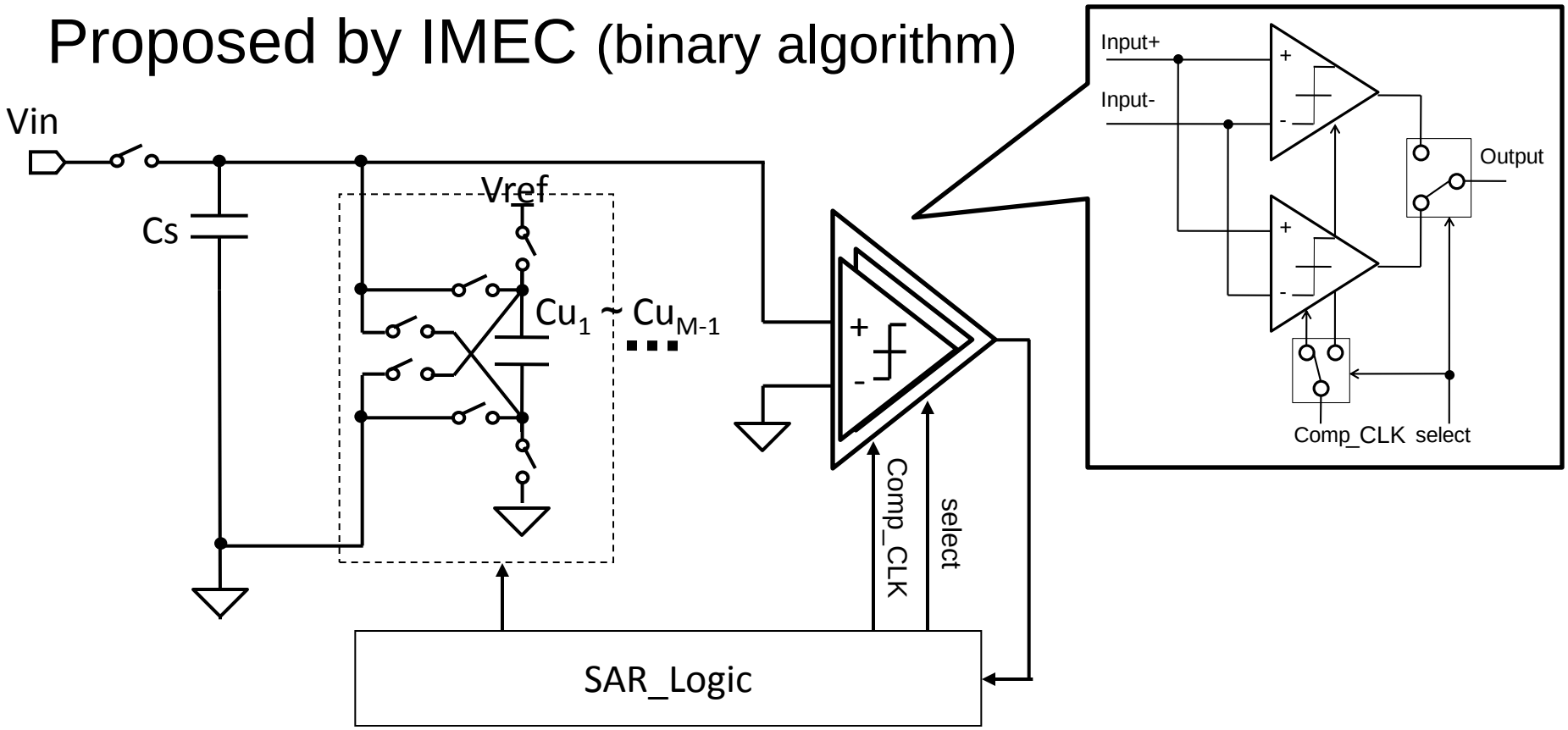
Two-Comparator Charge-Sharing SAR ADC

Proposed by IMEC (binary algorithm)



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[1] V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. V. Plas, J. Craninckx
" An 820 μW 9b 40MS/s Noise-Tolerant Dynamic-SAR ADC in 90nm Digital CMOS "
ISSCC (Feb.2008).

MATLAB Simulation（Ramp Input）

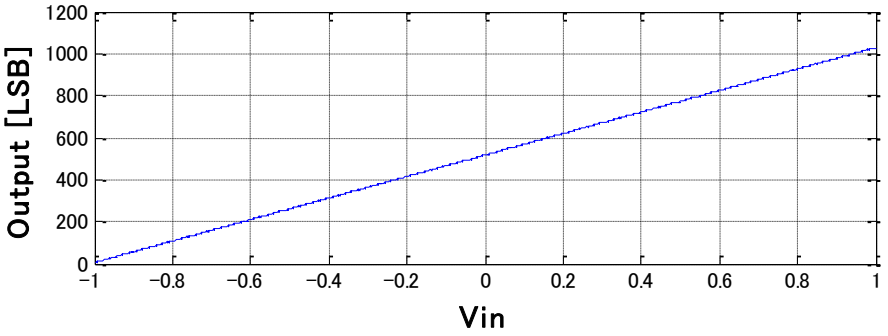
Vin: - 1 ~ +1, Vref = 1 V , Cs = 512 C

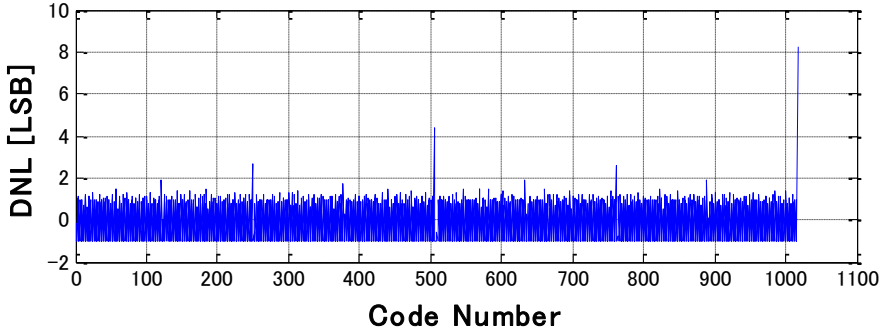
Comp1 (low power) offset : + 8.0 mV noise : 1.0 mV

Comp2 (high power) offset : - 7.0 mV noise : 0.2 mV

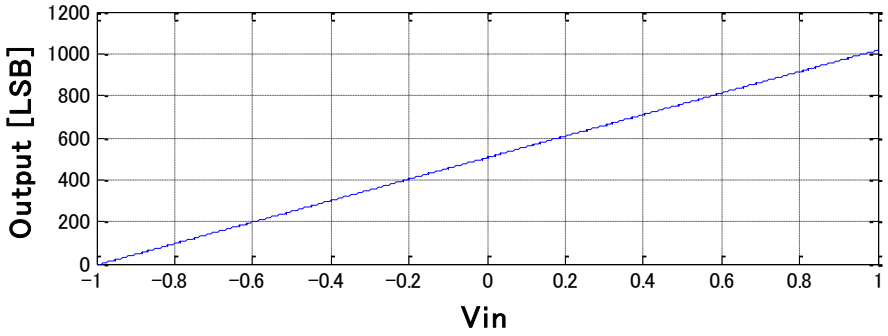
W/O analog tuning for comparator offsets

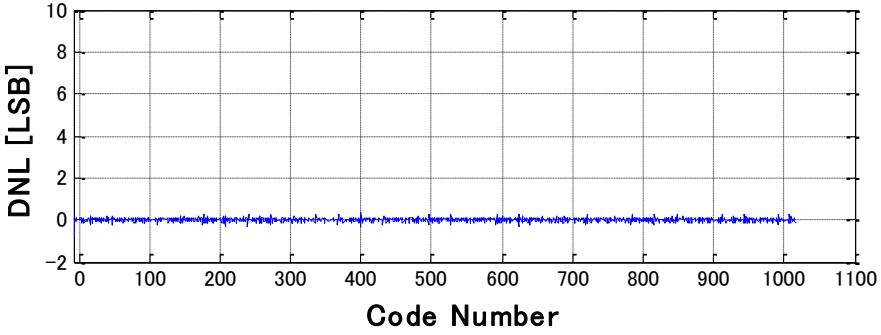
IMEC method (binary)





Proposed method (non-binary)





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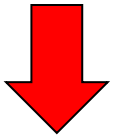
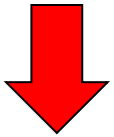
Conclusion

- Proposal of using a non-binary SA algorithm for low-power techniques:
  - Two-comparator
  - Charge-sharing
  - Their combination



- No analog tuning
- Only digital error correction



- Demonstrate with MATLAB simulation.