APCCAS 2010 Session :Hang Jebat 1 & 2 ADC / DAC II

Paper ID : 1569334445

SAR ADC That is Configurable to Optimize Yield

T. Ogawa, H. Kobayashi, Y. Tan, S. Ito, S. Uemori, N. Takai, K. Niitsu, T. J. Yamaguchi, T. Matsuura, N. Ishikawa

Gunma University

Supported by STARC

Outline

- **Research purpose**
- **Background**
- **Configurable non-binary algorithm SAR ADC**
- **Production-time configuration SAR ADC**
- **Test chip design & measurement Results**
- **Conclusion**

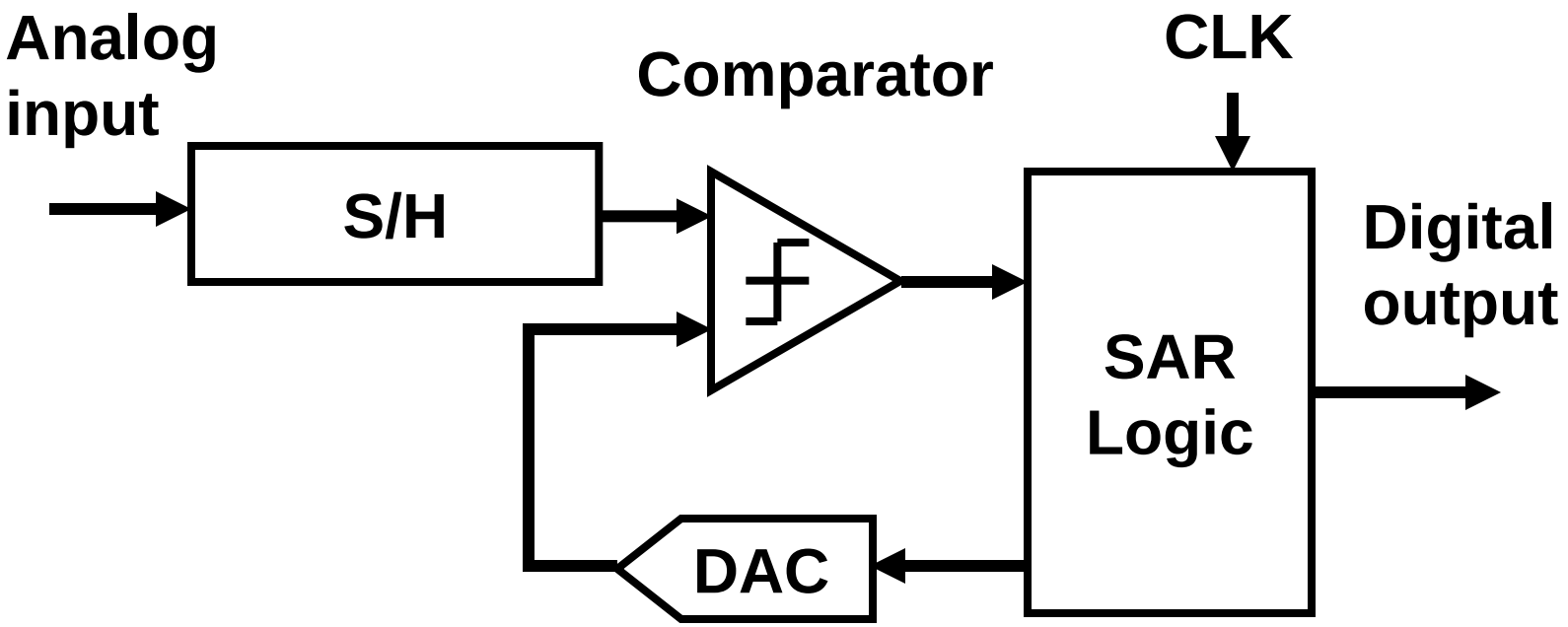
Research purpose

- **Non-binary SAR ADC can achieve …**
  - **High-speed operation** ☺
  - **Power consumption increased** ☹
- **This work introduces the solution for the speed-power trade-off for yield improvement.** ☺
  - **Propose the method of estimating the "DAC output settling time and speed margin" at production test.**
  - **Test chip fabrication & its measurements demonstrate the effectiveness of our approach.** ☺

Outline

- Research purpose
- **Background**
  - **Successive approximation algorithm**
  - DAC incomplete settling
  - SA algorithm selection
- Configurable non-binary algorithm SAR ADC
- Production-time configuration SAR ADC
- Test chip design & measurement Results
- Conclusion

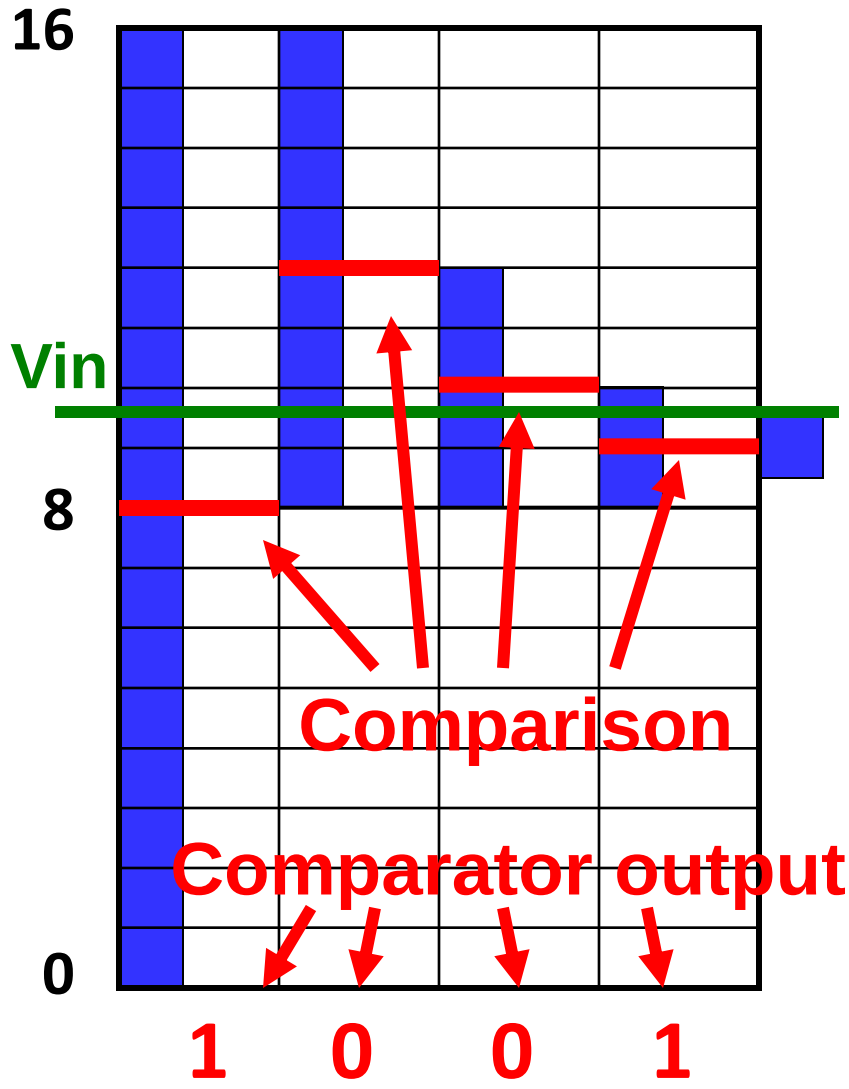
SAR ADC Block



SAR ADC is “digital rich” approach.

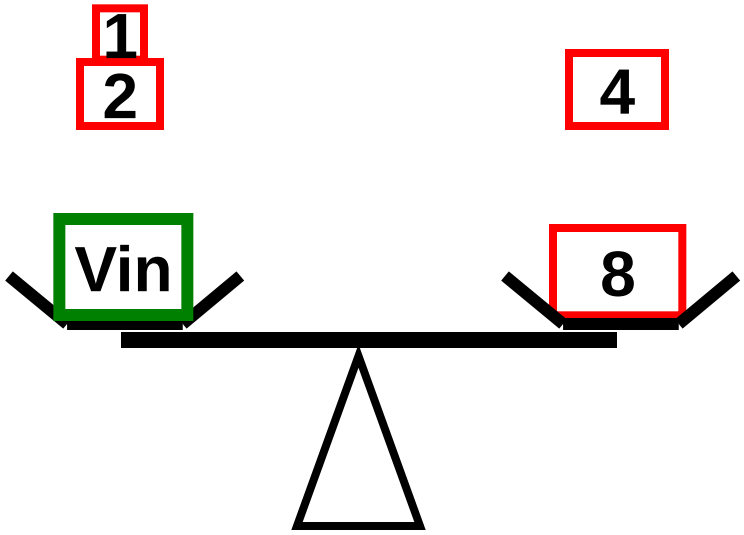
→ Suitable for fine CMOS implementation.

Binary search algorithm



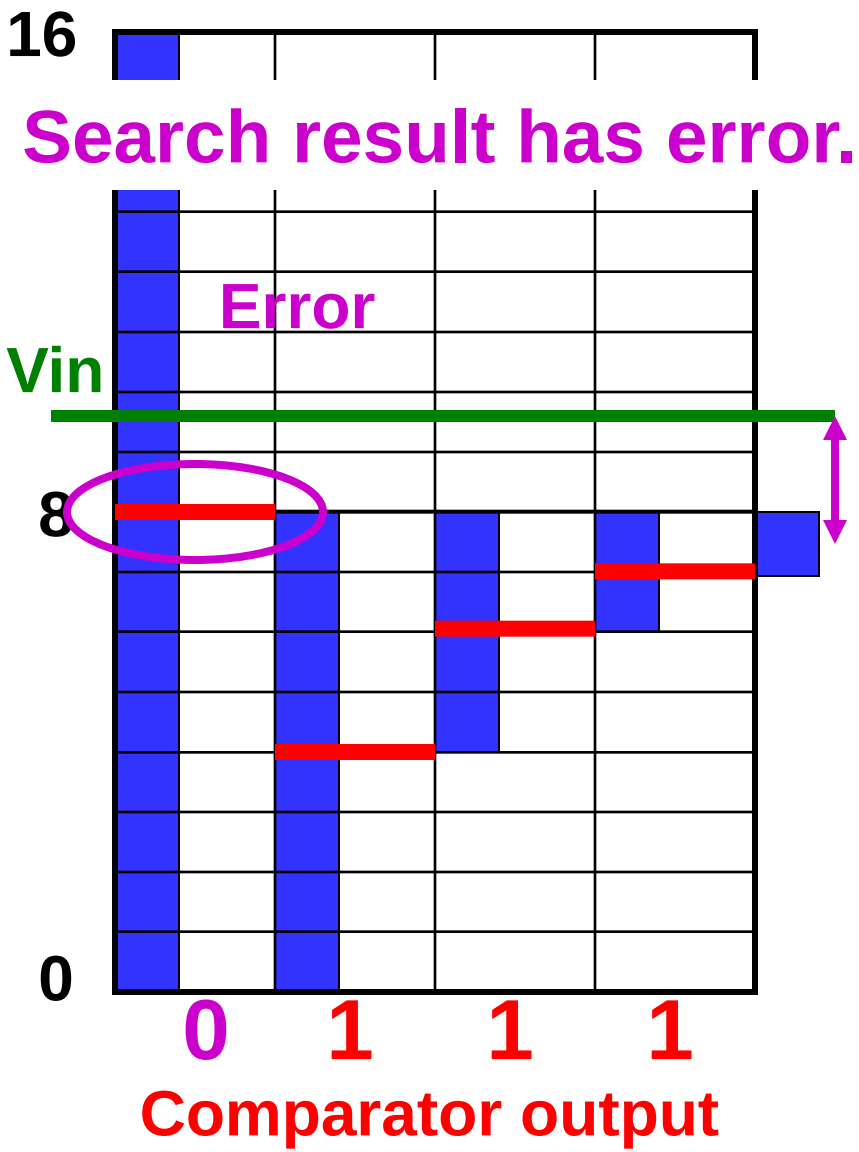
“Principle of a balance”

Binary weight 4bit 4step



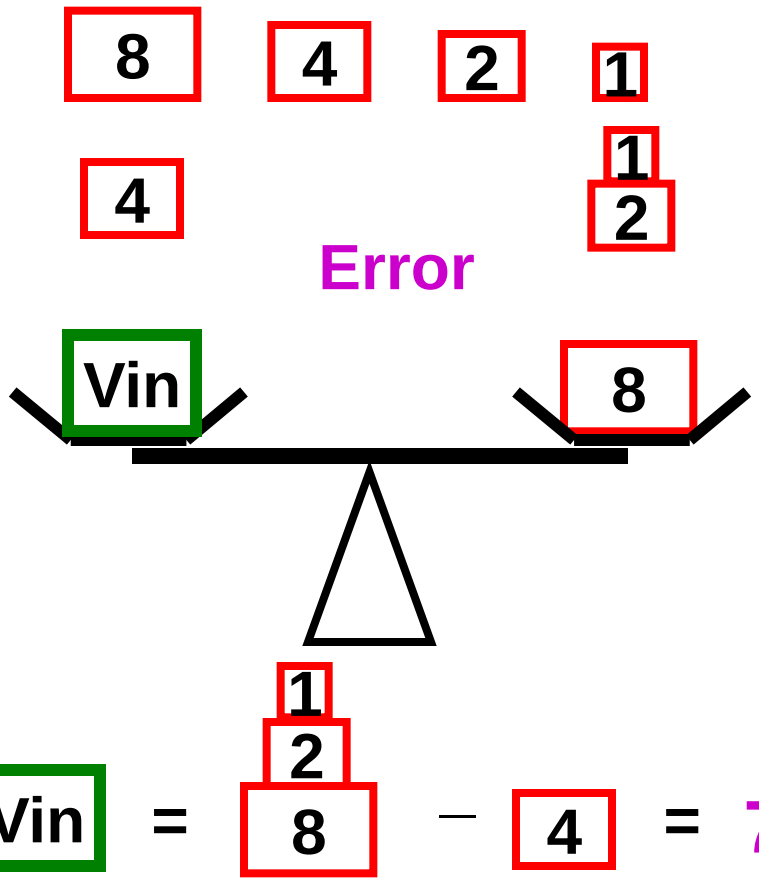
Vin = 4 + 8 − 1 + 2 = 9

Problem of binary search algorithm



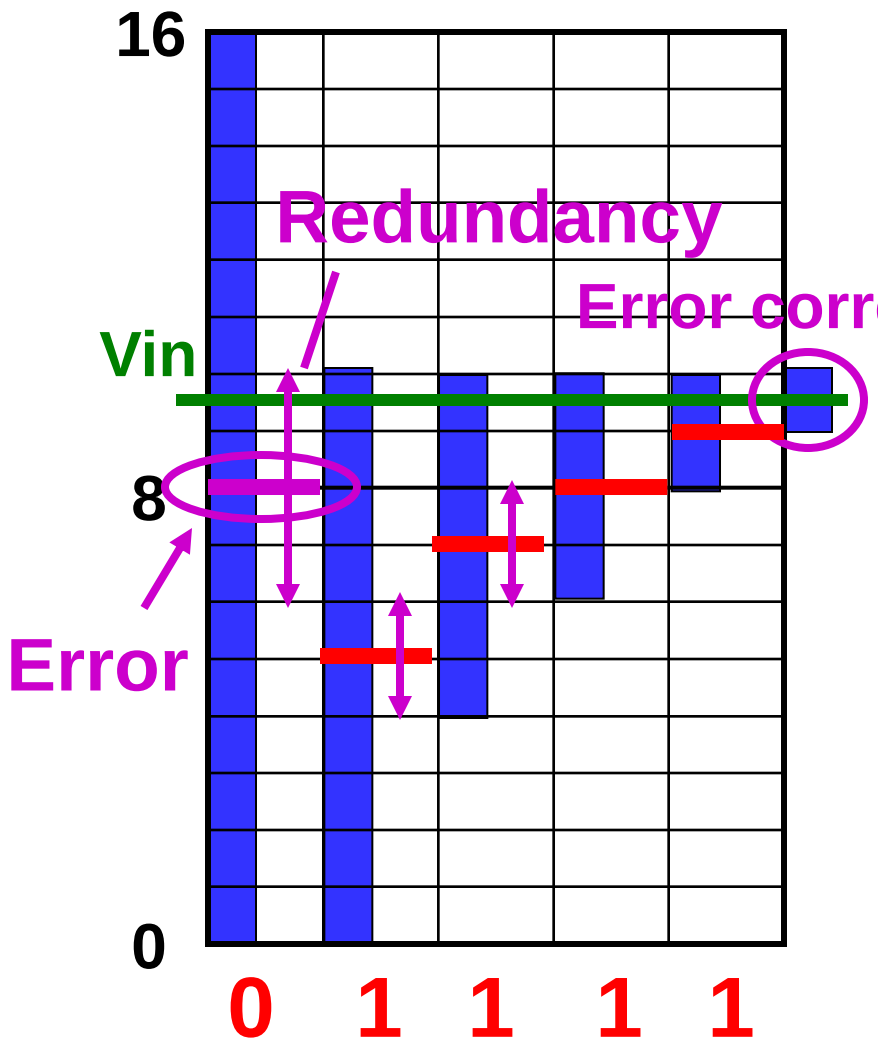
“Principle of a balance”

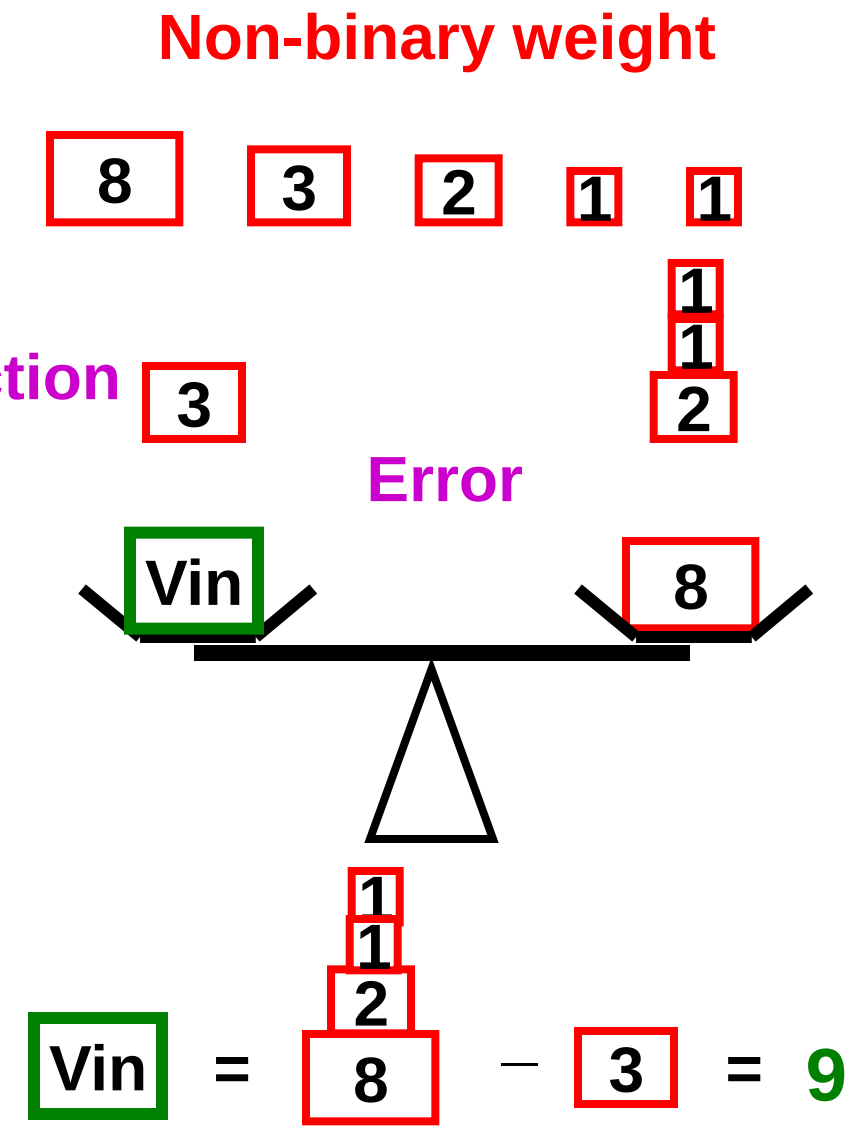
Binary weight 4bit 4step



Digital output has error.

Error correction with non-binary





4bit 5step Redundancy:1step

Digital error correction principle of non-binary algorithm

Digital output "9" case

Binary search algorithm

Error Correction : Not Available

Comparator output: 1 0 0 1

Dout = 8 + 4 – 2 – 1 + 0.5 – 0.5 = 9 ← **Only one**

Non-binary search algorithm

Error Correction : Available

Comparator output: 1 0 1 0 1

Dout = 8 + 3 – 2 + 1 – 1 + 0.5 – 0.5 = 9 ← **Multiple**

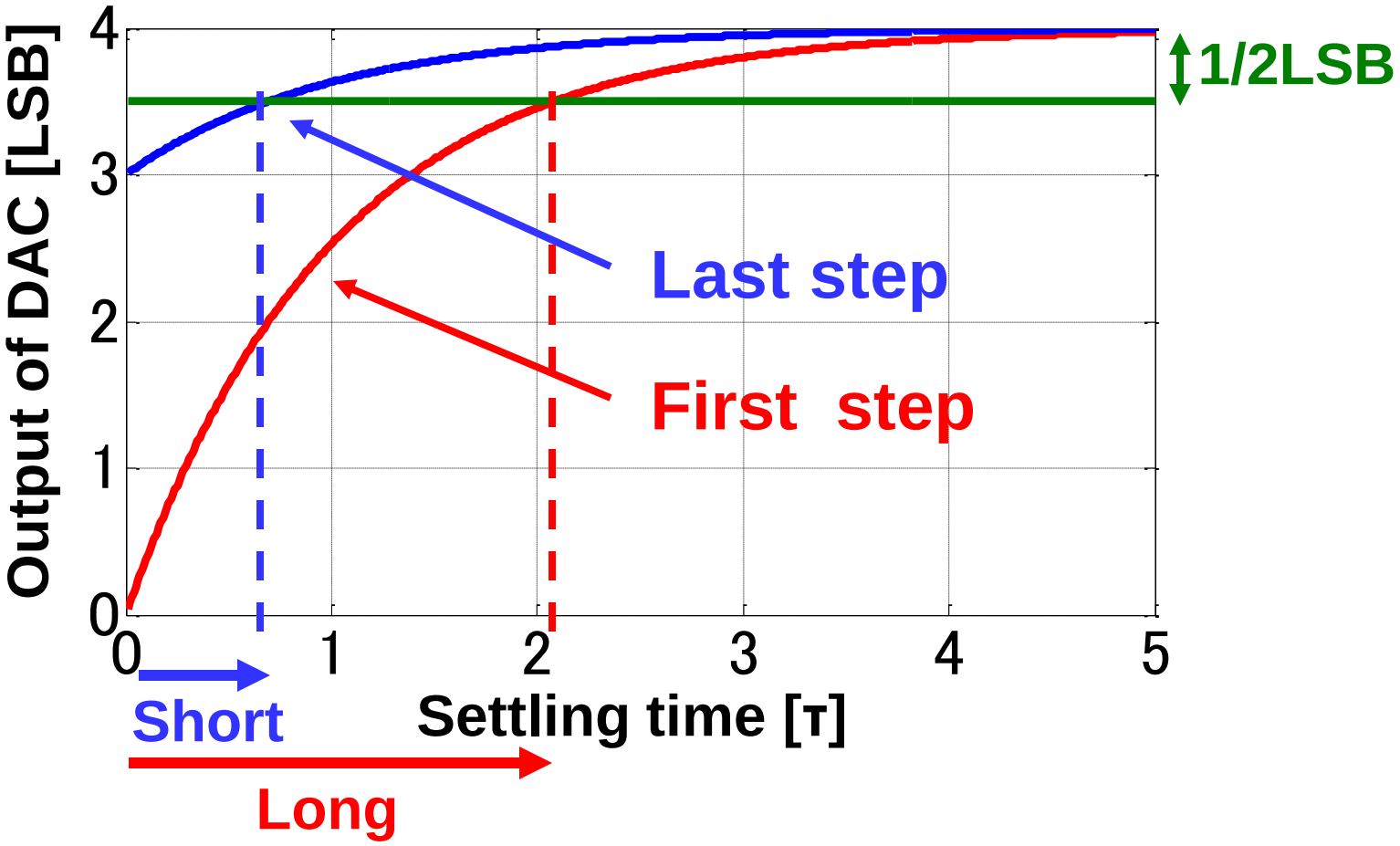
Comparator output: 0 1 1 1 1

Dout = 8 – 3 + 2 + 1 + 1 + 0.5 – 0.5 = 9

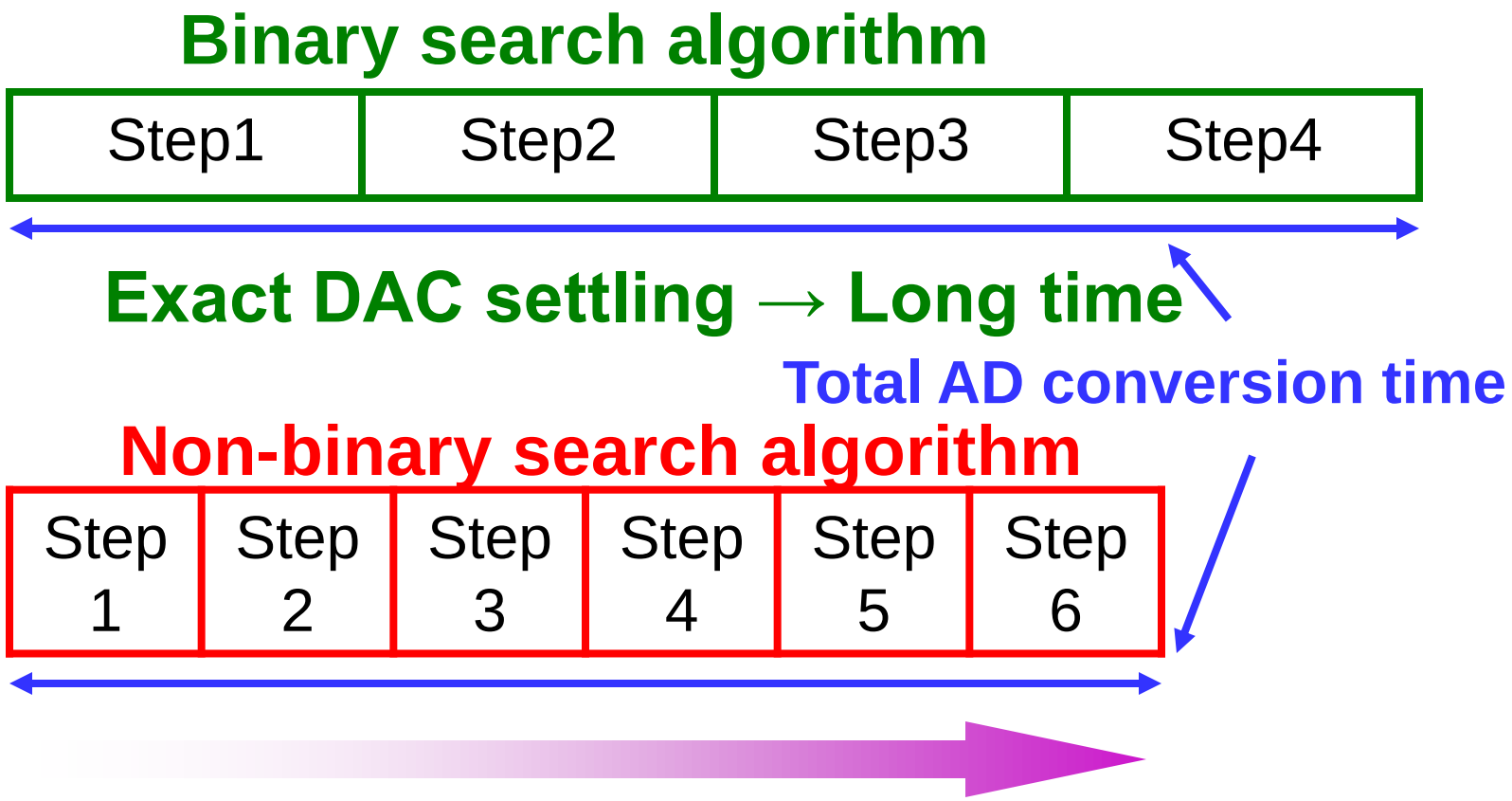
Outline

- Research purpose
- Background
  - Successive approximation algorithm
  - **DAC incomplete settling**
  - SA algorithm selection
- Configurable non-binary algorithm SAR ADC
- Production-time configuration SAR ADC
- Test chip design & measurement Results
- Conclusion

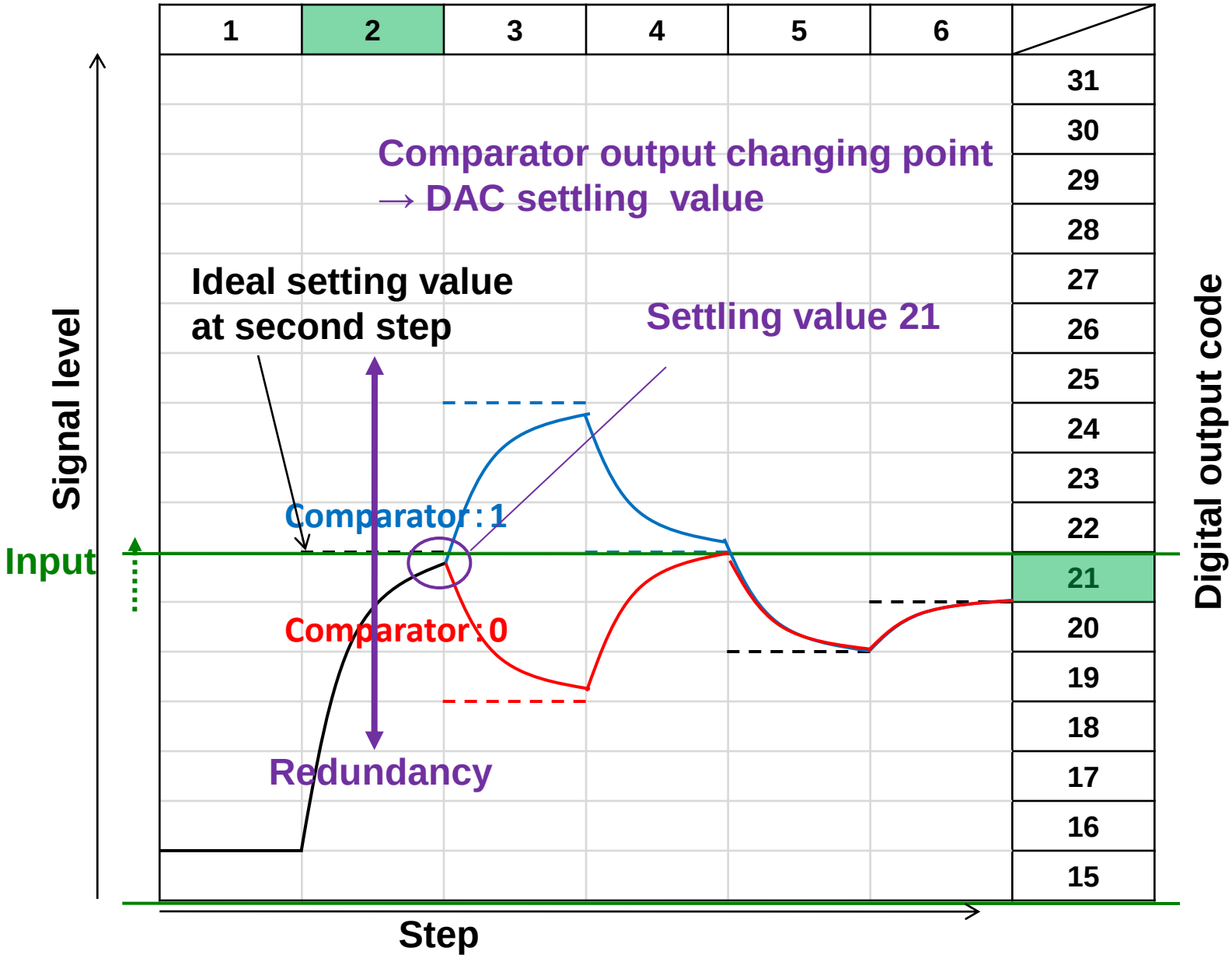
Settling of DAC output



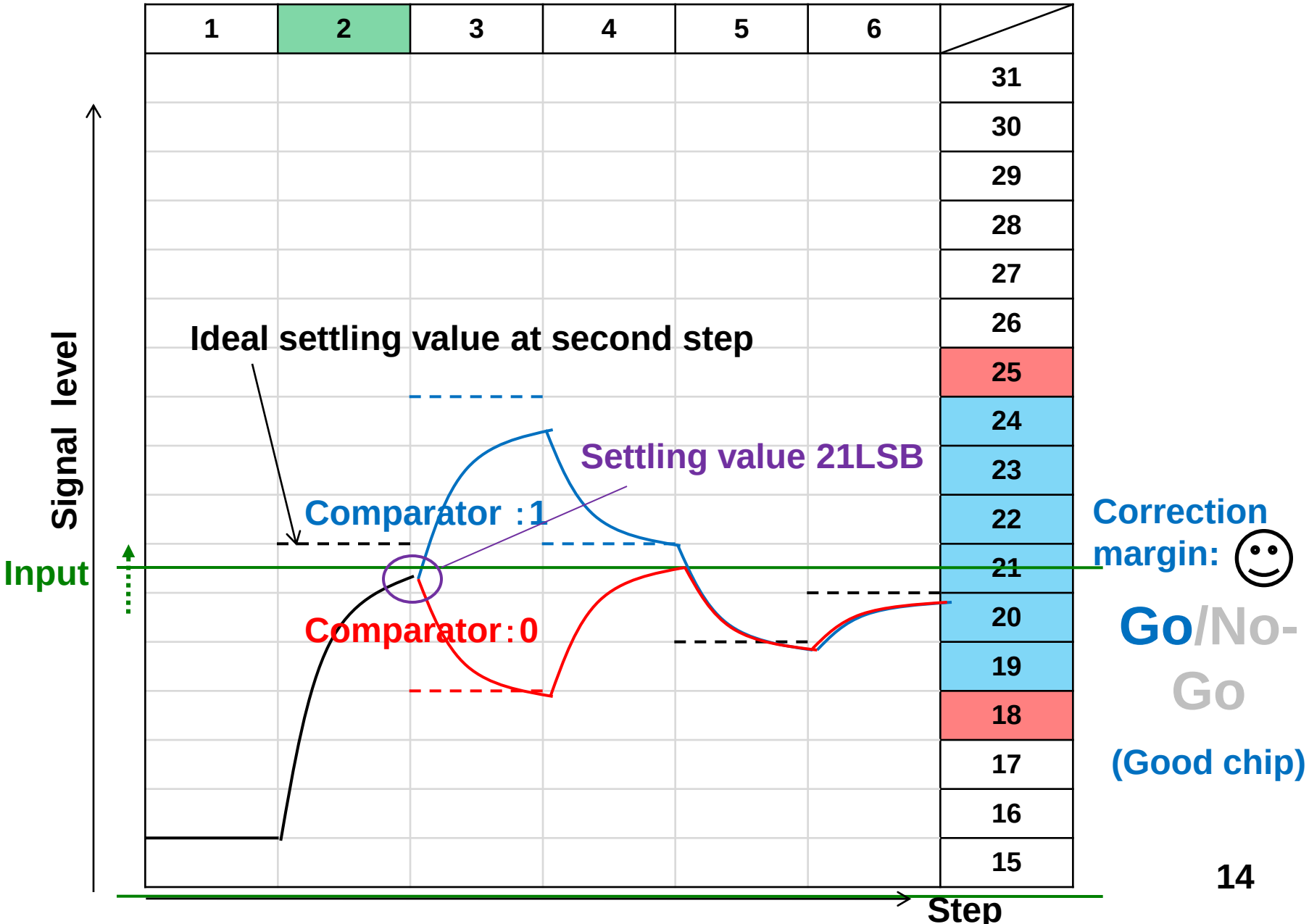
AD conversion time for both algorithms



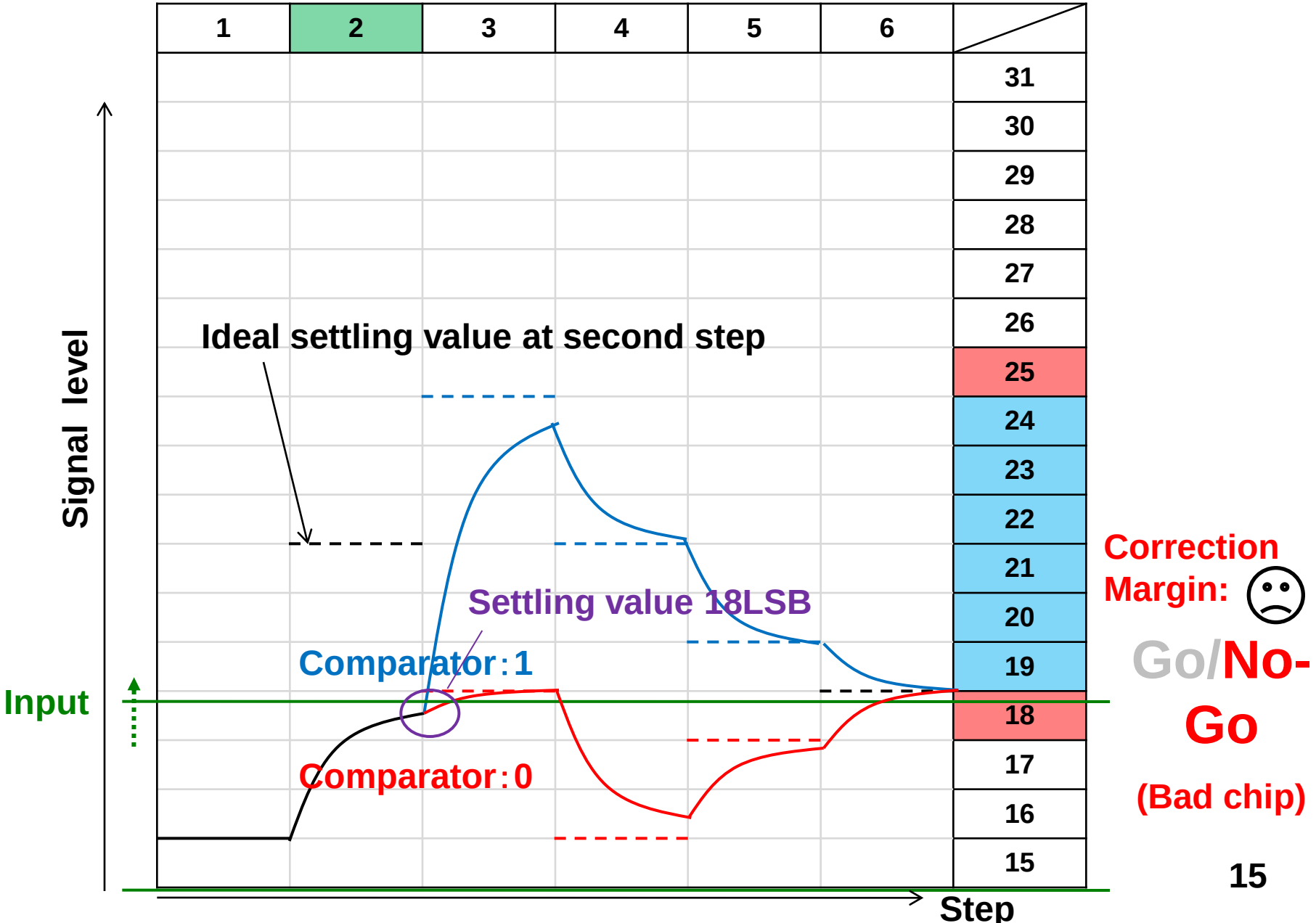
DAC settling estimation algorithm



Setting test at second step (5bit 6step)



Setting test at second step (5bit 6step)



Settling value at second step

$$V_{DAC}(k+1) = V_{DAC}(k) + DAC(k+1) * (1 - e^{-\frac{t}{\tau_{TP}}})$$

$$512 + 246(1 - e^{-\frac{2.3\tau_{TP}}{\tau_{TP}}}) = 733.3LSB$$

DAC Settling estimation

Step →

Comparator output

1	2	3	4	5	6	7	8	9	10	11	12	ADC output
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	0	1	1	733
1	1	0	0	0	0	0	1	1	0	1	1	**733**
1	0	1	1	0	1	0	1	0	0	1	1	**733**
1	0	1	1	0	1	0	1	0	0	1	1	733
1	0	1	1	0	1	0	1	0	0	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	0	1	731
1	0	1	1	0	1	0	0	1	1	0	1	731

Outline

- Research purpose
- Background
  - Successive approximation algorithm
  - DAC incomplete settling
  - **SA algorithm selection**
- Configurable non-binary algorithm SAR ADC
- Production-time configuration SAR ADC
- Test chip design & measurement Results
- Conclusion

SA algorithm selection for 10bit non-binary SAR ADC

Fast chip (τ=3.5 ns)
10bit 11step
Low-power

Step	P(k)
1	512
2	256
3	115
4	63
5	35
6	19
7	11
8	6
9	3
10	2
11	1

Middle chip (τ=4.0 ns)
10bit 12step
Middle-power

Step	P(k)
1	512
2	256
3	109
4	62
5	36
6	21
7	12
8	7
9	4
10	2
11	1
12	1

Slow chip (τ=4.5 ns)
10bit 13step
High-power

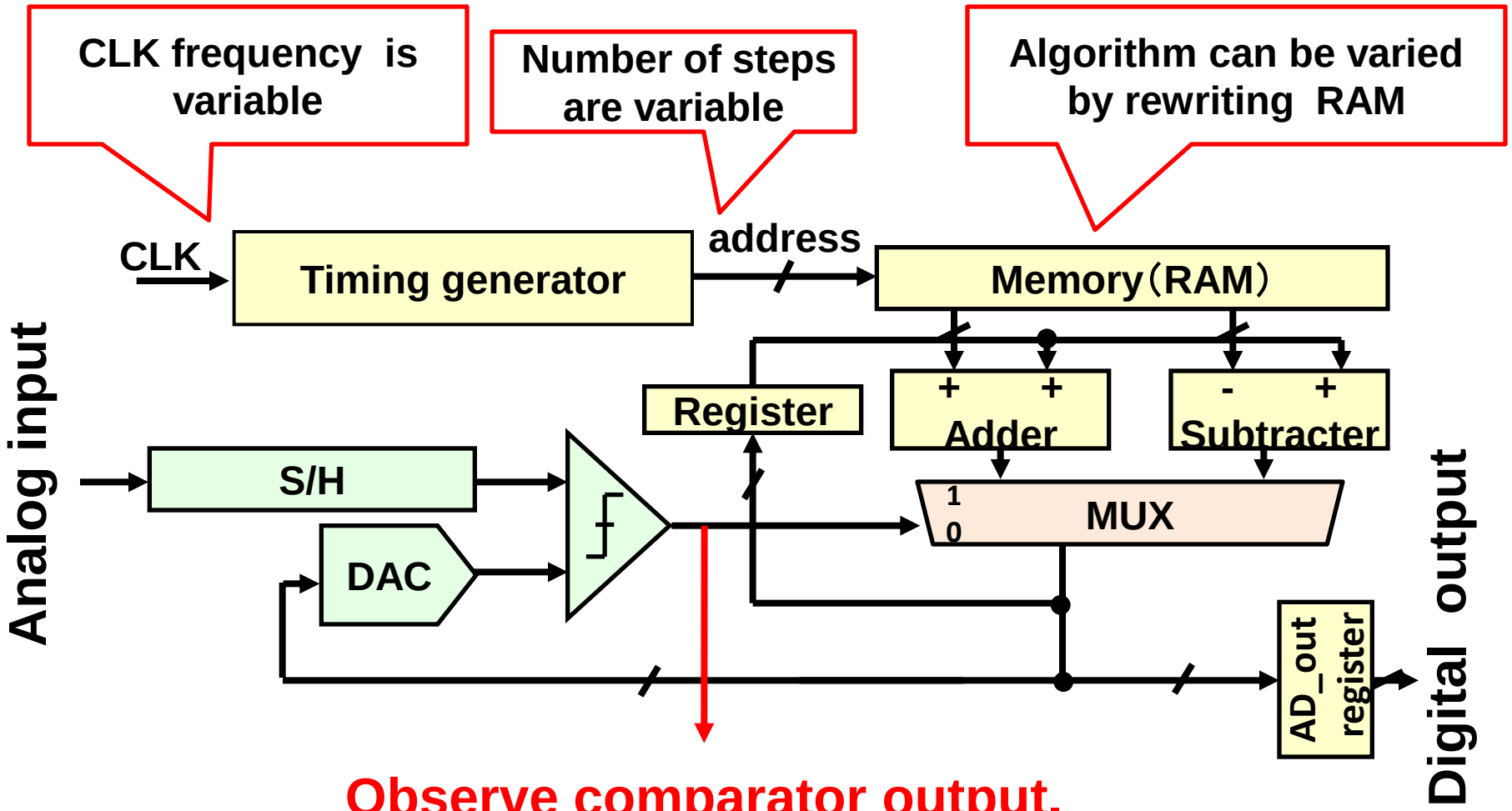
Step	P(k)
1	512
2	256
3	102
4	61
5	37
6	22
7	13
8	8
9	5
10	3
11	2
12	1
13	1

Even slow chips can meet the spec. (10MS/s) with additional power requirement.

Outline

- Research purpose
- Background
- **Configurable non-binary algorithm SAR ADC**
- Production-time configuration SAR ADC
- Test chip design & measurement Results
- Conclusion

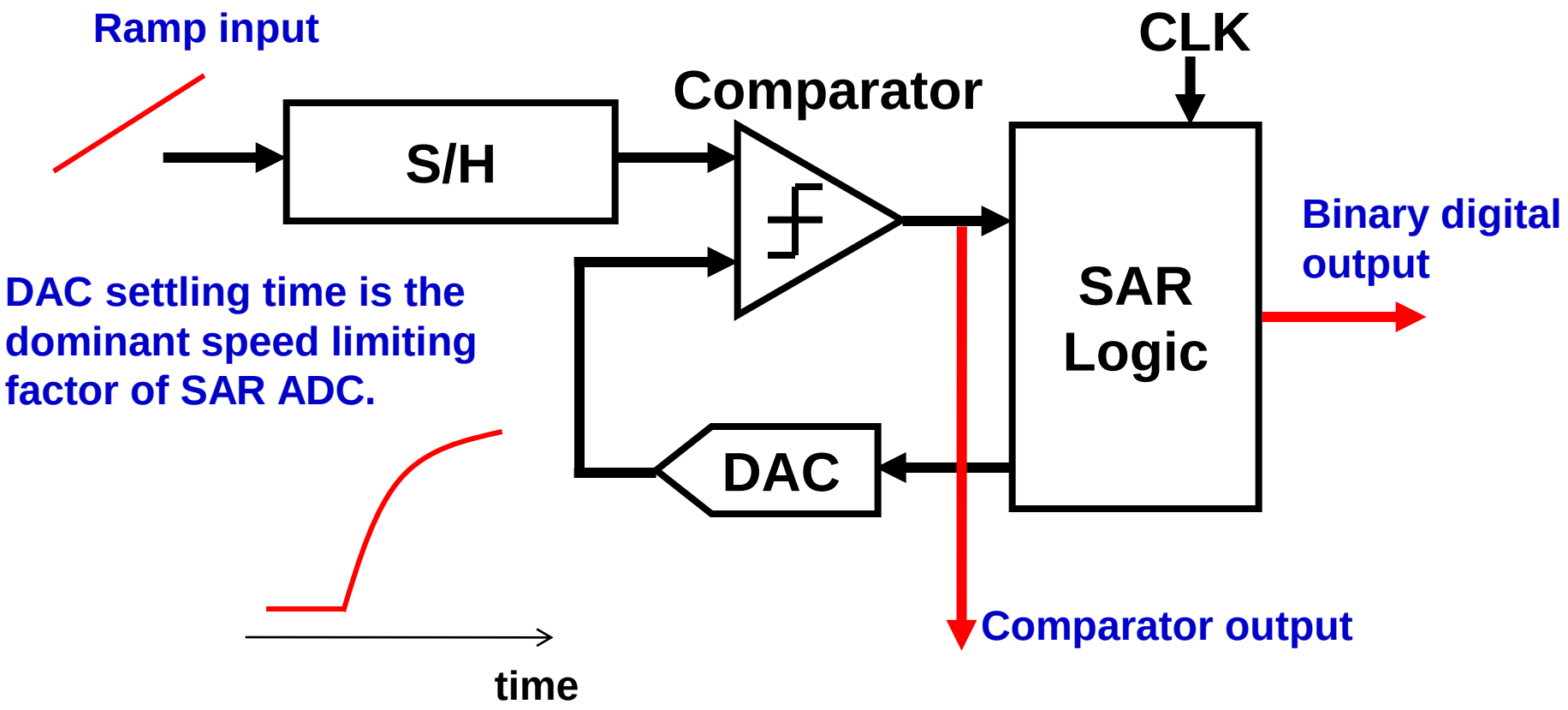
Configurable non-binary SAR ADC diagram



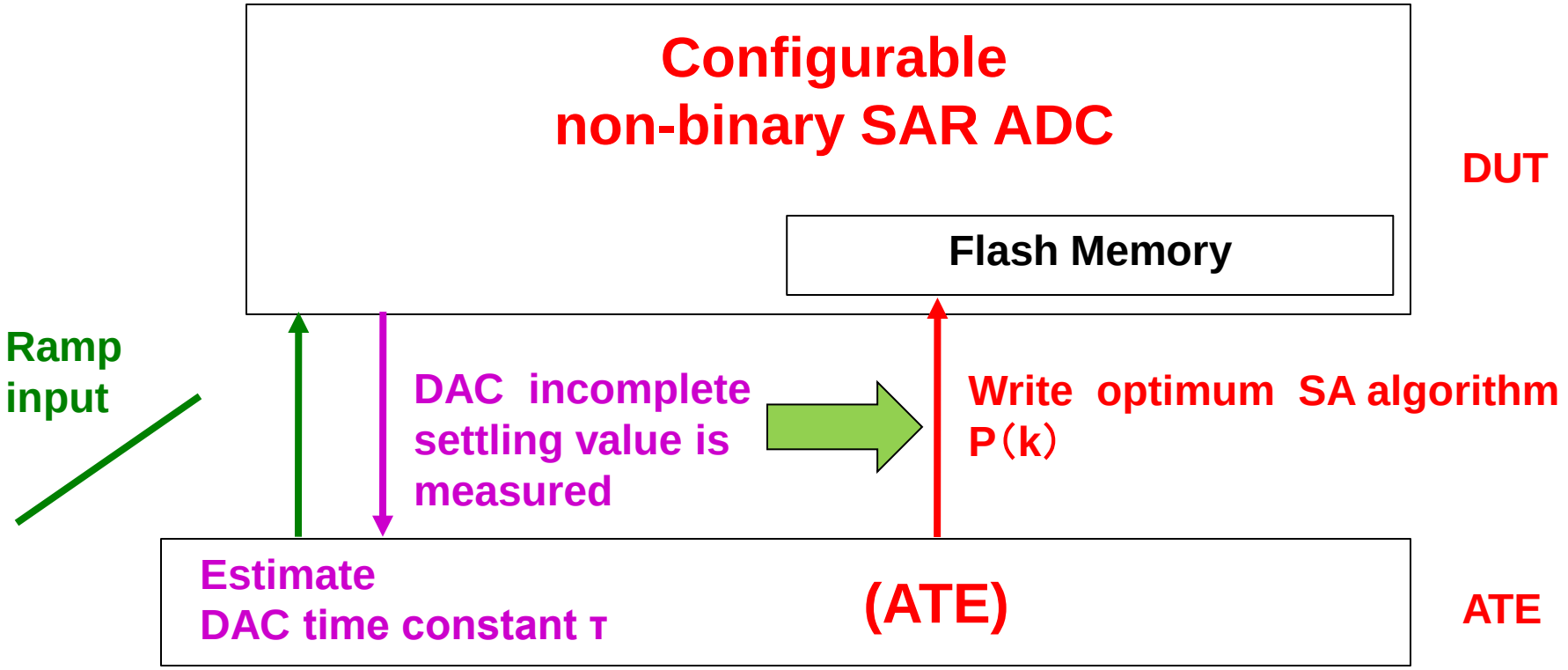
Outline

- Research purpose
- Background
- Configurable non-binary algorithm SAR ADC
- **Production-time configuration SAR ADC**
- Test chip design & measurement Results
- Conclusion

Test of the reconfigurable non-binary SAR ADC



Cooperation with ATE



τ is large ⇒ Satisfy speed spec. with large steps

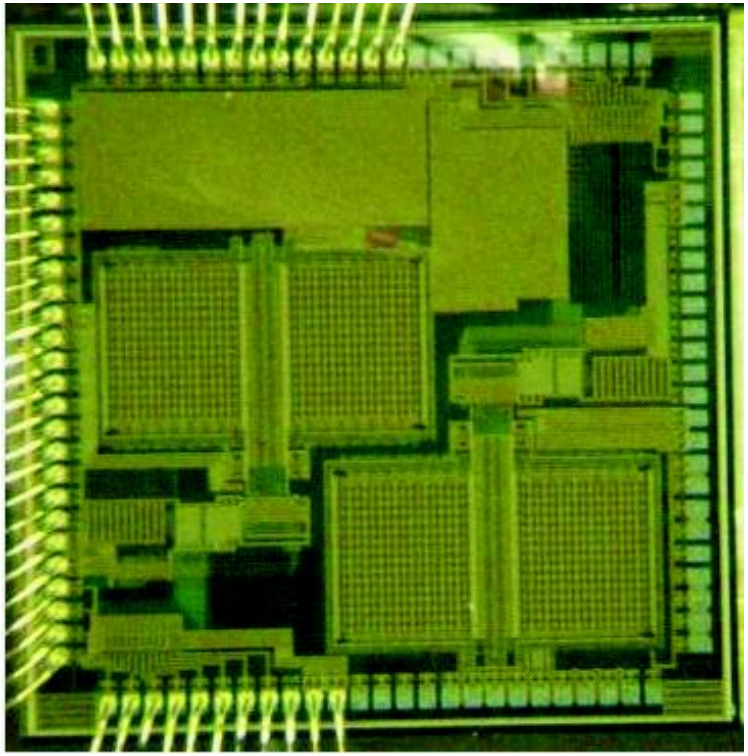
τ is small ⇒ Decrease power with small steps

※ATE: Automatic Test Equipment

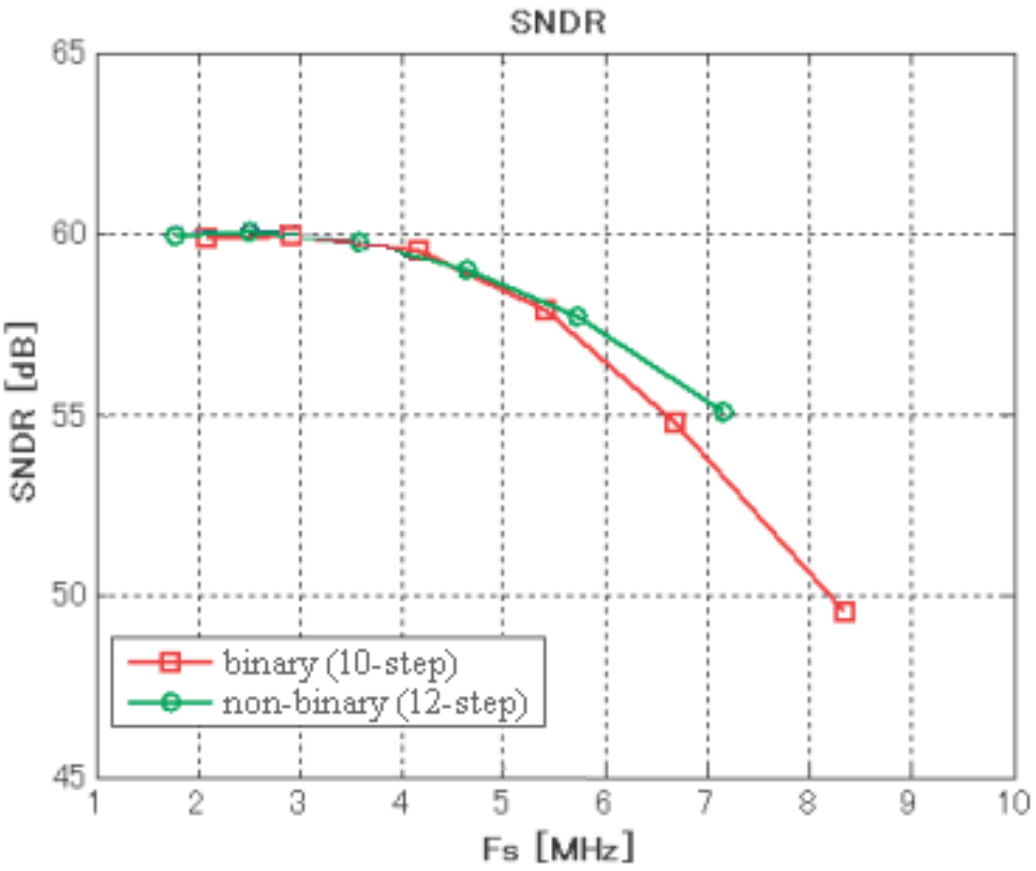
Outline

- Research purpose
- Background
- Configurable non-binary algorithm SAR ADC
- Production-time configuration SAR ADC
- **Test chip design & measurement Results**
- Conclusion

Reconfigurable Non-Binary SAR ADC Implementation and Measurement Results



0.18um CMOS
2.5mm x 2.5mm
with two SAR ADCs



SNDR comparison of
10step (binary) and 12step (non-binary)
F_{in}:100kHz

Verification with prototype chip

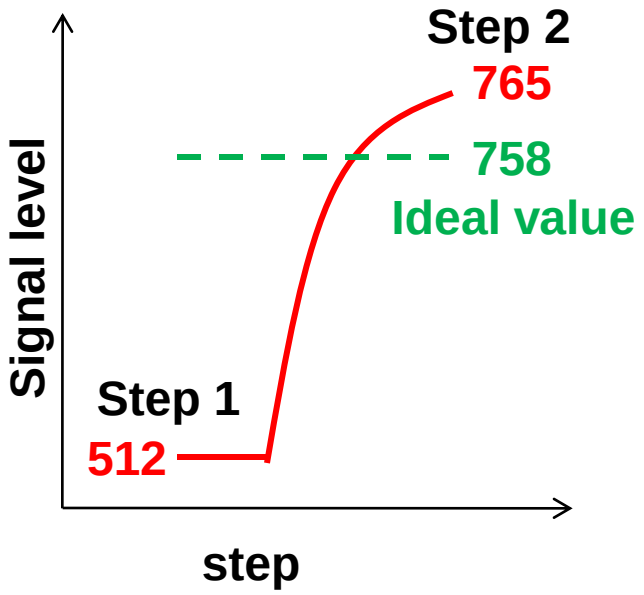
- **DAC settling value estimation by prototype**
  - **DAC output ringing case（ADC_A）**
  - **DAC output no-ringing case（ADC_B）**

→ Verify difference of settling values

※ADC_A：without bias capacitance

DAC settling estimation in ringing case

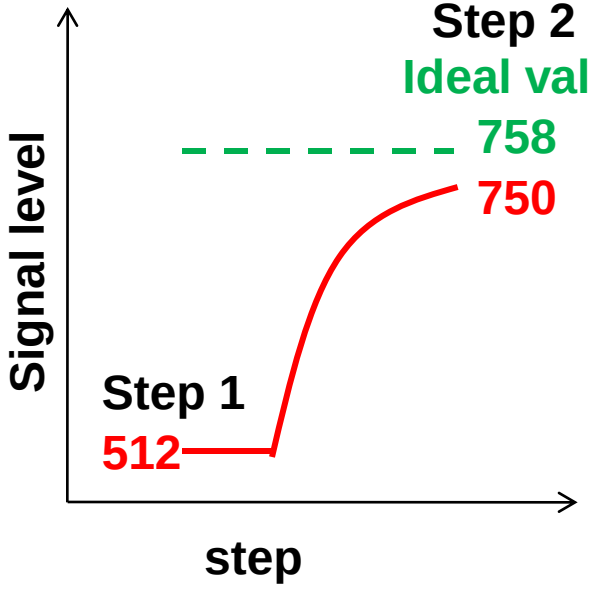
DAC settling value overshoots.



step1	step2	step3	step4	Comparator opinion
Ideal:512	Ideal:758 Estimate:765	Ideal:871 Estimate:876	Ideal:936 Estimate:939	1111
			Ideal:806 Estimate:809	1110
		Ideal:645 Estimate:647	Ideal:710 Estimate:712	1101
			Ideal:580 Estimate:580	1100
	Ideal:266 Estimate:258	Ideal:379 Estimate:377	Ideal:444 Estimate:443	1011
			Ideal:314 Estimate:311	1010
		Ideal:153 Estimate:146	Ideal:218 Estimate:214	1001
			Ideal:88 Estimate:84	1000

DAC settling estimation in no-ringing case

DAC settling is incomplete.



step1	step2	step3	step4	Comparator opinion
Ideal:512 Estimate:511	Ideal:758 Estimate:750	Ideal:871 Estimate:864	Ideal:936 Estimate:931	1111
			Ideal:806 Estimate:802	1110
		Ideal:645 Estimate:642	Ideal:710 Estimate:707	1101
			Ideal:580 Estimate:579	1100
	Ideal:266 Estimate:273	Ideal:379 Estimate:381	Ideal:444 Estimate:444	1011
			Ideal:314 Estimate:315	1010
		Ideal:153 Estimate:160	Ideal:218 Estimate:221	1001
			Ideal:88 Estimate:92	1000

Outline

- Research purpose
- Background
  - Successive approximation algorithm
  - DAC incomplete settling
  - SA algorithm selection
- Configurable non-binary algorithm SAR ADC
- Production-time configuration SAR ADC
- Test chip design & measurement Results
- **Conclusion**

Conclusion

- **Propose a configurable non-binary SAR ADC.**
  - Optimal yield

- **DAC output settling margin is estimated by checking comparator output at each step and ADC output at final step.**

- **Measurement and simulation results validate the effectiveness of our proposed SAR ADC.**