APCCAS

Session : Accord Network Room
Test Technology Ⅰ

ID : 1569327697

ADC Linearity Test Signal Generation Algorithm

S. Uemori, T. J. Yamaguchi, S. Ito,
Y. Tan, H. Kobayashi, N. Takai
Gunma University, Japan

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OUTLINE

- **Research purpose**
- **Conventional linearity testing**
- **Proposed test signal generation method**
- **Implementation method**
- **Conclusion**

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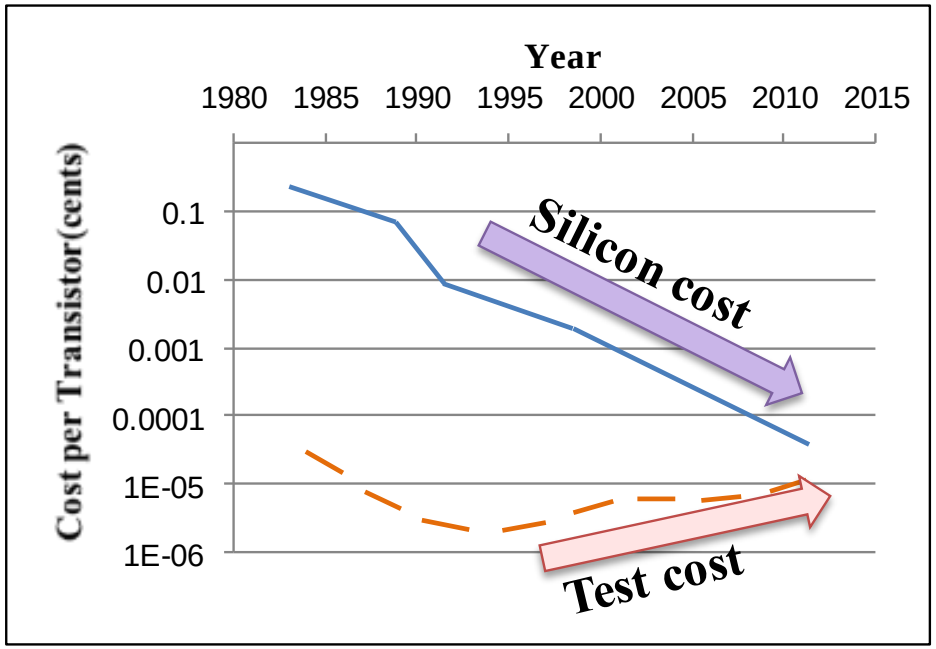
LSI Production Testing



- Test cost is proportional to testing time
- Important factors
  - Reducing testing cost
  - Improving testing quality

Agenda & Approach

- In mixed-signal SoCs, ADCs/DACs
  - DC linearity testing
    - Important
    - Long testing time 
- Requirements for DC linearity testing of ADCs
  - Short testing time
  - Good testing quality

This Work

- Propose "short-time" ADC Linearity Test Signal Generation Algorithm 

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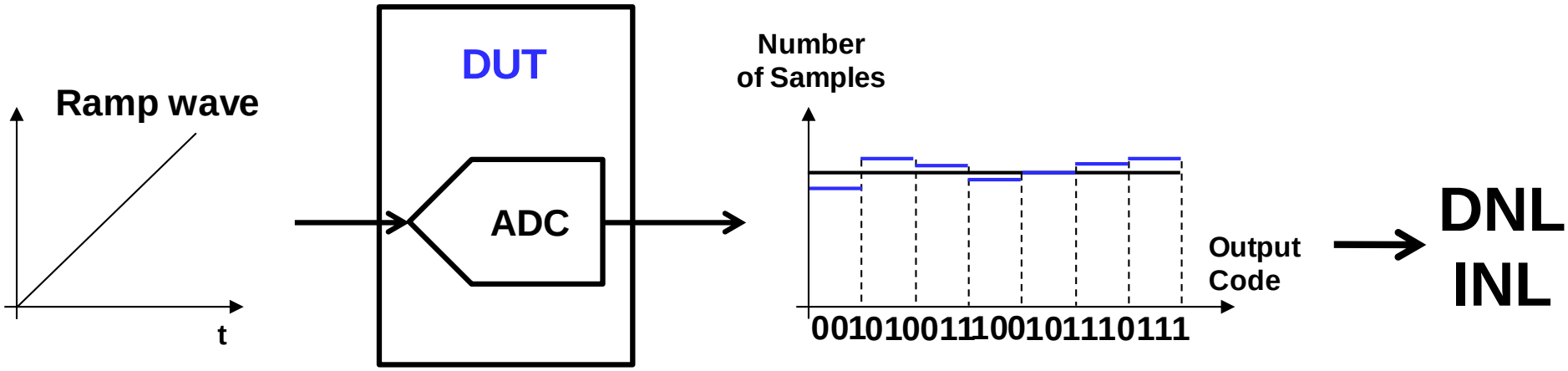
Conventional Linearity Testing 1

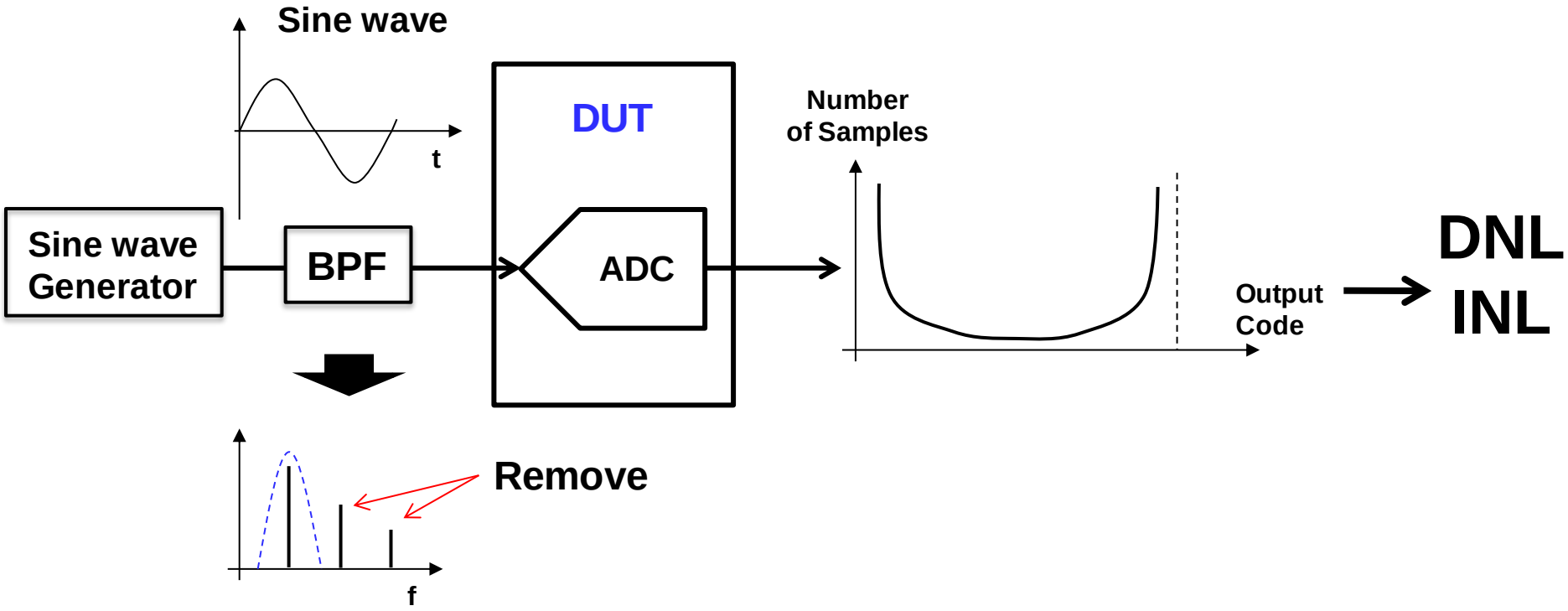
Histogram method (Ramp wave input)



- ADC output histograms for all bins are equal if ADC is perfectly linear
- Highly linear ramp signal generation is difficult 😖

Conventional Linearity Testing 2

Histogram method(Single sine wave input)



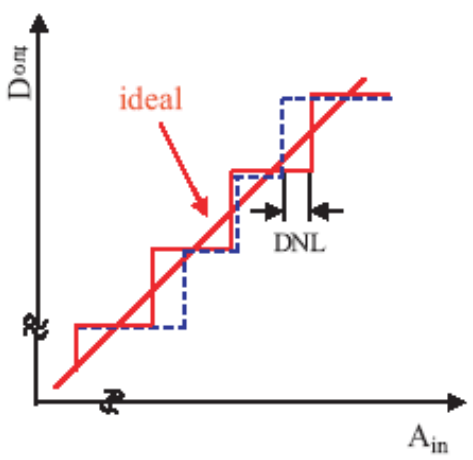
- The number of samples is small around the middle of output codes
- High accuracy sine wave can be generated using an analog filter

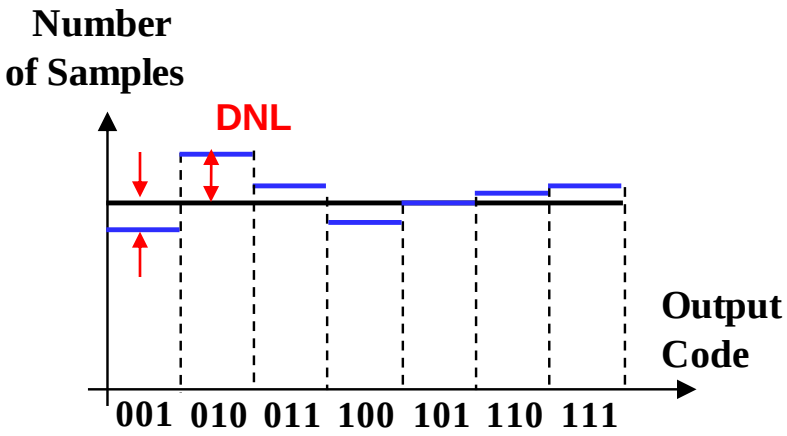
Target of This Research

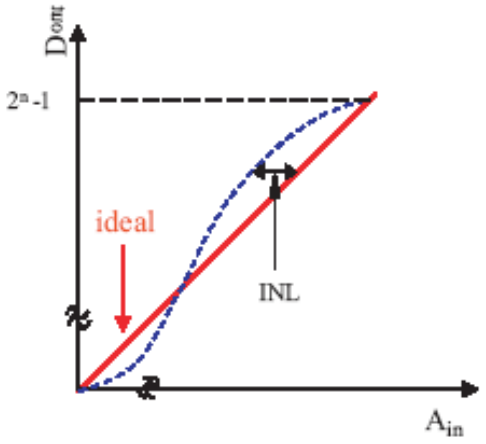
	Ramp Wave	Sine Wave	Proposed
Bin	 **All bins are equal**	 **Few samples around the center**	 **Middle range increases**
Signal Generation	 **Difficult**	 **Easy**	 **Easy**

 **Very Fine**  **Fine**  **Bad**

DNL & INL







- **Important testing for ADCs**

DNL : Difference between an actual step width and the ideal value

INL : Deviation from ideal conversion line

$$INL(k) = \sum_{i=1}^{k} DNL(i)$$

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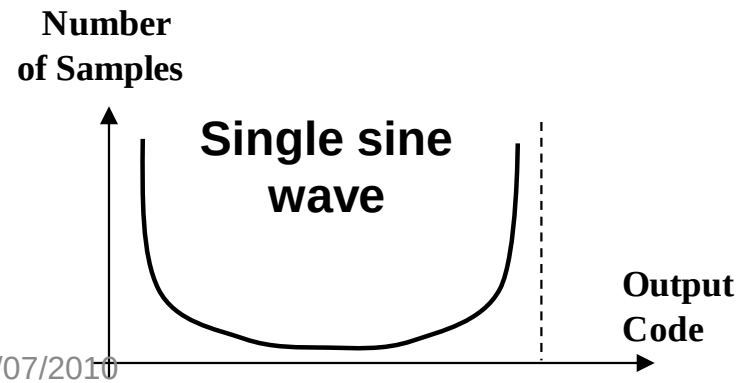
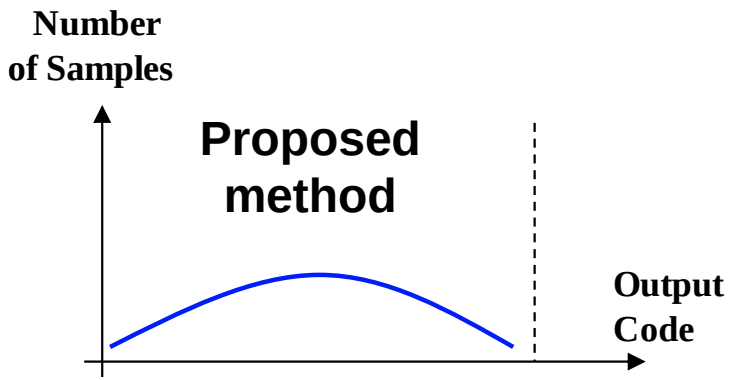
Linearity Testing of ADCs in SoCs

- In mixed-signal SoCs, …
  - Accurate ADC linearity evaluation "around the middle of its input range" is required
  - Single sine wave is unsuitable

This Work

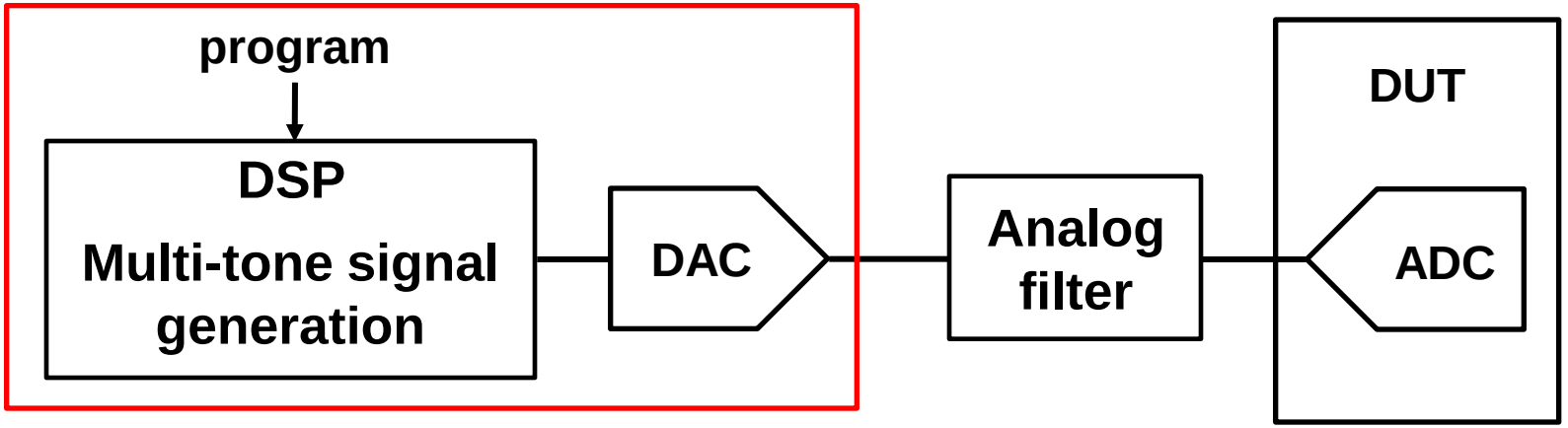
- **Middle range** of histogram increases





Architecture for Generating Proposed Test Signal

AWG : Arbitrary Waveform Generator



- DSP program : Multi-tone sine wave
- Analog filter : Harmonics removal

As a result …

- Histogram for the middle of ADC input range can be high ☺

Role of Analog Filter

- **Resolution of an ADC under test is 14 bits**
- **Linearity of AWG is less than 12 bits**
  → Not suitable if directly applied 😖
- **The analog filter can remove spurious components** ☺
  - **This method has compatibility with "moderate-performance" AWG** ☺

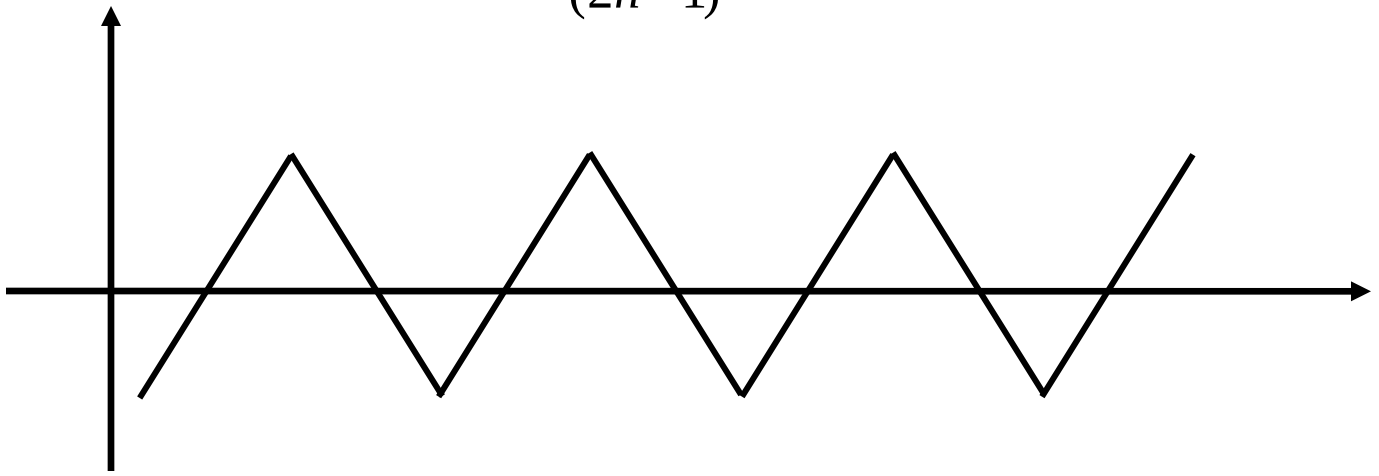
Proposed Test Signal Generation Method

- **Approximate triangle wave by multi-tone sine waves**

$$V_{in} = \frac{4}{\pi} \sum_{n=1}^{\infty} A_n \, V_n$$

$$V_n = \frac{\cos(2\pi \cdot (2n-1) \cdot f \cdot t)}{(2n-1)^2}$$

n=1,2,・・・

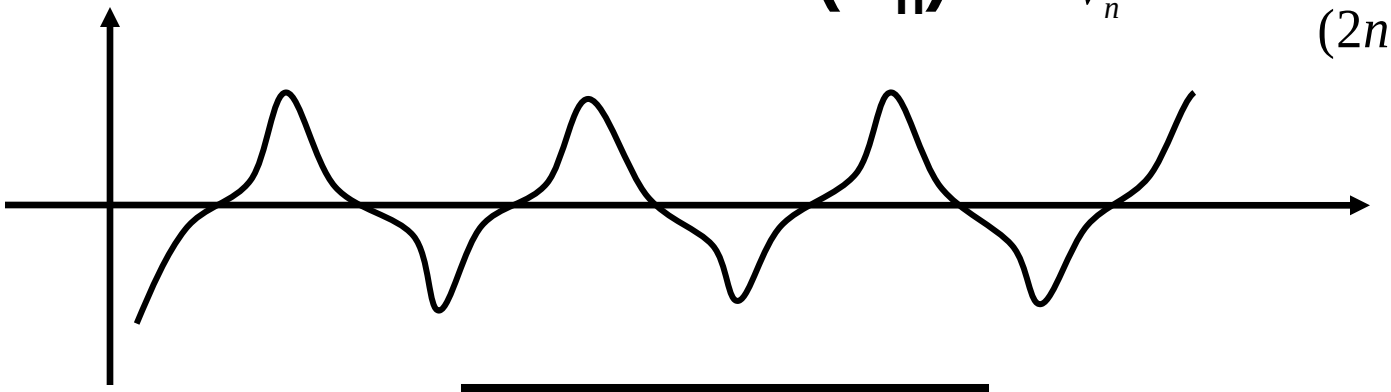


Proposed Test Signal Generation Method

- **Select terms (V_n)**
- **Decide their coefficients (A_n)**

$$V_{in} = \frac{4}{\pi} \sum_{n=1}^{\infty} A_n \, V_n$$

$$V_n = \frac{\cos(2\pi \cdot (2n-1) \cdot f \cdot t)}{(2n-1)^2}$$



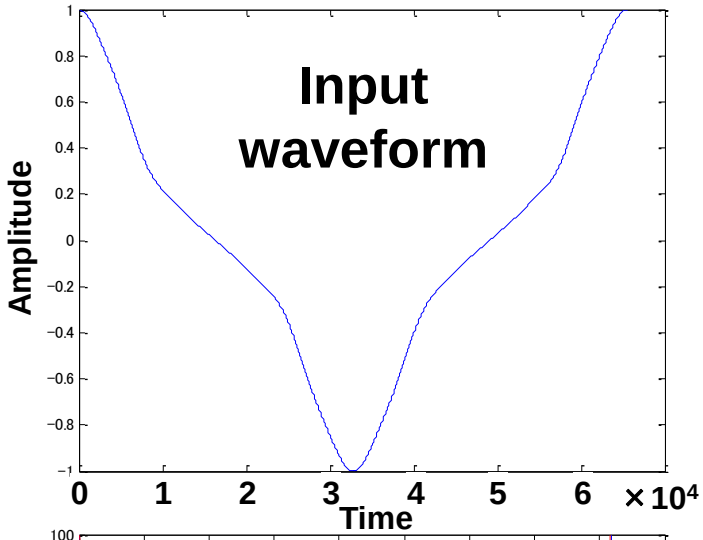
As a result …

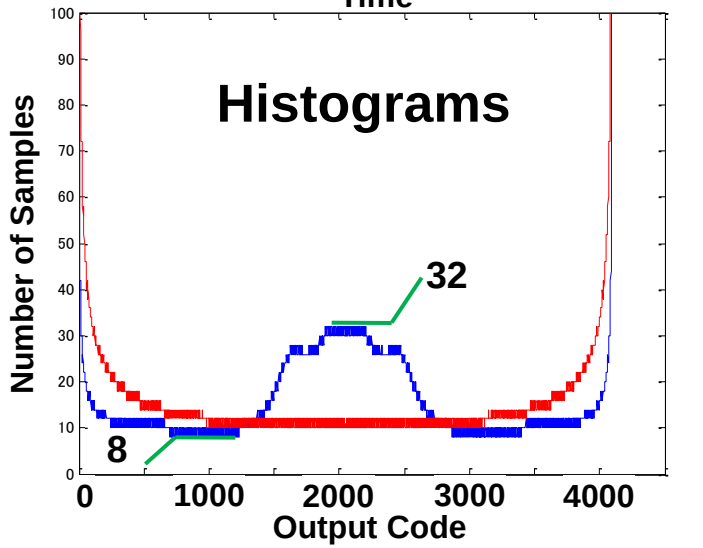
- **Histogram for the middle**

  of ADC input range increases

  - **Reducing test time**
  - **Maintaining the required testing quality**

Simulation Result of Proposed Method





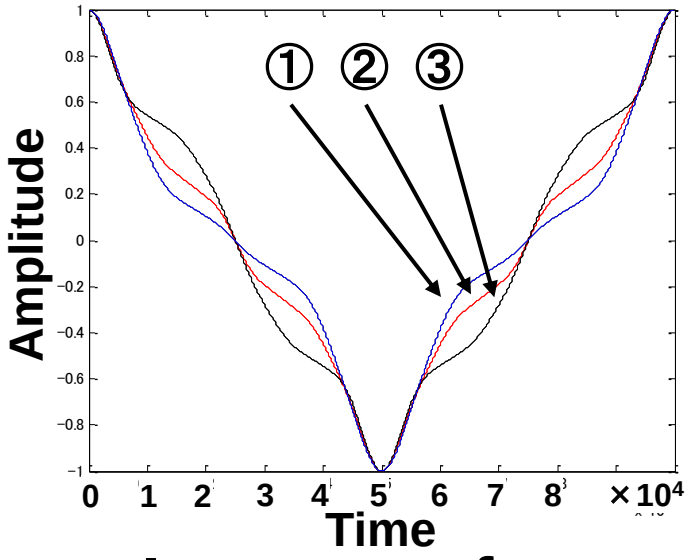
$$V_n = \frac{\cos\left((2n-1)\omega t\right)}{(2n-1)^2} \qquad \text{n=1,2,···}$$

$$V_{in} = \frac{4}{\pi}\left(V_1 + 2.6 \cdot V_2 + 1.8 \cdot V_3 + 1.4 \cdot V_6 + 1.2 \cdot V_7\right)$$

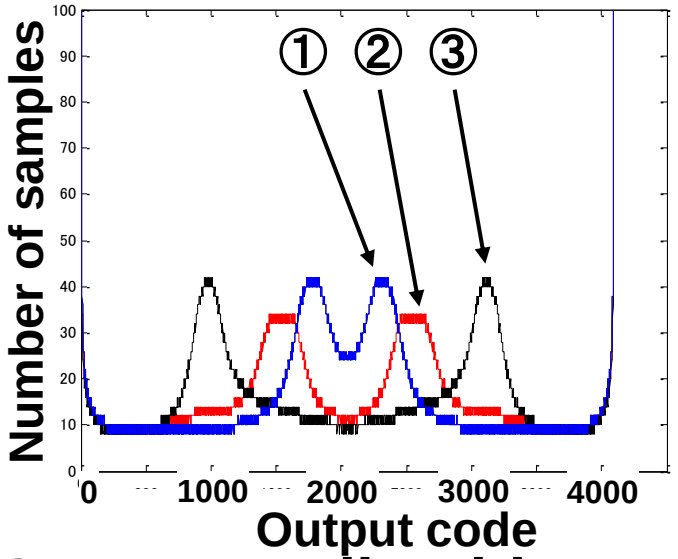
- Histogram for the middle of ADC input range increases

Simulation Result of Proposed Method

- **Proposed method can be applied to the several cases. (Shape of the histogram can be changed)**



Input waveform



Corresponding histograms

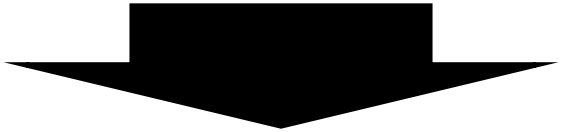
Contents of Testing Time with ATE

Table: ADC testing time with ATE

	Content	Time
1)	Setup time for module	Less than 1 msec
2)	Settling time for module and DUT	Several msec
3)	DC linearity testing time	2^{bit}×(16~64)×(ADC conversion time)
4)	SINAD testing time	2^{bit}×(1~4)×(ADC conversion time)
5)	Time for data transfer and operation	Several msec
6)	Other test time	Several msec

Estimation of ADC Test Time

- **Example : 12 bit 100kS/s SAR ADC**
  - **Setup time for measurement module and settling time for DUT : 10 msec**
  - **DC linearity testing time : $2^{12} \times 40 \times 10u$ sec = 1600 msec**
  - **SINAD testing time : $2^{12} \times 4 \times 10u$ sec = 160 msec**
  - **The time for data transfer and operation : 10 msec**



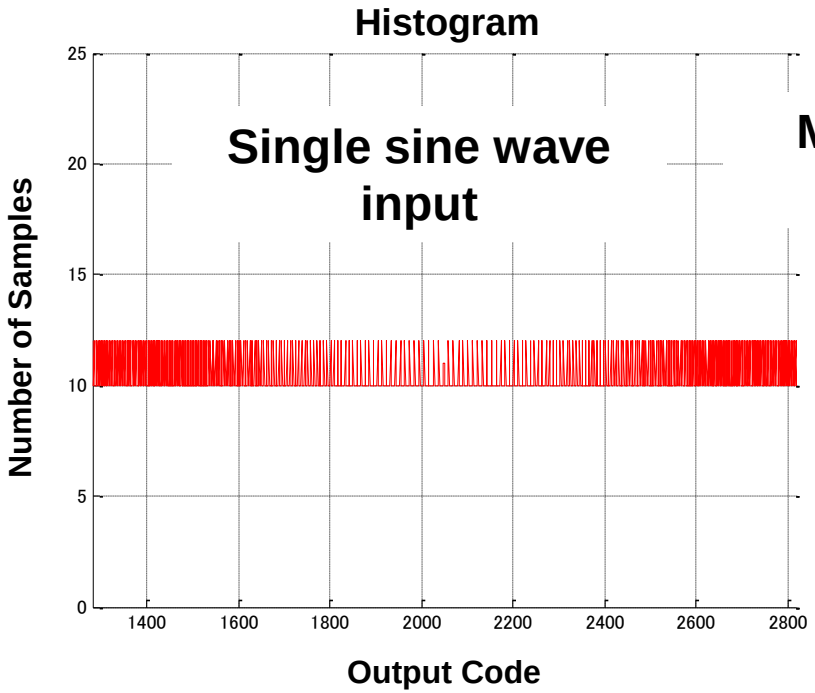
- **Conventional method**
  - **Total testing time = 1780 msec**

Acceptable Test Time

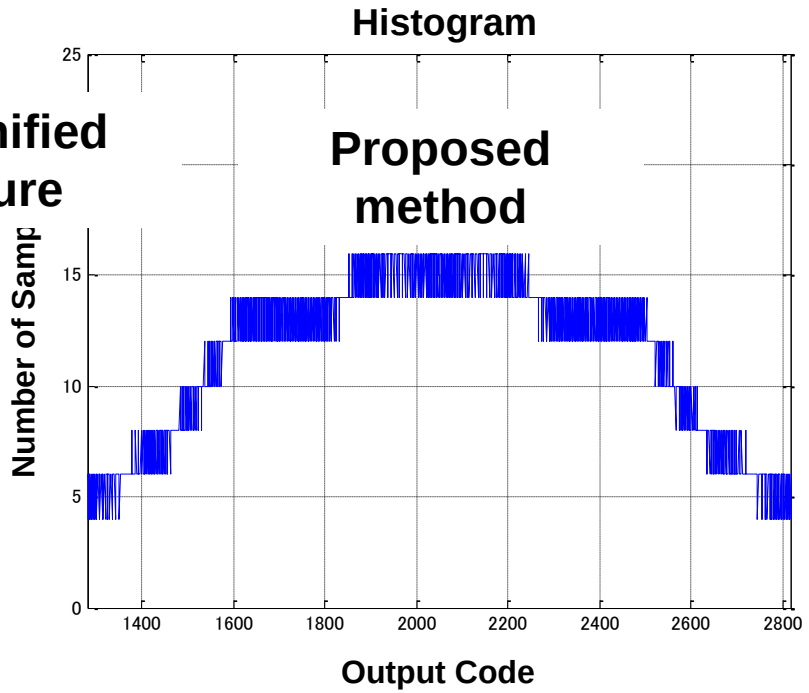
- **Testing time for high resolution, slow sampling rate ADCs**
  - **Very time consuming**
- **Testing time of 1 sec for a $1 chip is acceptable**
  - **Total test time (about 1.8 sec) is too long**
- **Reduce DC linearity test time**

Verification of Effectiveness

[Condition] Sampling points for the middle of ADC input range is more than 10 points, other range is more than 4 points



Magnified figure



Total sampling points : 65536

Total sampling points : 32768

Reduce the # of sampling points to half

- **Meet the bottom sampling points**

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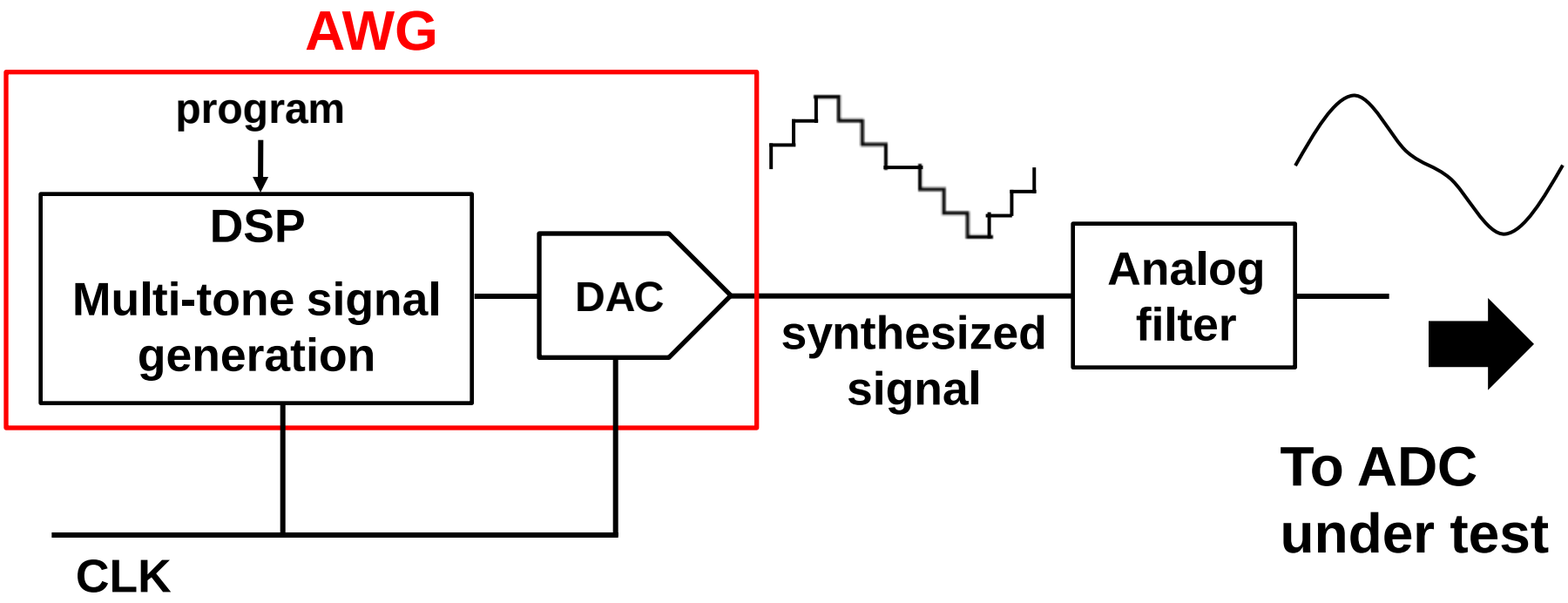
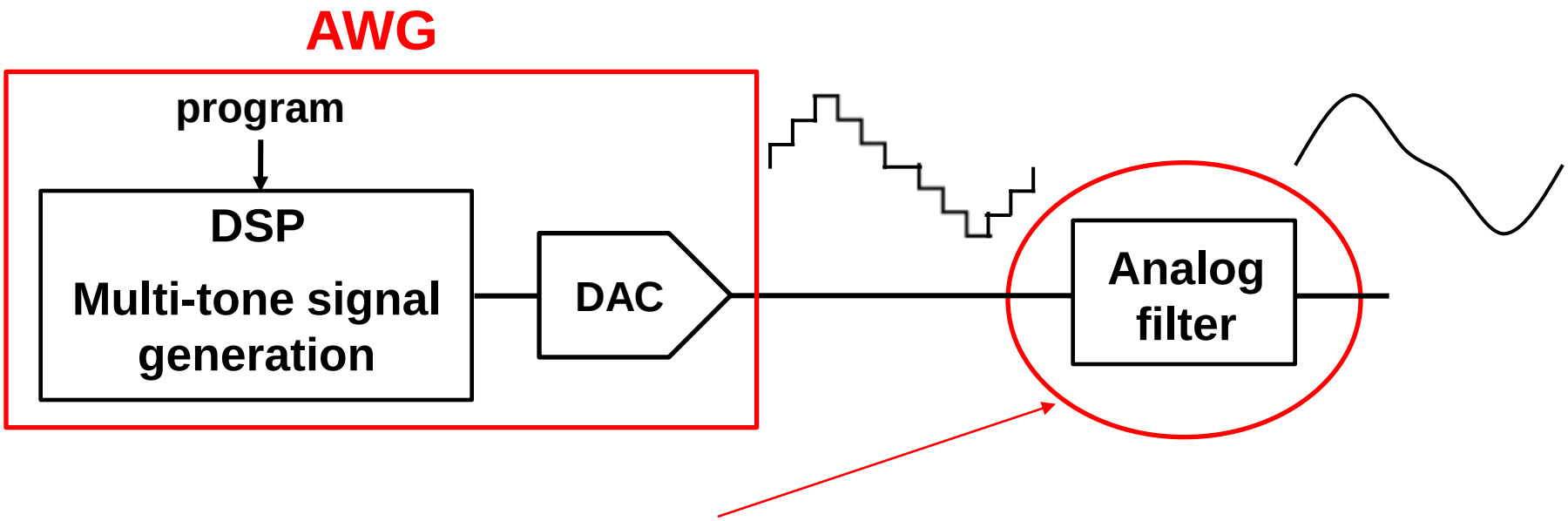
Implementation Method



Settling Time of Analog Filter



- Settling time of analog filter
  - 10X the time constant

    i.e. 10ms for a 1kHz filter
    - Doesn't interfere with the tests

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Conclusion

- **Propose DC linearity testing method for ADC in SoCs**
  - **Using multi-tone sine wave**
  - **Histogram for the middle of ADC input range is high**
- **Testing time for ADC DC linearity by half**
- **Implementation method**
  - **An AWG and an analog filter**