Background Calibration Algorithm for Pipelined ADC with Open-Loop Residue Amplifier Using Split ADC Structure

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Outline

- Research purpose
- Self-calibration of pipelined ADC
  - Nonlinearity calibration
  - Gain error and DAC capacitor mismatch calibration
- Background self-calibration circuit
- Simulation results
- Conclusion

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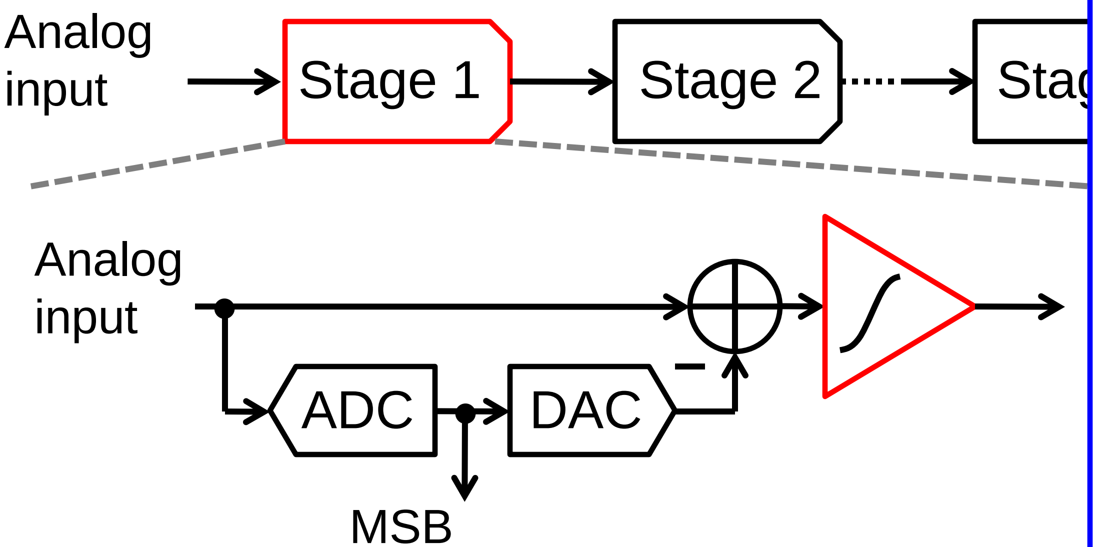
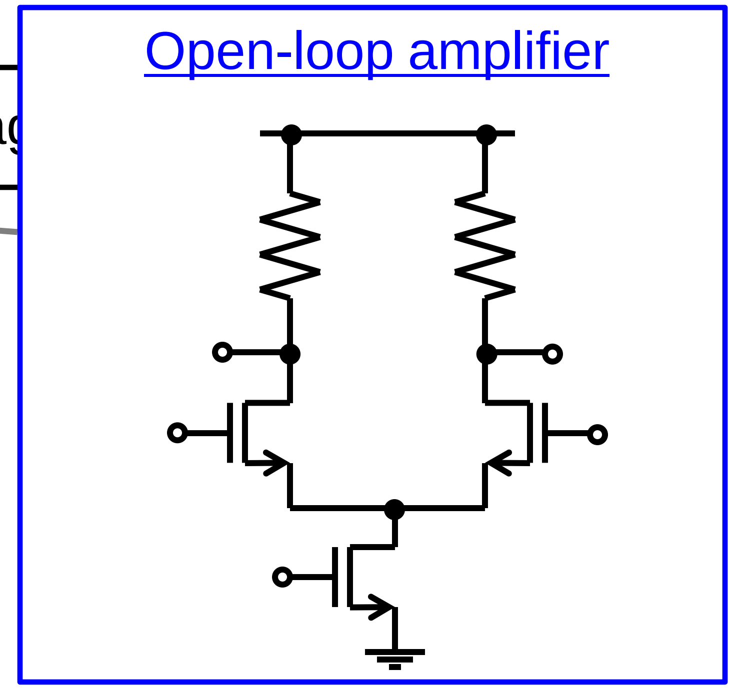
Power Consumption of Pipelined ADC

- First stage amplifier：Consumes considerable power



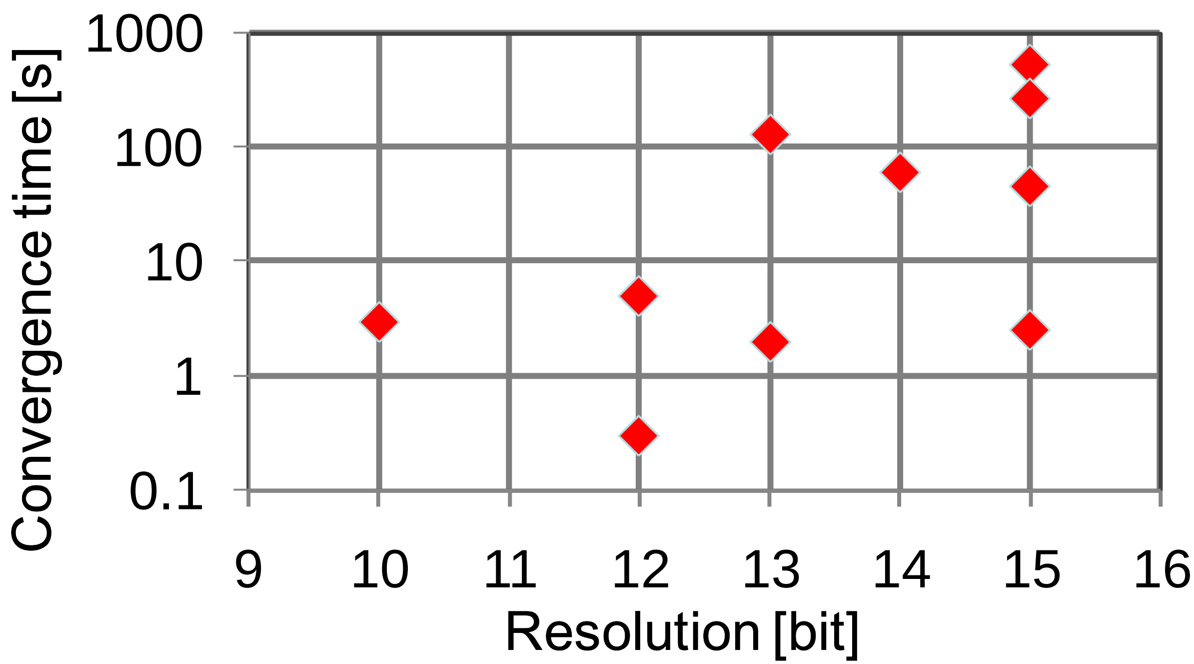


- [B Murmann JSSC 03]
  - First stage amplifier：Open-loop
  - Low power consumption
- Nonlinearity of open-loop amplifier : background self-calibration

Digitally-Assisted Analog Circuit Test

- Background calibration time → Long

[Pipelined ADC with calibration research paper in recent years]



- Total testing time = Background calibration time + Functional testing time
- Long testing time → increase testing cost

Research Purpose

- For low power pipelined ADC
  - An open-loop residue amplifier in the first stage

- For high-speed, high-precision pipelined ADC
  - Split ADC structure
  - Background digital self-calibration ：
    Nonlinearity of first stage amplifier, Gain error, DAC capacitor mismatch calibration

- Demonstrates the effectiveness with MATLAB

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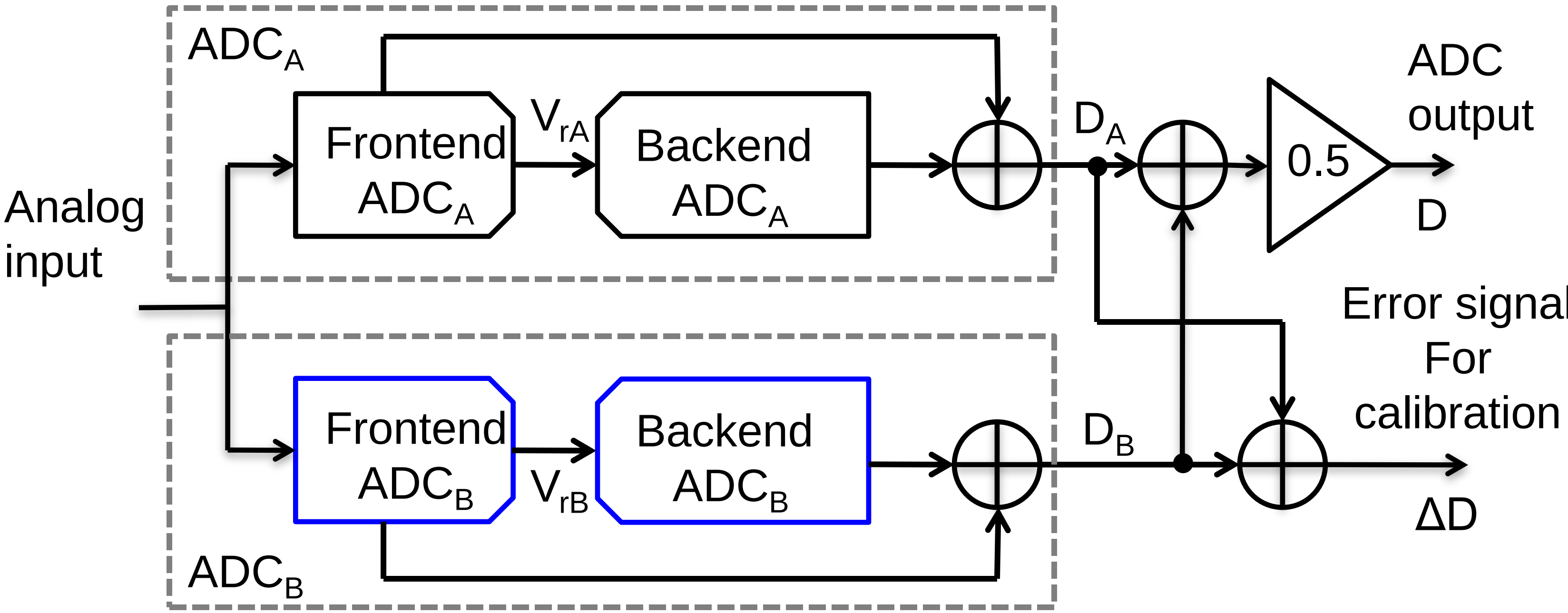
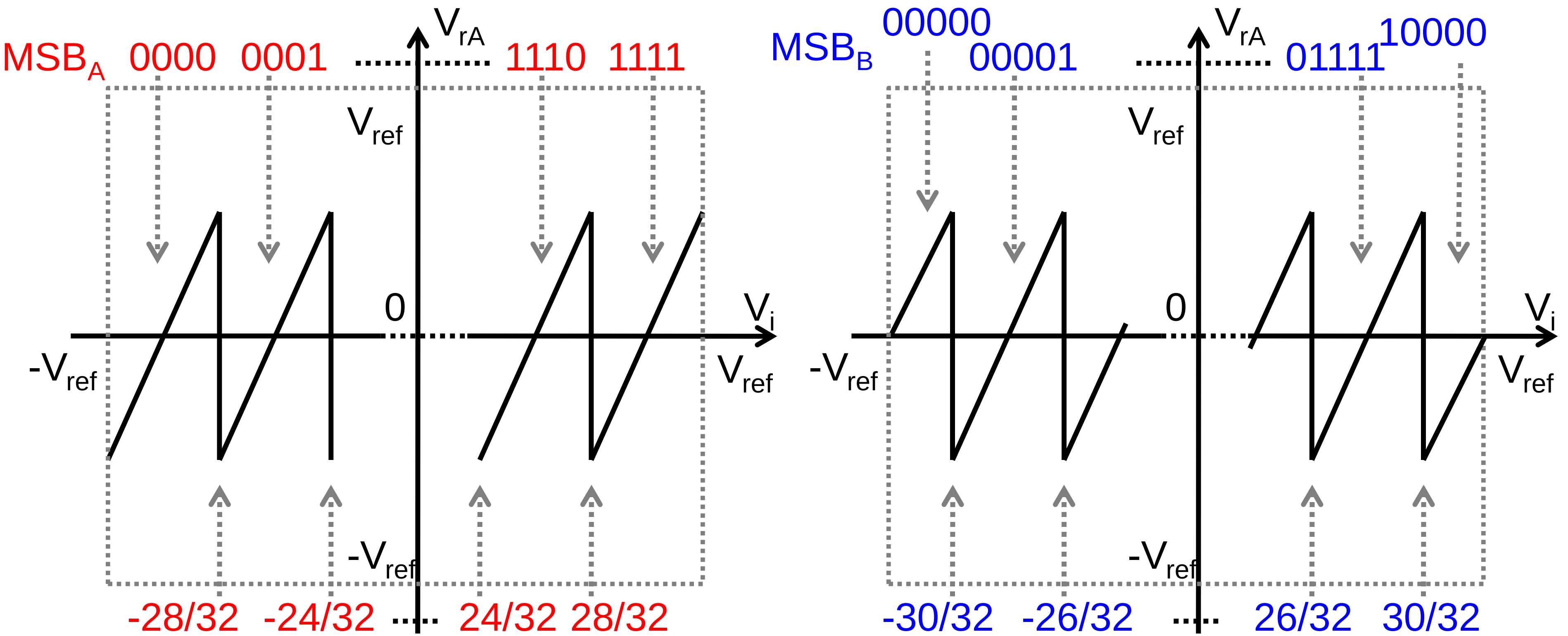
Split ADC Structure



- Converge : quickly
- Power consumption : small overhead
- Chip area : small overhead

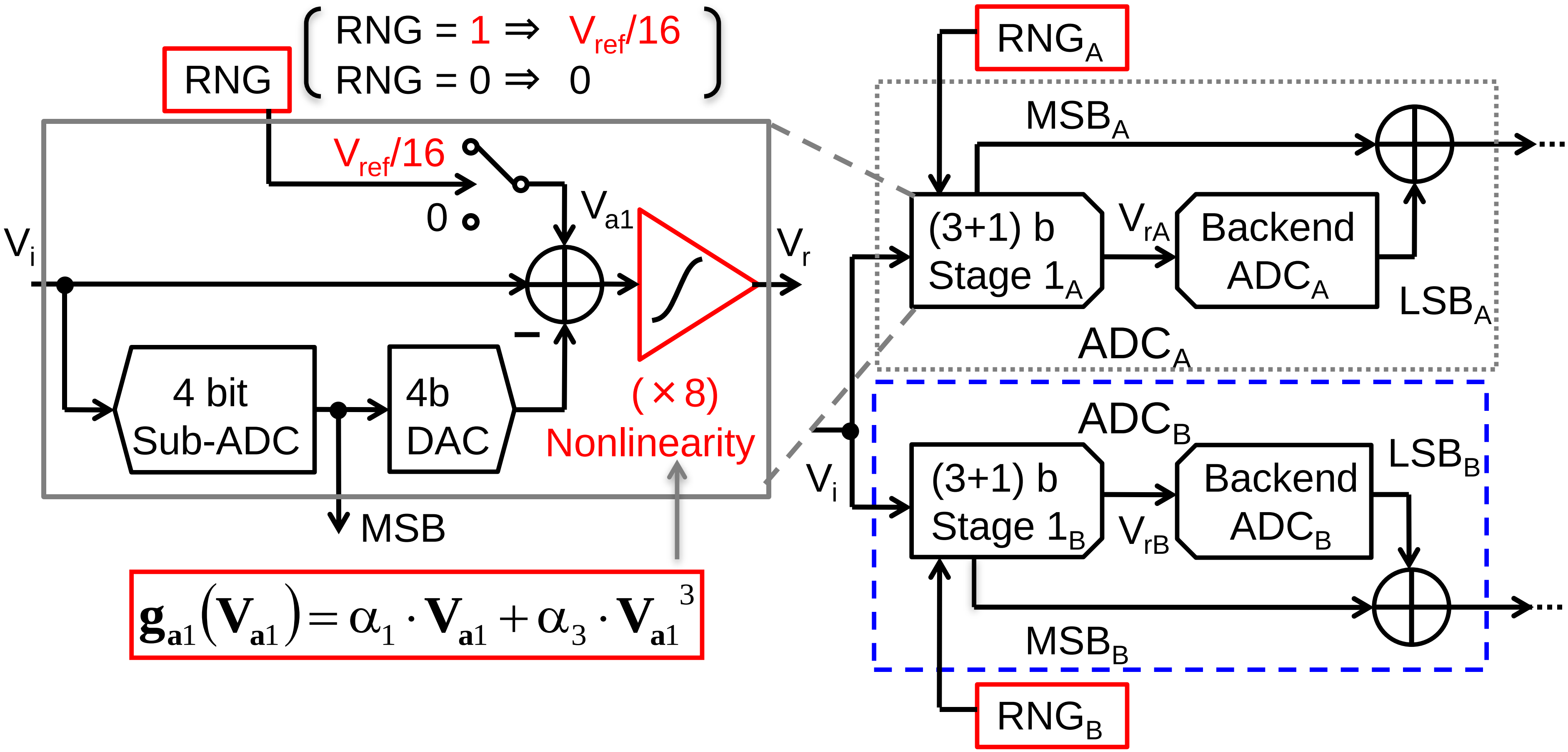
Residue Voltage of the First Stage

- Stage1$_A$
- Stage1$_B$



- Shift residue voltage about ADC$_A$ and ADC$_B$
  - Both ADCs have same error :
    Close to ideal with self-calibration

Nonlinearity Estimation of Open-Loop Amplifier with Pseudo Random Signal



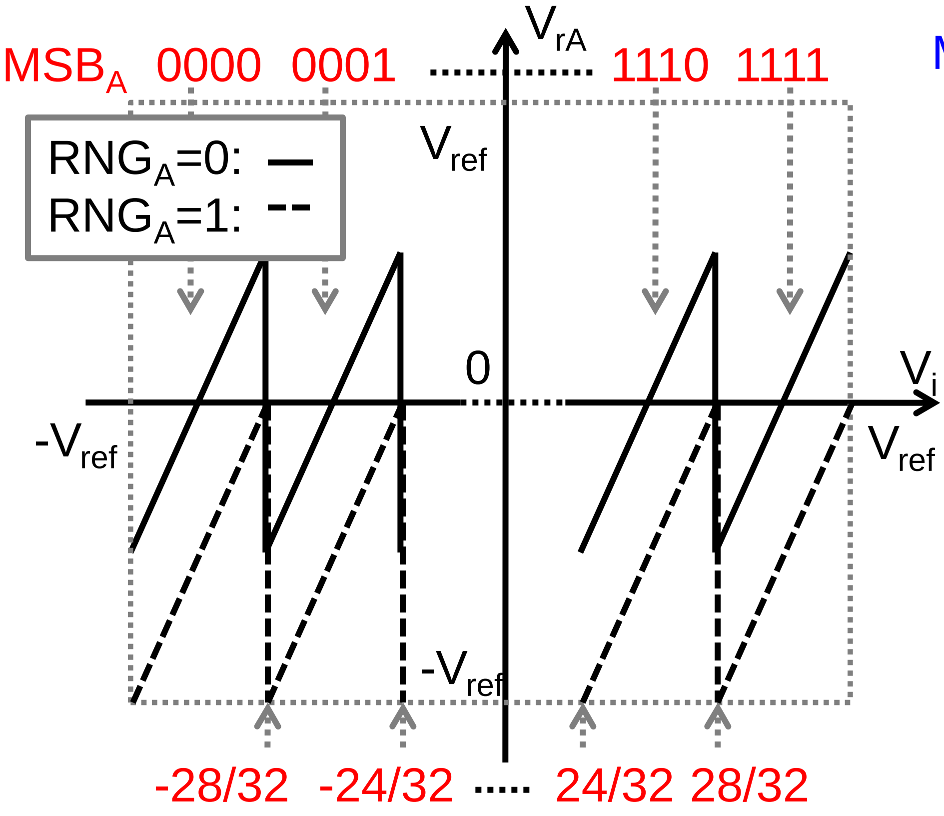
$$g_{a1}(V_{a1}) = \alpha_1 \cdot V_{a1} + \alpha_3 \cdot V_{a1}^{\ 3}$$

- Adding pseudo randomly
  → Generate two residue waveforms
- RNG(A & B) : Set default value to different

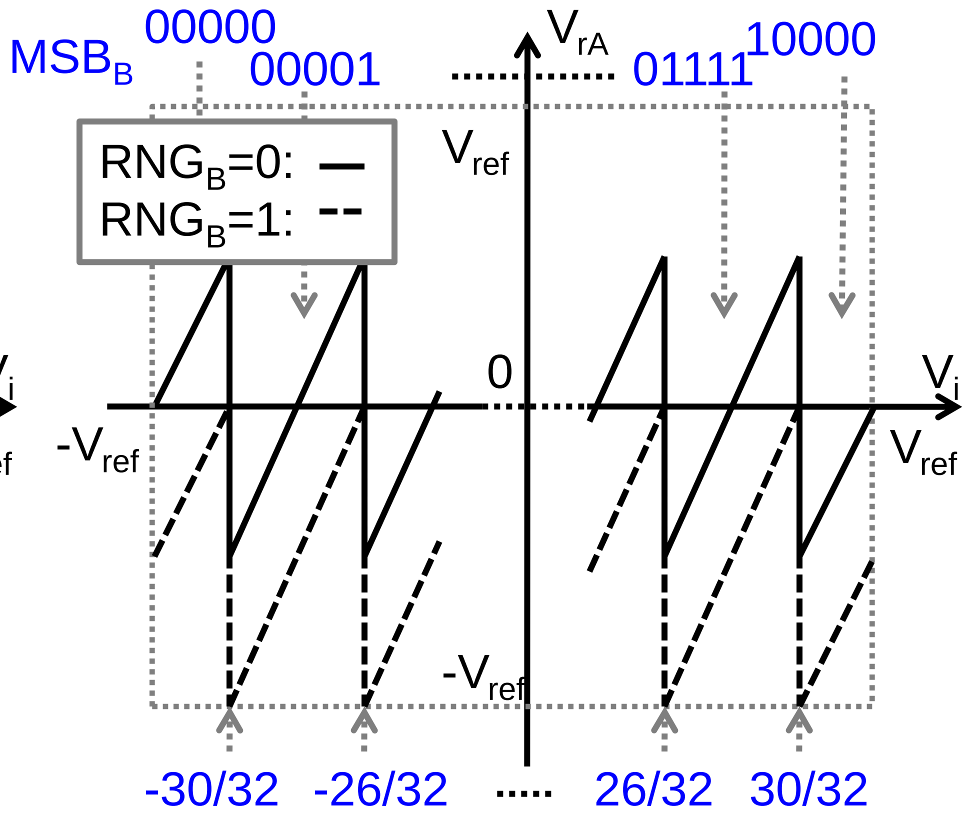
RNG:Random Numbar Generator

Two Residue Waveforms with Pseudo Random Signal

- Stage1$_A$

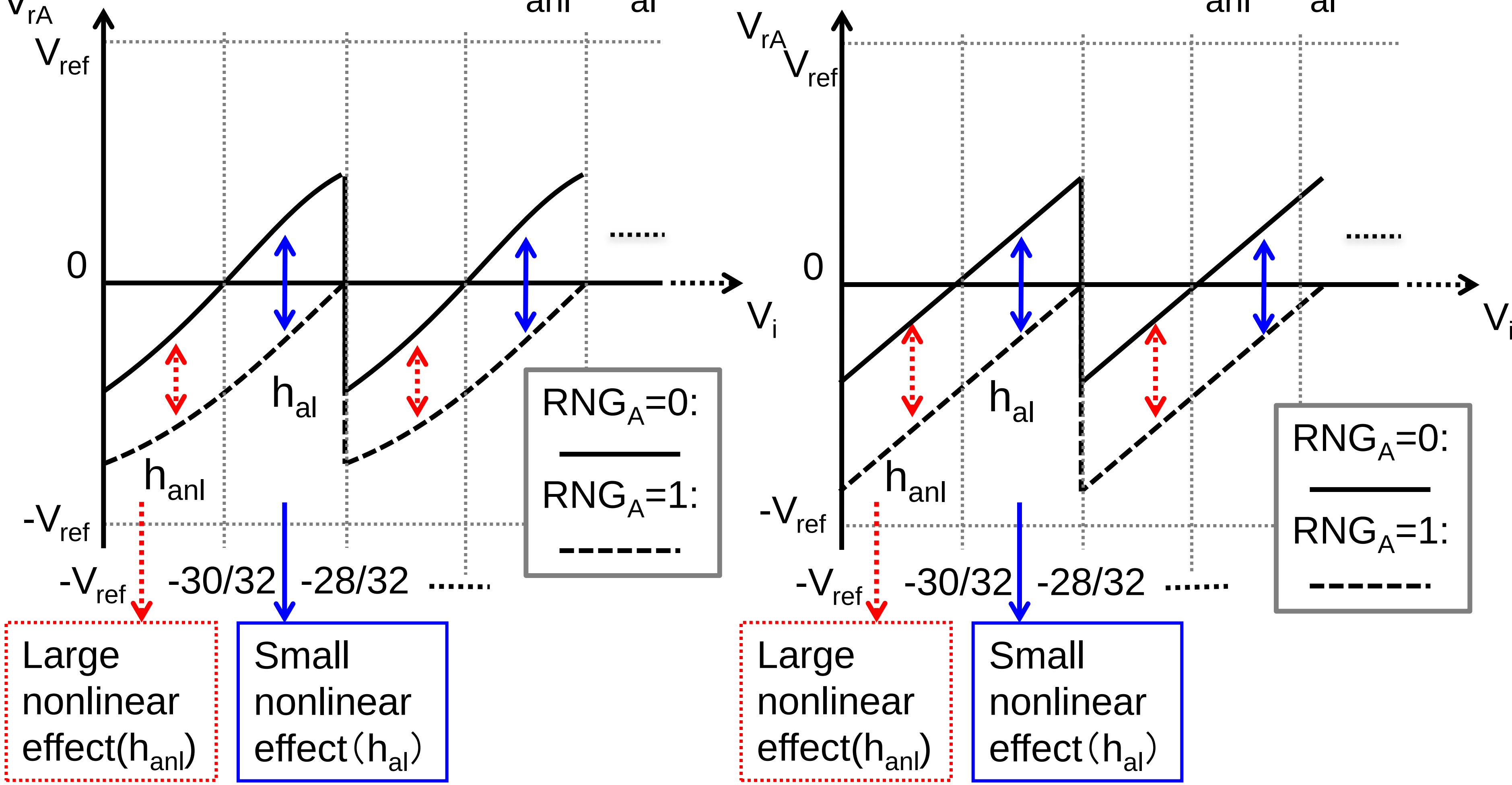


- Stage1$_B$



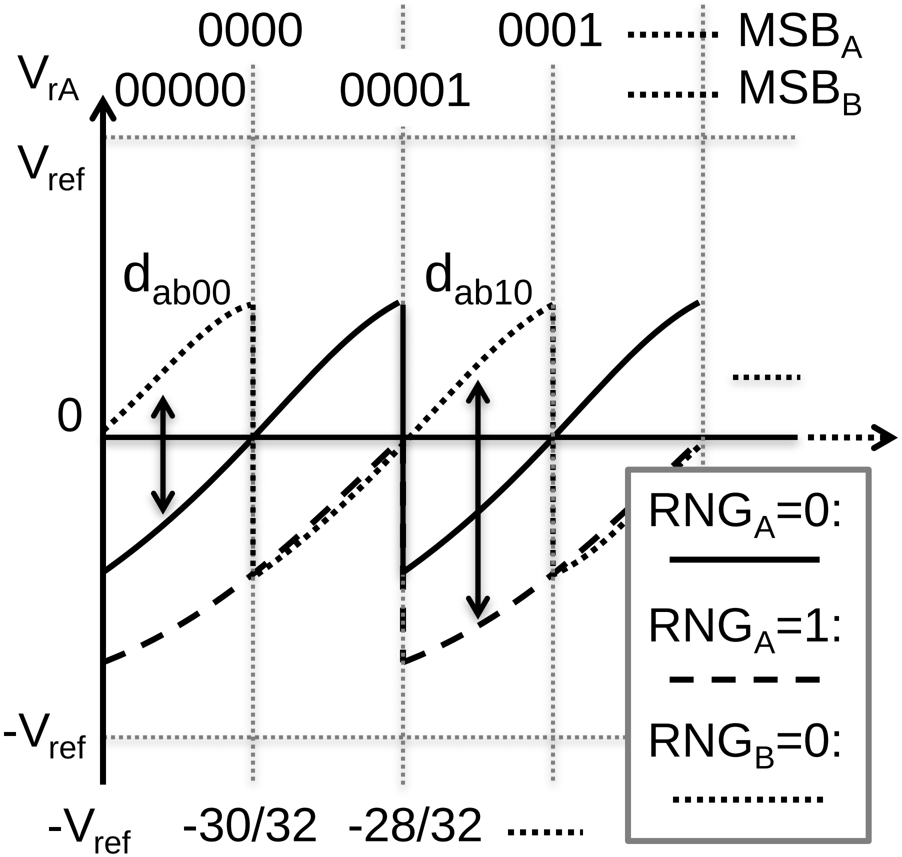
Compensation of Amplifier Nonlinearity

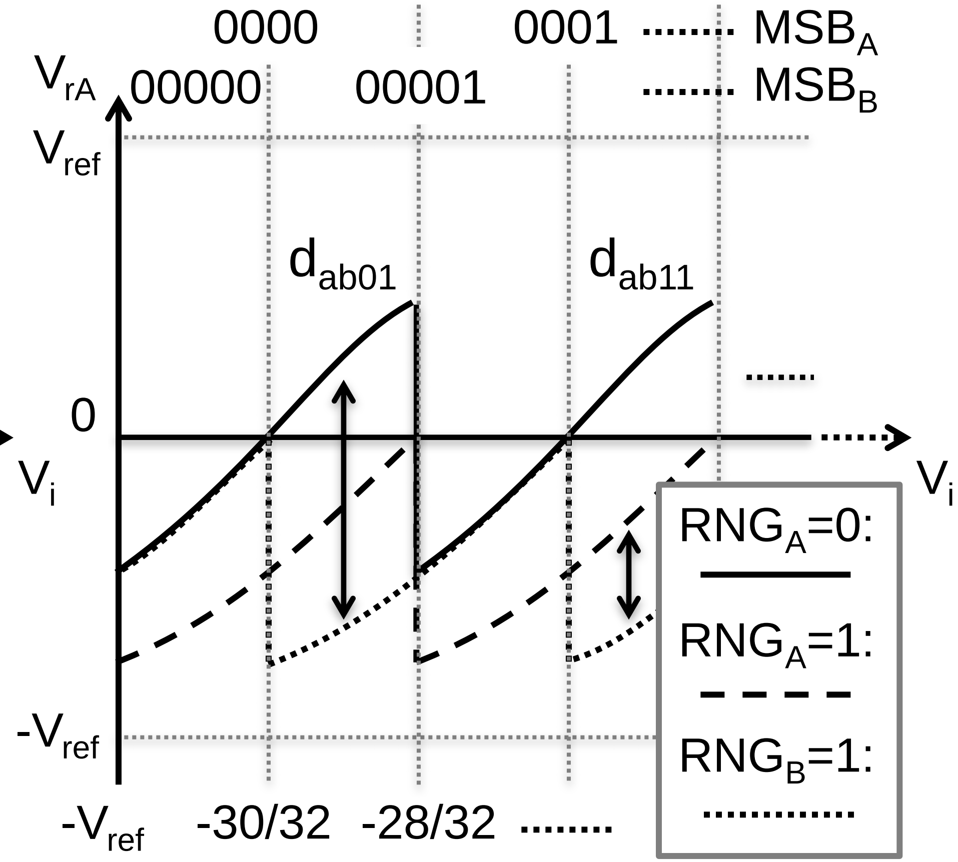
•No calibration : $\overline{h_{anl}} < \overline{h_{al}}$ •Calibration : $\overline{h_{anl}} = \overline{h_{al}}$



•Average distance：Equalize → nonlinearity compensated

Estimation of Distance “h”





- Case of stage1$_A$
  - ✓ $\overline{d_{ab00}} - \overline{d_{ab10}} = \overline{h_a}$
  - ✓ $\overline{d_{ab01}} - \overline{d_{ab11}} = \overline{h_a}$
- Case of stage1$_B$
  - ✓ $\overline{d_{ab00}} - \overline{d_{ab01}} = \overline{h_b}$
  - ✓ $\overline{d_{ab10}} - \overline{d_{ab11}} = \overline{h_b}$

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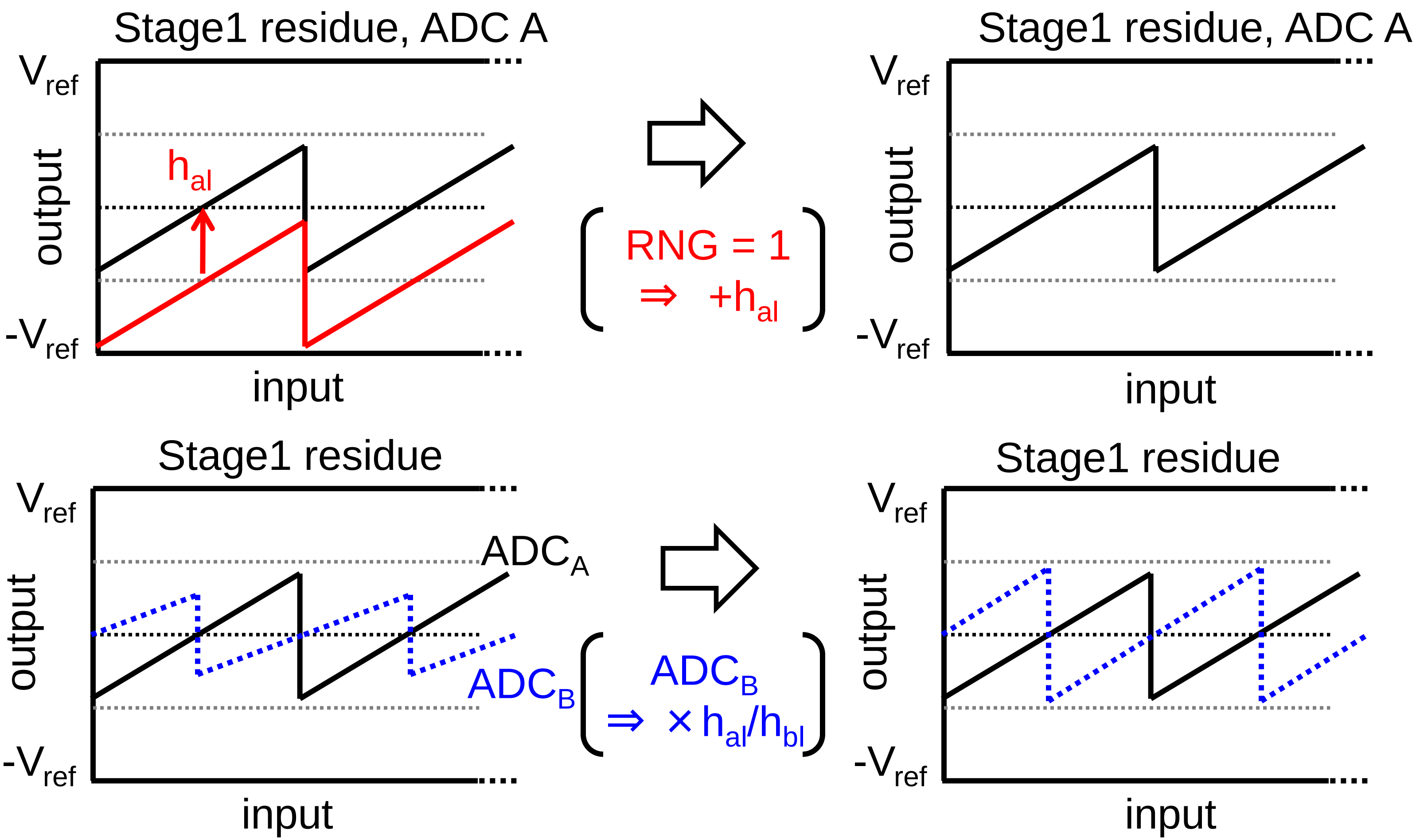
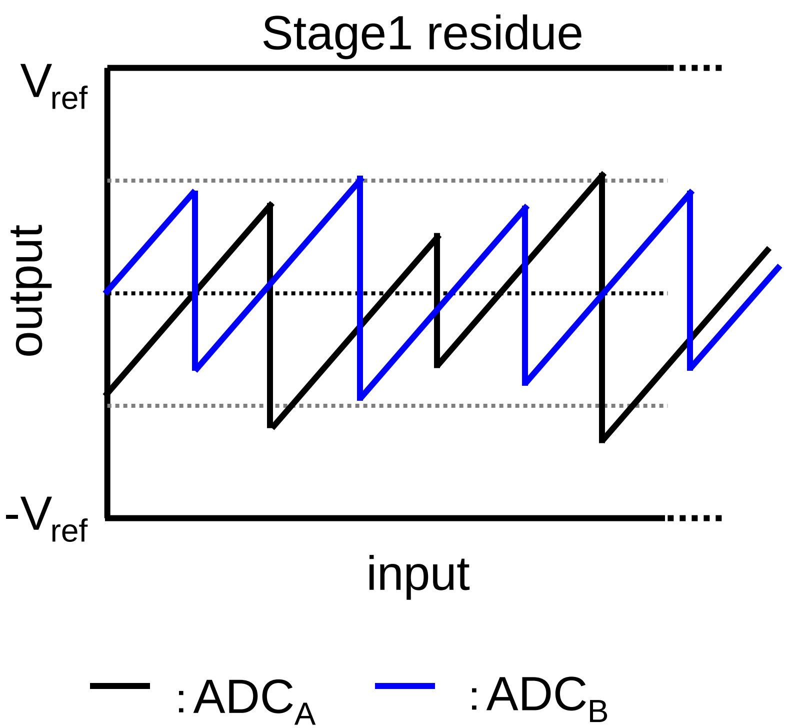
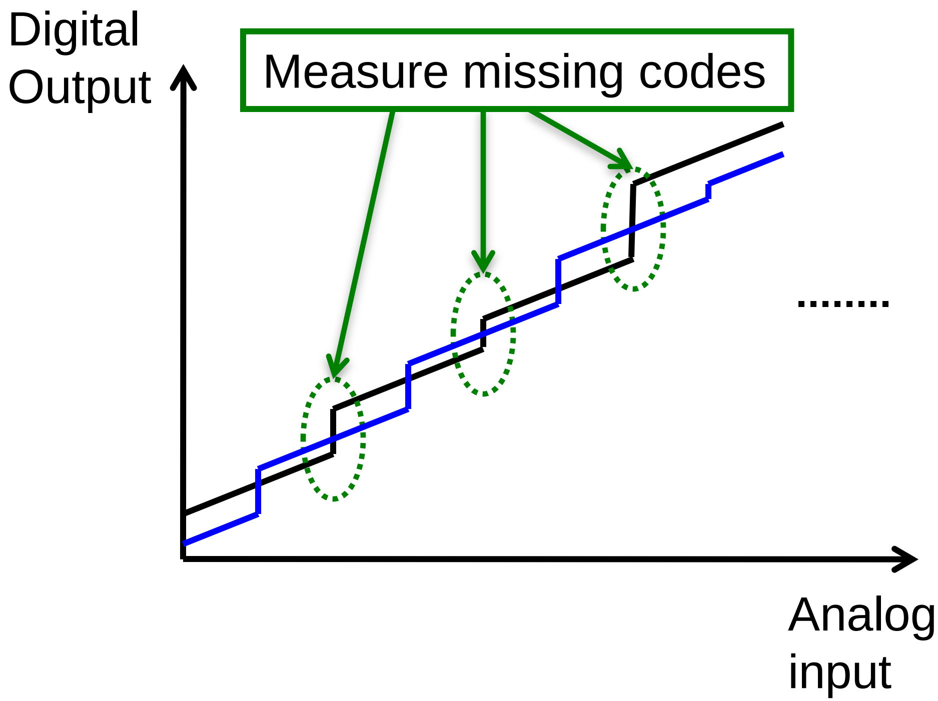
One Residue Signal Generation from Two Residue Signals



- Case of RNG_A=RNG_B=1 : subtracting h → one residue signal
- Slope mismatch(ADC_A and ADC_B) : compensate

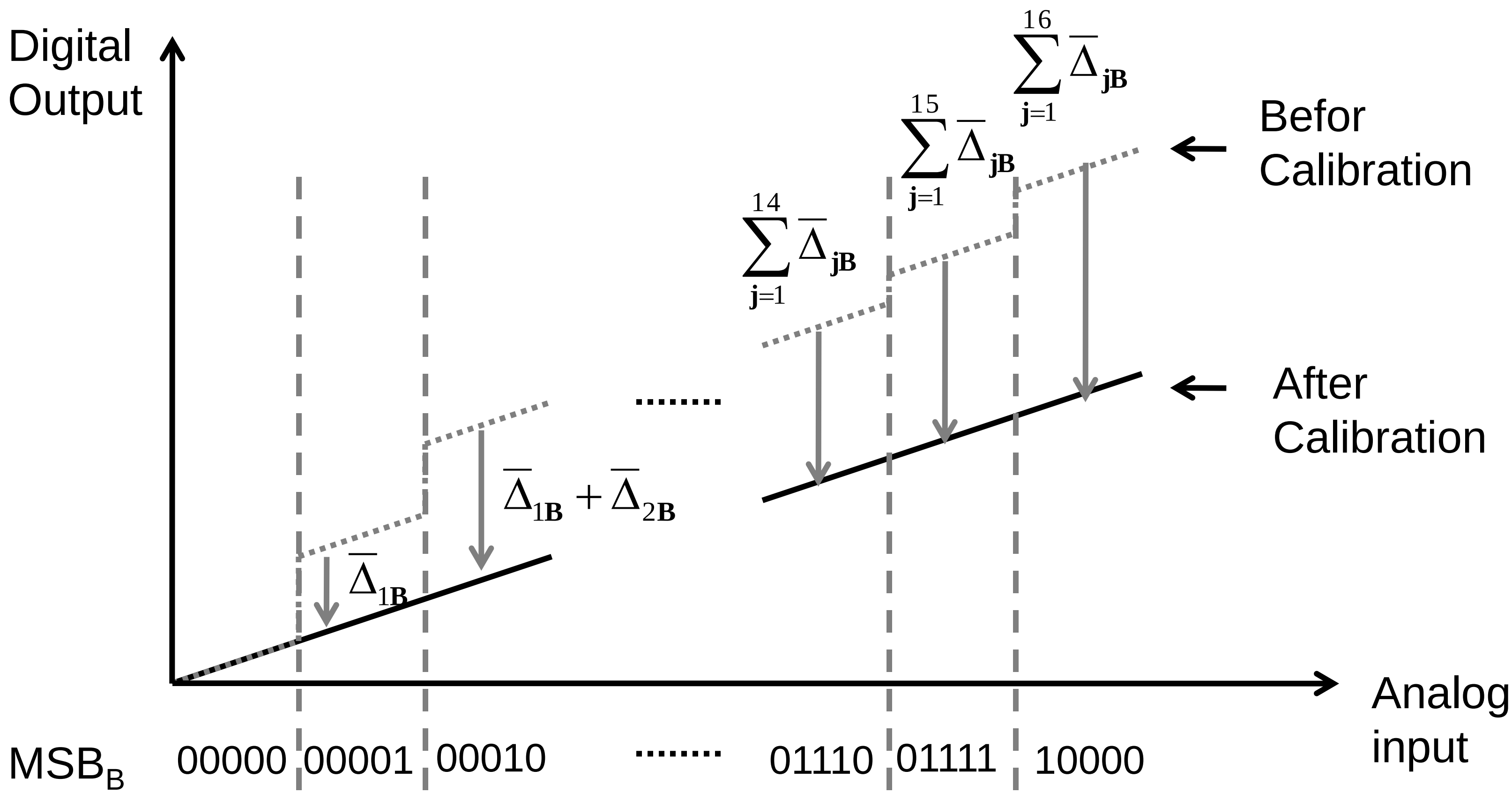
Gain Error and DAC Capacitor Mismatch Calibration





- Gain error and C mismatch
  → Cause missing codes
- Each missing codes : measured by other ADC

Gain Error and DAC Capacitor Mismatch Calibration



- Case of ADC_B (vice versa)
  - To compensate, Adding Δ_j

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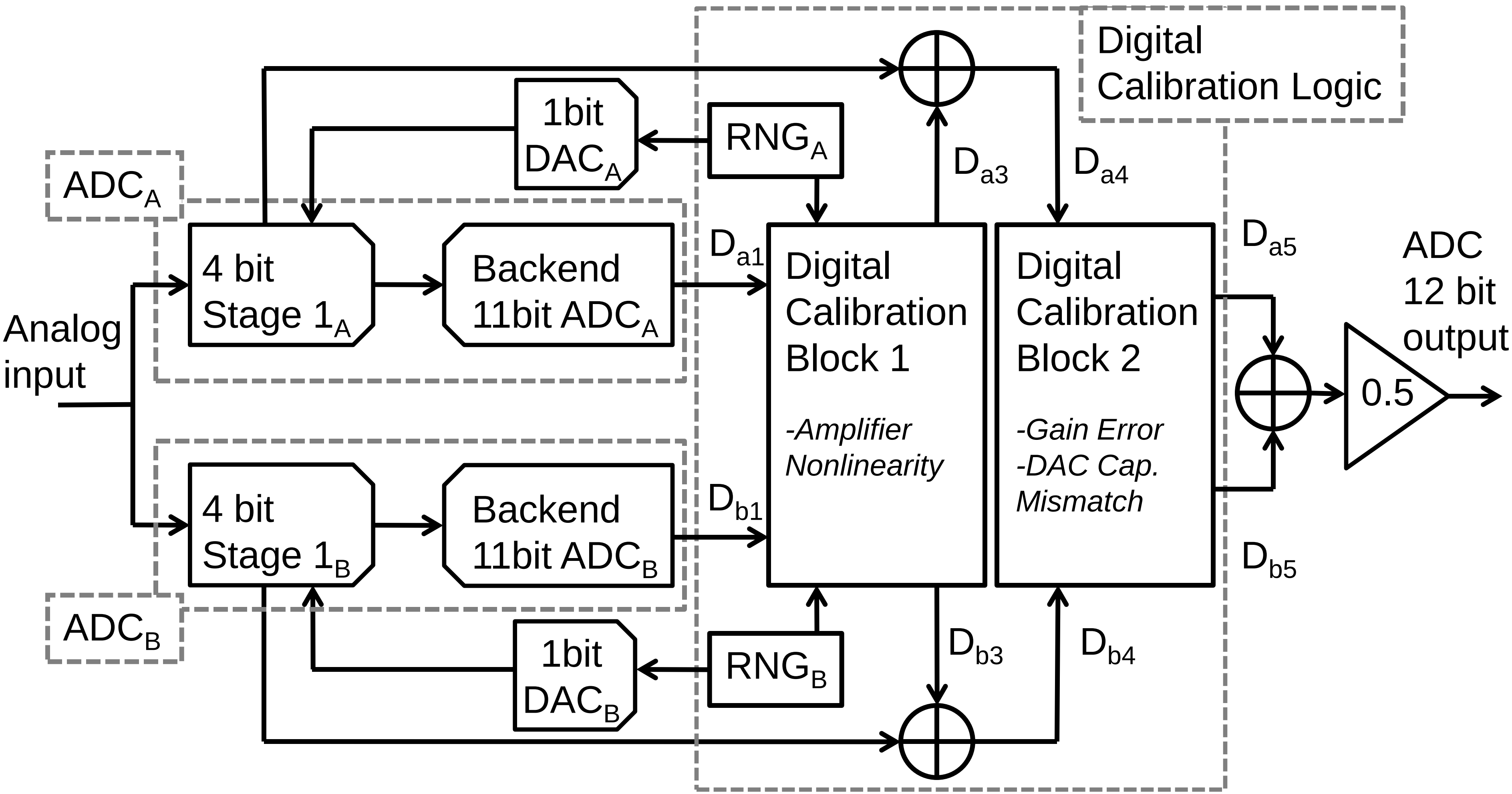
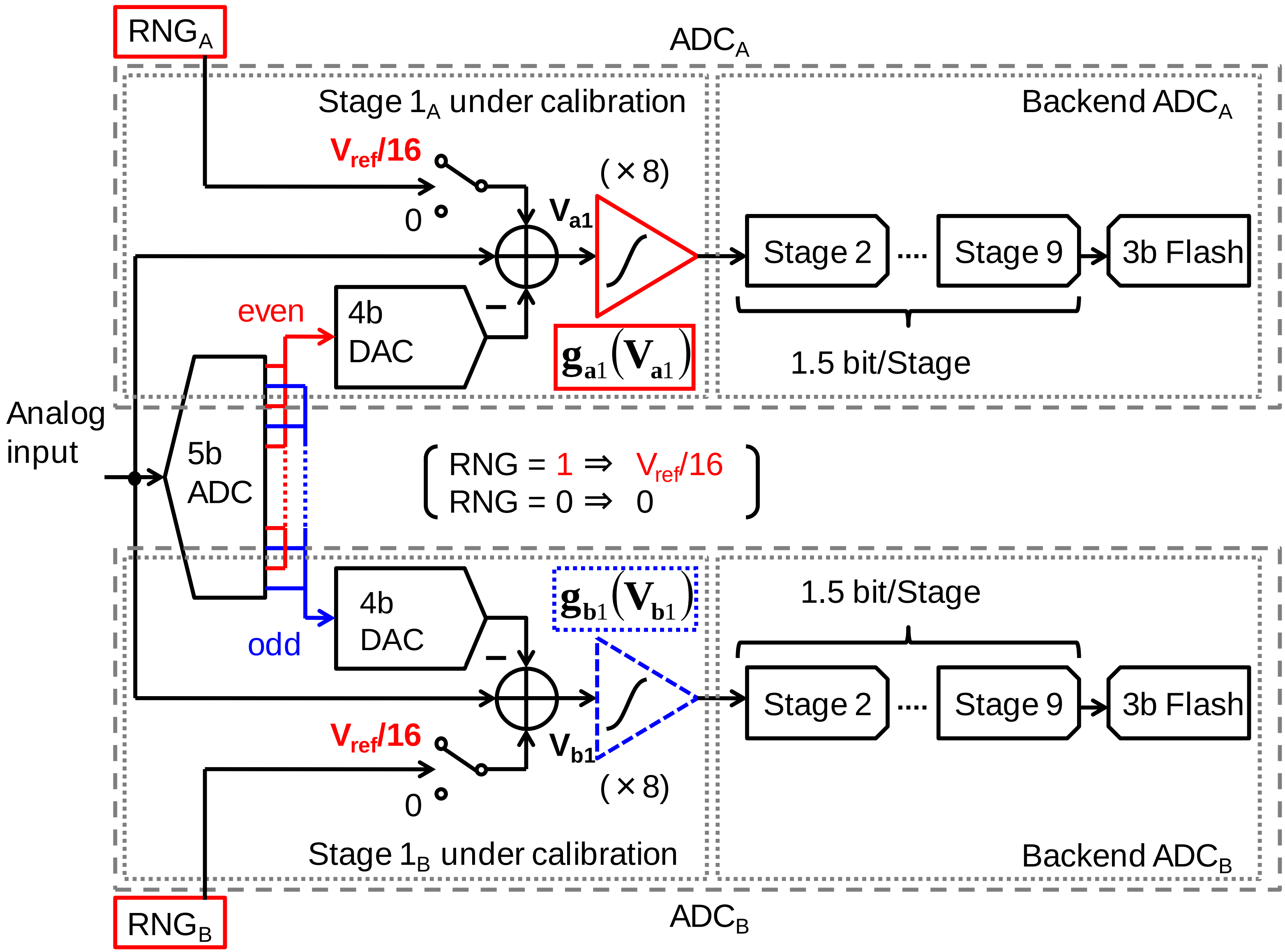
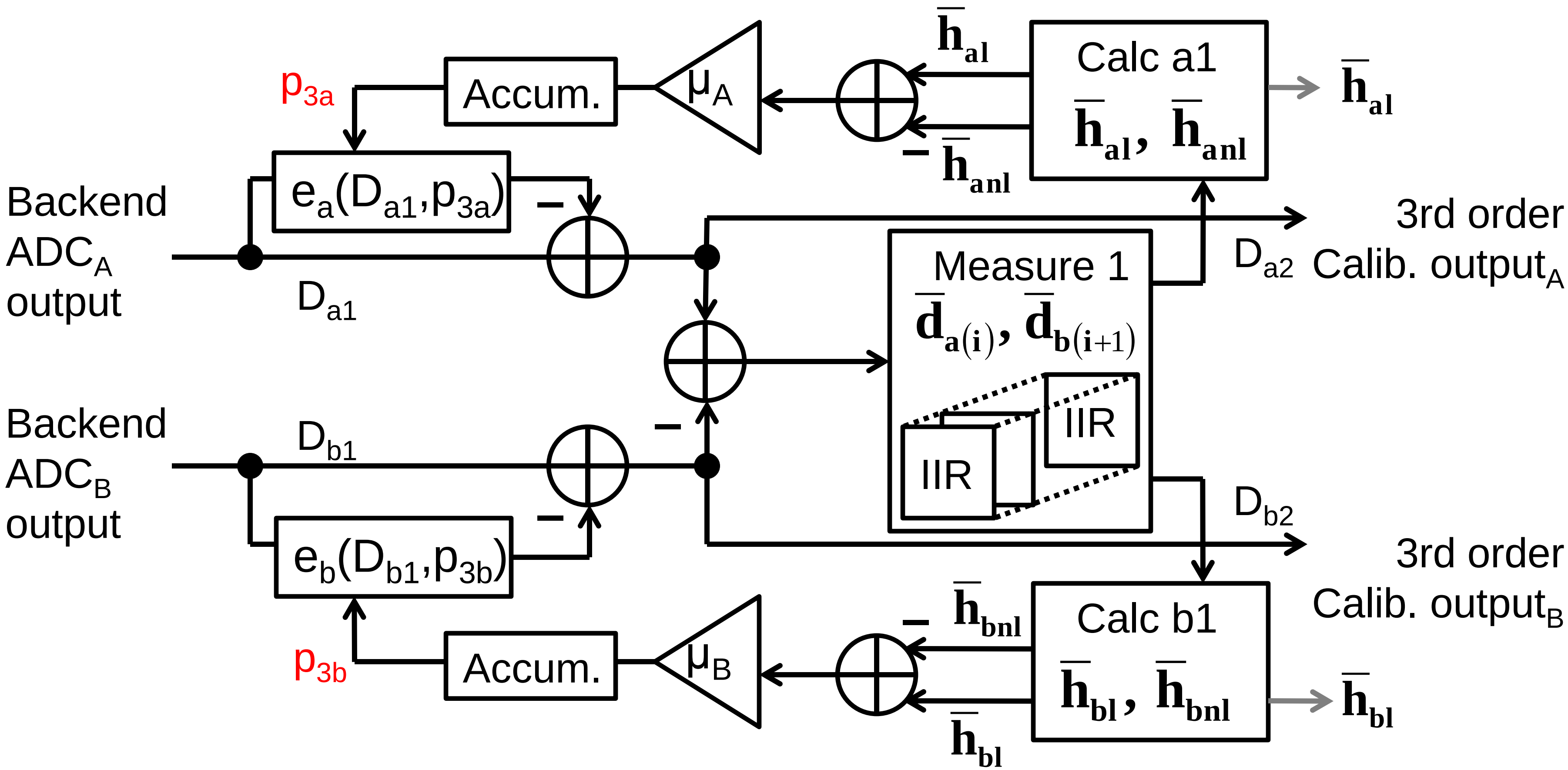
Architecture



Analog Portion of the Proposed Pipelined ADC Topology

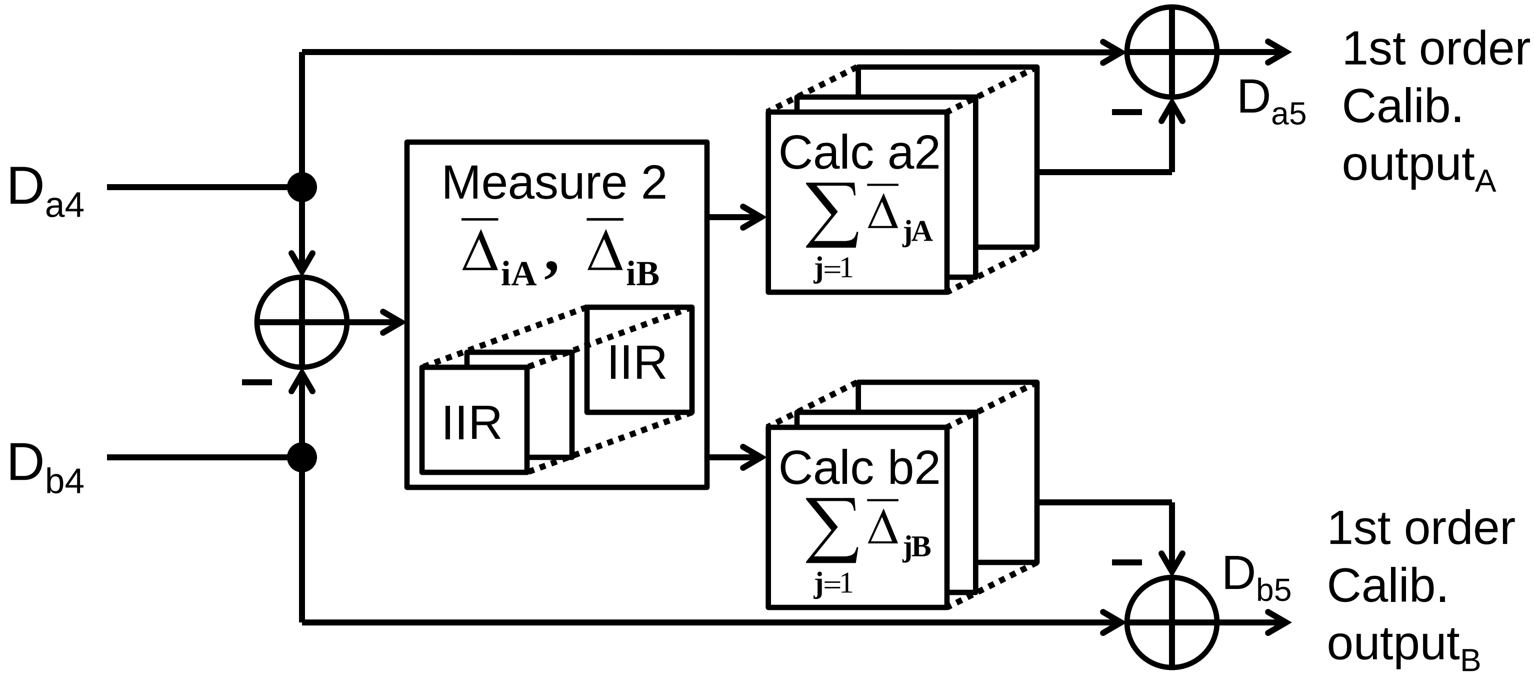


Digital Calibration Block 1-1 (for Amplifier Nonlinearity Correction)



- Calculate distance “h”

Digital Calibration Block 2 (for Gain Error and C Mismatch Compensation)



- Calculate missing codes
  → subtract missing codes from several output data

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Validate the Effectiveness with MATLAB

[Conditions]

ADC$_A$ (Stage1$_A$)

- C mismatch： 2% (σ)
- Nonlinearity of amplifier：

$$\mathbf{g}_{\mathbf{a}1}\left(\mathbf{V}_{\mathbf{a}1}\right)=7.5\cdot\mathbf{V}_{\mathbf{a}1}+\left(-15\right)\cdot\mathbf{V}_{\mathbf{a}1}{}^{3}$$

- Nonlinearity correction
  - ✓ LMS loop：
    μ_A= 1/8192
  - ✓ IIR filter gain：
    μ_{3a} = 1/512
- Gain error, C mismatch correction
  - ✓ IIR filter gain：
    μ_{1a} = 1/1024

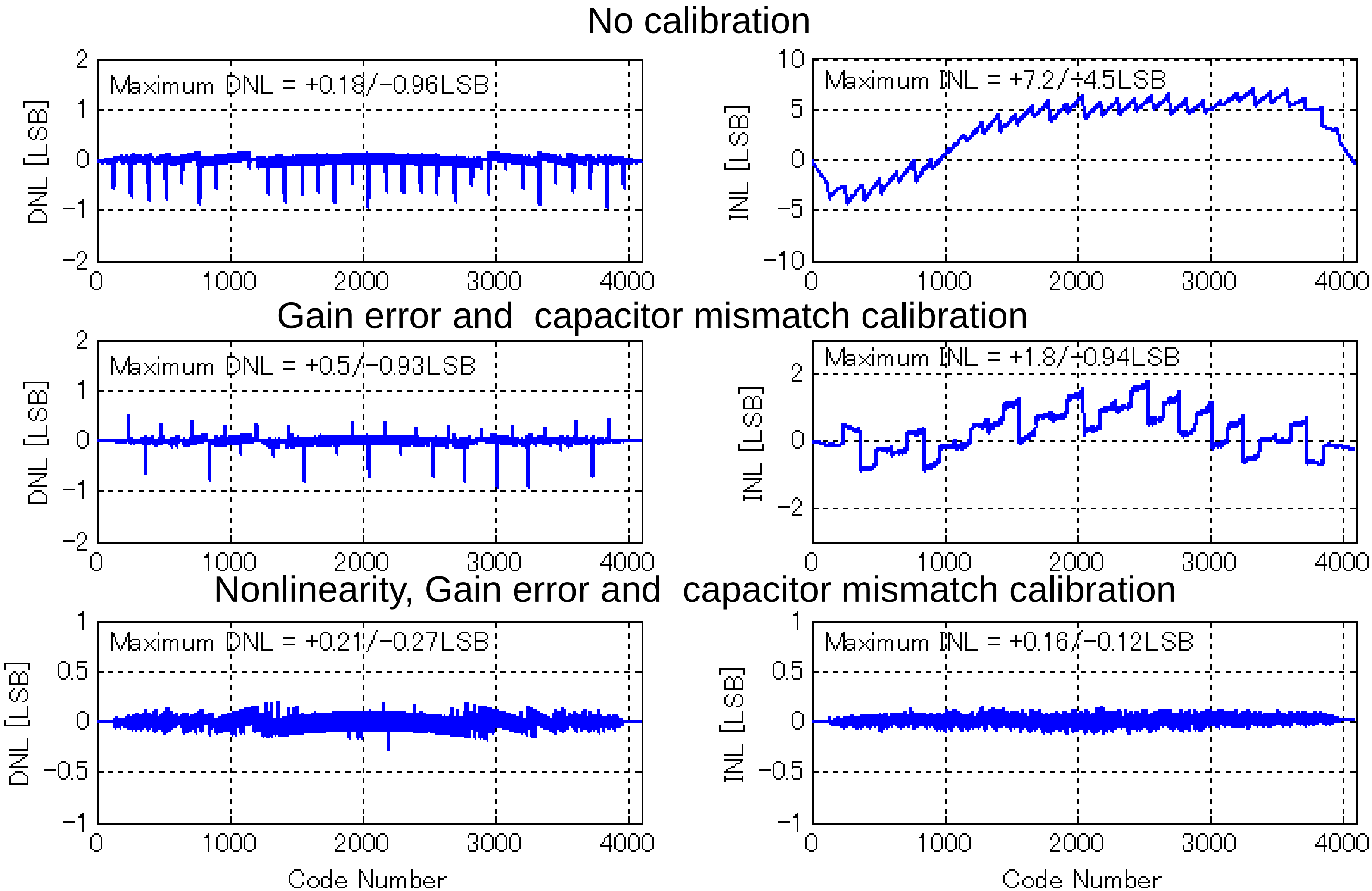
ADC$_B$ (Stage1$_B$)

- C mismatch： 2% (σ)
- Nonlinearity of amplifier：

$$\mathbf{g}_{\mathbf{b}1}\left(\mathbf{V}_{\mathbf{b}1}\right)=7.6\cdot\mathbf{V}_{\mathbf{b}1}+\left(-15.2\right)\cdot\mathbf{V}_{\mathbf{b}1}{}^{3}$$

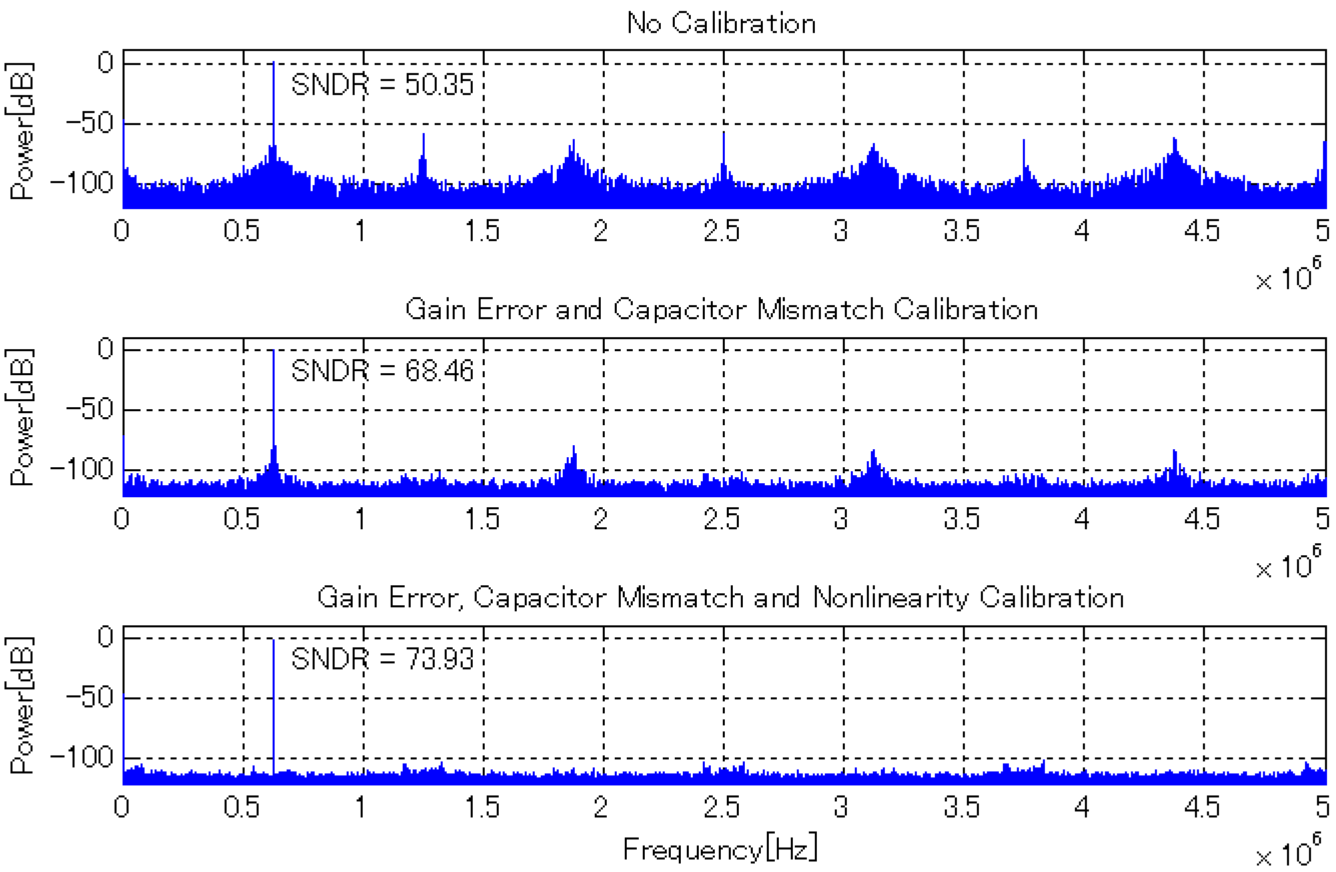
- Nonlinearity correction
  - ✓ LMS loop：
    μ_B= 1/8192
  - ✓ IIR filter gain：
    μ_{3b} = 1/512
- Gain error, C mismatch correction
  - ✓ IIR filter gain：
    μ_{1b} = 1/1024

DNL and INL of the ADC output



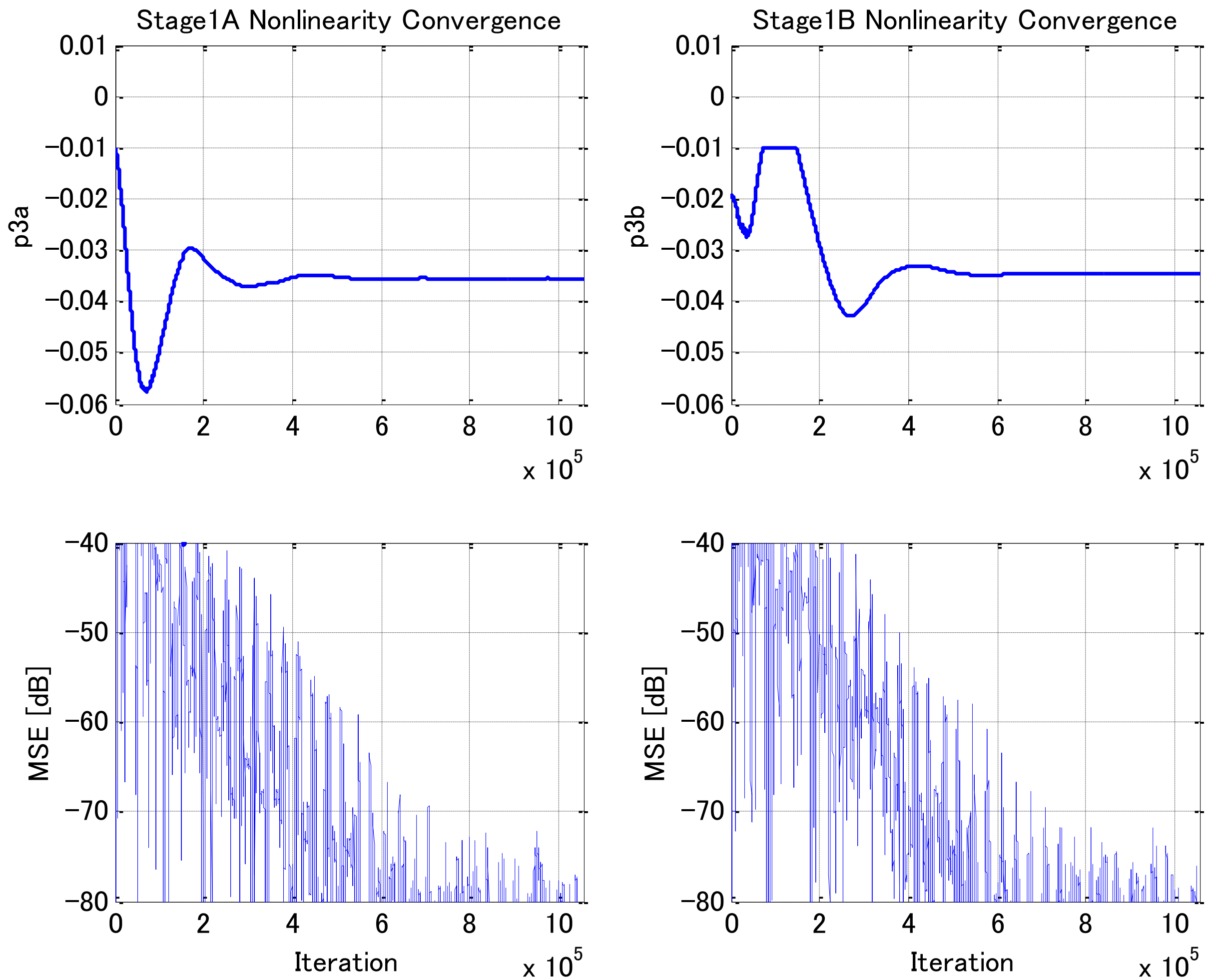
- Calibrate all error : DNL, INL are within ±0.5LSB

Output Power Spectrum



- Calibrate all error : SNDR=73.9dB

Convergence of 3rd-order term coefficient and mean square error in the LMS loop



MSE:
Mean Square Error

- $6*10^5$ samples : MSE is less -60dB (10MS/s , 0.06 sec)
  - Back-end ADC : 10bit accuracy

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Conclusion

- For low power pipelined ADC
  - Using open-loop residue amplifier in the first stage
- Propose the Background calibration algorithm
  - Apply split ADC structure
  - Open-loop residue amplifier
    - → Compensate nonlinearity and gain error
  - DAC → Compensate capacitor mismatches
  - Convergence time
    - → 100X faster than conventional method