PAPER Special Section on Analog Circuit Techniques and Related Topics

SAR ADC Algorithm with Redundancy and Digital Error Correction

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SUMMARY This paper describes an algorithm for Successive Approximation Register (SAR) ADCs with overlapping steps that allow comparison decision errors (due to, such as DAC incomplete settling) to be digitally corrected. We generalize this non-binary search algorithm, and clarify which decision errors it can digitally correct. This algorithm requires more SAR ADC conversion steps than a binary search algorithm, but we show that the sampling speed of an SAR ADC using this algorithm can be faster than that of a conventional binary-search SAR ADC — because the latter must wait for the settling time of the DAC inside the SAR ADC.

key words: *SAR ADC, digital error correction, non-binary, redundancy*

1. Introduction

SAR ADCs embedded in micro-controller chips are widely used in automotive electronics applications [1], and high reliability, high speed and high accuracy, low power and low cost are required in such applications.

In this paper we investigate a generalized non-binary algorithm that uses one comparator and requires M steps for N-bit resolution where M > N — in other words, it uses overlapping steps. Non-binary algorithms with a radix of $2^{N/M}$ have been used in SAR ADCs [2], [3], but here we describe a generalized non-binary algorithm without such radix restrictions. We describe the design methods and possible error correction range, and also show that SAR ADCs using this algorithm can be faster than those using binary search or prior non-binary search algorithms that have to allow for settling time of the DAC inside the ADC.

2. SAR ADC

SAR ADC Characteristics: Low-power SAR ADCs with small chip area are widely used for high-resolution (10–16 bit) and medium-sampling-speed applications, such as automotive, factory automation, and pen digitizer applications [4]–[13].

SAR ADC Configuration: SAR ADCs consist of a sample and hold circuit, comparator, DAC, SAR logic circuit and timing generator (Fig. 1).

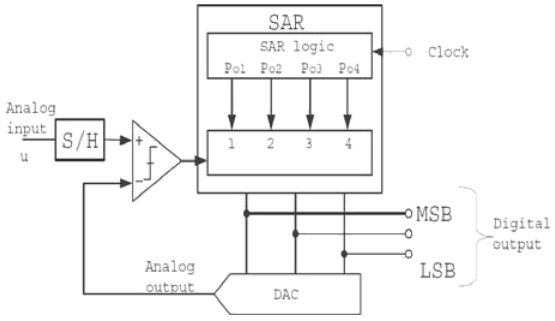

Fig. 1 Block diagram of an SAR ADC.

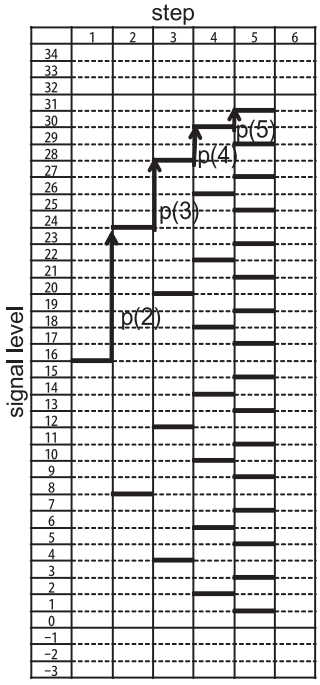

Fig. 2 Binary search algorithm of a 5-bit 5-step SAR ADC.

SAR ADC Operation: Conventional SAR ADCs use a multi-step binary search algorithm (Fig. 2).

3. Binary Search Algorithm

This section explains the binary search algorithm which re-

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alizes N-bit resolution SAR ADC with N steps, and we assume that the analog input range is normalized from 0 to $2^N - 1$. The comparator compares the analog input (V_{in}) and the reference voltage (DAC output), and its output $d(k)$ at k-th step is defined by

$$d(k) = \begin{cases} 1 & (\text{when } V_{in} > V_{ref}(k)) \\ 0 & (\text{otherwise}). \end{cases}$$

We also introduce a variable $s(k)$ defined by

$$s(k) = \begin{cases} 1 & (\text{when } d(k) = 1) \\ -1 & (\text{when } d(k) = 0). \end{cases}$$

The reference voltage in the first step ($V_{ref}(1)$) is given by

$$V_{ref}(1) = 2^{N-1}.$$

If the output of the comparator in (k-1)-th step ($d(k-1)$) is "1," the reference voltage in k-th step ($V_{ref}(k)$) is given by

$$V_{ref}(k) = V_{ref}(k-1) + 2^{N-k}.$$

If the output of the comparator in (k-1)-th step $d(k-1)$) is "0," $V_{ref}(k)$ is given by

$$V_{ref}(k) = V_{ref}(k-1) - 2^{N-k}.$$

Thus

$$V_{ref}(k) = 2^N \cdot \left(2^{-1} + \sum_{i=2}^{k} s(i-1)2^{-i}\right).$$

Then, the ADC output D_{out} is given by

$$\begin{aligned} D_{out} &= d(1)2^{N-1} + d(2)2^{N-2} + \ldots \\ &\quad \ldots + d(N-1)2 + d(N) \\ &= 2^{N-1} + \left(\sum_{i=2}^{N} s(i-1)2^{N-i}\right) + \frac{1}{2}(s(N) - 1). \end{aligned}$$

We see that if comparator decision errors occur, D_{out} cannot be corrected because there is no redundancy.

4. Prior Non-binary Algorithm

This section explains a prior non-binary search algorithm which realizes SAR ADC N-bit resolution with M steps (N ≤ M) using the radix $2^{N/M}$. In this algorithm, the reference voltages (which are different from those with the binary search algorithm) are given by

$$V_{ref}(k) = 2^{N-1} + \left(\sum_{i=2}^{k} s(i-1)\gamma^{M-i}\right).$$

Here $\gamma = 2^{N/M}$. The SAR ADC digital output is given by

$$D_{out} = 2^{N-1} + \left(\sum_{i=2}^{M} s(i-1)\gamma^{M-i}\right) + \frac{1}{2}(s(M) - 1)$$

This non-binary algorithm is restricted to the radix $\gamma = 2^{N/M}$.

5. Generalized Non-binary Algorithm

In this section, we propose a generalized non-binary algorithm which realizes N-bit resolution SAR ADC in M steps (N ≤ M) but it is not restricted to the radix of $2^{N/M}$. We give the reference voltage in k-th step($V_{ref}(k)$) as follows:

$$V_{ref}(k) = 2^{N-1} + \sum_{i=2}^{k} s(i-1)p(i). \tag{1}$$

Here $k = 1, 2, \ldots, M$, and $p(k)$ is the value for addition to (or subtraction from) the reference voltage in the previous step. Then we have the following ADC digital output:

$$D_{out} = 2^{N-1} + \sum_{i=2}^{M} s(i-1)p(i) + \frac{1}{2}(s(M) - 1). \tag{2}$$

We have derived that $p(i)$ must satisfy the following:

$$p(1) = 2^{N-1} \tag{3}$$

$$\sum_{i=1}^{M} p(i) = 2^N - 1 + (\text{over-range}). \tag{4}$$

Note that

- if $N = M$ and $p(i) = 2^{N-i}$, it is equivalent to the binary search algorithm.
- if $p(i) = \gamma^{-i}$ ($\gamma = 2^{N/M}$ and $1 < \gamma < 2$), it is the conventional non-binary search algorithm with radix γ.

Here "over-range (r)" is explained by the following example: the output range of an ordinary 5-bit resolution SAR ADC is from 0 to 31, but that of one with the generalized

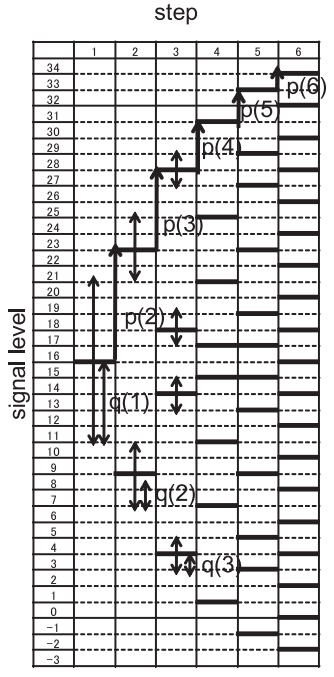

Fig. 3 Redundant search algorithm of a 5-bit 6-step SAR ADC (case 1).

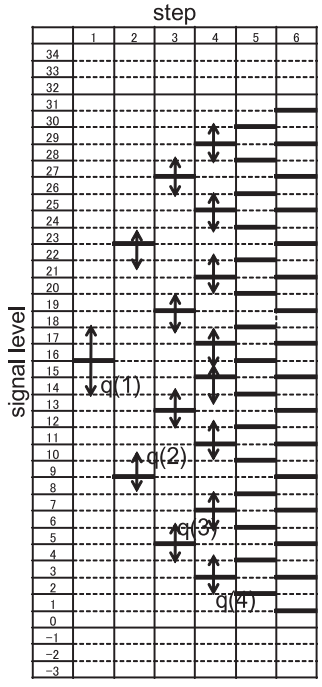

Fig. 4 Redundant search algorithm of a 5-bit 6-step SAR ADC (case 2).

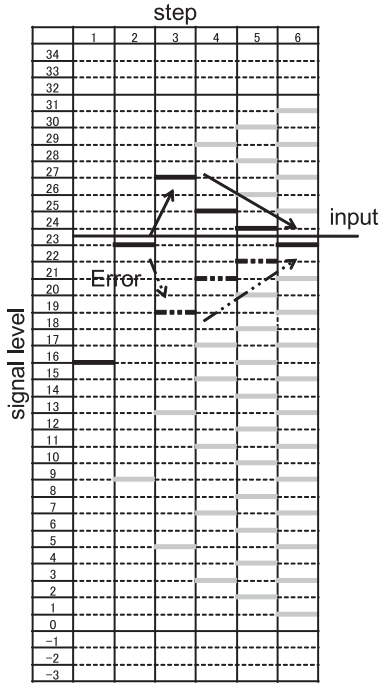

Fig. 5 Operation of the redundant search algorithm of a 5-bit 6-step SAR ADC (case 2).

non-binary algorithm of Fig. 3 is from −3 to 34. Here we call the range from −3 to −1 and also the range from 32 to 34 "over-range (±3LSB)," and $r = 3LSB$.

Example 1: Fig. 2 shows the reference voltages of a 5-bit resolution 5-step SAR ADC with the binary search algorithm, where $N = 5, M = 5, p(1) = 16, p(2) = 8, p(3) = 4, p(4) = 2, p(5) = 1$.

Example 2: Fig. 3 shows the reference voltages of a 5-bit resolution 6-step SAR ADC using the proposed generalized non-binary algorithm with over-range $r = 3$, $N = 5, M = 6, p(1) = 16, p(2) = 7, p(3) = 5, p(4) = 3, p(5) = 2, p(6) = 1$.

Example 3: Fig. 4 shows another case of reference voltages of a 5-bit resolution 6-step SAR ADC with the proposed algorithm, where over-range $r = 0$, $N = 5, M = 6, p(1) = 16, p(2) = 7, p(3) = 4, p(4) = 2, p(5) = 1, p(6) = 1$. Figure 5 shows operation of this SAR ADC when analog input is 23.5 and the output of the comparator is wrong in the second step, but correct ADC digital output is obtained.

6. Non-binary Search Algorithm and Digital Error Correction

For the non-binary search algorithm using Eq. (2), we see that there are 2^M comparison patterns (possible comparator output combination of all M steps) and 2^N output patterns (output codes in binary format), and since M is bigger than N, 2^M is bigger than 2^N. In other words, for a given output level D_{out}, there can be multiple comparison patterns, which means that there is some redundancy. Thus even if the comparator decision in a given step is wrong, correct ADC output may be obtained at the following step.

7. Analysis of Redundancy in Generalized Non-binary Search Algorithm

We define "the redundancy in k-th step ($q(k)$)"as follows:

$$q(k) = -p(k+1) + 1 + \sum_{i=k+2}^{M} p(i). \tag{5}$$

$q(k)$ in Eq. (5) indicates the overlap between output ranges of one comparison pattern and the next pattern for the k-th step. Comparator decision error within this range can be corrected.

Proposition 1: Even if the comparator result is wrong in the k-th step, if $|V_{in} - V_{ref}(k)| < q(k)$ is satisfied, we obtain correct ADC output.

Figure 5 shows one example, where the analog input (V_{in}) is 23.5. The input is compared with $V_{ref}(1) = 16$ in the first step, and the comparator decision is correct. In the second step the input is compared with $V_{ref}(2) = 23$, but the comparator output is wrong. However we obtain the correct ADC output because $|V_{in} - V_{ref}(2)| < q(2), (q(2) = 1)$ is satisfied.

In the case of an N-bit M-step SAR ADC with the generalized non-binary algorithm, we have derived the design method of error correction range or redundancy $q(k)$ ($k = 1, 2, \ldots, M$), and the calculation method of $p(k)$ ($k = 1, 2 \ldots, M$) as follows:

Proposition 2:

$$2^M - 2^N = \left(\sum_{i=1}^{M-1} 2^i q(i) \right) + 2 \cdot \text{over-range}. \tag{6}$$

Proof: See Appendix.

Example 1: Fig. 2 shows the case for $N = 5, M = 5, p(1) = 16, p(2) = 8, p(3) = 4, p(4) = 2, p(5) = 1, q(1) = q(2) = q(3) = q(4) = q(5) = 0$.

Example 2: Fig. 3 shows the case for over-range $r = 3$, $N = 5, M = 6, p(1) = 16, p(2) = 7, p(3) = 5, p(4) = 3, p(5) = 2, p(6) = 1$, $q(1) = 5, q(2) = 2, q(3) = 1, q(4) = 0, q(5) = 0$. The following are satisfied, which agrees with Eq. (A· 5):

$$\begin{aligned} p(2) &= 16 - q_(1) - q(2) - 2q(3) - 4q(4) - 8q(5) = 7 \\ p(3) &= 8 - q(2) - q(3) - 2q(4) - 4q(5) = 5 \\ p(4) &= 4 - q(3) - q(4) - 2q(5) = 3 \\ p(5) &= 2 - q(4) - q(5) = 2 \\ p(6) &= 1 - q(5) = 1. \end{aligned}$$

As Eq. (6) is satisfied,

$$2^6 - 2^5 = 2q(1) + 4q(2) + 8q(3) + 16q(4) + 32q(5) + 2r.$$

Example 3: Fig. 4 shows the case for over-range $r = 0$, $N = 5, M = 6, p(1) = 16, p(2) = 7, p(3) = 4, p(4) = 2, p(5) = 1, p(6) = 1$, $q(1) = 2, q(2) = 1, q(3) = 1, q(4) = 1, q(5) = 0, q(6) = 0$.

Remarks: (i) If an N-bit M-step SAR ADC with the proposed algorithm is designed to satisfy Eq. (6) for redundancy of each step $q(k)$ and over-range r, $p(k)$ that realize these values can be calculated from Eq. (A· 2).

(ii) $\sum_{i=1}^{M-1} 2^i q(i)$ is the total number of error correction patterns, because in Eq. (6), $\sum_{i=1}^{M-1} 2^i q(i)$ is equal to (the total number of comparison patterns) - (the total number of output levels). Since the total number of patterns when all comparator decisions are correct is equal to the total number of output patterns, $\sum_{i=1}^{M-1} 2^i q(i)$ is the total number of error correction patterns.

(iii) The coefficient of $q(i)$, "2^i," of $\sum_{i=1}^{M-1} 2^i q(i)$ in Eq. (6) can be explained as follows: 2^{i-1} is the total number of comparison patterns from the first step to i-th step, and 2 is the number of correction cases: one case is that "1" is in error, and another case is that "0" is in error. Therefore, the sum of length of all arrows of $q(i)$ in Fig. 3 is equal to $\sum_{i=1}^{M-1} 2^i q(i)$.

(iv) The circuit complexity for the generalized non-binary algorithm implementation is almost the same as that for the conventional non-binary one [2], [3] (we just need to change the data of coefficient RAM [10], [11]).

8. DAC Incomplete Settling

We consider the incomplete settling effects of the DAC for generating the reference voltage inside the SAR ADC. We assume that the DAC is a first-order system with a time constant of τ, and the actual reference voltage (DAC output) $V_{ref}^{act}(k)$ at k-th step is given by

$$V_{ref}^{act}(k) = V_{ref}^{act}(k-1) + [V_{ref}(k) - V_{ref}^{act}(k)][1 - e^{-\frac{T_{step}}{\tau}}].$$

Here T_{step} is the time slot for each step, and also we assume

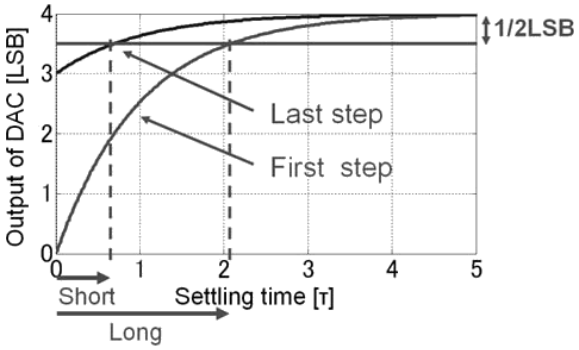

Fig. 6 Settling of the DAC output to generate a reference voltage at each stage.

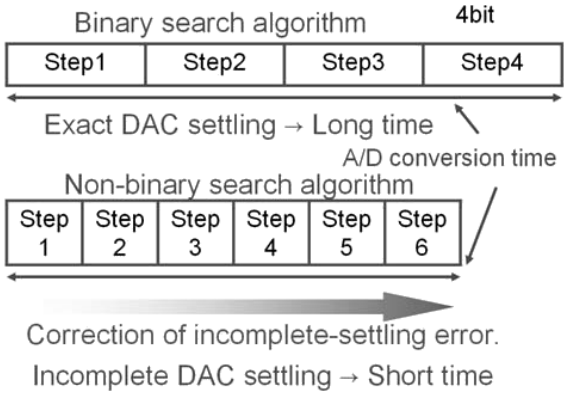

Fig. 7 AD conversion time explanation for the binary and non-binary algorithms.

$V_{ref}(1) = V_{ref}^{act}(1) = 2^{N-1}$. The following reference voltage error at k-th step is due to incomplete settling of the DAC output:

$$V_{ref,er}(k) = V_{ref}^{act}(k) - V_{ref}(k).$$

If time slot "T_{step}" is long enough, the error becomes small. Note also that the error is smaller in later steps because the change in the reference voltage between steps is smaller. Note that the SAR ADC with the binary algorithm has to wait for the DAC to settle within 1/2 LSB in each step (Fig. 6). The non-binary search algorithm can correct for error due to incomplete DAC settling at the previous step, and we do not have to wait for the DAC to settle within 1/2 LSB (Figs. 7 and 8). Also we can optimize the design of the proposed non-binary algorithm.

We here assume that the DAC is a segmented current-mode DAC (which consists of current sources, current switches and decoder logic circuit) [6] or a segmented capacitor-array DAC [2], [3]. Since we assume the segmented structure DAC, its time constant is always the same at each step. (Also note that if we use pipeline and/or parallel processing logic for decoder part, the decoding time would be relatively small [2].) We are designing the SAR ADC with the proposed algorithm using a capacitor-array DAC and our SPICE simulation shows that its DAC output can be approximated with the first-order model.

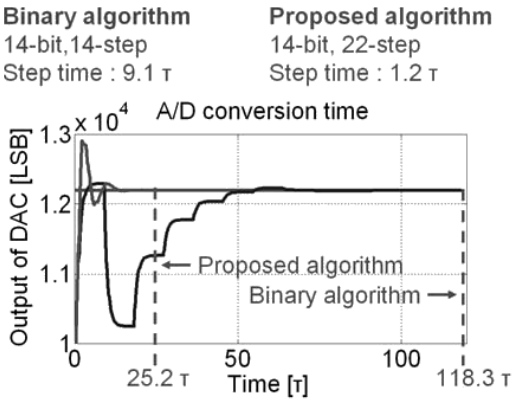

Fig. 8 Simulation of the DAC output transition in the SAR ADC for the binary and non-binary algorithms.

Table 1 10-bit 12-step SAR ADC conversion speed comparison and design parameter values.

Algorithm	Binary	Prior	Generalized
Time slot for each step	6.3τ	2.2τ	1.9τ
Number of steps	10	12	12
Total conversion time	56.7τ	24.2τ	20.9τ

	Prior non-binary		Generalized non-binary	
step k	p(k)	q(k)	p(k)	q(k)
1	512	90	512	20
2	323	51	246	40
3	181	28	113	23
4	102	16	65	14
5	57	9	37	9
6	32	5	21	4
7	18	3	13	3
8	10	1	7	2
9	6	1	4	2
10	3	0	2	0
11	2	0	2	0
12	1	0	1	0

9. Discussion

(1) We have simulated and compared the speed (conversion time) the SAR ADCs with the following conditions:

- 10-bit, 12-bit, 14-bit and 16 bit resolution cases.
- Redundant number of steps is 2 or 5 ($M = N + 2$ or $M = N + 5$, $N = 10, 12, 14, 16$).
- SAR ADC has correct ADC output.
- Time slot of each step is the same.

Tables 1–8 show the results of a simulated conversion-time comparison of SAR ADCs using the binary algorithm, the prior non-binary algorithm and the generalized non-binary algorithm, as well as the design parameter values; their values would be useful for actually designing an SAR ADC with the proposed algorithm. We see that the SAR ADC with the generalized non-binary algorithm is the fastest.

(2) We have discussed theoretically the generalized non-binary SAR ADC algorithms with two or three comparators in [12], [13], and we also investigate the implementation of the three comparators case in [4]–[6]. (Here two-comparator case corresponds to 1.5-bit/stage and three-comparator case corresponds to 2-bit /stage.) We have found the following: if we use multiple comparators, the number of conversion steps can be smaller (hence the conversion rate is faster). However we need multiple DACs to generate reference voltages for multiple comparators if we implement directly (i.e., more hardware and power are required). Also the offset mismatch among multiple comparators is a problem for a high resolution SAR ADC (which is different from a pipelined ADC case).

Table 2 10-bit 15-step SAR ADC conversion speed comparison and design parameter values.

Algorithm	Binary	Prior	Generalized
Time slot for each step	6.3τ	2.0τ	1.3τ
Number of steps	10	15	15
Total conversion time	56.7τ	28.0τ	18.2τ

	Prior non-binary		Generalized non-binary	
step k	p(k)	q(k)	p(k)	q(k)
1	512	285	512	2
2	406	179	255	71
3	256	113	93	46
4	161	70	59	29
5	102	44	38	19
6	64	28	24	13
7	40	18	15	10
8	25	11	9	7
9	16	7	6	5
10	10	5	4	3
11	6	3	3	2
12	4	1	2	2
13	3	0	1	1
14	2	0	1	0
15	1	0	1	0

Table 3 12-bit 14-step SAR ADC conversion speed comparison and design parameter values.

Algorithm	Binary	Prior	Generalized
Time slot for each step	7.7τ	2.3τ	2.1τ
Number of steps	12	14	14
Total conversion time	84.7τ	29.9τ	27.3τ

	Prior non-binary		Generalized non-binary	
step k	p(k)	q(k)	p(k)	q(k)
1	2048	290	2048	26
2	1248	160	1011	125
3	689	89	456	75
4	380	49	253	40
5	210	27	144	24
6	116	15	80	14
7	64	9	45	7
8	35	4	26	5
9	20	2	14	3
10	11	1	8	3
11	6	1	4	1
12	3	0	3	0
13	2	0	2	0
14	1	0	1	0

Table 4 12-bit 17-step SAR ADC conversion speed comparison and design parameter values.

Algorithm	Binary	Prior	Generalized
Time slot for each step	7.7τ	2.0τ	1.4τ
Number of steps	12	17	17
Total conversion time	84.7τ	32.0τ	22.4τ

	Prior non-binary		Generalized non-binary	
step k	p(k)	q(k)	p(k)	q(k)
1	2048	901	2048	0
2	1539	552	1024	280
3	944	338	372	178
4	579	207	237	109
5	355	128	153	72
6	217	79	95	49
7	133	48	59	32
8	82	30	38	20
9	50	18	25	13
10	31	11	16	9
11	19	6	10	5
12	12	4	7	4
13	7	3	4	2
14	4	1	3	1
15	3	0	2	1
16	2	0	1	0
17	1	0	1	0

Table 5 14-bit 16-step SAR ADC conversion speed comparison and design parameter values.

Algorithm	Binary	Prior	Generalized
Time slot for each step	9.1τ	2.6τ	2.2τ
Number of steps	14	16	16
Total conversion time	118.3τ	39.0τ	33.0τ

	Prior non-binary		Generalized non-binary	
step k	p(k)	q(k)	p(k)	q(k)
1	8192	970	8192	36
2	4871	529	4078	460
3	2656	289	1827	255
4	1448	157	1016	143
5	790	85	564	79
6	431	46	314	45
7	235	25	174	25
8	128	13	97	14
9	70	7	54	8
10	38	3	30	4
11	21	2	17	3
12	11	1	9	2
13	6	1	5	1
14	3	0	3	0
15	2	0	2	0
16	1	0	1	0

(3) Our SAR ADC implementation with the proposed algorithm is shown in Fig. 9; it consists of a timing generator, a comparator, a capacitor-array DAC and SAR logic with coefficient RAM and adder/subtracter. The coefficient RAM stores the non-binary steps to choose the next reference level. When the comparator output is "1," the RAM data is read and added to the current reference level with the adder, while it is "0," the data is subtracted with the subtracter. The result is given to the DAC as its digital input. This is based on the architecture of [2], [3] and the only RAM contents are changed. Our chip is fabricated and tested, and its details may be reported elsewhere.

Table 6 14-bit 19-step SAR ADC conversion speed comparison and design parameter values.

Algorithm	Binary	Prior	Generalized
Time slot for each step	9.1τ	2.1τ	1.5τ
Number of steps	14	19	19
Total conversion time	118.3τ	37.8τ	27.0τ

	Prior non-binary		Generalized non-binary	
step k	p(k)	q(k)	p(k)	q(k)
1	8192	2952	8192	0
2	5899	1771	4096	914
3	3540	1063	1591	559
4	2124	637	973	342
5	1275	382	595	209
6	765	229	364	129
7	459	138	222	79
8	275	83	136	49
9	165	50	83	30
10	99	31	51	19
11	59	18	31	12
12	36	12	19	7
13	21	7	12	5
14	13	4	7	2
15	8	2	5	3
16	5	1	2	1
17	3	0	2	1
18	2	0	1	0
19	1	0	1	0

Table 7 16-bit 18-step SAR ADC conversion speed comparison and design parameter values.

Algorithm	Binary	Prior	Generalized
Time slot for each step	10.4τ	2.9τ	2.3τ
Number of steps	16	18	18
Total conversion time	156.0τ	49.3τ	39.1τ

	Prior non-binary		Generalized non-binary	
step k	p(k)	q(k)	p(k)	q(k)
1	32768	3326	32768	36
2	19112	1796	16366	1644
3	10321	969	7379	905
4	5574	523	4059	498
5	3010	283	2233	275
6	1625	152	1228	153
7	878	82	675	84
8	474	44	372	46
9	256	24	205	25
10	138	12	113	14
11	75	7	62	8
12	40	3	34	4
13	22	1	19	3
14	12	1	10	1
15	6	1	6	1
16	3	0	3	0
17	2	0	2	0
18	1	0	1	0

Table 8 16-bit 21-step SAR ADC conversion speed comparison and design parameter values.

Algorithm	Binary	Prior —	Generalized
Time slot for each step	10.4τ	2.1τ	1.7τ
Number of steps	16	21	21
Total conversion time	156.0τ	42.0τ	34.0τ

	Prior non-binary		Generalized non-binary	
step k	p(k)	q(k)	p(k)	q(k)
1	32768	9966	32768	0
2	22791	5877	16366	2994
3	13440	3465	6695	1771
4	7926	2043	3959	1048
5	4674	1205	2341	619
6	2756	711	1385	366
7	1625	418	819	217
8	959	247	484	129
9	565	146	286	77
10	333	85	169	46
11	197	50	100	26
12	116	30	60	16
13	68	18	35	9
14	40	10	21	6
15	24	6	12	4
16	14	4	7	3
17	8	2	4	1
18	5	1	3	2
19	3	0	1	1
20	2	0	1	0
21	1	0	1	0

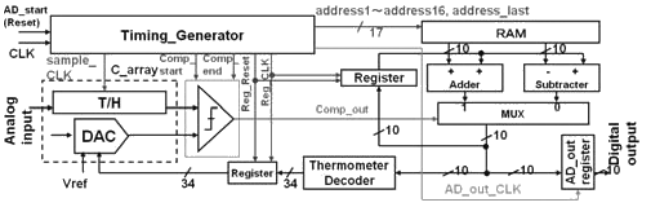

Fig. 9 Block diagram of the designed SAR ADC with the generalized non-binary algorithm.

10. Conclusions

We have proposed and analyzed a generalized non-binary algorithm for a high reliability, high speed SAR ADC. We have developed the design method, and also shown that SAR ADCs with the proposed algorithm are faster than those with binary search or prior non-binary algorithms when we take DAC settling time into account.

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Appendix

This Appendix gives the proof of Proposition 2.
It follows from Eq. (5) that

$$p(k+1) = -q(k) + 1 + \sum_{i=k+2}^{M} p(i). \quad (\mathrm{A}\cdot 1)$$

Then we have

$$p(k+1) = -q(k) + 2^{M-k-1} - \sum_{i=k+1}^{M-1} 2^{i-k-1} q(i). \quad (\mathrm{A}\cdot 2)$$

We have the following for $k = 1$ from Eq. (A· 2):

$$p(2) = -q(1) + 2^{M-2} - \sum_{i=2}^{M-1} 2^{i-2} q(i) \quad (\mathrm{A}\cdot 3)$$

$$2^{M-2} = p(2) + q(1) + \left(\sum_{i=2}^{M-1} 2^{i-2} q(i) \right) \quad (\mathrm{A}\cdot 4)$$

$$2^M = 4p(2) + 4q(1) + \sum_{i=2}^{M-1} 2^i p(i). \quad (A\cdot 5)$$

Also we have the following for $k = 1$ from Eq. (A· 1):

$$p(2) = -q(1) + 1 + \sum_{i=3}^{m} p(i). \quad (A\cdot 6)$$

From Eq. (A· 6) we have

$$2p(2) = -q(1) + 1 + \sum_{i=2}^{M} p(i). \quad (A\cdot 7)$$

Also from Eqs. (A· 7) and (A· 5) we have

$$2^M = 2\left[-q(1)+1+\sum_{i=2}^{M} p(i)\right]+4q(1)+\sum_{i=2}^{M-1} 2^i q(i) \quad (A\cdot 8)$$

$$2^M = 2\left[1 + \sum_{i=2}^{M} p(i)\right] + \sum_{i=1}^{M-1} 2^i q(i). \quad (A\cdot 9)$$

In Eq. (A· 9), the left side term 2^M is the total number of comparison patterns and $2(1 + \sum_{i=2}^{M} p(i))$ on the right side is the total number of output levels. For N-bit resolution, the number of the necessary output levels is 2^N, and hence $2(1 + \sum_{i=2}^{M} p(i)) = 2^N + 2 \cdot$ (over-range). Thus Eq. (A· 9) reduces to

$$2^M - 2^N = \left(\sum_{i=1}^{M-1} 2^i q(i)\right) + 2 \cdot (\text{over-range}).$$

(Q.E.D)

Note that the derivation of Eq. (A· 2) is given as follows: We have the following from Eq. (A· 1):

$$p(k+1) = -q(k) + 1 + p(k+2) + \sum_{i=k+3}^{M} p(i). \quad (A\cdot 10)$$

We expand Eq. (A· 10) using Eq. (A· 1):

$$\begin{aligned}
p(k+1) &= -q(k) + 1 + \sum_{i=k+3}^{M} p(i) \\
&\quad + \left(- q(k+1) + 1 + \sum_{i=k+3}^{M} p(i)\right). \\
p(k+1) &= -q(k) - q(k+1) + 2\left(1 + \sum_{i=k+3}^{M} p(i)\right). \\
p(k+1) &= -q(k) - q(k+1) \\
&\quad + 2\left(1 + p(k+3) + \sum_{i=k+4}^{M} p(i)\right). \\
p(k+1) &= -q(k) - q(k+1) - 2q(k+2) \\
&\quad + 4\left(1 + \sum_{i=k+4}^{M} p(i)\right).
\end{aligned}$$

We repeat this procedure and we have Eq. (A· 2).

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