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Presentation file

Challenge for Analog Circuit Testing in Mixed-Signal SOC

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1. Introduction
2. Review of Analog Circuit Testing in Mixed-Signal SOC
3. Research Topics
4. Challenges & Conclusion

Contents

Sense of balance is important

- Analog portion continues to be difficult part of SOC test.
- Balance between costs and benefits is important in LSI testing.

This makes issues and challenges of analog circuit testing in mixed-signal SOC to be clear and logical.

Contents

Management Strategy

- Strategy 1 :

  Use low cost ATE and develop analog BIST to make testing cost lower.

- Strategy 2 :

  Use high-end mixed-signal ATE as well as its associated services & know how.
  Fast time-to-market & no BIST can make profits much more than testing cost.

Save or Earn

ATE: Automatic Test Equipment
BIST: Built-In Self-Test

Low Cost Testing

Ideal :

- 100% chips work well. No testing

Reality :

- Low cost ATE
- Short testing time
- Multi-site testing
  (Simultaneous multiple-chip test)
- Minimum or no chip area penalty for BIST

A penny saved is a penny earned.

Benefits of Testing

- Better quality: Less penalty costs for repairing/replacing faulty LSI
- Diagnosis

  Automotive application IC

  ⇒ very high reliability
- Yield enhancement

  Testing and DFT can help yield enhancement

DFT: Design For Testability

Test and Measurement are different

- Production Test : 100% Engineering

  Decision of “Go” or “No Go”

  For example, it can be performance comparison between DUT and “Golden Device”.

  LSI testing is production/manufacturing engineering.

- Measurement : 50% Science, 50% Engineering

  Accurate performance evaluation of circuit

Measurement can be costly, but testing should be at low cost.

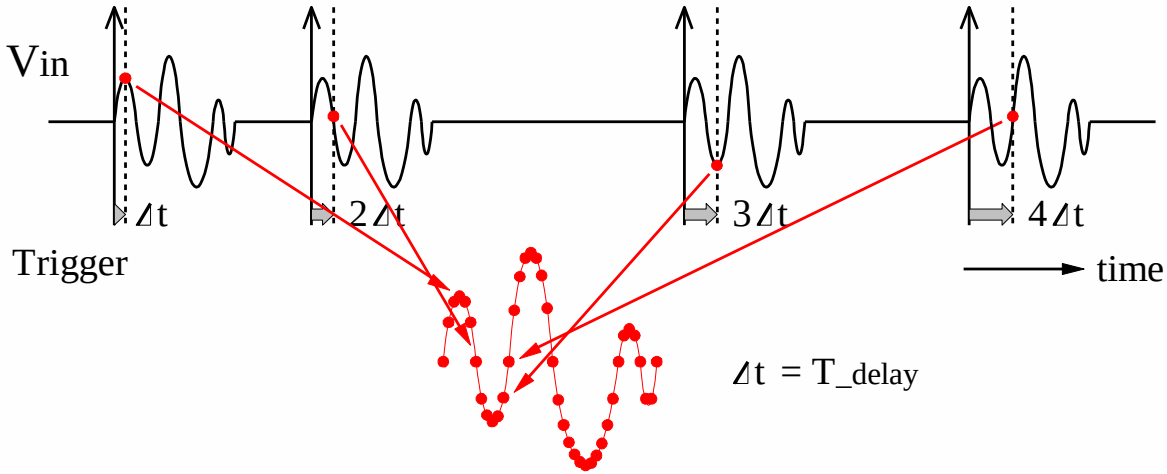
DUT: Device Under Test

Equivalent-time Sampling in Testing

- Production Test :

  Input signal is controllable

  ➡ Equivalent-time sampling



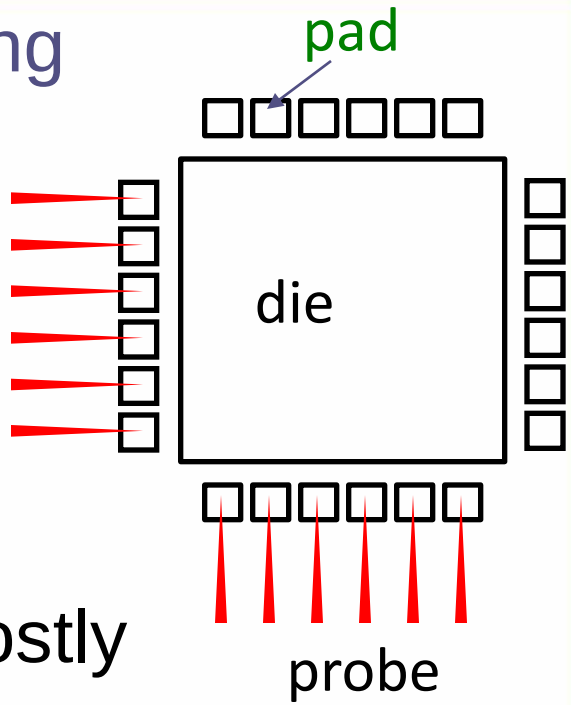
Waveform reconstruction of repetitive signal

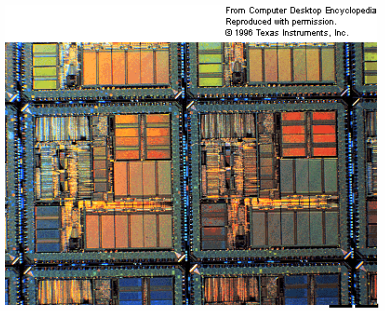
- Measurement : Input signal is unknown

Equivalent-time sampling can test high frequency signal at low cost.

On-Wafer Probing Testing

- On-wafer testing before packaging reduces IC cost.
- Probing has some issues:
  - On-resistance of probing
  - Probing damages PAD
    - ⇨ MEMS probe may alleviate it.
  - High-frequency signal probe is costly
    - ⇨ No test after yield becomes better.
  - Multi-site probing is difficult.
- Wireless communication technology may realize contact-less probing.





Analog BIST

- BIST for digital : Successful
  (scan path, memory BIST)
  BIST for analog : Not very successful
- Digital test : Functionality ⇨ Easy
  Analog test : Functionality & Quality ⇨ Hard

Analog: parametric fault as well as fatal fault.

Prof. A. Chatterjee
Specification-based Test Alternative Test Defect-based Test

- In many cases
  - Analog BIST depends on circuit.
  - No general method like scan path in digital.
  - One BIST, for one parameter testing

Two Contradictions of Analog BIST

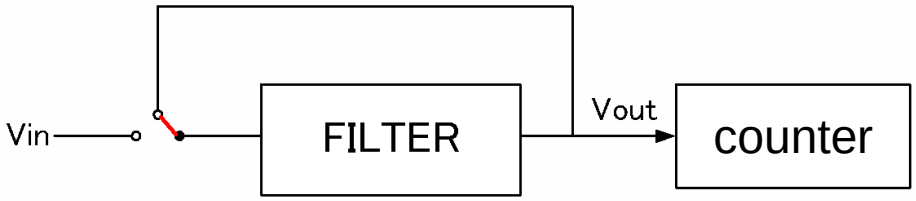
- Analog BIST has to have no defects.
- Analog BIST often has to have better performance than circuit under test.

To solve these contradictions, analog BIST must be small & simple.

Analog BIST chip area and testing cost are trade-off.

Analog BIST Example

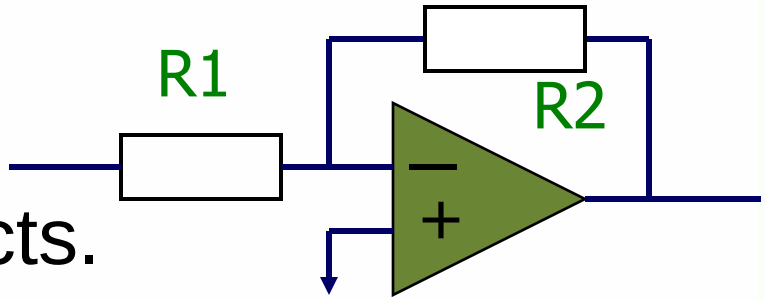
- ΔΣ modulation for signal generation
- Time-domain analog processing
- Analog boundary scan
- Use of power supply line
- Oscillation during test (analog filter, OpAmp)



- "Controllability", "Observability" are useful concepts.

Robust Design and Testing

Robust design makes its testing difficult.



- Feedback suppresses parameter variation effects.
- Self-calibration and redundancy hide defects in CUT.
- Background calibration takes long time for its testing due to calibration convergence.

Robust design (yield enhancement) and testing cost reduction are trade-off.

ADC Testing (DC Linearity)

- DC linearity test is the most important.
  - Precise ramp generation is challenging.
  - High resolution ADC ⇨ long testing time

- DC testing time is proportional to

  number of codes / sampling frequency

  large slow

High resolution ADC DC linearity test takes long time and is costly.

ADC Testing (AC Performance)

- ADC AC performance testing
  - Sampling clock jitter
  - High frequency input signal
- We have to build low clock jitter system and apply high frequency input signal.

  No alternative method so far.

Development of ADC AC performance testing system is costly.

RF Testing

- RF testing technology is different from analog testing technology.
- Testing item examples:
  - EVM test
  - System level testing, GSM/EDGE
  - AM/PM distortion
  - Jitter, Phase noise
- High-speed I/O testing is another challenging area.

Seven Rules of Mixed-Signal DFT & BIST

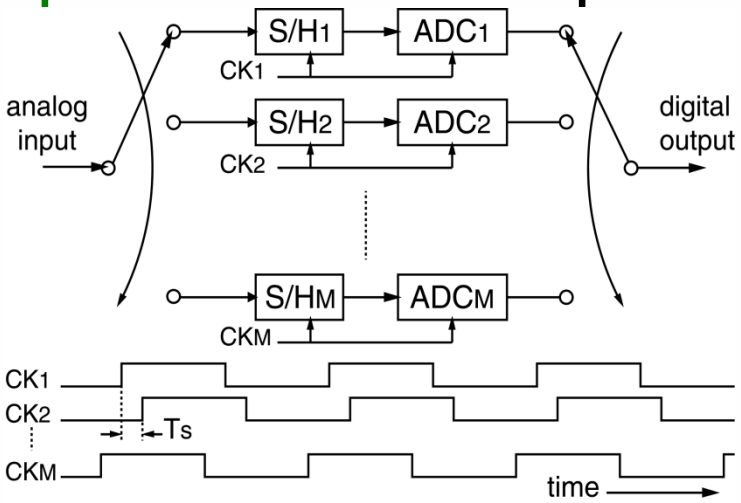
① Oversampling the test output signal.
② Undersampling of
a high-frequency periodic signal.
③ Differential measurement of
the test output signal.
④ Use digital techniques as much as possible.
⑤ Apply off-line calibration, auto-zero techniques.
⑥ Exploit redundancy in CUT
to provide test reference
⑦ Reuse circuit under test parts to perform test

K. Arabi (Qualcomm), IEEE VTS 2010

ATE for Mixed-Signal Testing

- Analog part is costly for development.
- Analog BIST is also beneficial
  for mixed-signal ATE manufacturer
- ATE must be designed with today's technology for next generation higher performance chip testing.

Interleaved ADC used in ATE
to realize very high sampling rate
with today's ADCs



Low Cost ATE

- Digital ATE
  - No analog option such as Arbitrary Waveform Generator: AWG
  - Input/output are mainly digital.
- Replacement of analog ATE with digital ATE
  - Multi-site testing becomes possible.
  - Still short testing time is important.
- Secondhand ATE, In-house ATE

Cooperation among Engineers

- Collaboration is important
  - Circuit designer
  - LSI testing engineer
  - ATE manufacturer engineer
  - Management
  - LSI testing researcher in academia
- For example, analog BIST acceptance by circuit designer is needed.
- Strong background of analog circuit design as well as LSI testing is required for analog testing research.

New Trend
On-chip Instrumentation

On-chip instrumentation is becoming a must for LSI testing.

Example:

- On-chip temperature sensors
- On-chip voltage sensors
- On-chip jitter measurement DFT
- On-chip signal generation DFT

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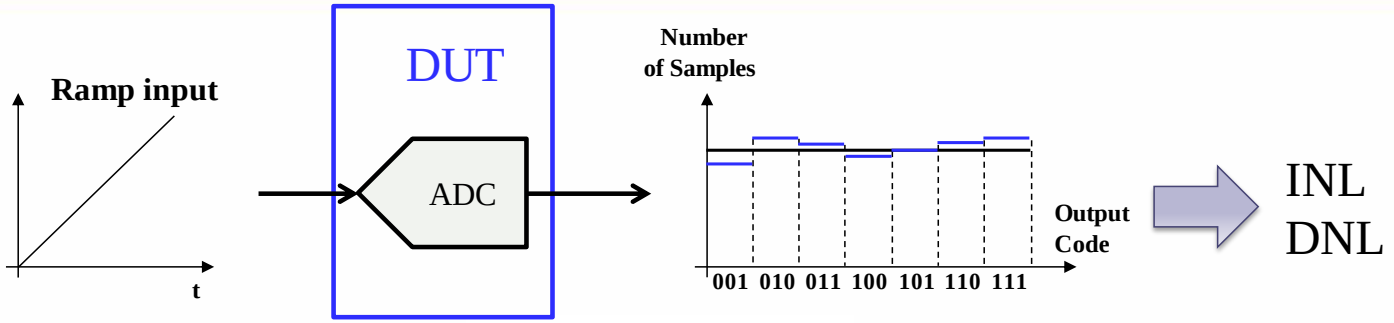
Research Topics 1

ADC Linearity Test Signal Generation
for Short Testing Time

Ref. [5] S. Uemori, et. al., ADC Test Signal Generation
IEEE APCCAS (Dec. 2010)

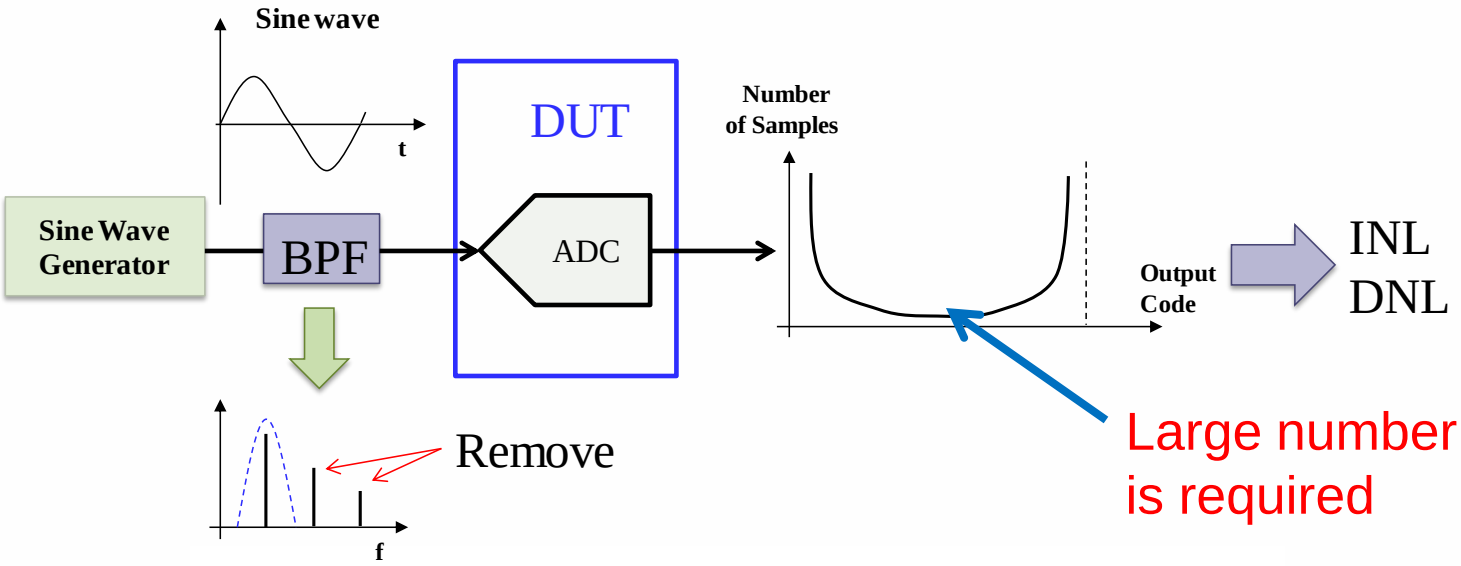
DC linearity testing time for
a high-resolution low-sampling ADC is long,
and it is costly.

Conventional ADC Linearity Test Signals



Ramp input

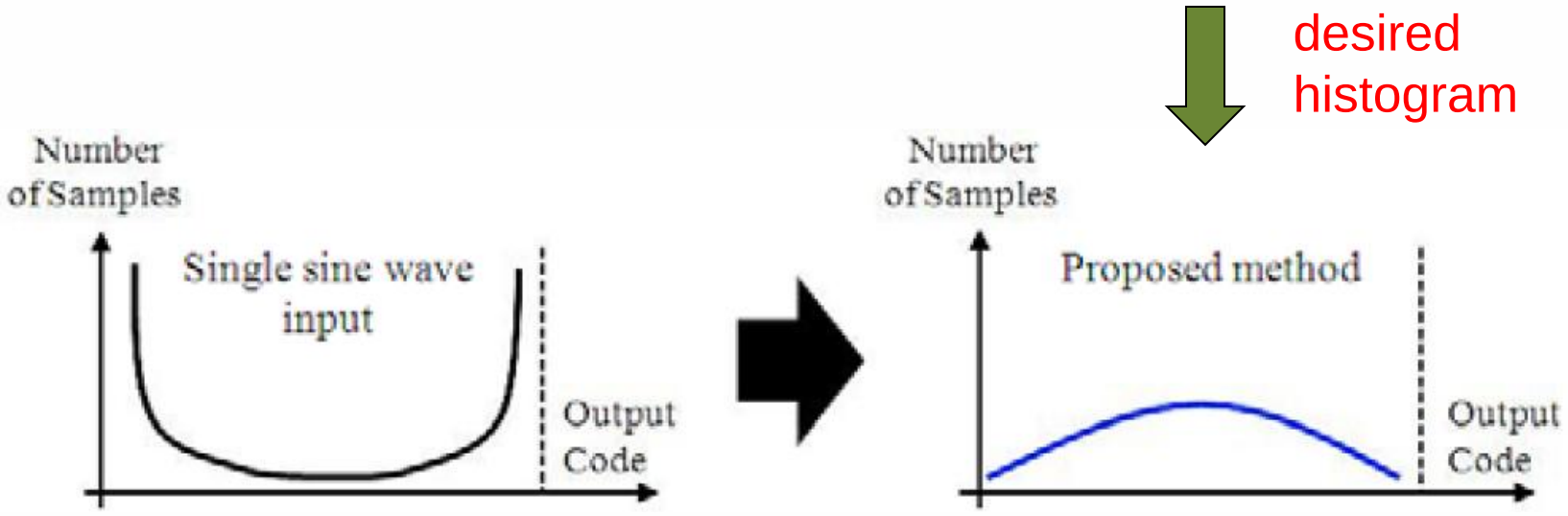
Accuracy is limited



Single sine wave input

ADC Output Histograms

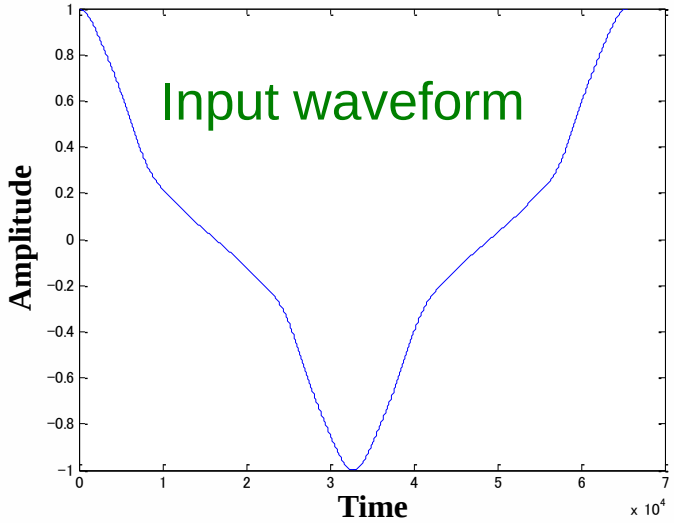
- In some mixed-signal SOCs, accurate ADC linearity evaluation is required around the middle of its input range.

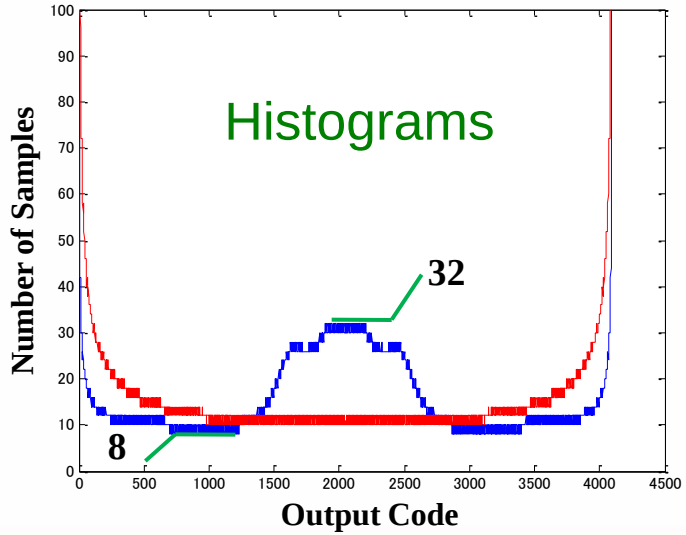


Sine wave

Proposed method

Proposed Method



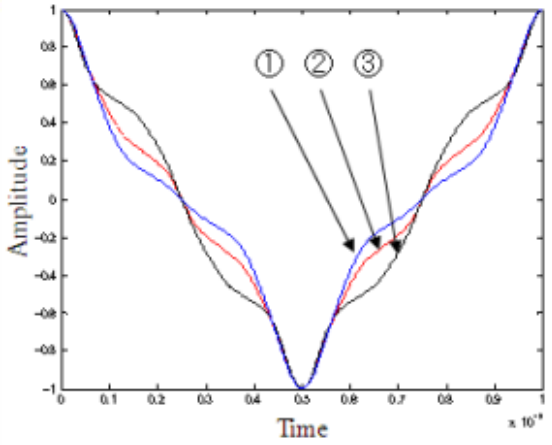


$$V_n = \frac{\cos((2n-1)wt)}{(2n-1)^2} \qquad n=1,2,\cdots$$

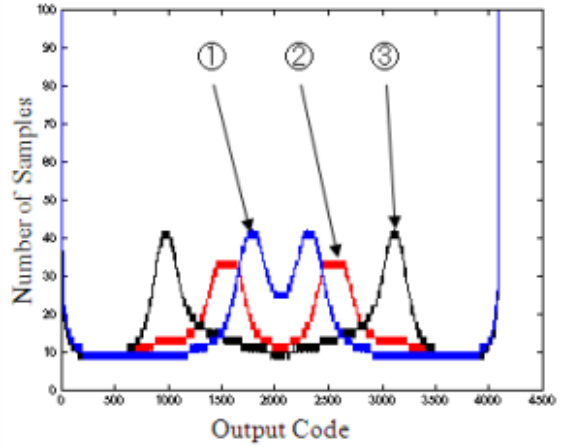
$$V_{in} = \frac{4}{\pi}\left(V_1 + 2.6 \cdot V_2 + 1.8 \cdot V_3 + 1.4 \cdot V_6 + 1.2 \cdot V_7\right)$$

Histogram for the middle of ADC input range increases.

Simulation Results of Proposed Method



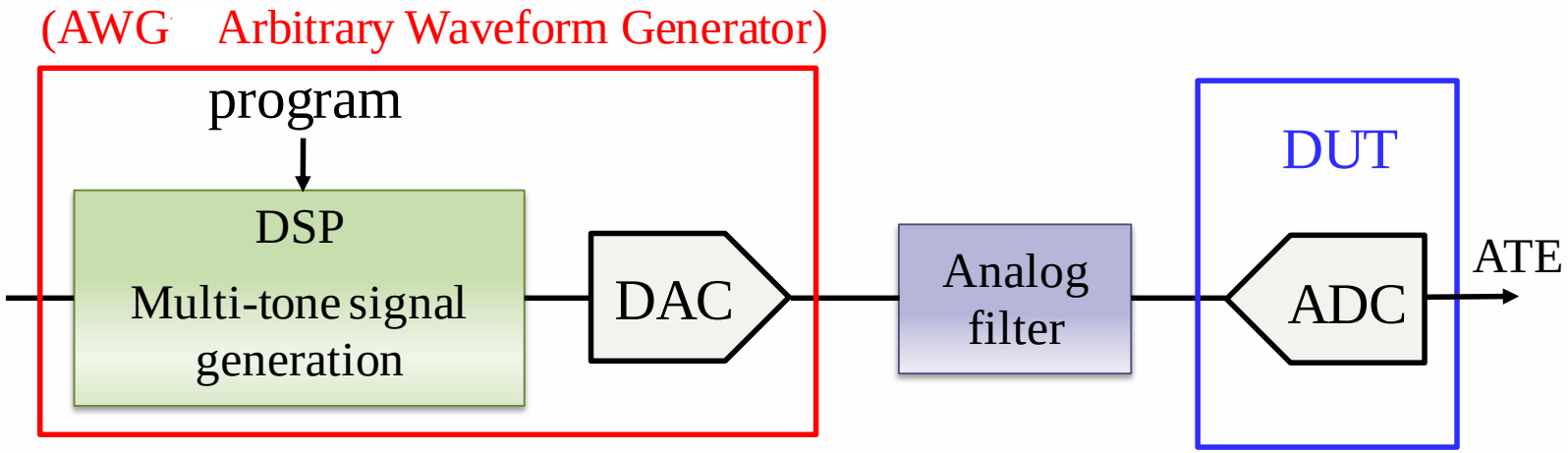
Input waveform



Corresponding histograms

Several cases

System for Generating Proposed Test Signal



- DSP synthesizes multi-tone signal.
- Analog filter eliminates their harmonics.

Histogram for the middle of ADC input range is high.

Effectiveness of Proposed Method

Example: 12bit 100kS/s SAR ADC

Conventional method: testing time =1780 msec

Reduction **by half** by the proposed method

Table: ADC Testing Time with ATE

	Content	Time
1)	Setup time for module	less than 1 msec
2)	Settling time for module and DUT	several msec
3)	DC linearity testing time	$2^{bit} \times (16 \sim 64) \times$ (ADC conversion time)
4)	SINAD testing time	$2^{bit} \times (1 \sim 4) \times$ (ADC conversion time)
5)	Time for data transfer and operation	several msec
6)	Other test time	several msec

Research Topics 2

High-Resolution High-Linearity

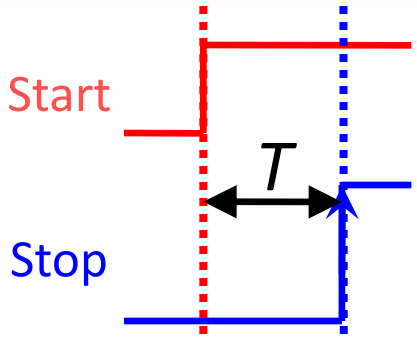
Time-to-Digital Converter (TDC)

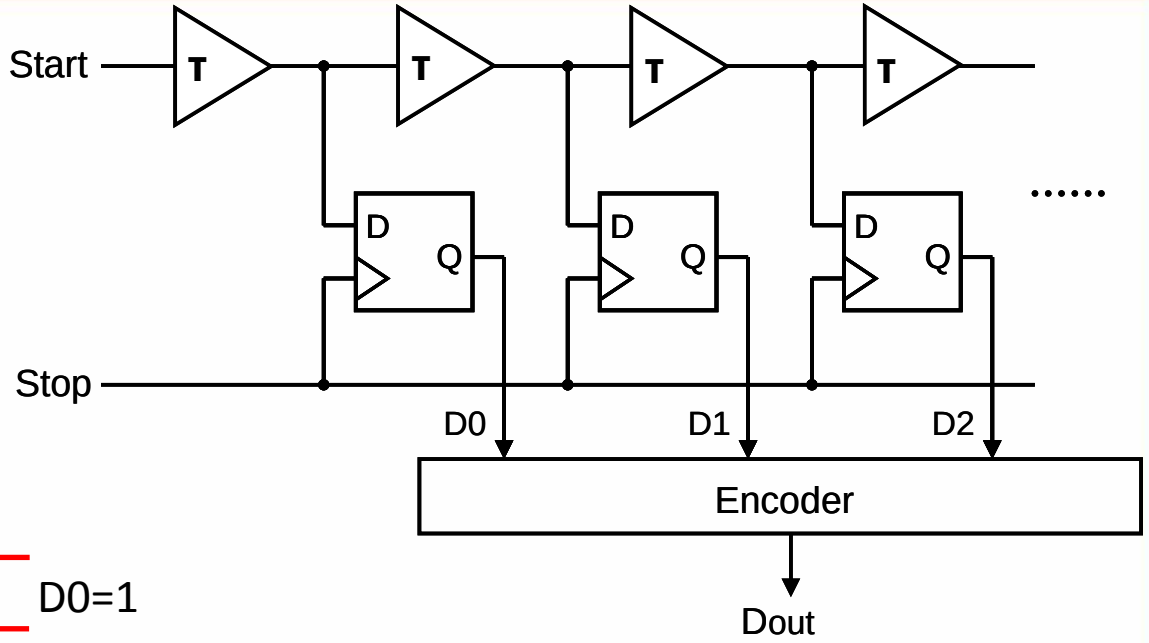
for Jitter Measurement BIST, digital sensor interfaces.

TDC is a key component as analog BIST.

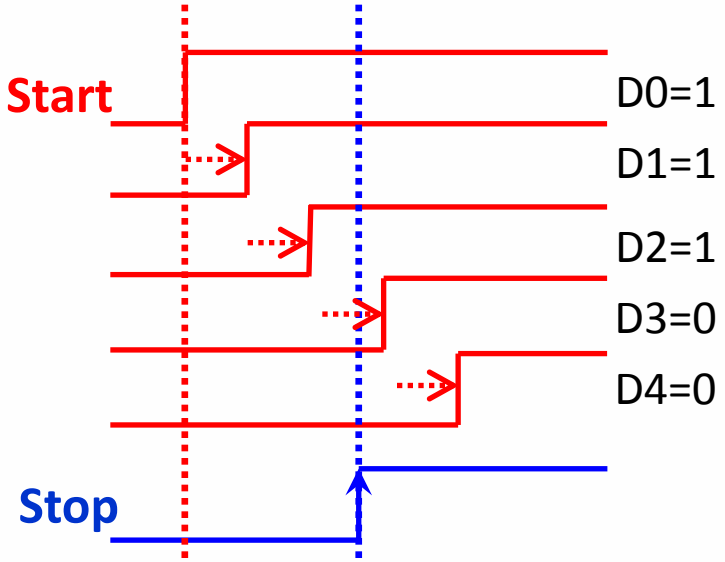
Ref. [3] S. Ito, et. al.,
Stochastic TDC Architecture with Self-Calibration,
IEEE APCCAS (Dec. 2010)

Basic TDC architecture





Timing chart



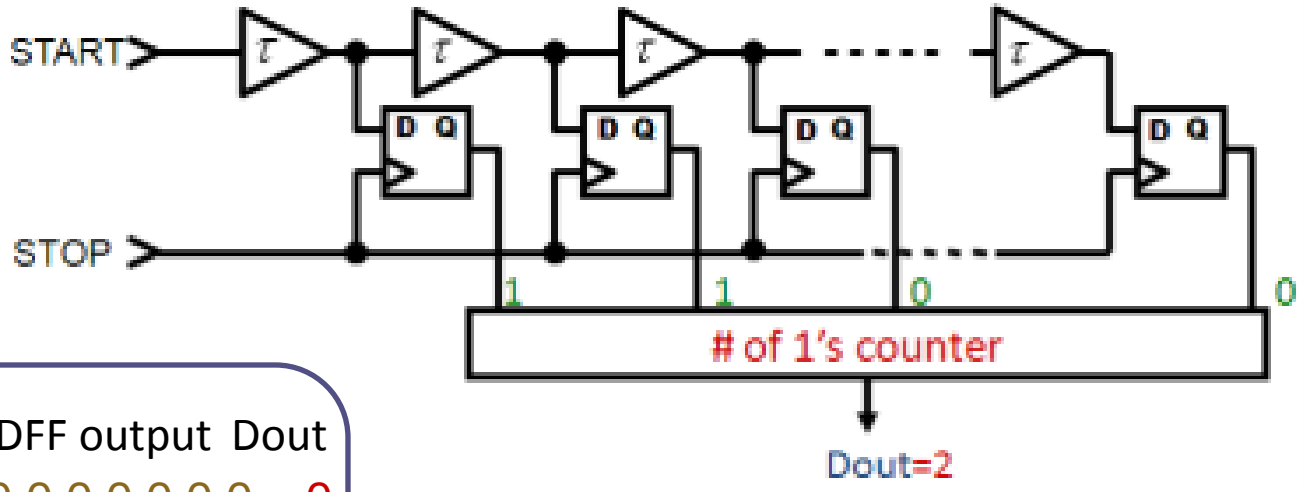
Encoder

Thermometer code

⇩

binary code

Bubble Error Compensation

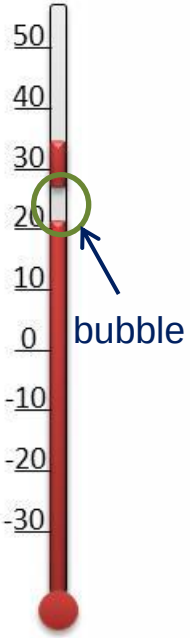


DFF output	Dout
0 0 0 0 0 0 0 0	0
1 0 0 0 0 0 0 0	1
1 1 0 0 0 0 0 0	2
1 1 1 0 0 0 0 0	3
1 1 1 1 0 0 0 0	4
1 1 1 1 1 0 0 0	5
1 1 1 1 1 1 0 0	6
1 1 1 1 1 1 1 0	7
1 1 1 1 1 1 1 1	8

DFF offset, buffer delay mismatch

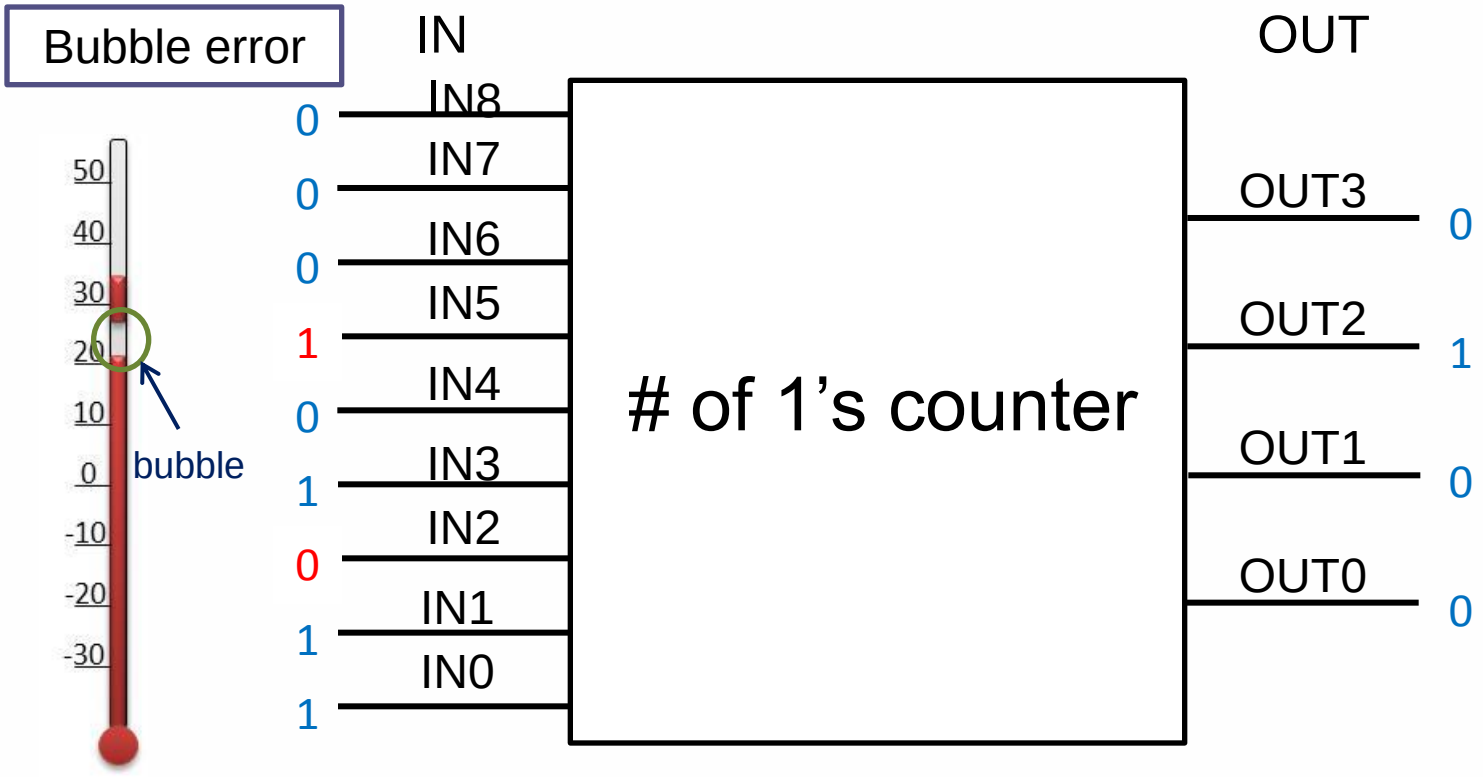
bubble error

1 0 1 0 0 0 0 0	2
1 1 1 0 0 0 0 0	3
1 1 1 0 1 0 0 0	4
1 1 1 0 1 0 1 0	5
1 1 1 0 1 0 1 1	6



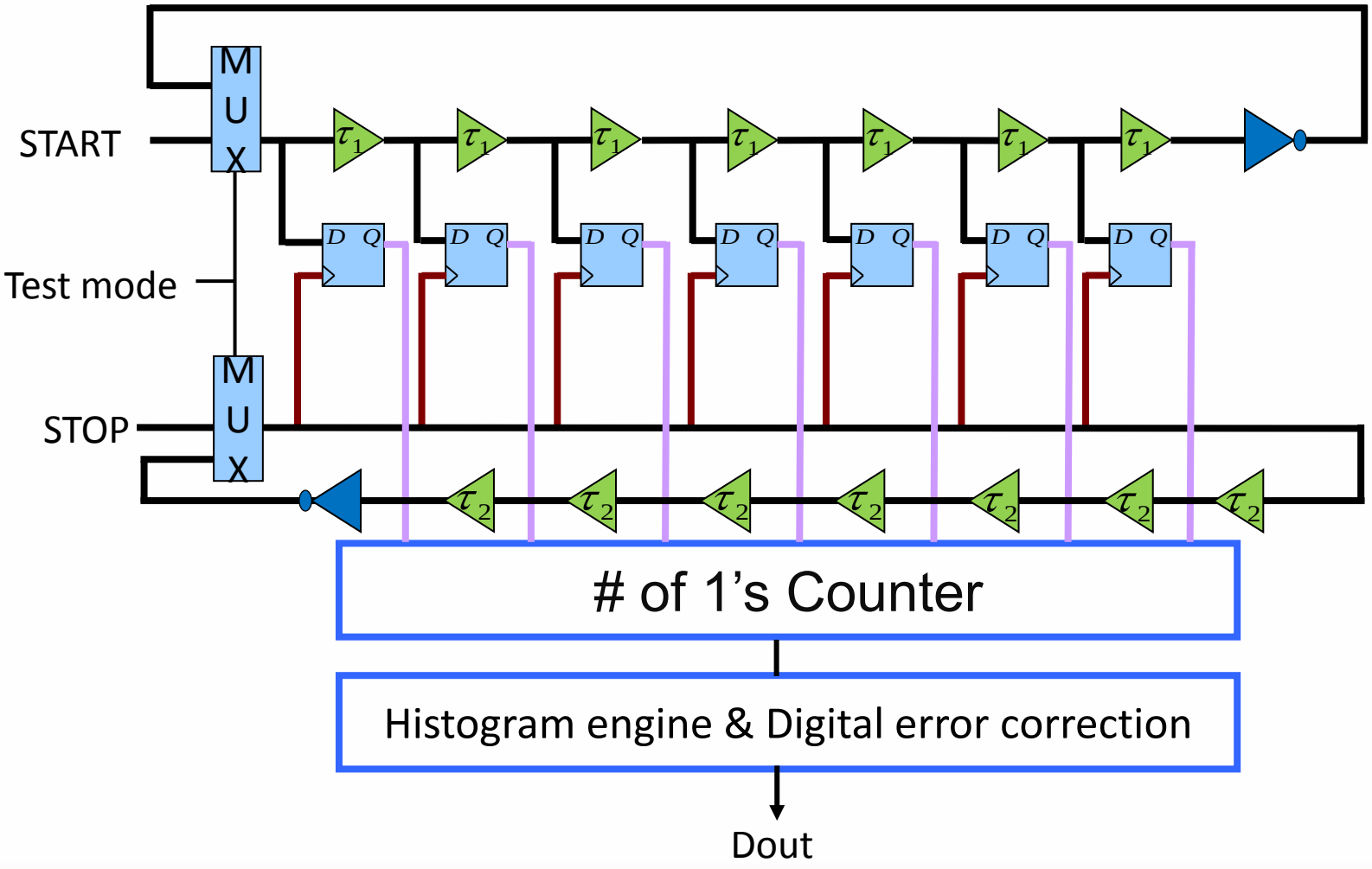
thermometer

Encoder Counts # of 1's from DFF Outputs

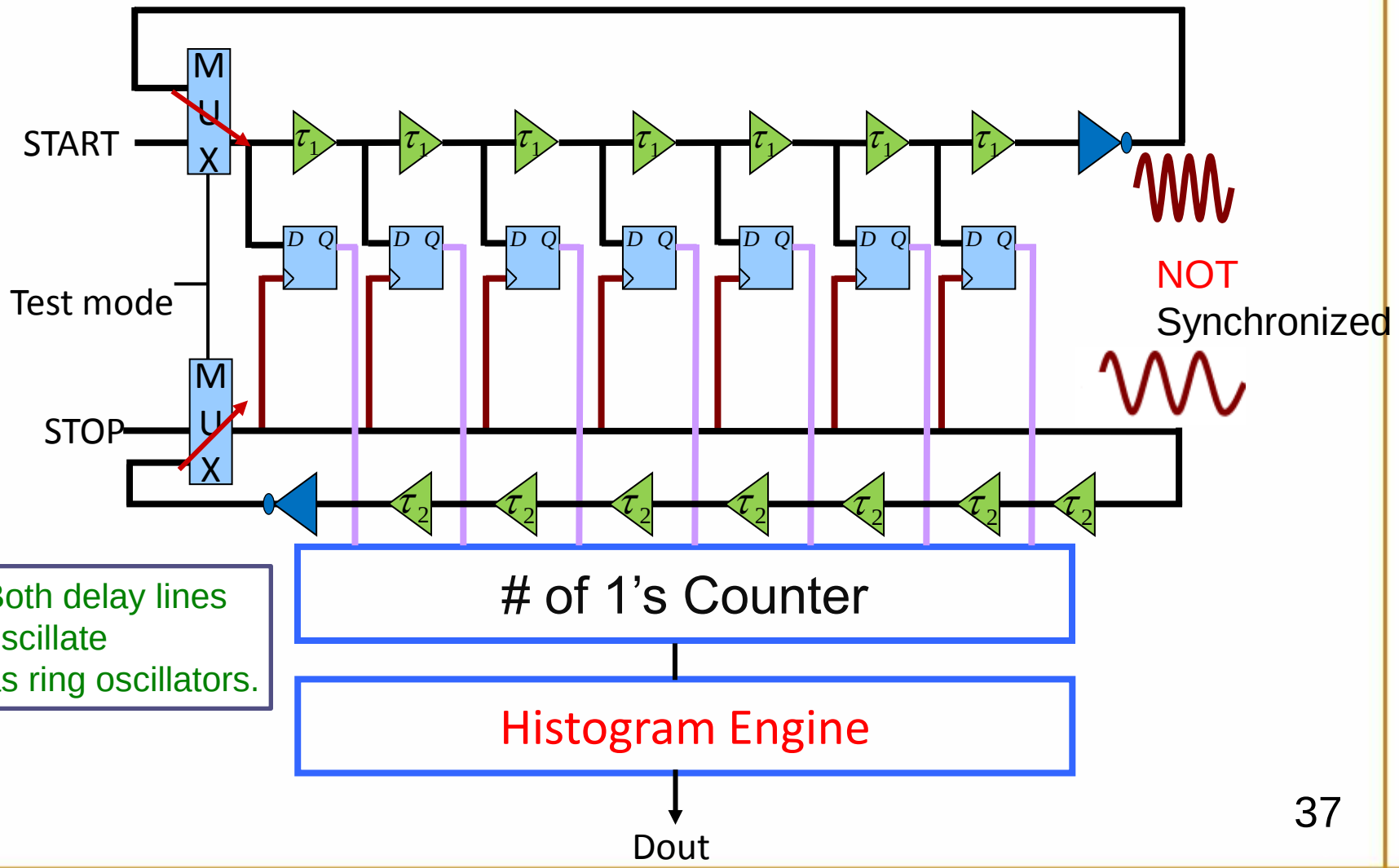


Bubble error effects are suppressed.

Proposed TDC Architecture with Self-Calibration

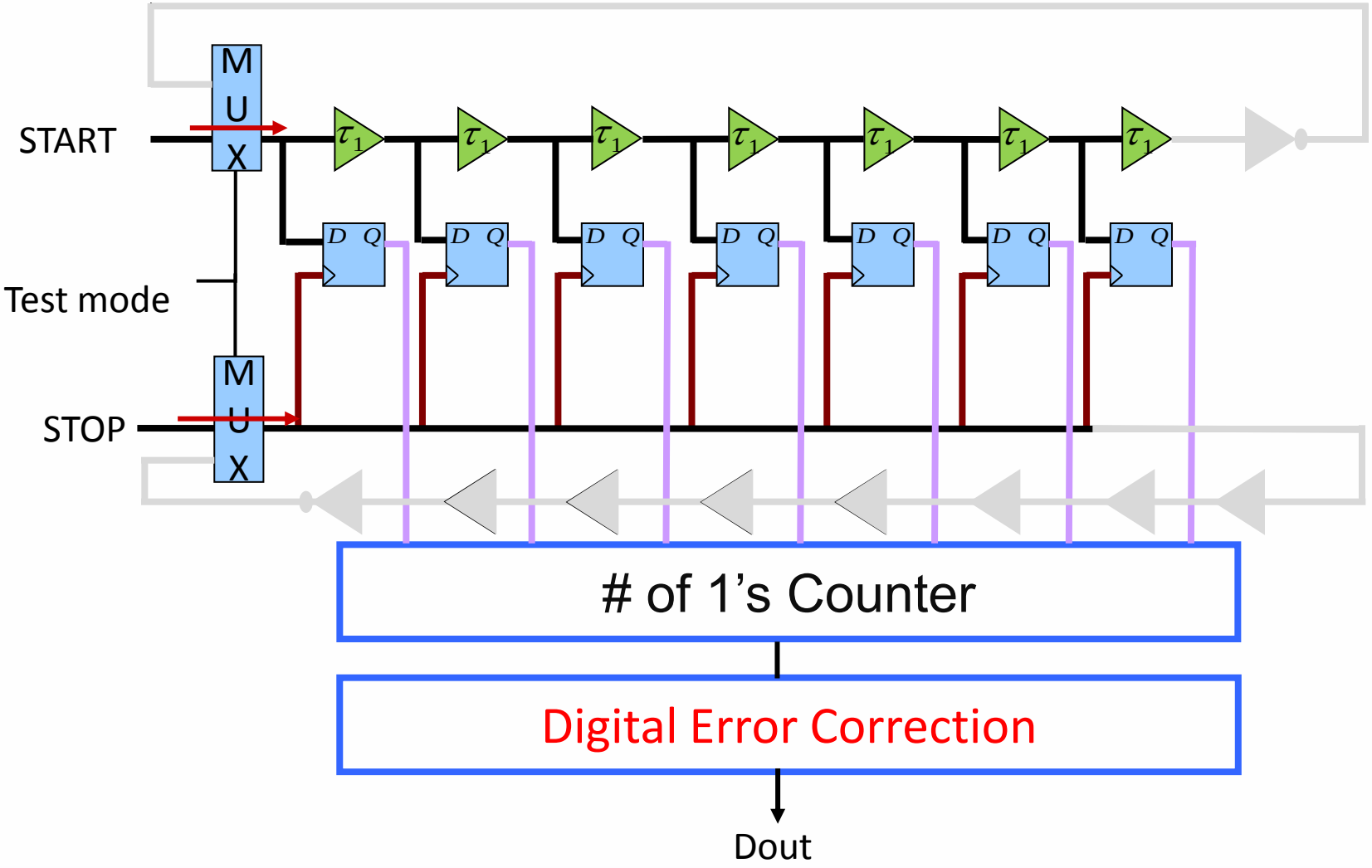


Self-Calibration Mode

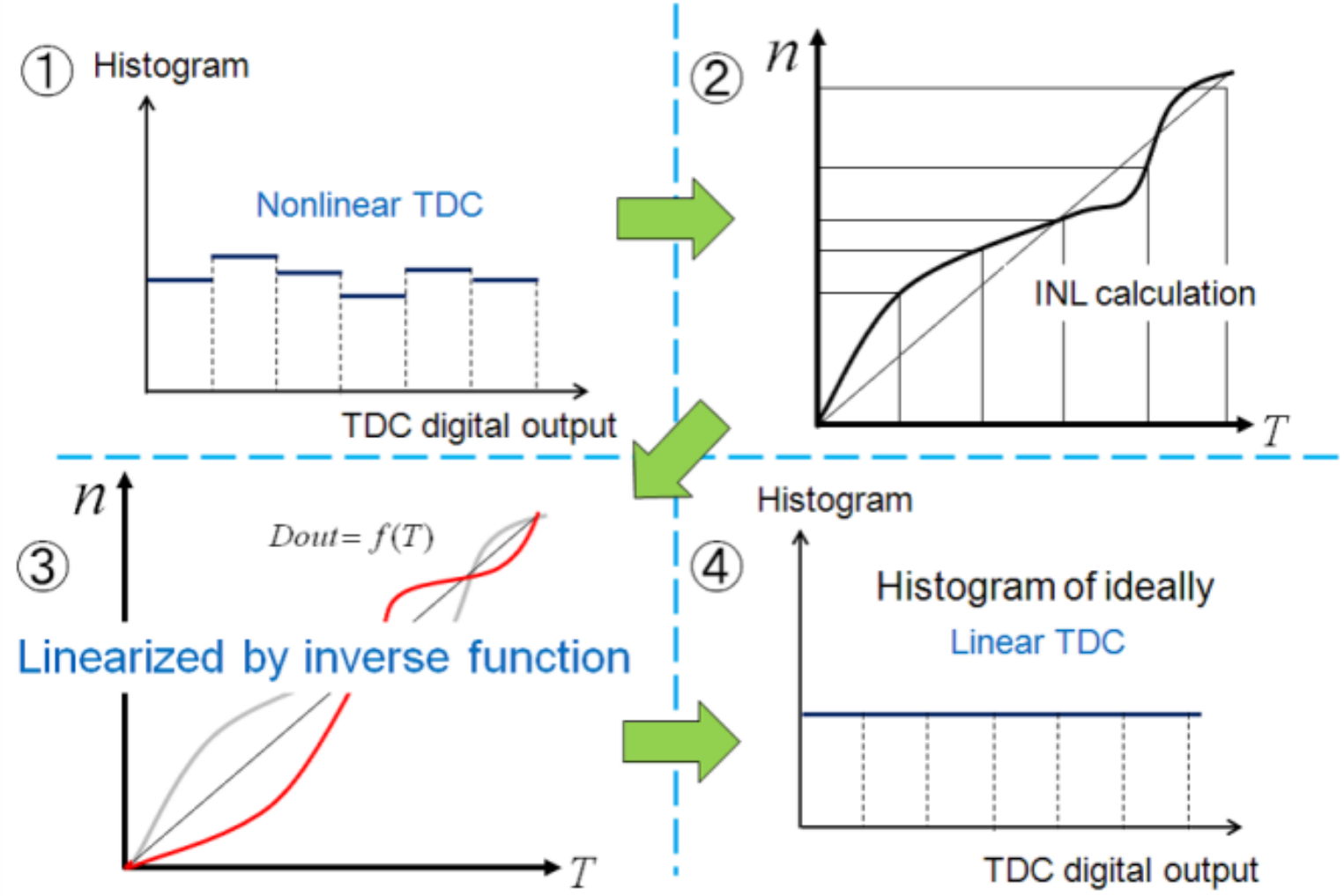


Both delay lines oscillate as ring oscillators.

Normal Operation Mode

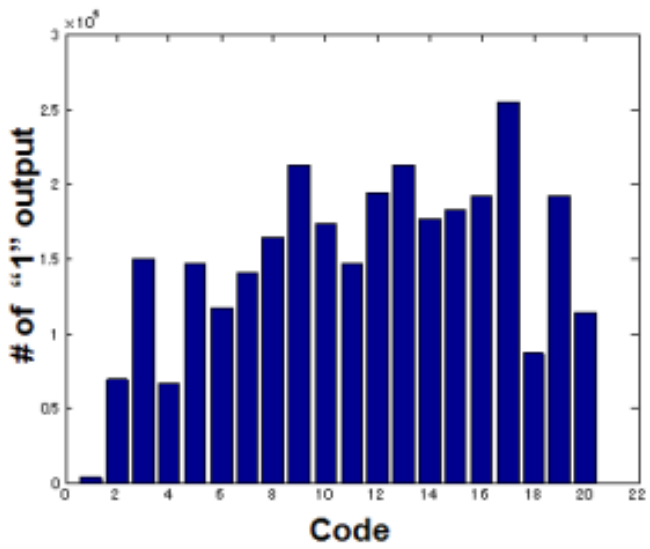


Principle of Self-Calibration

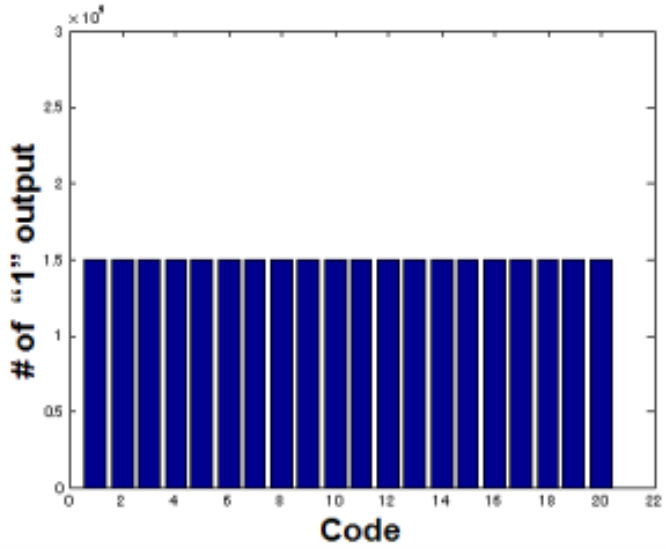


Simulation Result of Self-Calibration

Histogram for each bin is the same when the TDC is linear.

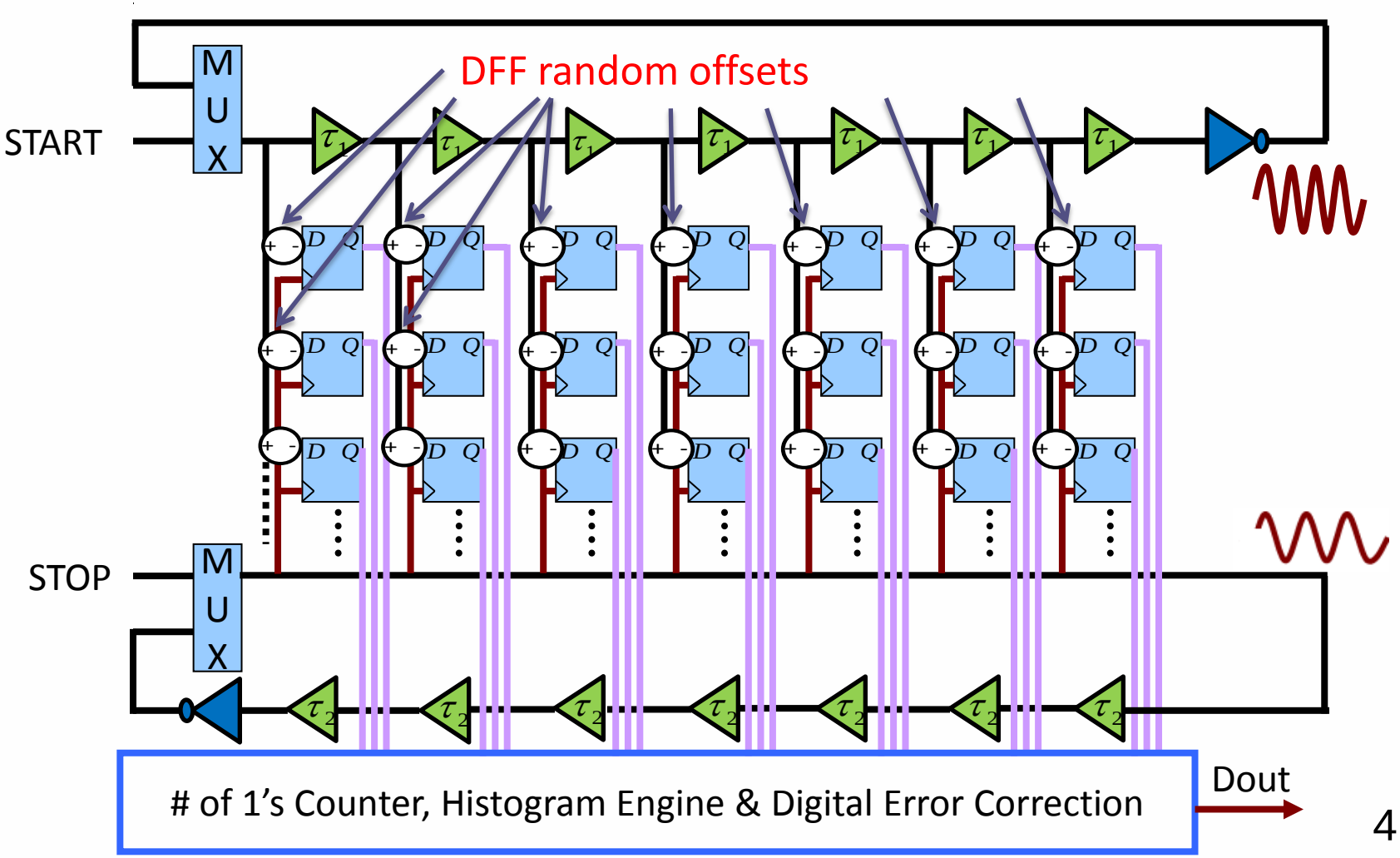


before calibration

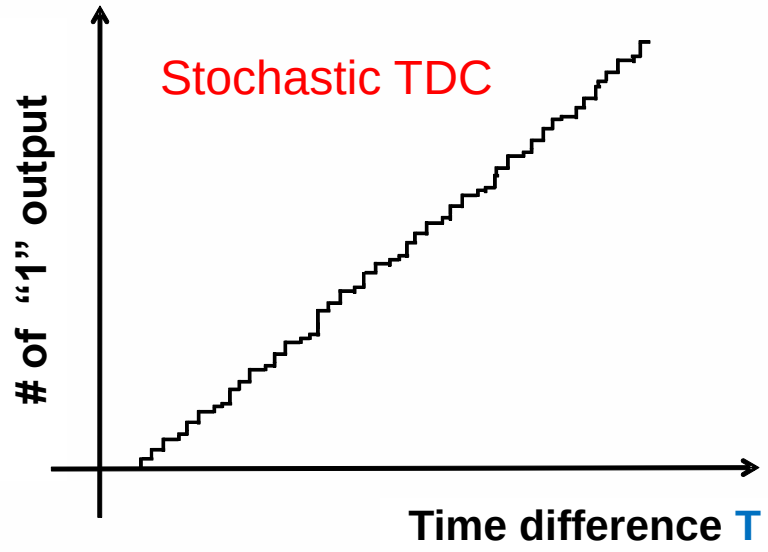


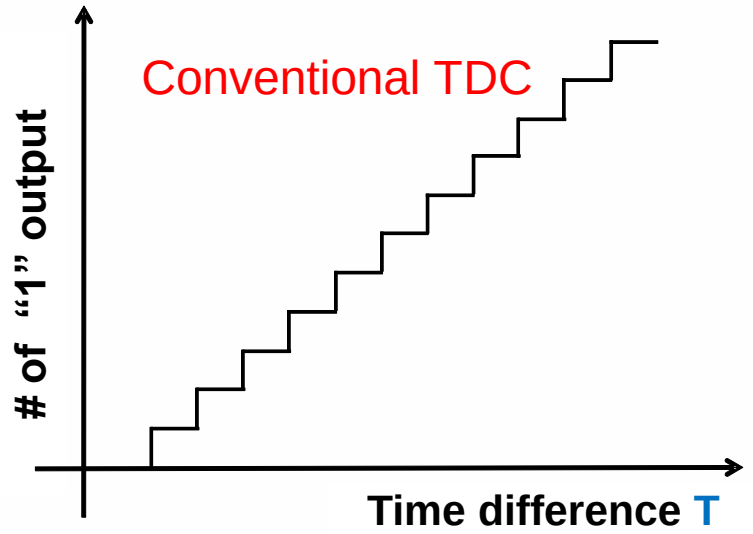
after calibration

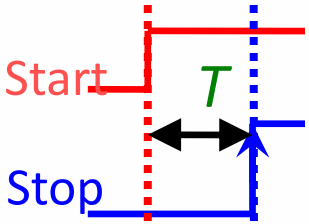
Stochastic TDC for Fine Time Resolution



Fine Time Resolution of Stochastic TDC



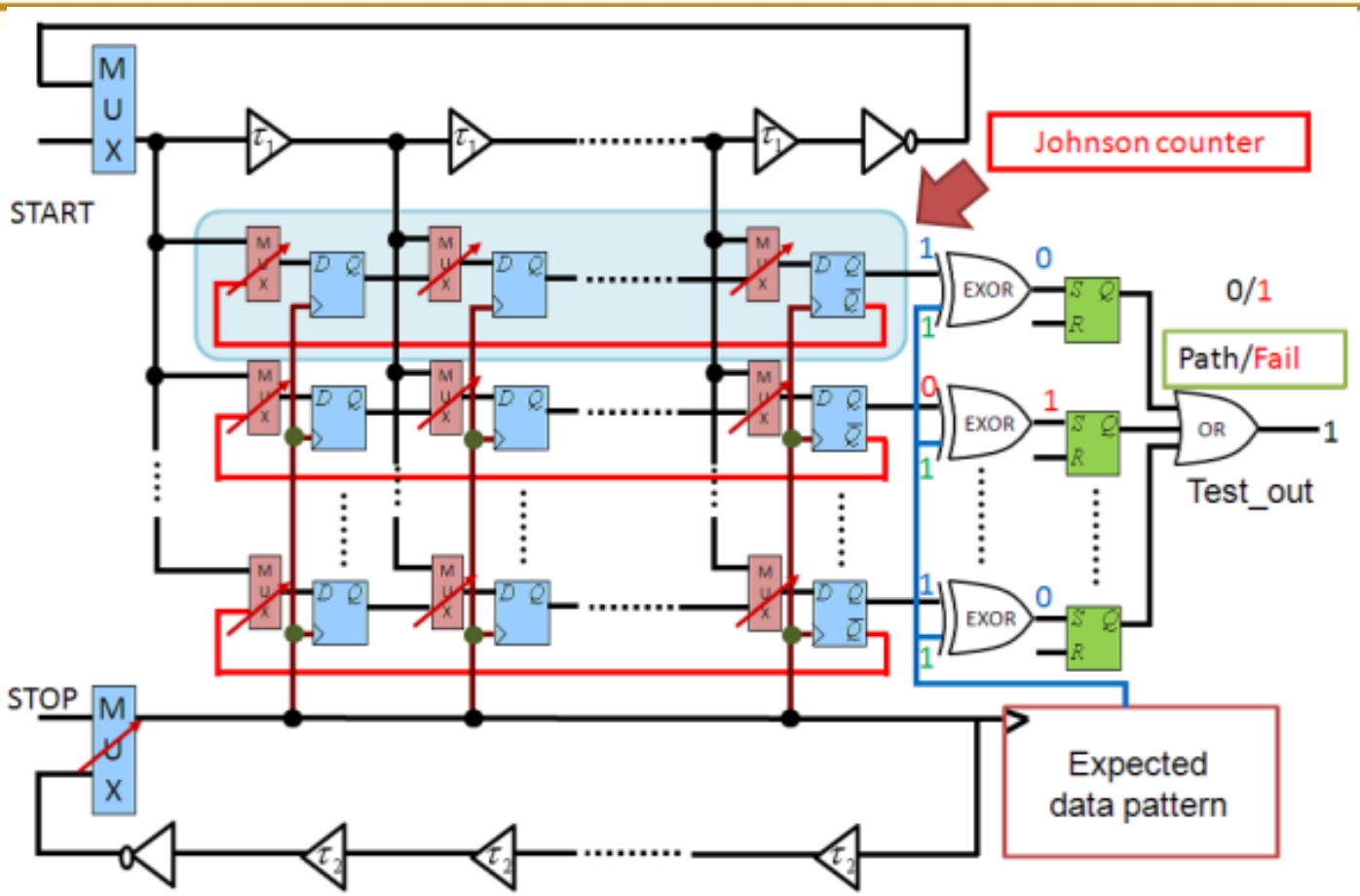




- Encoder (# of 1's counter) and self-calibration make the stochastic TDC practical.

Self-Testing Function

Important for automotive applications



All flip-flops are reset.
Then, Johnson counter configuration starts self-testing.

Research for Future Mixed-Signal SOC Architecture

- Self-Calibration
- Self-Testing
- Self-Diagnosis
- Self-Repairing

Self-Completed Mixed-Signal SOC

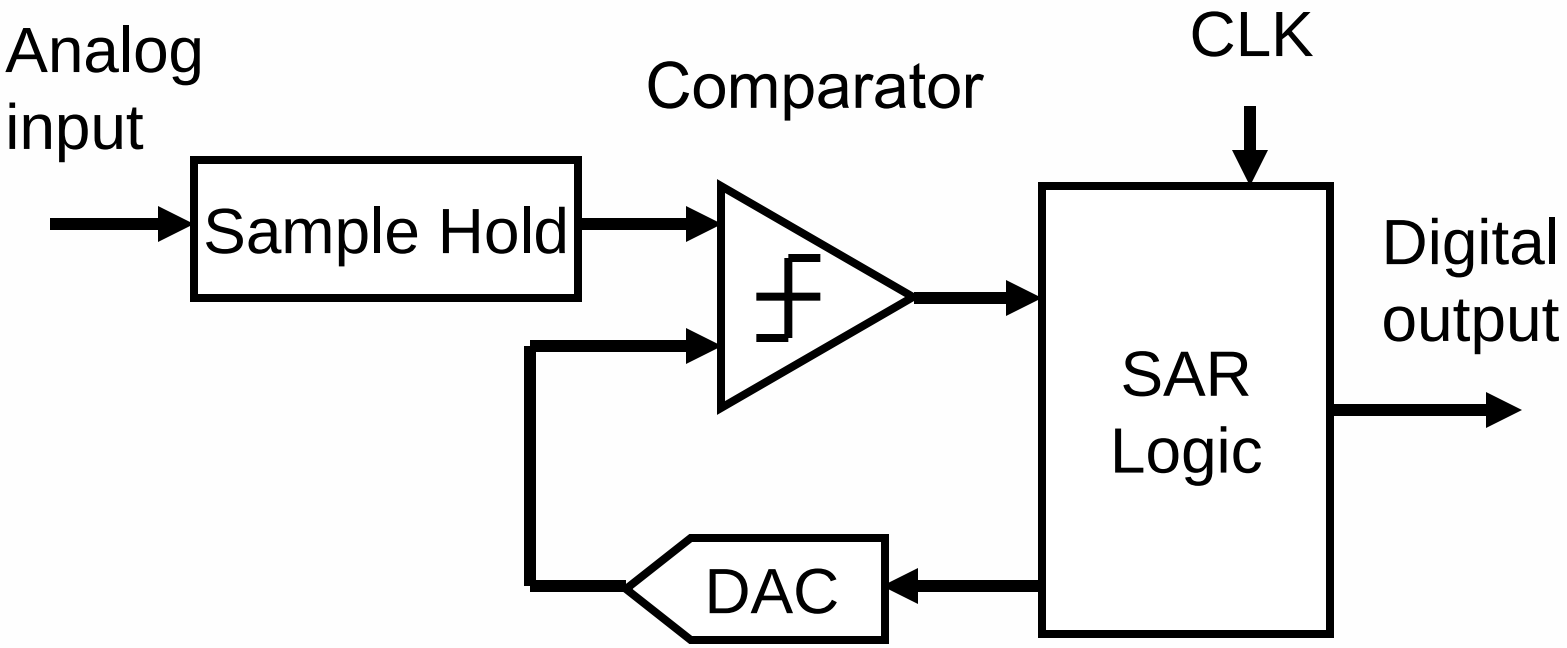
Research Topics 3

Optimization of the trade-off between the sampling speed and power of an SAR ADC at production testing.

Ref. [4] T. Ogawa, et. al., “SAR ADC That is Configurable to Optimize Yield”, IEEE APCCAS (Dec. 2010)

SAR ADC Yield Enhancement

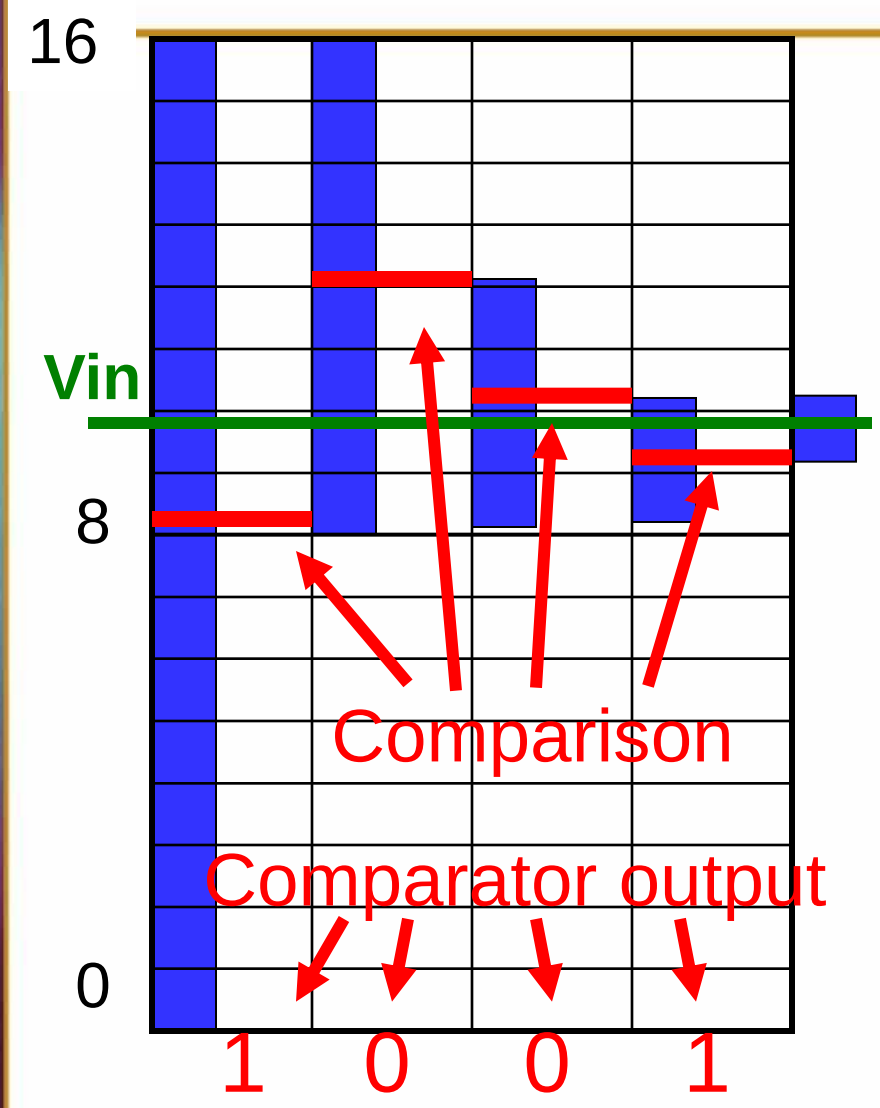
SAR ADC Block



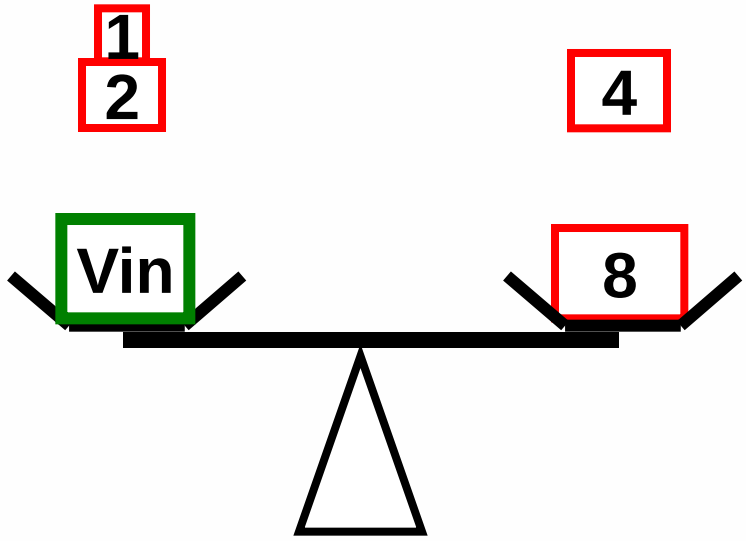
SAR ADC is digital centric.

→ Suitable for fine CMOS implementation.

Binary Search Algorithm

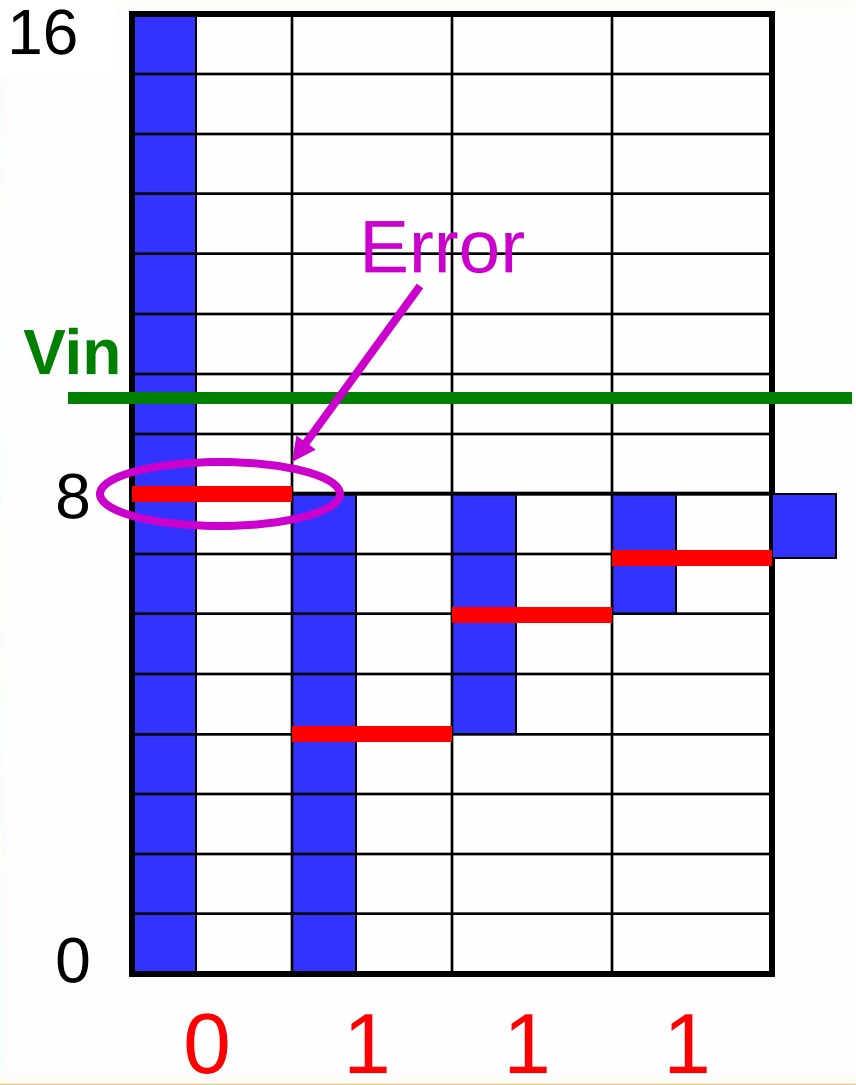


"Principle of a balance"



Vin = 4 + 8 − 1 + 2 = 9

Problem of Binary Search Algorithm

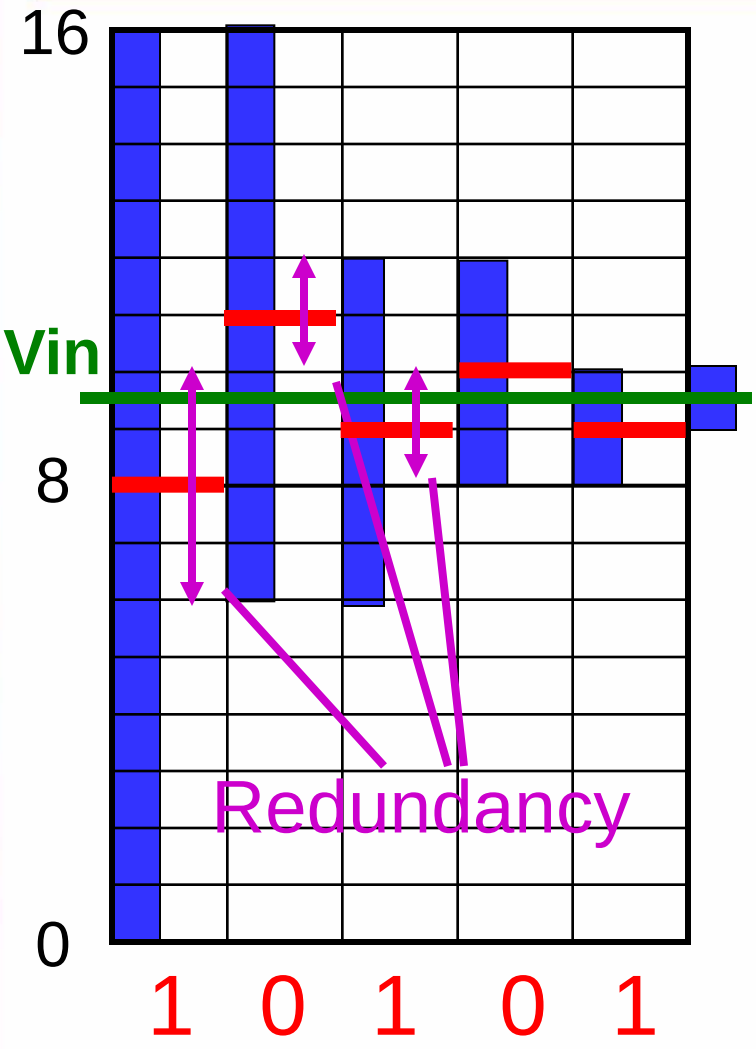


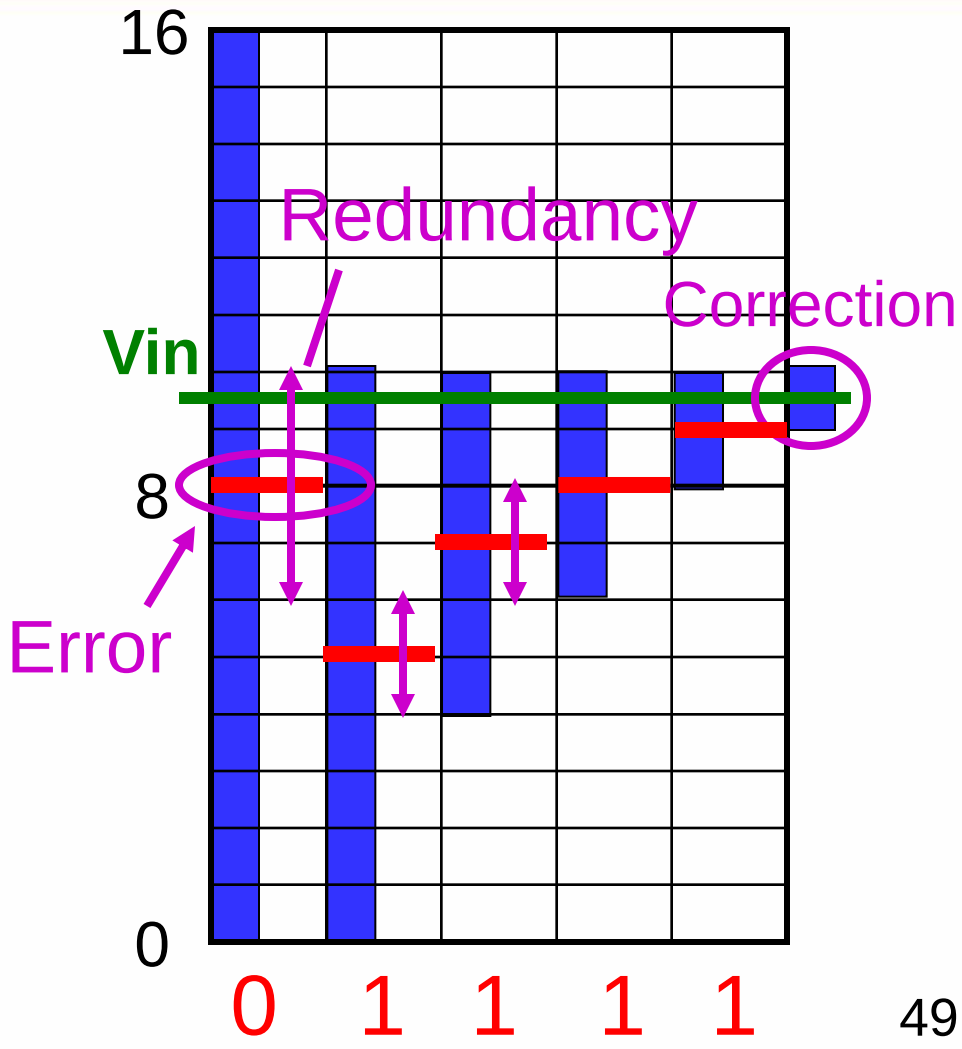
No redundancy

Search result has error.

Digital output has error.

Non-binary Search Algorithm





Non-binary Search Algorithm

Binary search algorithm(4-bit 4-step)

$$Dout = 2^3 + 2^2 \cdot d_1 + 2 \cdot d_2 + 1 \cdot d_3 + 0.5 \cdot d_4 - 0.5$$

Binary (Radix :2)

Non-binary search algorithm (4-bit 5-step)

$$Dout = 2^3 + \gamma^3 \cdot d_1 + \gamma^2 \cdot d_2 + \gamma \cdot d_3 + 1 \cdot d_4 + 0.5 \cdot d_5 - 0.5$$

Radix : γ

$$\gamma = 2^{\frac{3}{4}}$$

d_k : +1 or -1

Principle of Error Correction

Binary search algorithm

Comparator output : **1 0 0 1** ← Only one

Dout = 8 + 4 – 2 – 1 + 0.5 – 0.5 = 9

Non-binary search algorithm

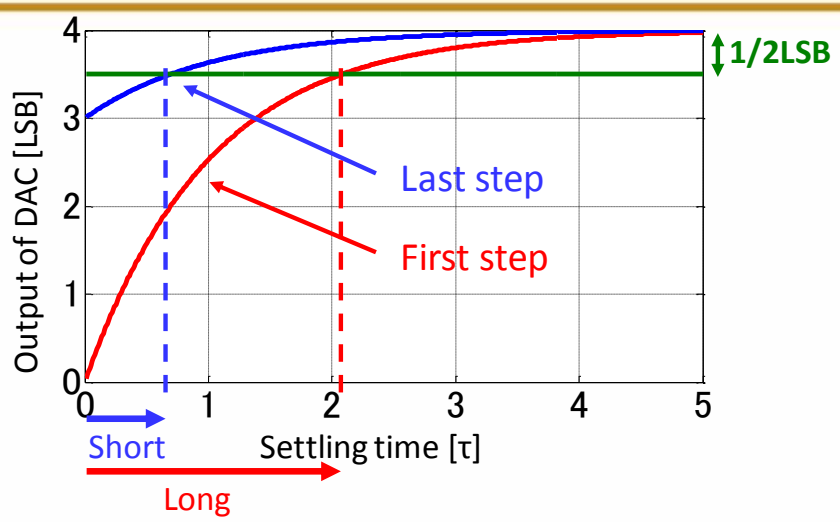
Comparator output : **1 0 1 0 1** ← Multiple

Dout = 8 + 3 – 2 + 1 – 1 + 0.5 – 0.5 = 9

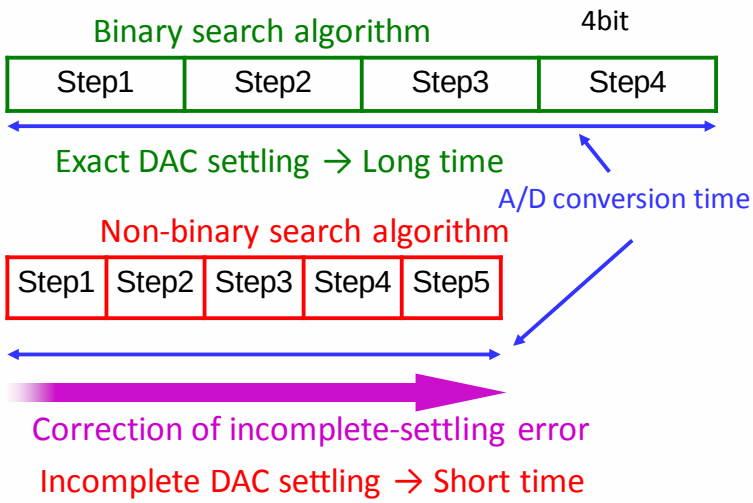
Comparator output : **0 1 1 1 1**

Dout = 8 – 3 + 2 + 1 + 1 + 0.5 – 0.5 = 9

Non-binary SAR ADC is faster



Settling of the DAC output
to generate a reference voltage
at each stage.



Non-binary SAR ADC
can be faster
If DAC settling is considered.

Basic Idea
Example: 10MS/s 10bit SAR ADC

Fast chip

Estimated DAC time constant

τ=3.5ns

SA Algorithm

10-bit 11-step

Low power

due to 11 steps

Slow chip

Estimated DAC time constant

τ =4.5ns

SA Algorithm

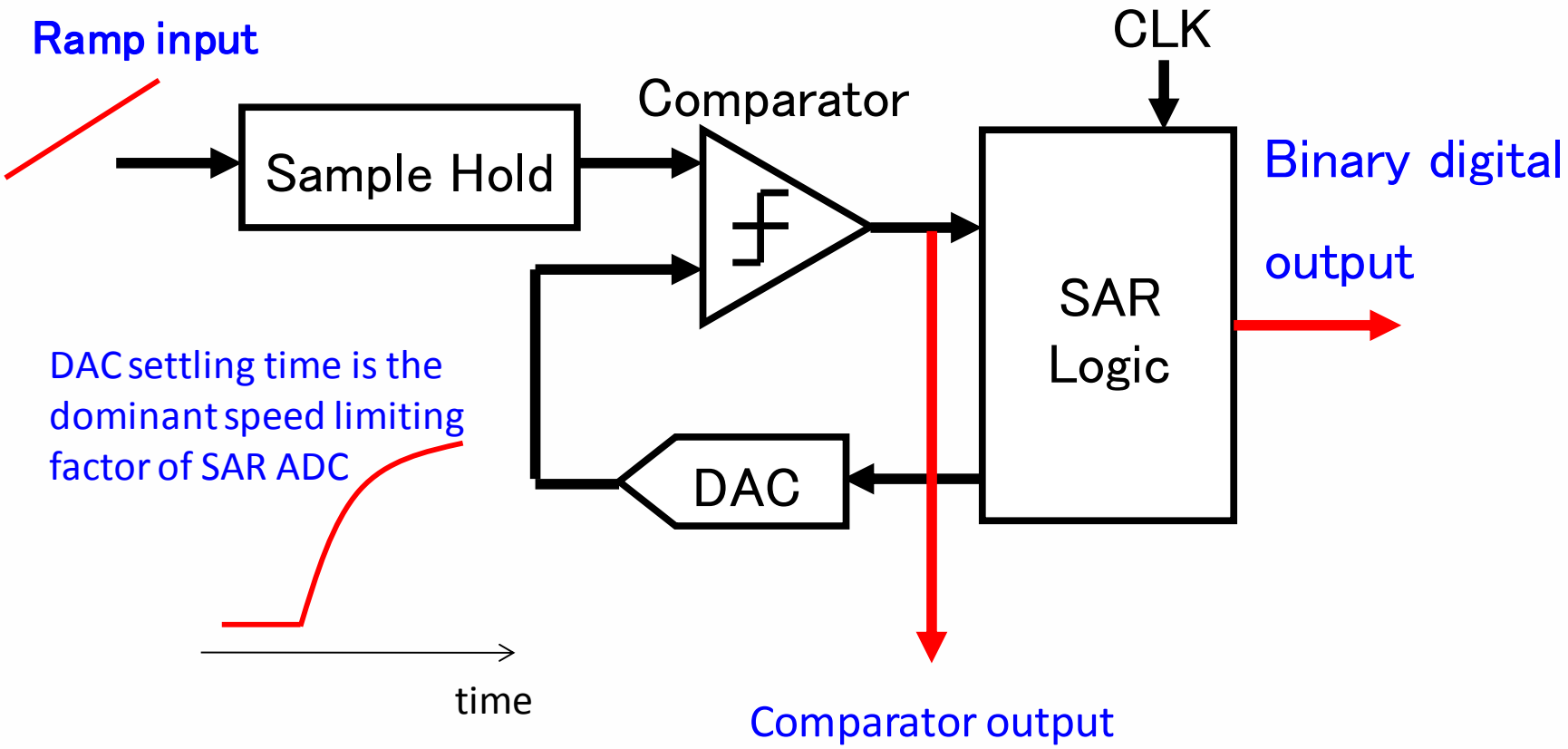
10bit 13-step

Power increases

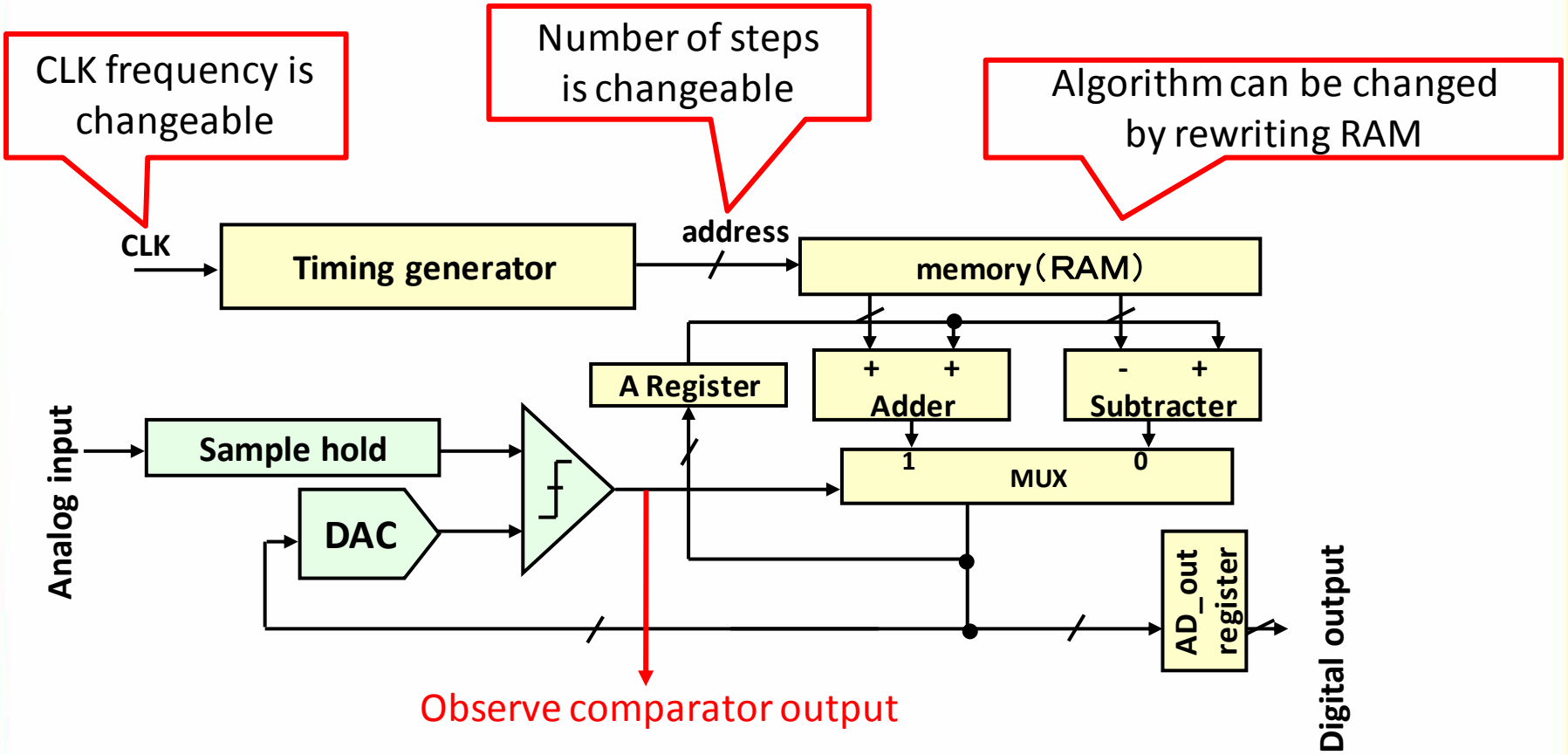
due to 13 steps

Both chips can meet the spec. of 10MS/s

Interface of Reconfigurable Non-Binary SAR ADC



Block Diagram of Reconfigurable Non-binary SAR ADC

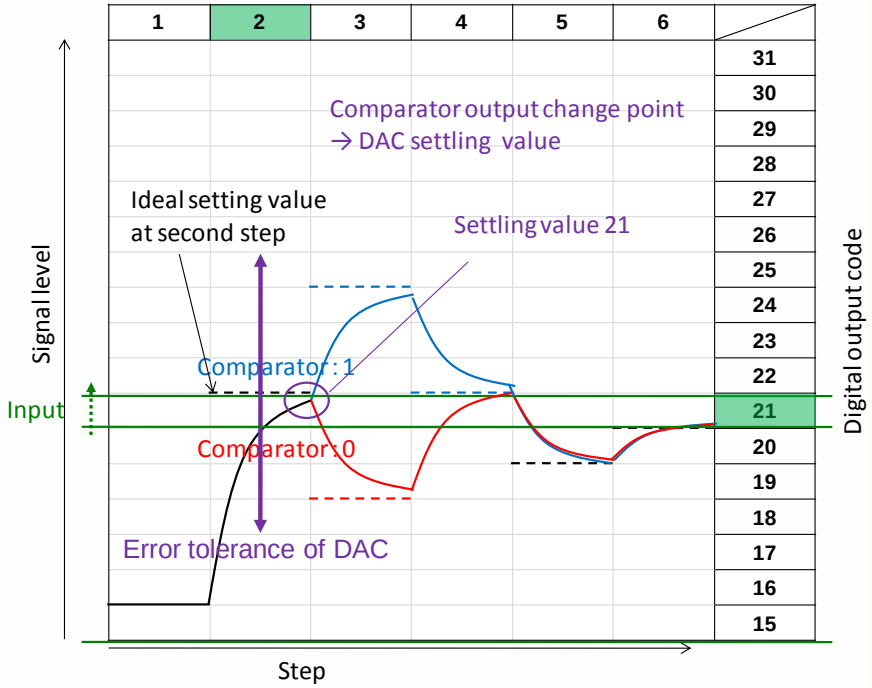


DAC Settling Time Estimation Algorithm

step →

1	2	3	4	5	6	7	8	9	10	11	12	ADC output
1	1	0	0	0	0						0	734
1	1	0	0	0	0						0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	1	0	0	734
1	1	0	0	0	0	0	1	1	0	1	1	733
1	1	0	0	0	0	0	1	1	0	1	1	**733**
1	0	1	1	0	1	0	1	0	0	1	1	**733**
1	0	1	1	0	1	0	1	0	0	1	1	733
1	0	1	1	0	1	0	1	0	0	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	1	0	732
1	0	1	1	0	1	0	0	1	1	0	1	731
1	0	1	1	0	1	0	0	1	1	0	1	731

Comparator output

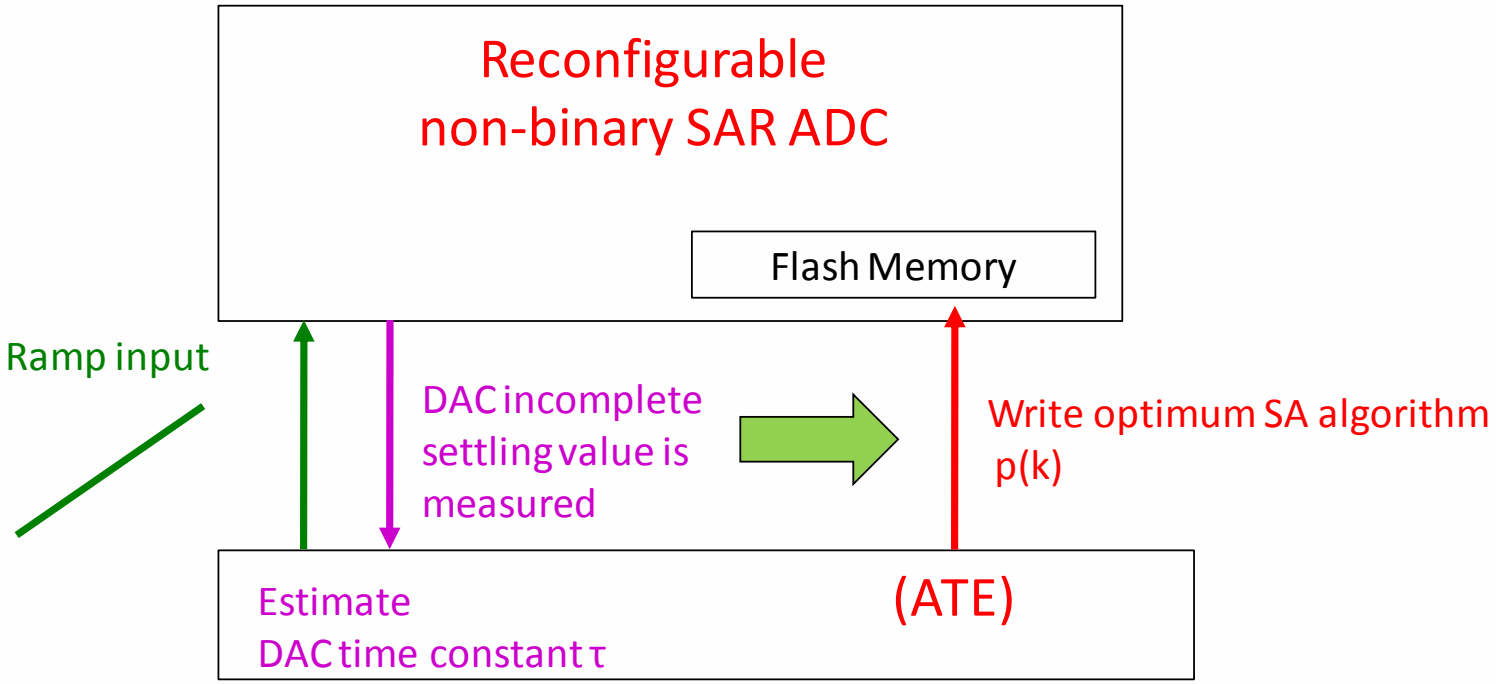


Comparator output pattern ➡ DAC output waveform

can estimate DAC time constant **T**

Reconfiguration of Non-binary SAR ADC

Cooperation with ATE

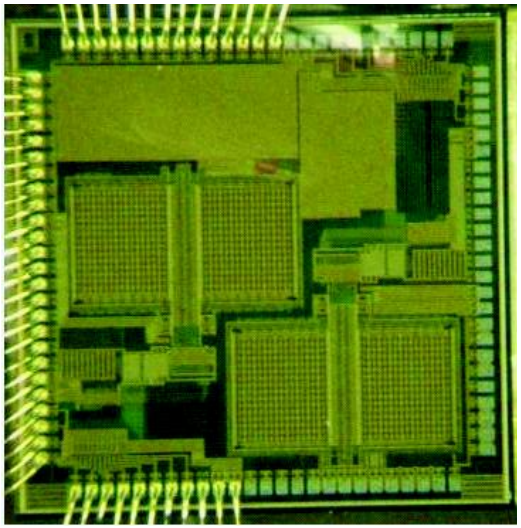


τ is large (slow process) → Satisfy speed spec. with large M

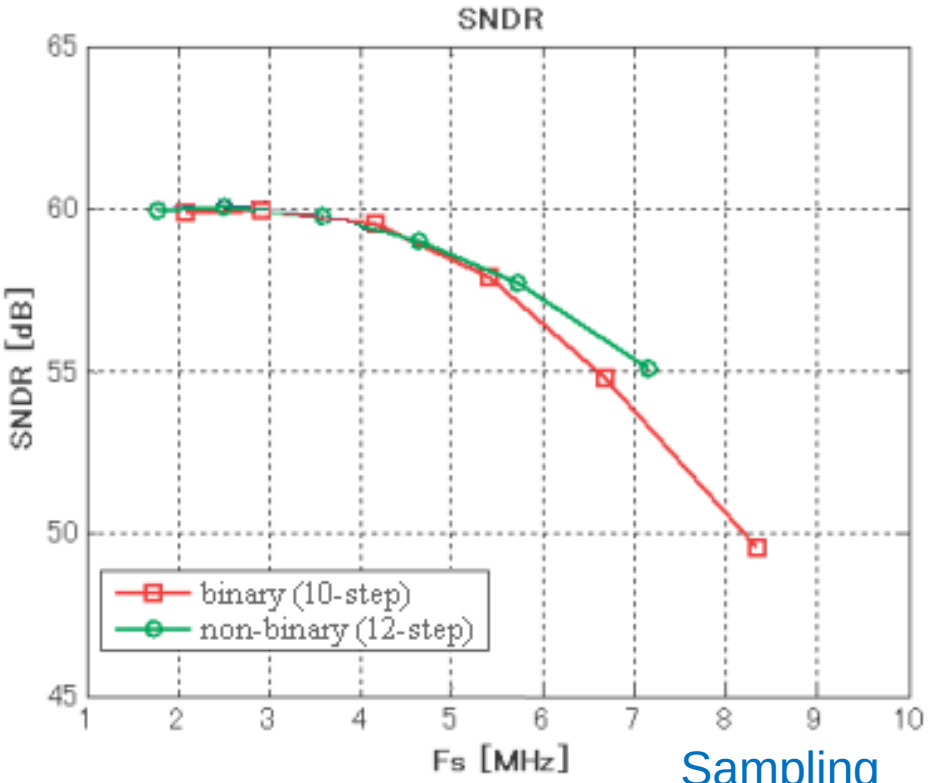
τ is small (fast process) → Decrease power with small M

M: number of SA steps

Reconfigurable Non-Binary SAR ADC Implementation and Measurement Results



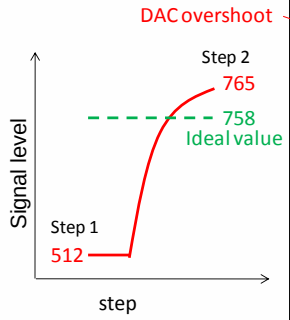
0.18um CMOS
2.5mm x 2.5mm
with two SAR ADCs



Sampling frequency

SNDR comparison of
10-step (binary) and 12-step (non-binary)

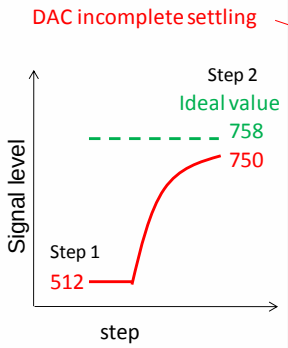
Measurement Result of 10bit 12step SAR ADC



step1	step2	step3	step4	Comparator opinion
Ideal:512	Ideal:758 Estimate:765	Ideal:871 Estimate:876	Ideal:936 Estimate:939	1111
			Ideal:806 Estimate:809	1110
		Ideal:645 Estimate:647	Ideal:710 Estimate:712	1101
			Ideal:580 Estimate:580	1100
	Ideal:266 Estimate:258	Ideal:379 Estimate:377	Ideal:444 Estimate:443	1011
			Ideal:314 Estimate:311	1010
		Ideal:153 Estimate:146	Ideal:218 Estimate:214	1001
			Ideal:88 Estimate:84	1000

DAC output waveform estimation

DAC output ringing



step1	step2	step3	step4	Comparator opinion
Ideal:512 Estimate:511	Ideal:758 Estimate:750	Ideal:871 Estimate:864	Ideal:936 Estimate:931	1111
			Ideal:806 Estimate:802	1110
		Ideal:645 Estimate:642	Ideal:710 Estimate:707	1101
			Ideal:580 Estimate:579	1100
	Ideal:266 Estimate:273	Ideal:379 Estimate:381	Ideal:444 Estimate:444	1011
			Ideal:314 Estimate:315	1010
		Ideal:153 Estimate:160	Ideal:218 Estimate:221	1001
			Ideal:88 Estimate:92	1000

No ringing

Reconfigurable Chip

- Conventional reconfigurable chip
  - ➡ to meet different specifications.

- Proposed reconfigurable chip
  - ➡ to meet one specification (speed)
    - save chips with slow process
    - reduce power of chips with fast process

Contents

1. Introduction
2. Review of Analog Circuit Testing in Mixed-Signal SOC
3. Research Topics
4. Challenges & Conclusion

Challenges of Analog Testing

- Analog part testing is important for mixed-signal SOC cost reduction.
- Sense of balance between LSI testing cost and benefits is important.
- Solve the problems one by one. No general or systematic method.
- Analog BIST technique progress may be slow but it is steady.
- On-chip instrumentation will be must.
- Use engineering sense, as well as science

Challenges of Analog Testing

- Use all aspects of technologies
  - Circuit technique
  - Cooperation among BIST, BOST & ATE
  - Signal processing algorithm
  - Use resources in SOC

    such as μP core, memory, ADC/DAC

BOST:
Built-Out Self-Test

Especially utilization of powerful digital in SOC.

No royal road to analog testing

Gunma Univ. has been involved in this area collaborating with industry (STARC, Advantest, …)

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http://www.el.gunma-u.ac.jp/~kobaweb/

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