A Small, Low Power Boost Regulator Optimized for Energy Harvesting Applications

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***Abstract*—A small, low power bootstrapped boost regulator is introduced that can start up with an input voltage of 240mV and achieve a maximum efficiency of 96%. The effectiveness of this approach is shown through Spectre simulation results.**

I. Introduction

Recently there have been great advances in the realm of Energy Harvesting. Using vibrational, thermal, and solar transducers, small amounts of power can be captured by latent energy sources [1]–[8]. While previous works have shown that capturing power from these micro-power sources is feasable, each approach has drawbacks. Some approaches require an external battery [1] or a storage capacitor [2] with a voltage of several volts to bias the control circuitry. Others have designed their circuits with external bias circuitry [3] or require a mechanical switch in order to start up the converter [4]. Furthermore, previous works also are not suitable to drive realistic loads, as their maximum load capability is in the μW range [1]–[6]. In real-world applications, where energy harvesters are used in hard-to-reach places, it would be impractical to replace the batteries used in these energy harvesting systems. Additionally, since a typical low-power microcontroller requires several mW of power to operate, conventional circuits are unsuitable for real-world applications.

In order to address these issues, we have created a low-power boost circuit that is only operational when its input source is large enough to bootstrap the system. Our circuit is also optimized to provide several mW of power, which would be suitable to drive a low-power Micro-Controller Unit (MCU). Additionally, as previous papers only briefly mention total system efficiency, our circuit is designed to maximize efficiency, which, in a real-world application, would increase the maximum amount of energy that is available to the load.

This paper introduces a regulator that is able to start up with an input voltage of 240mV, and can supply up to 6.6mW of power with a maximum efficiency of 96%. With our approach, these results are achieved with only 3 external components—an input capacitor, an output capacitor, and an inductor. The feasibility of our approach is shown with Spectre simulation results.

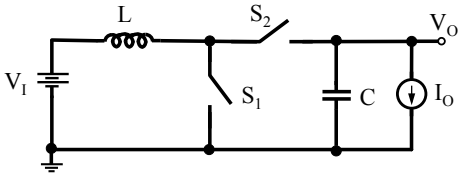


Fig. 1. Ideal synchronous boost converter.

II. Boost Regulator Principles

A. Ideal Boost Regulator Operation

A boost or step-up regulator is a commonly used DC-DC converter, whose output voltage is higher than the input voltage. Fig. 1 shows the schematic of an ideal synchronous boost converter, where the two switches S_1 and S_2 are switched out of phase with a fixed duty cycle D. When S_1 is on, current in inductor L increases linearly by the function $\Delta I/\Delta t = V_I/L$. Next, turning off S_1 (and hence turning on S_2) transfers the current built up in the inductor to the output capacitor and load. By operating this circuit at a constant D, it has been shown [9] that the steady state output voltage of the boost regulator is:

$$\frac{V_O}{V_I} = \frac{1}{1-D} \tag{1}$$

While (1) is a decent approximation, it suggests that at 100% duty cycle, the output voltage would rise to infinity. However, in this situation (i.e S_1 is always on), the current in the inductor would rise unencumbered until any component failed, never delivering its current to the output capacitor nor the output load, and hence the output voltage would be 0. Because of this effect, it is of paramount importance that switch S_1 turn off for some amount of time (and hence S_2 must turn on), guaranteeing that the output voltage will rise.

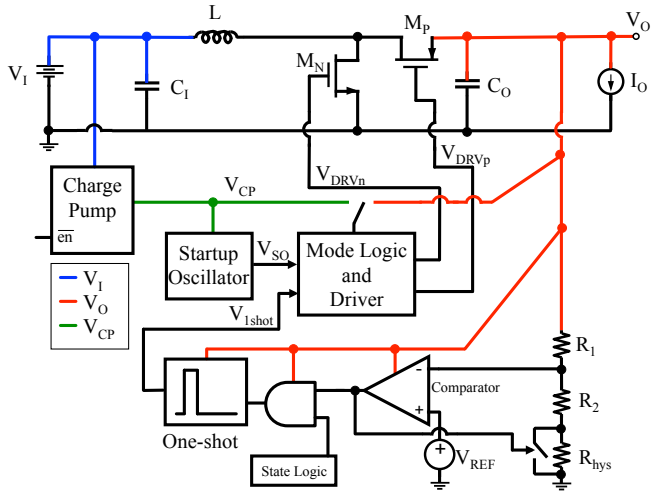


Fig. 2. Bootstrapped boost converter block diagram.

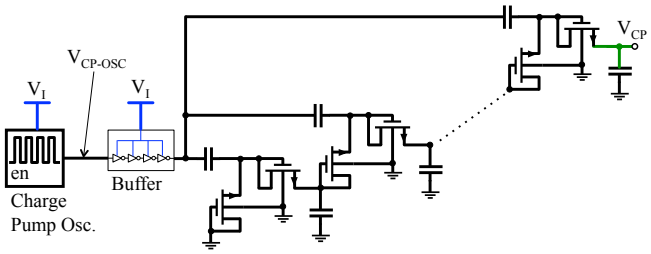


Fig. 4. Full charge pump schematic.

TABLE I
TRANSISTOR THRESHOLD VOLTAGE V_{t0}

Transistor Type	Model V_{t0}
Native NMOS	-0.02V
Low–V_t PMOS	-0.13V
Low–V_t NMOS	0.27V
Nominal–V_t PMOS	-0.44V
Nominal–V_t NMOS	0.44V

III. Proposed Circuit Operation

A. Block Diagram

A block diagram of the proposed circuit is shown in Fig. 2. The components L, M_N, M_P and C form the core of a basic boost converter, similar to that in Fig. 1. Since the output voltage V_O will be well regulated and larger than the input, it is suitable for supplying power to the internal control circuitry: namely the voltage loop comparator, one shot and voltage reference. In order to initially raise the output voltage however, we are using a charge pump circuit that can operate from a very low input voltage, which will be described in Section III-B. The output of this charge pump is then fed to a fixed-frequency startup oscillator and to the main drivers that commutate the switches and raise the output voltage to bias the internal circuitry. Once the output voltage has reached an acceptable level, the charge pump and startup oscillator are stopped, and the driver power source switches to the output voltage. When this handoff is complete, the circuit begins running in a constant-on-time hysteretic mode, as described in Section III-D. The input voltage V_I, output voltage V_O and charge pump output voltage V_{CP} are highlighted in different colors to help easily understand the voltage domains present in the proposed circuit.

B. Startup Charge Pump

The proposed circuit is being designed in a 0.18μm CMOS process that supports NMOS native–V_t and low–V_t transistors (threshold voltages for all available 1.8V transistors are shown in Table I). In order to reduce leakage current however, nominal V_t devices are used as the output drivers and switches. Because the threshold voltage of the nominal devices is greater than 400mV, an on-chip charge pump is used to ensure that the system can operate with V_I less than the switch threshold voltage. Fig. 3 shows the oscillator used to operate the charge pump circuit. By using low-Vt transistors and a 20fF capacitor, this circuit operates at 40MHz with an input voltage of 300mV. Since the charge pump is only used during the initial startup mode of the circuit, this oscillator needs to be disabled when the constant-on-time loop takes over. To this end, the final PMOS M_{P3} in the oscillator of Fig. 3 is designed with a size of 2μm/5μm in order to minimize current consumed when this cell is disabled. The other PMOS transistors are 5μm/250nm and the NMOS transistors are 2μm/300nm, where 250nm and 300nm are the minimum channel length for low–V_t PMOS and NMOS transistors, respectively.

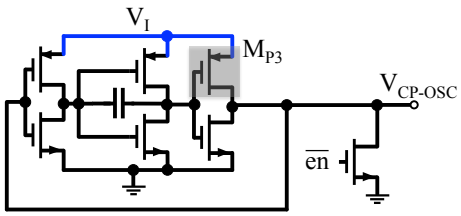


Fig. 3. Startup charge pump oscillator.

Fig. 4 shows the complete charge pump schematic. The oscillator from Fig. 3 is fed through a buffer before connecting to a diode-connected native–V_t NMOS charge pump, similar to the approach in [10]. Unlike the previous work, our system relies on an oscillator signal generated on-chip and is connected to the output switch drivers, which require a large amount of power to operate. Because of these drawbacks, while using a 10 stage design, our charge pump achieves a peak voltage of only 950mV from a 300mV source. In our implementation of this charge pump, all native-V_t NMOS transistors are designed with a size of 40μm/500nm and the capacitors are 10pF metal-metal capacitors. Note that in the CMOS process we are using, 500nm is the minimum channel length for native–V_t NMOS transistors.

C. Startup Oscillator and Driver

In order to raise the output voltage to an appreciable value to bias the hysteretic control circuitry, a high-duty-

cycle oscillator is applied to the gate driver circuitry for the switch transistors, powered by the charge pump described in Section III-B. Using an oscillator similar to that in Fig. 3, but running at a frequency of 100kHz, this low-frequency clock is modified to run at a very high duty cycle (83%). Fig. 5 shows the high duty cycle transformation circuit. As long as either of the inputs to the NAND gate are low, the output of this circuit will be high. Since the input comes from a clock running at about 50% duty cycle, the output is only low during the delay when the oscillator goes from LO to HI. During this time, the output V_{SO} will be low until the input signal propagates through the three inverter, two capacitor delay. As was described in Section II-A, The duty cycle of the converter must be less than 100% to ensure that current from the inductor is transferred to the output capacitor, and hence the output voltage can rise. The schematic of this high-duty-cycle system connected to the drivers and output switches is shown in Fig. 6

D. Hysteretic Control

1) Overview: The main control loop for the proposed circuit is implemented using the constant-on-time control scheme shown in Fig. 7. If the feedback voltage is below the reference voltage, the one-shot circuit will trigger, causing the NMOS switch to turn on for a fixed period of time. At the same time, the switch across R_{hys} will close, effectively setting the voltage threshold to a higher level and adding a predictable amount of positive hysteresis. Once the one-shot times out, the NMOS turns off and the PMOS turns on, until the current through the inductor reaches 0. At this point, the same process repeats until V_O reaches the comparator threshold, at which point the circuit goes into a low-power coasting mode and the R_{hys} switch turns off, returning the circuit to its lower threshold as it waits for the output voltage to fall again. A state diagram of the proposed control scheme is shown in Fig. 8.

2) Output Voltage Ripple: By examining Fig. 9 and assuming the output current I_O is zero, a closed-form expression can be developed for the output voltage ripple, Δv_O. In the zero-load condition, the output voltage of the constant on-time regulator only increases when the inductor is discharging, and hence, transferring its energy to the output capacitor. During this time (t_1 to t_2), switch S_1 is OFF while S_2 is ON as shown in Fig. 9a. The current in the inductor over an entire switching period is shown in (2).

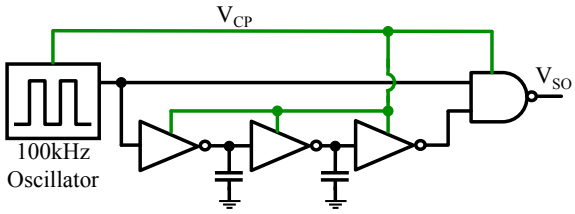


Fig. 5. Startup oscillator and high-duty-cycle circuitry.

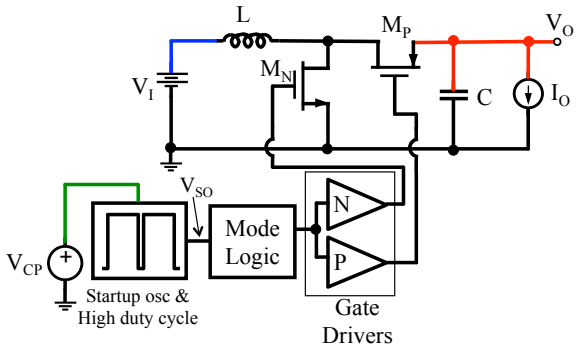


Fig. 6. Startup circuitry connected to drivers and output switches.

$$i_L(t) = \begin{cases} \dfrac{V_I}{L}t, & t_0 < t \le t_1 \quad (2a) \\ I_P - \dfrac{V_O - V_I}{L}(t - t_1), & t_1 < t \le t_2 \quad (2b) \end{cases}$$

And hence,

$$t_{off} = t_2 - t_1 = \frac{I_P L}{V_O - V_I}. \tag{3}$$

During t_{off}, when the current from the inductor flows to the output capacitor and load, the output voltage will increase for each cycle. Assuming the load current, I_O is zero, This change in output voltage, Δv_O, can be derived as shown in (4).

$$\begin{aligned} \Delta v_O &= \frac{1}{C_O}\int i_L(t)\,\mathrm{d}t \\ &= \frac{1}{C_O}\int_{t_1}^{t_2}\left(I_P - \frac{V_O - V_I}{L}(t - t_1)\right)\mathrm{d}t \\ &= \frac{I_P^2 L}{2C_O(V_O - V_I)} \end{aligned} \tag{4}$$

From (2a), it can be shown that I_P=V_I t_{on}/L, and thus (4) can be simplified to the more readable expression shown in (5).

$$\Delta v_O = t_{on}^2 \frac{V_I^2}{2LC_O(V_O - V_I)} \tag{5}$$

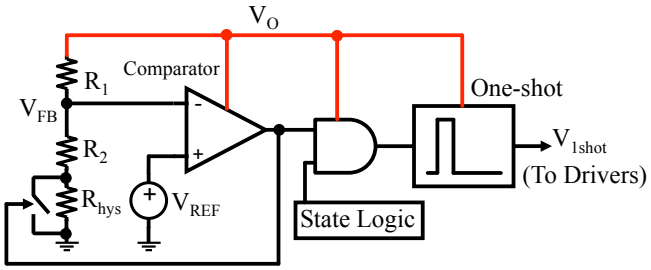


Fig. 7. Hysteretic control schematic.

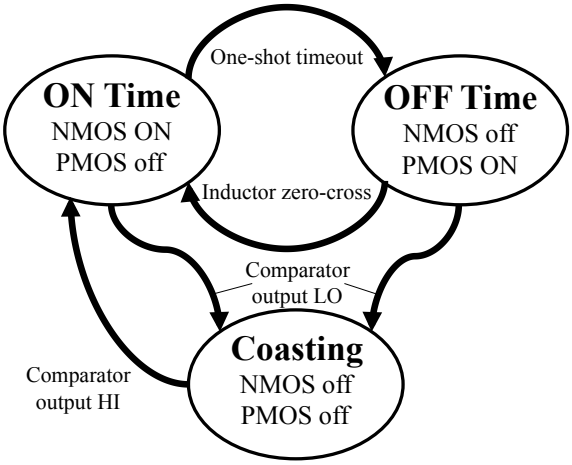


Fig. 8. Hysteretic control state diagram.

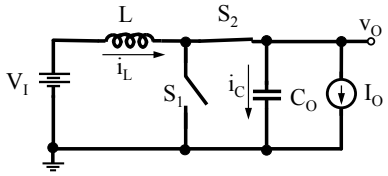
3) Maximum Load Current: Using the superposition principle, the output voltage ripple including effects from the load current I_O can be written as:

$$\Delta v_O = t_{on}^2 \frac{V_I^2}{2LC_O(V_O - V_I)} - \frac{I_O\,(t_{on} + t_{off})}{C_O}. \quad (6)$$

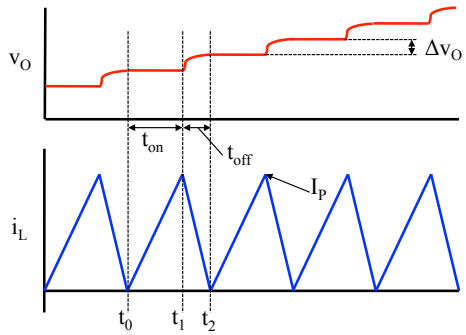
And since the output voltage ripple will be zero at the maximum output current (i.e. the output voltage cannot increase), the maximum load is as shown in (7). Note that the result from (1) was substituted in order to make this result more compact.

$$I_{O(max)} = t_{on} \frac{V_I^2}{2LV_O}. \quad (7)$$

While increasing the on time or reducing the value of the inductor increases the available load, the peak inductor current also increases. While this is not a problem in the ideal



(a) Off-time schematic.



(b) Switching inductor current and output voltage.

Fig. 9. Constant on-time voltage ripple analysis.

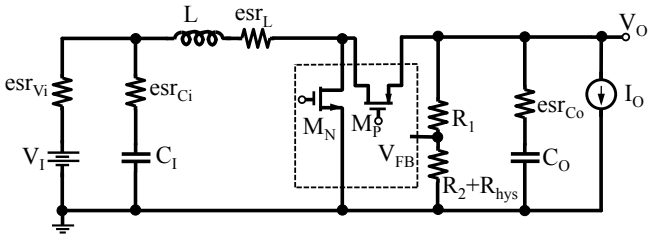


Fig. 10. Simulation schematic including parasitic resistances.

TABLE II
SIMULATION VALUES

Circuit Component	Value
V_I	300mV
V_O	1.0V
L	10μH
C_I	2.2μF
C_O	5.0μF
esr_{Vi}	100mΩ
esr_L	90mΩ
esr_{Ci}	10mΩ
esr_{Co}	10mΩ
R_1	2MΩ
R_2	1.9MΩ
R_{hys}	100kΩ
t_{on}	1.5μs
V_{REF}	500mV
NMOS	5mm / 0.18μm
PMOS	10mm / 0.18μm

mathematical case, larger peak currents are a problem in our practical circuit, where the switch resistance $r_{DS(on)}$ is fairly high. Because of this limitation, simulations have shown that with a peak inductor current of I_P = 45mA.

4) Voltage Hysteresis Value: By analyzing the circuit of Fig. 7, and ignoring non-idealities in the comparator, it can easily be shown that the value of the voltage hysteresis, ΔV_O is

$$\Delta V_O = V_{REF} \frac{R_{hys}}{R_1}. \quad (8)$$

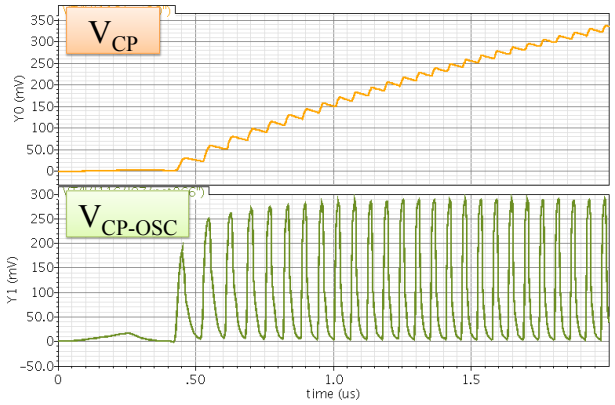
E. Ideal Components

In the currently described circuit there are two ideal components still present in the system, namely the voltage reference V_{REF} and the inductor current sensor. In order to compensate for the current required to power these two components, a 10μA load is added to the output, which has a negative effect on the circuit efficiency, but effectively models the impact these circuits will have on the complete system.

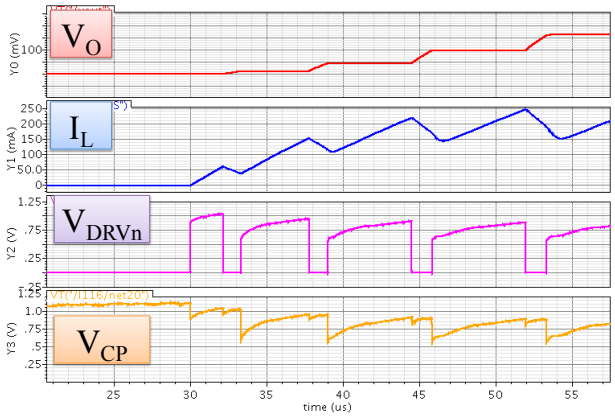
IV. Simulation Results

A. Simulation Schematic

Simulations have been performed on the circuit shown in Fig. 10, with the simulation values shown in Table II. Since



(a) Initial V_{CP} startup.



(b) V_{CP} driving switch transistors.

Fig. 11. Charge pump startup simulation.

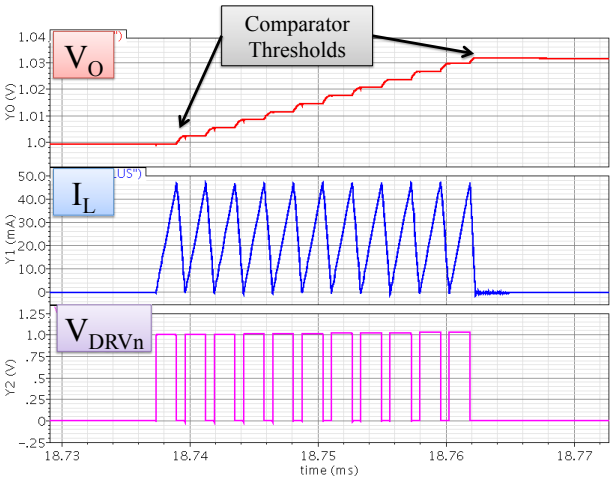


Fig. 12. Steady state operation simulation.

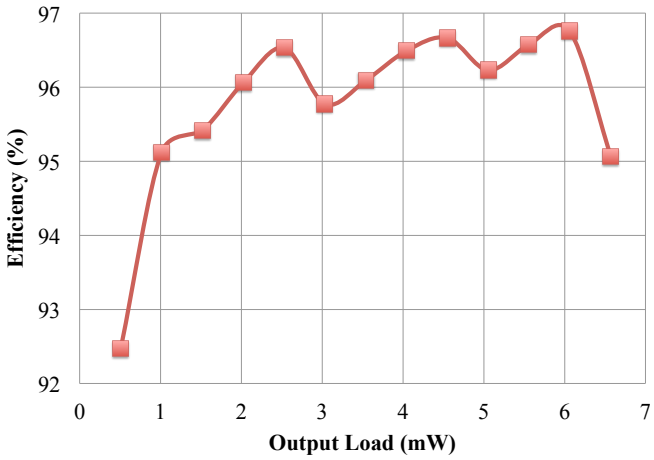


Fig. 13. Efficiency over load range.

circuit parasitics have a large effect on the operation of a boost regulator, parasitic resistances have been included wherever possible. Note that the dashed box in the middle of Fig. 10 shows the internal (transistor-level) circuitry, while everything outside this box is an external component.

B. Startup Results

The initial startup of the regulator, using the charge pump circuitry and oscillator described in III-B is shown in Fig. 11. Once the charge pump oscillator starts switching, the output of the charge pump gradually rises (Fig. 11a). Once the charge pump output is large enough to run the startup oscillator and drivers (shown previously in Fig. 6), the main switches start commutating, and the output voltage V_O slowly rises as shown in Fig. 11b. Once V_O has risen to the reference point, the constant-on time controller takes over and the circuit switches to the steady state, constant on-time mode.

C. Steady State Operation

Fig. 12 shows the steady-state operation of the proposed circuit. Starting from the far left of the figure, both switches are off and the output voltage is slowly coasting downward, with a slope determined by the output load current. During the coast time however, the hysteretic comparator is still watching V_O, and as soon as it reaches the lower threshold of the comparator, the constant-on time control is enabled. Until the comparator reaches its upper threshold, the circuit turns on the NMOS (and hence charges the inductor) for a fixed amount of time, then turns off the NMOS (and hence turns on the PMOS) until the inductor current reaches 0. When the upper threshold of the comparator is finally reached, both switches are turned off and the circuit re-enters the coasting mode, as was previously shown in the state diagram of Fig. 8.

D. Calculation and Simulation Comparison

Using the values shown in Table II along with the analysis in Sec. III-D, we notice that the maximum load should be $I_{O(max)} = 6.75\text{mA}$ with a peak-to-peak voltage ripple of $\Delta V_O = 25\text{mV}$. As can be seen in Fig. 13, the maximum load is just past $P_O = 6.8\text{mW}$, and hence this agrees well with the predicted value. From Fig. 12 however, the voltage ripple is closer to 30mV, due to non-idealities in the comparator.

E. Efficiency

The total end-to-end efficiency of the proposed circuit is shown in Fig. 13. While the efficiency drops off slightly at

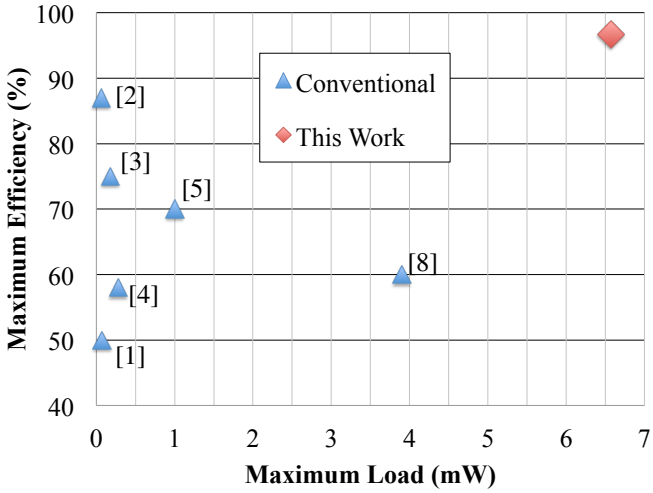


Fig. 14. Comparison of maximum efficiency and output power with cited papers.

lower load, it remains above 95% for most of the load range, reaching a maximum of 96.8% at a load of 6.1mW. The high efficiency in the proposed circuit is a virtue of the fact that switching losses are very low, and the control circuitry consumes very little quiescent current. A comparison between our peak efficiency and maximum load with recently published papers is shown in Fig. 14.

V. Conclusion

We have introduced a low-power boost regulator that is optimized for energy harvesting applications. While previously presented papers have shown that it is possible to convert energy from extremely low-power input sources, these papers have not designed their circuits to work with a realistic load nor to maximize the system efficiency. Compared to previously presented approaches, our circuit can handle enough output load to power a typical microcontroller system, while maximizing the end-to-end efficiency over the entire load range. Finally, the circuit we have introduced accomplishes all of this while only requiring three external components—an input capacitor, an output capacitor, and an inductor.

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