BRIEF PAPER

Background Self-Calibration Algorithm for Pipelined ADC Using Split ADC Scheme

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SUMMARY This brief paper describes a background calibration algorithm for a pipelined ADC with an open-loop amplifier using a Split ADC structure. The open-loop amplifier is employed as a residue amplifier in the first stage of the pipelined ADC to realize low power and high speed. However the residue amplifier as well as the DAC suffer from gain error and non-linearity, and hence they need calibration; conventional background calibration methods take a long time to converge. We investigated the split ADC structure for its background calibration with fast convergence, and validated its effectiveness by MATLAB simulation.
key words: *ADC, self-calibration, pipelined ADC, split ADC, digitally-assisted analog technology*

1. Introduction

Attention is being paid to digitally-assisted technology for pipelined ADC implementation with fine CMOS processes [1]–[3]. A residue amplifier in the first stage consumes considerable power, hence an open-loop residue amplifier has been proposed in [1], [2] for its low power and high speed; its nonlinearity is self-calibrated in the background. However its calibration convergence time is long, which may cause problems such as long testing time (i.e. high testing cost) [4].

A split ADC structure has been proposed for fast convergence of self-calibration [5]–[7], for calibration of the following cases:
(1) Gain error of the residue amplifier and the DAC nonlinearity (DAC capacitor mismatches).
(2) Gain error and nonlinearity of the residue amplifier.
We here consider how to make the method described in [8] more practical for low-power, high-speed, high-precision pipelined ADC design by compensating for gain error and nonlinearity of the residue amplifier as well as DAC nonlinearity, using:

1. An open-loop residue amplifier in the first stage.
2. Background digital self-calibration for its nonlinearity as well as its gain error and the DAC nonlinearity.
3. Split ADC structure for fast convergence.

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We will describe the above structure and calibration algorithm, and validate its effectiveness (fast convergence and high linearity) by Matlab simulation.

2. Pipelined ADC with Split ADC Structure

Figure 1 shows a block diagram of a pipelined ADC, where DAC capacitor mismatch, finite gain and nonlinearity of the operational amplifier degrade the SNDR of the pipelined ADC; here we consider how to calibrate for them. Figure 2 shows a Split ADC structure, and it has been shown in [5], [6] that there is a class of background calibration algorithms that can converge quickly.

Since the two split pipelined ADC outputs (and hence noise effects) are averaged in Figs. 2 and 3, the values of capacitors and g_m's can be halved in DACs and amplifiers (keeping C/g_m constant) [5], [6], and hence their overhead is small.

3. Self-Calibration of Pipelined ADC

We here consider using an open-loop residue amplifier (Fig. 4) for low power, and calibrating for its large nonlin-

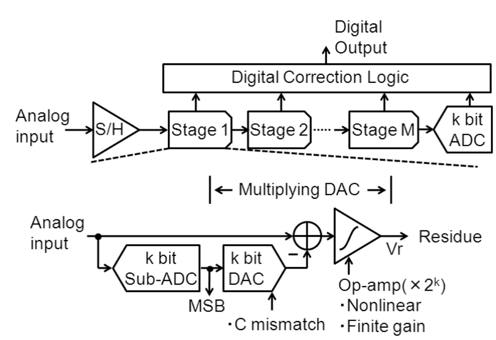

Fig. 1 Pipelined ADC topology, and stage circuit non-idealities.

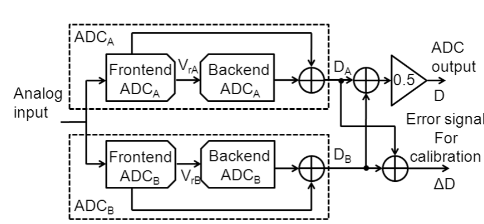

Fig. 2 Split ADC topology example.

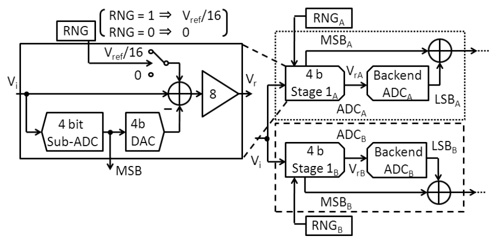

Fig. 3 First stage topology in a pipelined ADC.

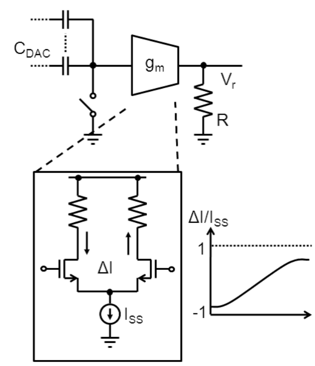

Fig. 4 Example of an open loop amplifier.

earity as well as for its gain error and for DAC capacitor mismatch. We model its nonlinearity as follows, assuming a differential open-loop amplifier:

$$g_a(V_a) = V_r = \alpha_1 \cdot V_a + \alpha_3 \cdot V_a^3$$

3.1 Residue Amplifier Nonlinearity Calibration

We consider adding "0" or "1", generated pseudo randomly by a random number generator (RNG) to stages 1_A and 1_B (Fig. 3) to generate two residue waveforms (Figs. 5, 6), and compensate for the amplifier nonlinearity. (RNGs for stages 1_A and 1_B are designed to be different.) Each stage uses 1-bit redundancy and generates the other residue waveform by adding the offset [1], [2]. The difference in residue waveforms between ADC_A and ADC_B is used to compensate for gain error and DAC capacitor mismatch [5], [6], as described later.

We obtain calibration signals from the difference between residue signals in stages 1_A and 1_B with RNG=0, or 1; four averaged values d_{ab00} (for RNG_A=0, RNG_B=0), d_{ab01} (for RNG_A=0, RNG_B=1), d_{ab10} (for RNG_A=1, RNG_B=0), and d_{ab11} (for RNG_A=1, RNG_B=1). Then we obtain the time-averaged distance h_a of two residue waveforms in stage 1_A for several digital output codes of 4 upper bits (Fig. 7). When the upper-four-bit output is "0000", the average distance h_{anl} of two residues can be obtained by "d_{ab00} and d_{ab10}" (or "d_{ab01} and d_{ab11}"), and here the residue waveforms are strongly affected by amplifier nonlinearity. Similarly we can obtain the distances between the residue waveforms for upper-four-bit outputs from "0001" to "1111", and also in stage 1_B.

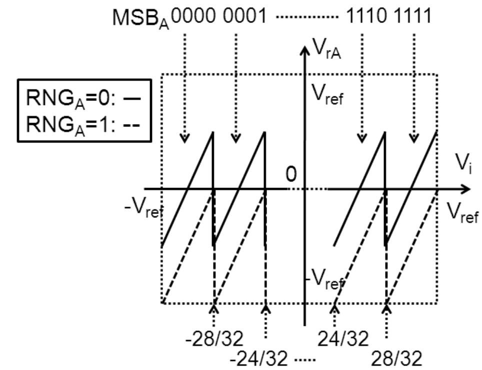

Fig. 5 Stage1_A input-output characteristics.

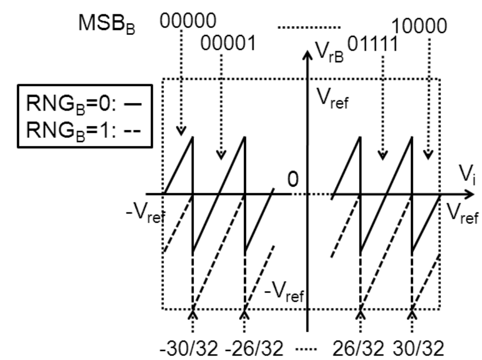

Fig. 6 Stage1_B input-output characteristics.

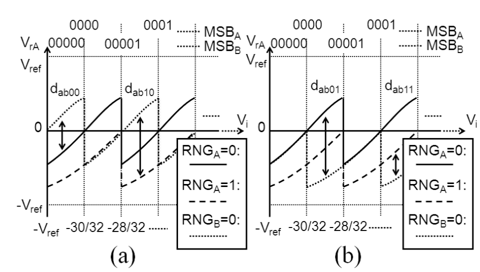

Fig. 7 Estimation of the difference d_{ab00}, d_{ab01}, d_{ab10} and d_{ab11} of the residue curves. (a) Stage1_A residue curves and Stage1_B residue curves in case of RNG_B = 0. (b) Stage1_A residue curves and Stage1_B residue curves in case of RNG_B = 1.

Digital calibration works to equalize the digitally-corrected average distances for several digital codes, then we have the correct ADC output, with amplifier nonlinearity compensated, in stage 1_A. Similarly we have the correct ADC output in stage 1_B (Fig. 8).

3.2 Residue Amplifier Gain Error and DAC Capacitor Mismatch Calibration

This section describes our method of background self-calibration for residue amplifier gain error and DAC capacitor mismatch, based on [3]; this calibration is performed after the above-mentioned nonlinearity calibration.

First, we have only one residue waveform by subtracting the offset (Fig. 9). Next, we compensate for slope mis-

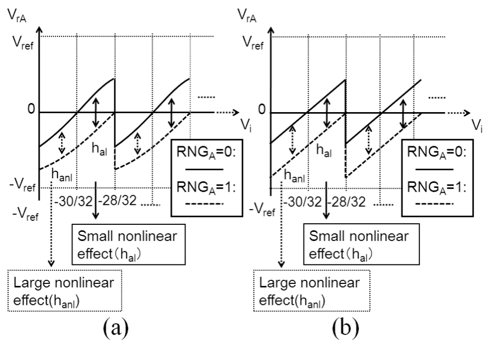

Fig. 8 Estimation of the distance h_{al} and h_{anl} of the residue curves. (a) Before calibration. (b) After calibration.

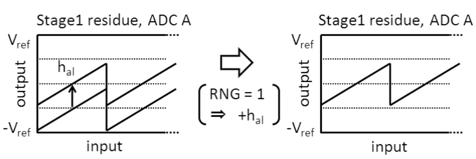

Fig. 9 Translation of two residue curves into one residue curve.

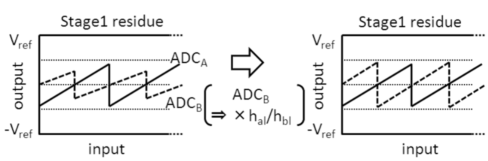

Fig. 10 Gain mismatch correction between ADC_A and ADC_B.

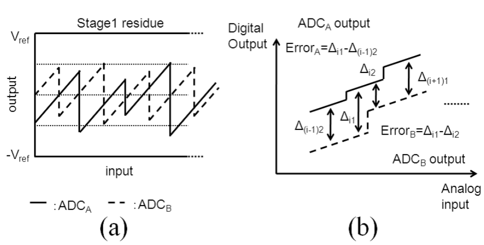

Fig. 11 (a) Transfer curves of $Stage1_A$ and $Stage1_B$. (b) Measurement for missing codes of ADC_A output and ADC_B output in finite gain error and capacitor mismatch case.

match of the residue waveforms in stages 1_A and 1_B by multiplying h_a/h_b by the waveform in stage 1_B (Fig. 10). We have a calibration signal of the difference between the ADC_A and ADC_B output codes. Gain error and capacitor mismatch may cause missing codes (Fig. 11). Since the reference voltages of sub-ADCs in ADC_A and ADC_B are designed to be different, missing codes in ADC_B can be measured by ADC_A, vice versa, and they are corrected (Fig. 12, [3]).

4. Background Self-Calibration Circuit

Figure 13 shows a block diagram of the pipelined ADC with background self-calibration, and Fig. 14 shows the analog part employing a Split ADC structure. The first stage is split

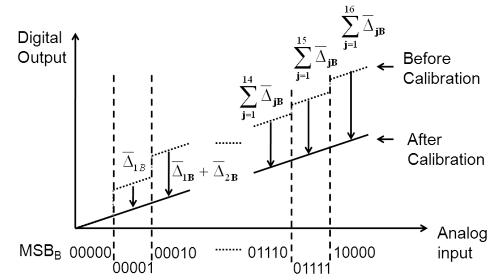

Fig. 12 Compensation for finite gain and capacitor mismatch in ADC_B.

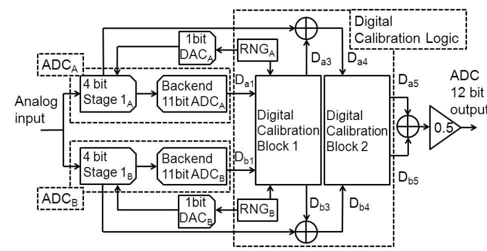

Fig. 13 Whole ADC block diagram of the proposed topology.

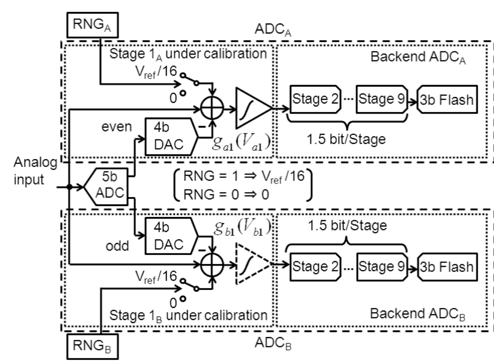

Fig. 14 Analog portion of the proposed pipelined ADC topology.

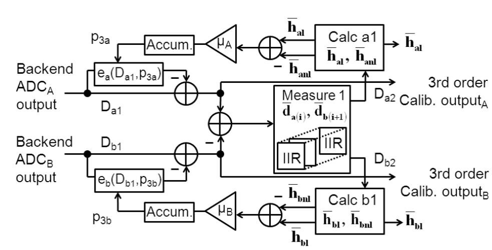

Fig. 15 Digital calibration block 1-1 (for amplifier non-linearity correction).

into ADC_A and ADC_B. The digital calibration block consists of block 1 for nonlinearity correction (Fig. 15) and block 2 for gain error and capacitor mismatch correction (Fig. 16).

5. Simulation Results

We have performed Matlab simulation to validate the effectiveness of our proposed method.

Simulation conditions: 12 bit 10 MS/s pipelined ADC us-

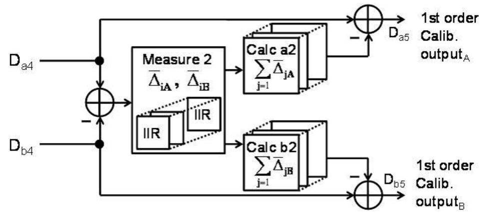

Fig. 16 Digital calibration block 2 (for amplifier gain error and capacitor mismatch compensation).

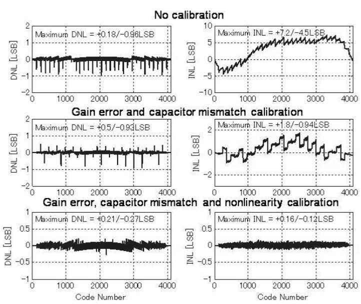

Fig. 17 DNL and INL of the ADC output.

ing a residue amplifier with the following nonlinear characteristics:

$$g_a(V_a) = g_m R \cdot \left[\left(\frac{V_a}{V_{ref}} \right) - \frac{1}{8} \left(\frac{V_{ref}}{V_{ov}} \right)^2 \left(\frac{V_a}{V_{ref}} \right)^3 \right].$$

Reference voltage V_{ref}=1 V, Overdrive voltage V_{ov} = 0.25 V, g_mR of the amplifier in stage 1A, 1B = 7.5, 7.6 respectively. Capacitor mismatch σ in DAC = 2%. Gain μ in LSM loop in block 1 =1/8192, IIR filter gain μ_3, μ_1 in self-calibration block 1, 2 =1/512, 1/1024 respectively.

Figure 17 shows DNL and INL, while Table 1 summarizes the simulation results. We see that our calibration for gain error, capacitor mismatch and nonlinearity is effective. We have also checked convergence time ($\approx 6 \times 10^5$ sampling periods, [8]) and it is about 1/100 of the conventional method in [1], [2].

6. Conclusion

We have proposed a background calibration algorithm for

Table 1 Summary of simulated ADC performance.

	No calibration	After calibration for gain error, & C mismatch	After calibration for gain error, C mismatch & nonlinearity
INL [LSB]	+7.2/−4.6	+1.8/−0.94	+0.16/−0.12
DNL [LSB]	+0.18/−0.96	+0.5/−0.93	+0.21/−0.27
SNDR [dB]	50.4	68.5	73.9

a pipelined ADC with an open-loop residue amplifier using a Split ADC structure; the algorithm compensates for nonlinearity and gain error of the open-loop residue amplifier and DAC capacitor mismatches all together, and provides fast convergence. We have shown by Matlab simulation that the proposed method can converge 100 times faster than a conventional method.

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