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A Twistedly-Cascaded Time Difference Amplifier for High Robustness Against Process Variation

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1. Introduction

A high-gain time difference amplifier (TDA) has been developed for high-resolution on-chip timing jitter measurement [1]. In order to obtain a high-gain TDA, a cascaded structure is one of the most feasible [2]. However, a cascaded structure may cause large output time offset, which degrades the jitter measurement performance.

This work presents a twistedly-cascaded structure for high robustness against process variation. By cascading TDAs twistedly based on the test results of each TDA, output time offset of each stage can be canceled and total output time offset can be minimized. Minimized total offset allows smaller size of the variable delay for calibration and implementation cost can be reduced as shown in Fig. 1.

2. Test and Reconfiguration of Twistedly-Cascaded TDA

In a cascaded TDA, multiple open-loop TDAs exploiting the variable delay of an SR latch subject to nearly coincident input edges [3] are serially connected. It has been shown that an open-loop TDA is very sensitive to process variations due to its operation mechanism [3]. Unfortunately, the cascaded structure makes this sensitivity more serious.

Figure 2 shows the test and reconfiguration of twistedly-cascaded TDA. In order to realize the twisted-connection, the polarity of time offset has to be tested. Each connection point between TDAs can be reconfigured after taking the test results into account. Based on the test results, the connection is changed to minimize the time offset.

3. Time Offset Reduction with Twistedly-Cascaded TDA

Figure 3 illustrates the influence of device variation on an open-loop TDA. Process variation shifts the curve of the output time difference as a function of input time difference. This shift results in generation of output time offset.

In order to simplify the model of TDAs under process variation, gains and output time offsets of all TDAs are assumed to be α and β respectively, where β>0. Under this prerequisite, the relationship between ΔT_{IN} and ΔT_{OUT} is expressed as followings:

$$\Delta T_{OUT} = \alpha \Delta T_{IN} + \beta \quad (1).$$

Therefore, total time offset, β_{TOTAL} in the upper part of Fig. 4, becomes:

$$\beta_{TOTAL} = \left(\alpha^{n-1} + \alpha^{n-2} + \cdots + \alpha^2 + \alpha + 1\right)\beta \quad (2).$$

This equation indicates that time offset increases as an edge propagates through each TDA. Thus the non-twisted cascaded TDA maximizes the total time offset, i.e. the worst-case time offset, as shown in the upper part of Fig. 4.

On the other hand, twisted-cascaded TDA minimizes the total time offset β'_{TOTAL}, as shown in the lower part of Fig. 4:

$$\beta'_{TOTAL} = \left(\alpha^{n-1} - \alpha^{n-2} - \cdots - \alpha^2 - \alpha - 1\right)\beta \quad (3).$$

Figure 5 plots the calculated total time offset as a function of the number of stages. The results are calculated with Eqs. (2) and (3). As shown in Fig. 5, the absolute value of time offset reduction increases as the number of stages increases. This means that the length of the variable delay for calibration can be reduced by a greater amount when there are a greater number of stages, resulting in a larger cost reduction.

Figure 6 plots the time offset reduction as a function of the number of stages. Figure 6 indicates that a larger time offset reduction can be obtained when using a greater number of stages. Time offset reduction as a function of gain per stage is also demonstrated in Fig. 6. The lower the gain, the larger reduction in total time offset obtained.

4. Simulation Results

In order to evaluate the proposed twistedly-cascaded TDA, we have performed SPICE simulation in 65 nm CMOS technology with a 1.2 V power supply. Figure 7 shows the simulation results when comparing twistedly and non-twistedly cascaded TDAs under process variations. Simulation results show that the proposed twistedly-cascaded TDA dramatically reduces time offset. Under each process condition (FF, TT, SS), time offset is reduced by 55.1%, 58.8%, 61.0%, respectively, which match well with calculation results using Eqs. (2) and (3).

5. Conclusions

This work presents a highly robust twistedly-cascaded TDA. By cascading TDAs twistedly based on test results, the total output time offset can be reduced. SPICE simulations with 65 nm CMOS have proved the effectiveness of the proposed structure. Simulation results show 58.8% output time offset reduction of a 4-stage cascaded TDA when gain per stage is 3.3, which matches well with theoretical investigation.

Acknowledgement
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References

[1] K. Niitsu, et al., "An On-Chip Timing Jitter Measurement Circuit Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier with Duty-Cycle Compensation," *submitted to* IEEE Asian Solid-State Circuits Conference 2011.

[2] S. K. Lee, et al., "A 1 GHz ADPLL With a 1.25 ps Minimum-Resolution Sub-Exponent TDC in 0.18 μm CMOS," IEEE JSSC, Vol.45, No.12, pp.2874-2881, Dec. 2010.

[3] M. Lee, et al., "A 9 b, 1.25 ps Resolution Coarse-Fine Time-to-Digital Converter in 90 nm CMOS that Amplifies a Time Residue," IEEE JSSC, Vol.43, No.4, pp.769-777, Apr. 2008.

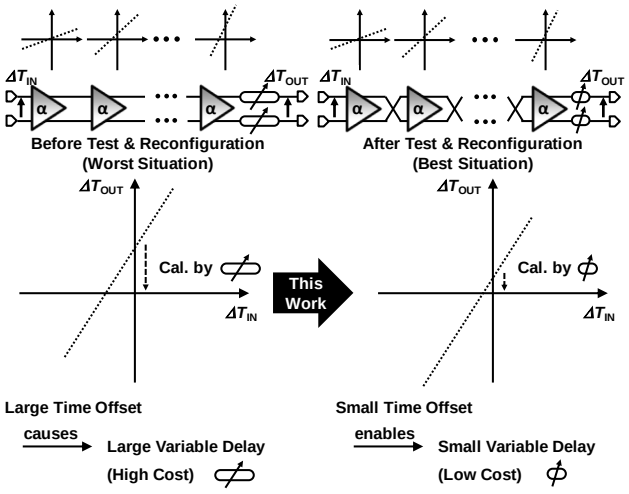

Fig. 1. Concept of this work.

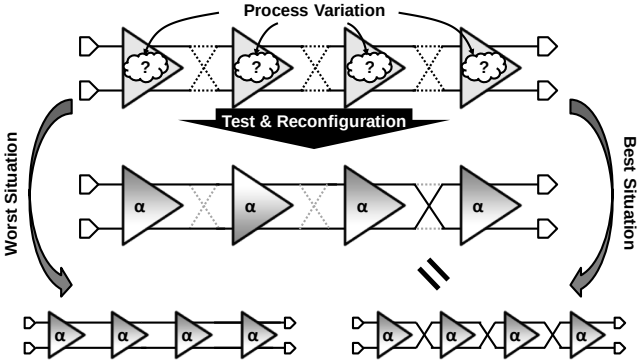

Fig. 2. Test and reconfiguration of the proposed twistedly-cascaded TDA.

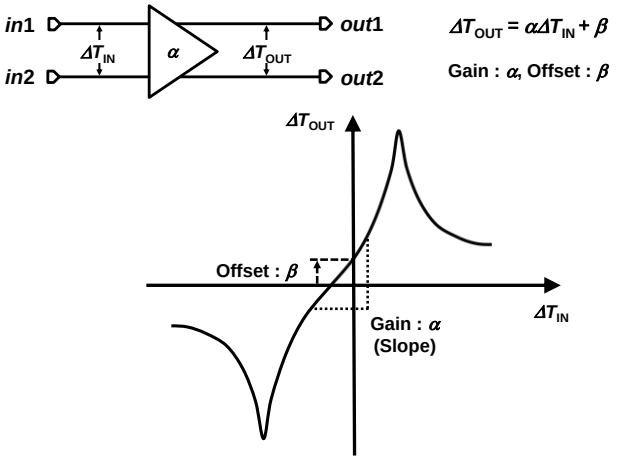

Fig. 3. Model of gain and time offset in TDA.

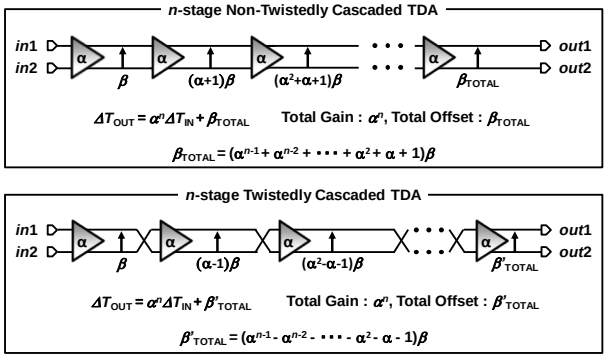

Fig. 4. Total time offset of non-twistedly and twistedly cascaded TDAs.

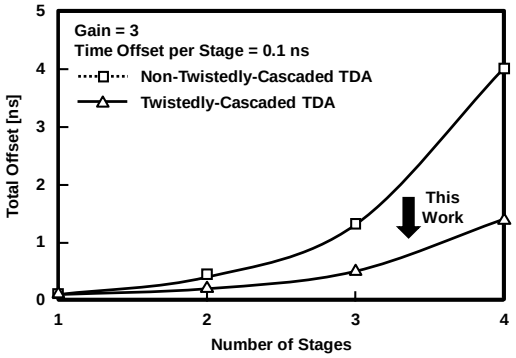

Fig. 5. Total time offset as a function of number of stages.

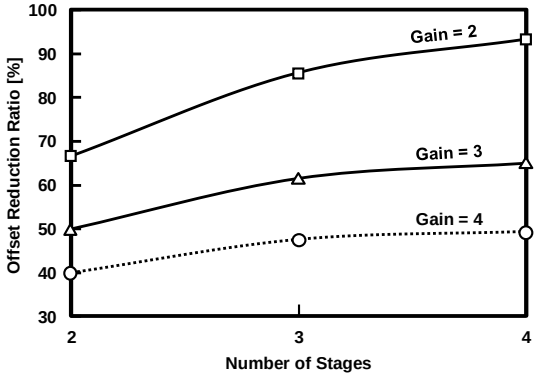

Fig. 6. Time offset reduction as a function of number of stages.

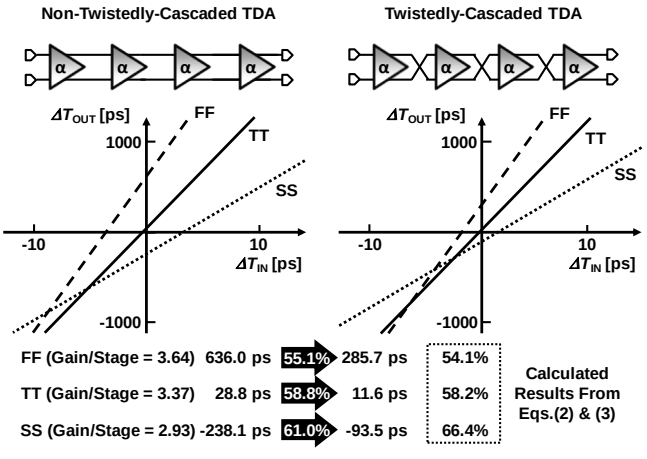

Fig. 7. Simulated time offset as a function of input time under each process condition.