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An On-Chip Timing Jitter Measurement Circuit Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier with Duty-Cycle Compensation

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***Abstract* - This paper demonstrates a reference-free, high-resolution on-chip timing jitter measurement circuit. It combines a self-referenced clock and a cascaded time difference amplifier (TDA) with duty-cycle compensation, which results in reference-free, high-resolution timing jitter measurement without sacrificing operational speed. The test chip was designed and fabricated in 65 nm CMOS. Measured results of the proposed circuit show the possibility of detecting a timing jitter of 1.61-ps RMS in 820 MHz clock with less than 4% error.**

I. Introduction

Since all digital phase-locked loops (ADPLL) together with analog PLLs will continue to play an important role both in communications and I/O links, it is critically important to realize an on-chip circuit for measuring the jitter of the on-chip PLL or CDR without requiring a jitter-free reference clock. Timing jitter is the uncertainty in the zero crossing point of a clock (Fig. 1(a)), while period jitter is the measure of the period fluctuation (Fig. 1(b)). Thus, timing jitter measurements are critically important to validate the performance of PLLs or CDRs. This timing jitter has spectra of the form $1/f^n$ where f is the offset frequency from the carrier. This results in a ps or sub-ps jitter value over the out of band of the PLL: $\Delta\phi_{RMS} = \int_{f_{PLL}}^{\infty} f^{-n} df$. Thus, for measuring out-of-band timing jitter in a PLL output, it is required to have some jitter amplification approach to accurately detect a small out-of-band timing fluctuations.

Previously reported on-chip circuits for measuring timing jitter requires a jitter-free reference clock [1, 2]. On the other hand, for period jitter, a self-referenced clock technique was proposed by M. Ishida [3] and successfully applied to period jitter measurements [3, 4]. Note that the circuit of [3] integrates period jitter, which is detected using the self-referenced clock technique, to measure timing jitter. Hence, no traditional circuit was proposed to measure timing jitter using the self-referenced clock technique. This paper introduces a new self-referenced clock technique to directly measure timing jitter. It also proposes a technique for measuring timing jitter in fine time resolution, which uses a cascaded time difference amplifier with duty-cycle compensation, while maintaining high-speed operation.

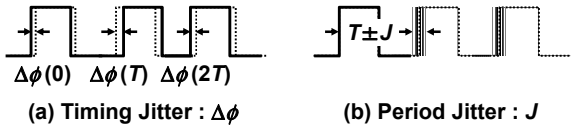

Fig. 1. Timing jitter (a) and period jitter (b).

This paper is organized as follows: Jitter measurement circuits are revisited in Section II. Section III introduces a self-referenced clock technique. Section IV presents a cascaded time difference amplifier with duty-cycle compensation. Test chip design and measurement results are summarized in Section V and VI. Section VII concludes this paper.

II. Jitter Measurement Circuits Revisited

In this section, jitter measurement circuits are revisited to clarify the difference between our proposed circuit and conventional circuits [1, 2, 3, 4]. A mathematical model for measuring timing jitter and period jitter is also developed.

Timing fluctuations can be detected by latching the clock-under-test with a reference clock (i.e. timing comparison). Since this latching process can be regarded as a random skew measurement. The root mean square (RMS) value of timing fluctuations is measured as a random skew. Thus, from (13) of [5],

$$\hat{\sigma}_{Skew} = \sqrt{\left(\Delta\phi_{RMS}^{Data}\right)^2 + \left(\Delta\phi_{RMS}^{Clk}\right)^2 - 2\rho\Delta\phi_{RMS}^{Data}\Delta\phi_{RMS}^{Clk}}. \quad (1)$$

where $\Delta\phi_{RMS}^{Data}$ and $\Delta\phi_{RMS}^{Clk}$ are the RMS values of the timing jitter (Fig. 1 (a)) of the data signal and the clock signal, respectively. ρ is the cross-correlation coefficient between the two timing jitter sequences of the data signal and the clock signal, where $|\rho| \le 1.0$.

On-chip jitter measurement circuits in [1] and [2] make both the clock under test and a reference clock go through delay lines of matched electrical length. The clock under test is then latched at the rising edge of the reference clock. From (1), the corresponding RMS value is given by

$$\hat{\sigma}_{Skew} \approx \Delta\phi_{RMS}^{Data}. \quad (2)$$

Therefore, the circuits can extract the timing jitter (Fig. 1(a)) from the clock under test. However, this approach assumes that the jitter of the reference clock is very small:

$$\Delta\phi_{RMS}^{Data} >> \Delta\phi_{RMS}^{Clk}. \quad (3)$$

Unfortunately, it is extremely difficult to have a jitter-free reference clock by either on-chip generation or being fed from an external source. Thus, it is desirable to remove the requirement for a reference clock altogether from the measurement circuit.

In previous works [3] and [4] where the reference clock is not needed, the clock signal under test is split into two paths: one path that goes directly into the latch, and another path that goes through a programmable delay line, whose delay is set to one clock period T. The time difference between the clock under test and the delayed clock is then measured. Since the timing jitter of the delayed clock is non-zero, the random skew value of (1) gives

$$\hat{\sigma}_{Skew} = \sqrt{\left\langle \left(\Delta\phi^{Data}[T]\right)^2 + \left(\Delta\phi^{Data}[0]\right)^2 - 2\rho\Delta\phi^{Data}[T]\Delta\phi^{Data}[0] \right\rangle}$$
$$\approx \sqrt{\left\langle \left(\Delta\phi^{Data}[T] - \Delta\phi^{Data}[0]\right)^2 \right\rangle}$$
$$\approx J_{RMS}. \quad (4)$$

where $\langle x \rangle$ is the average of x. Since $\Delta\phi^{Data}[T]$ and $\Delta\phi^{Data}[0]$ are adjacent edges, $\rho \approx 1.0$ is assumed. Therefore, the circuits can directly extract the period jitter, J_{RMS} (Fig. 1 (b)) from the clock under test without requiring a reference clock.

Similarly the proposed timing jitter measurement circuit adopts self-referenced clock technique to eliminate the requirement for a reference clock. However, unlike the previous approaches, our proposed method set delay of the delay line to multiples of the clock period nT, with $n > 2$. Note that the timing jitter of the delayed clock is non-zero. On the other hand, two edges which are apart from each other by nT, are uncorrelated with each other [6]: $\rho \approx 0.0$. From (1), the time difference between the clock under test and the delayed clock is detected as

$$\hat{\sigma}_{Skew} = \sqrt{\left\langle \left(\Delta\phi^{Data}[nT]\right)^2 + \left(\Delta\phi^{Data}[0]\right)^2 \right\rangle}$$
$$\approx \sqrt{2\left(\Delta\phi^{Data}_{RMS}\right)^2} = \sqrt{2}\Delta\phi^{Data}_{RMS}. \quad (5)$$

Hence, the proposed circuit can directly measure the timing jitter $\Delta\phi_{RMS}$ (Fig. 1(a)) from the clock under test without requiring a reference clock. Note also that a nT delay measures the jitter with a gain of $\sqrt{2}$.

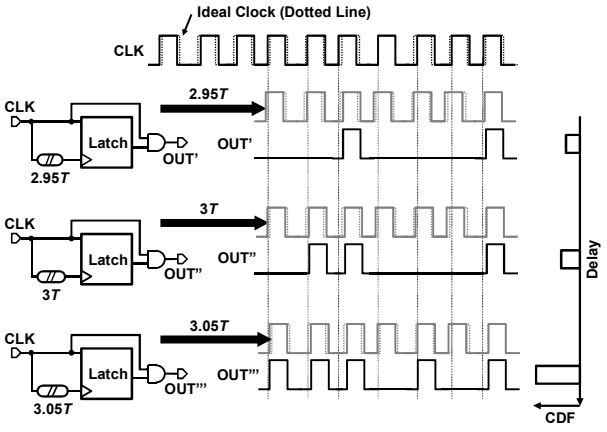

Fig. 2. Concept of the proposed jitter measurement using self-referenced clock with nT delay (n=3).

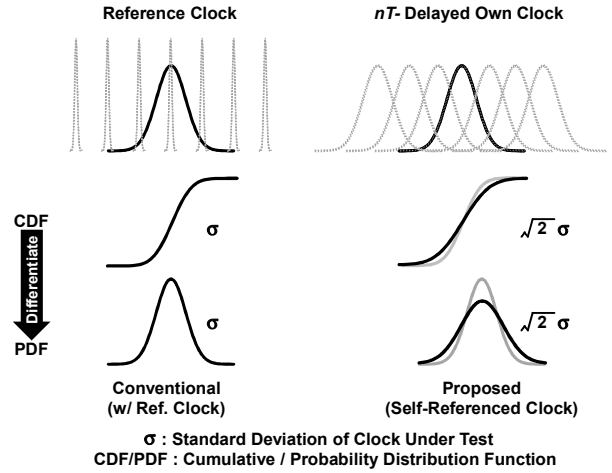

Fig. 3. The difference of obtained PDF and CDF between the reference-required conventional circuit and proposed reference-free circuit.

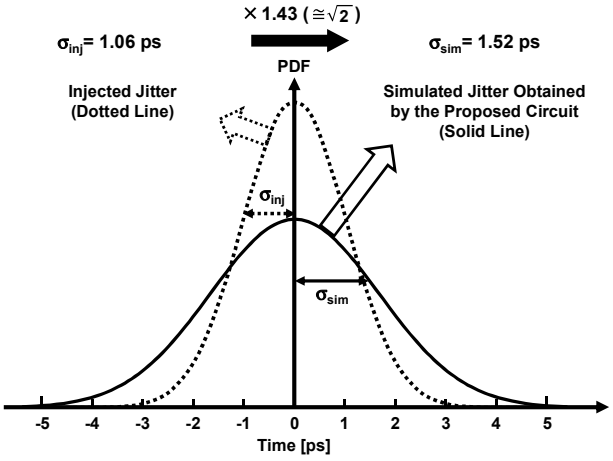

Fig. 4. Simulated jitter obtained by the proposed circuit with self-referenced clock.

III. Self- Referenced Clock for Measuring Timing Jitter

Fig. 2 illustrates the concept of the proposed self-referenced clock technique. The latch operates as a timing comparator and the output pulse is activated when the delay clock catches up with the clock. By incrementing the delay around nT, the cumulative distribution function (CDF) can be obtained. By differentiating CDF, the probability distribution function (PDF) becomes available, and RMS jitter can be calculated from the PDF.

Fig. 3 shows the comparison of obtained CDF and PDF, which shows the CDF and PDF is broadened by a factor of $\sqrt{2}$. This broadening of the distribution functions shows that the self-referenced clock topology both removes the need for a reference clock while relaxing the requirement for time resolution. The reference clock removal also contributes to accuracy enhancement because the proposed method does not suffer from jitter in the reference clock.

HSPICE simulation was performed in order to verify the proposed technique. As predicted from (5), simulated results show a gain of $\sqrt{2}$ in Fig. 4.

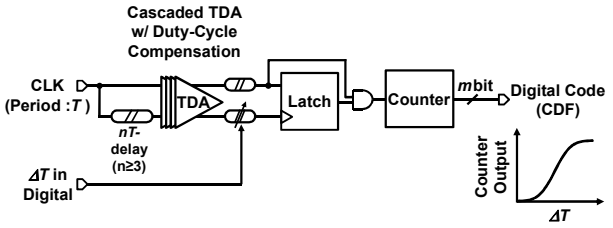

Fig. 5. Schematic of the proposed on-chip jitter measurement circuit.

Fig. 5 shows the schematic of the proposed circuit. It consists of variable delay elements, a latch, a cascaded TDA and counters. The proposed circuit delays its input clock by nT instead of using an external reference clock. In order to generate an nT-delayed clock, a delay chain is implemented, which results in the additional silicon area compared with the previous work [2]. However, this area overhead is much smaller than that required for getting a reference clock delivered from an external source. This nT delay eliminates the correlation between the rising edges of the clock and the delayed clock.

IV. Cascaded Time Difference Amplifier with Duty-Cycle Compensation

A four-stage cascaded TDA with approximately 100x gain amplifies the time difference between the rising edges of the non-delayed and nT-delayed clocks. The cascaded TDA is composed of multiple instances of the conventional TDA in [7]. The number of stages was determined in order to realize a TDA of high gain (> 100x) at operational frequency = 820 MHz under the input range of time difference [-5 ps, +5 ps]. By implementing a digitally-controlled delay with 4-ps step in [8], 28-fs (4 ps / ($\sqrt{2}\times100$)) resolution was obtained.

Fig. 6 (a) illustrates the motivation of the duty-cycle compensation. High gain TDA causes large recovery time, T_{out1} and T_{out2} as stated by (3) in [7]. Rising edges of the output signals are determined by T_{out1} and T_{out2}. On the other hand, the falling edges are determined by the delays of the circuit, which are approximately same values for both outputs. Therefore, the output pulse disappears when the falling edge is earlier than the rising edge.

Duty-cycle compensation solves the above issue as shown in Fig. 6 (b). By implementing the duty-cycle control circuit in front of the input of TDA, the falling edge of the output delays. This delayed falling edge can restore pulses that disappeared under the case in Fig. 6 (a).

Fig. 7 depicts simulated and measured operational frequency as a function of duty cycle. Measured results were obtained from the test chip explained in the following section. Since a large duty cycle causes overlapping with rising edges of the next cycle, duty cycle has an optimum point.

V. Test Chip Design & Measurement Setup

A test chip was designed and fabricated in a 65 nm CMOS technology as depicted in Fig. 8. The proposed two circuits without a TDA and with a TDA occupy silicon areas of 490 μm^2 and 1350 μm^2, respectively. A BERTS (Agilent 81250) was used to generate a clock pattern at f = 820 MHz and 410 MHz while intrinsic timing jitter of 1 ps RMS was measured by an oscilloscope (Tektronix DSA71254B).

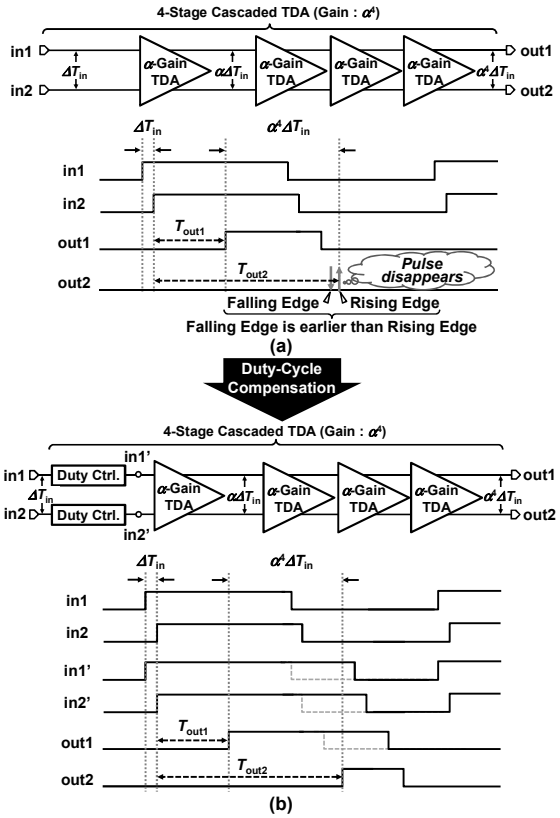

Fig. 6. Concept of the duty-cycle compensation: (a) Before the compensation, (b) After the compensation.

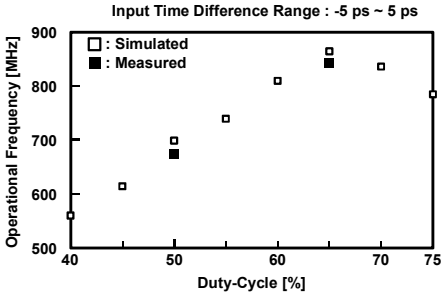

Fig. 7. Simulated and measured operational frequency as a function of duty cycle.

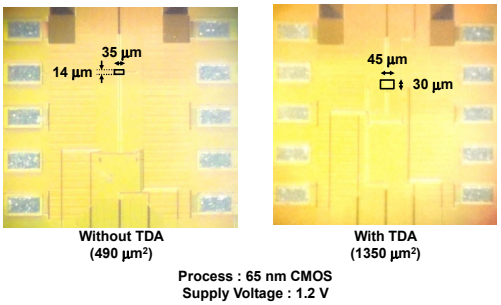

Fig. 8. Test chip microphotograph.

VI. Measurement Result

Fig. 9 shows the timing jitter CDF measured by the proposed circuit. By incrementing the nT-delay around 3T, count of output pulse increased. The measured gain of a cascaded TDA is depicted in Fig. 10. A gain of

approximately 100 was confirmed. By combining the results shown in Figs. 9 and 10, a timing jitter PDF in Fig. 11 was obtained. The proposed circuit successfully measured 1.61 ps RMS jitter with an error of 0.06 ps, which corresponds to 4% error. Fig. 12 shows the strong correlation between the timing jitter values measured by the proposed circuit and the jitter values measured by an oscilloscope (Tektronix DSA71254B).

When the applied jitter value is expected to be greater than 2 ps RMS, frequency of the clock under test was set to 410 MHz. This frequency limitation is due to the retainment of measurement accuracy: if the RMS value of the measured jitter ($\sqrt{2}$ -time by self-referenced clock and 100-time by cascaded TDA) is around the period of an 820 MHz clock, accurate measurements become impossible.

Measured results obtained by the proposed circuit match well with the injected jitter measured by an oscilloscope. A linearity error of less than 0.12 ps RMS was achieved. Performance comparison is summarized in Table I.

The proposed circuit was verified to provide reference-free, high-resolution on-chip timing jitter measurements at a cost of small additional chip area. Moreover, operational speed can be increased from 820 MHz to 3.5 GHz by introducing a simplified structure without a TDA, as was confirmed by test chip measurements.

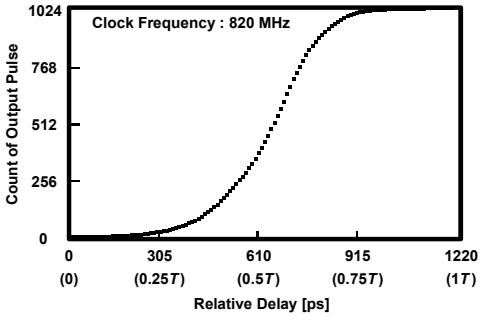

Fig. 9. Measured timing jitter CDF.

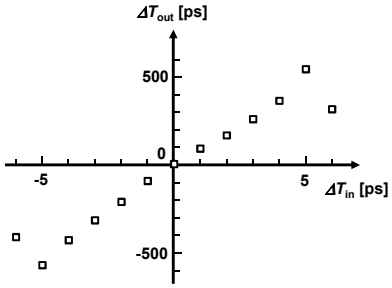

Fig. 10. Measured gain of a cascaded TDA.

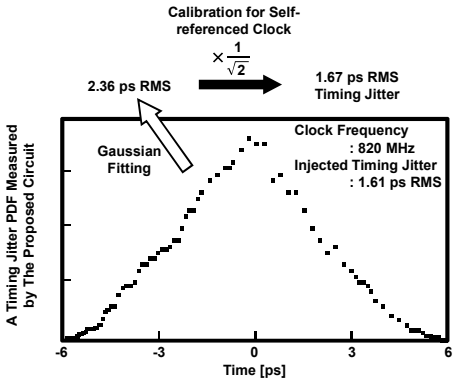

Fig. 11. Measured timing jitter PDF.

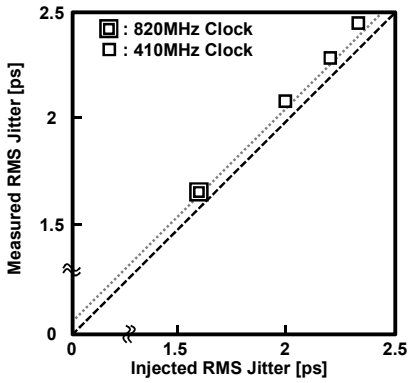

Fig. 12. Measured timing jitter values as a function of values of injected timing jitter.

TABLE I
PERFORMANCE SUMMARY

	This Work		Conventional [2]	Conventional [3]
	w/o TDA	w/ TDA		
Measured Jitter	Timing		Timing	Timing
Reference Clock	Unnecessary		Necessary	Unnecessary
Output Signal	Digital		Digital	High-Speed Analog
Process	65 nm		130 nm	130 nm
Frequency	3.5 GHz	820 MHz	2.5 GHz	2 GHz
Resolution	2.8 ps	28 fs	0.4 ps	N/A
Area	490 μm^2	1350 μm^2	3200 μm^2	117000 μm^2 + I/O Pad

VII. CONCLUSION

This paper introduced a new self-referenced clock technique to directly measure timing jitter. It also proposed a technique for measuring timing jitter in fine time resolution, which uses a cascaded time difference amplifier with duty-cycle compensation. The circuits were implemented in a 65 nm CMOS process with 1.2 V supply. It successfully measured the 1.61-ps RMS timing jitter of 820 MHz clock with an error of less than 4%. A mathematical model for measuring timing jitter and period jitter was also developed.

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