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Architecture of High-Efficiency Digitally-Controlled Class-E Power Amplifier

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Abstract. This paper describes the analysis and design of digitally-controlled class-E power amplifiers, which are suitable for fine CMOS implementation. Two methods for implementing digitally-controlled class-E(-like) amplifiers have already been proposed: using NMOS switch arrays or digital PWM. In this paper we analyze the operation and efficiency of these methods, and then we propose combining them to achieve higher efficiency.

Introduction

Class-E amplifiers are widely used due to their high efficiency [1-7]. Digitally-controlled class-E(-like) amplifiers that use an N-channel Metal-Oxide-Semiconductor (NMOS) switch array or digital pulse width modulation (PWM) have recently been proposed in [8-11]. Compared to ideal class-E amplifiers, the efficiency of these amplifiers is degraded because they cannot achieve zero-voltage, zero- derivative switching. Since these are largely digital circuits however, they are suitable for fine complementary MOS (CMOS) implementation.

In this paper we analyze the operation and efficiency of NMOS switch array and digital PWM methods, then we propose using a combination of these methods to achieve higher efficiency. This proposed method requires a complicated look up table (LUT) to choose the best combination of duty ratio and number of on-state NMOS Field-Effect-Transistors (FETs) for high efficiency and distortion compensation. While this approach sounds difficult, recent rapid advances in digital technology make it feasible to implement, and our simulations validate its effectiveness.

Class-E Power Amplifier

The basic circuit of the class E power amplifier is shown in Fig. 1 [1-7]. It consists of a choke inductor L_f, a power MOSFET operating as a switch, shunt capacitance C_1, and an L-C-R series-resonant circuit. The switch is turned on and off at the operating frequency $f = \omega/(2\pi)$ by the gate driver circuit. The transistor output capacitance, choke parasitic capacitance, and stray capacitances are included in the shunt capacitance C_1. The resistance R is the output load. The choke inductance L_f is assumed to be large enough that AC current ripple on the DC supply current (I_{DD}) can be neglected [1]. An ideal class-E amplifier can achieve high efficiency because of its zero-voltage and zero-derivative switching.

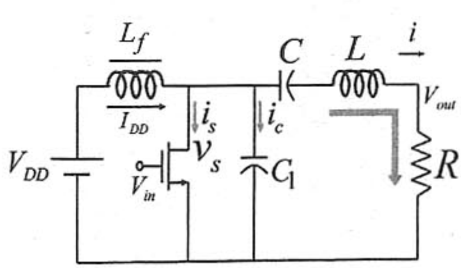


Fig. 1: Basic class E power amplifier circuit.

Class E Amplifier with Digitally-Controlled MOS Switch Array

A fully digital amplitude-controlled class-E (-like) power amplifier using an array of NMOS switches is proposed in [8] (Fig. 2). With amplitude control digital signals (d_1, d_2, d_3, d_4,...) and phase modulation signal (PM), polar modulation is realized. The output signal amplitude will change according to which switches are activated, and this is suitable for fine CMOS implementation. As is clarified later, the amplifier in Fig.2 is not an ideal class-E amplifier as it cannot achieve zero-voltage switching. This is due to the fact that the activated NMOS FETs (whose width is limited) operate as current sources and not as ideal switches. To the best of our knowledge, the efficiency of this amplifier in Fig.2 has not been clarified yet.

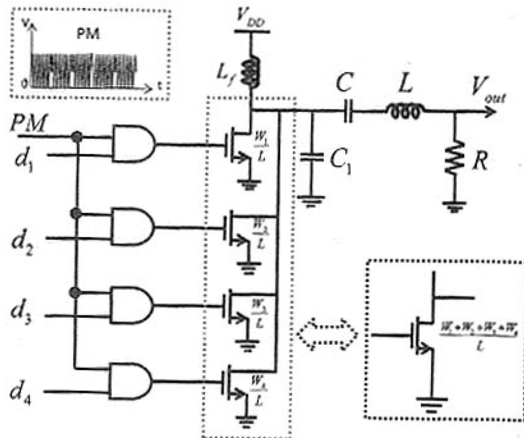


Fig. 2: Digital amplitude control with NMOS switch array.

Class-E Amplifier with Digital PWM Control

The output voltage amplitude of the class E amplifier can be adjusted by changing the switch duty cycle as shown in Fig. 3 and 4. The highest output voltage amplitude is attained with the following duty ratio:

$$D = \frac{T_1}{T_1 + T_2} \tag{1}$$

where $T_1 = 1/f_1$, $T_2 = 1/f_2$ and

$$f_1 = \frac{1}{2\pi\sqrt{LC}} \quad f_2 = \frac{1}{2\pi\sqrt{L\dfrac{C \cdot C_{tot}}{C + C_{tot}}}} \tag{2}$$

Here f_1 is the resonant frequency when the transistor is off and f_2 is that when it is on. With our design parameters, the calculated result is D=0.58 ($C_{tot} \approx C_1$), which is close to 0.65 of the simulation result. A digitally-controlled PWM class-E amplifier is proposed in [9,10], which emphasize that digital PWM with fine time resolution is relatively easy to implement with a fine CMOS process.

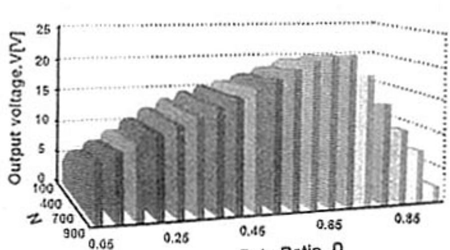


Fig.3: Output voltage and duty ratio vs. *N*

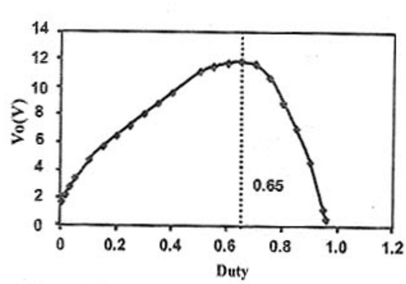


Fig.4: Output voltage vs. duty ratio.

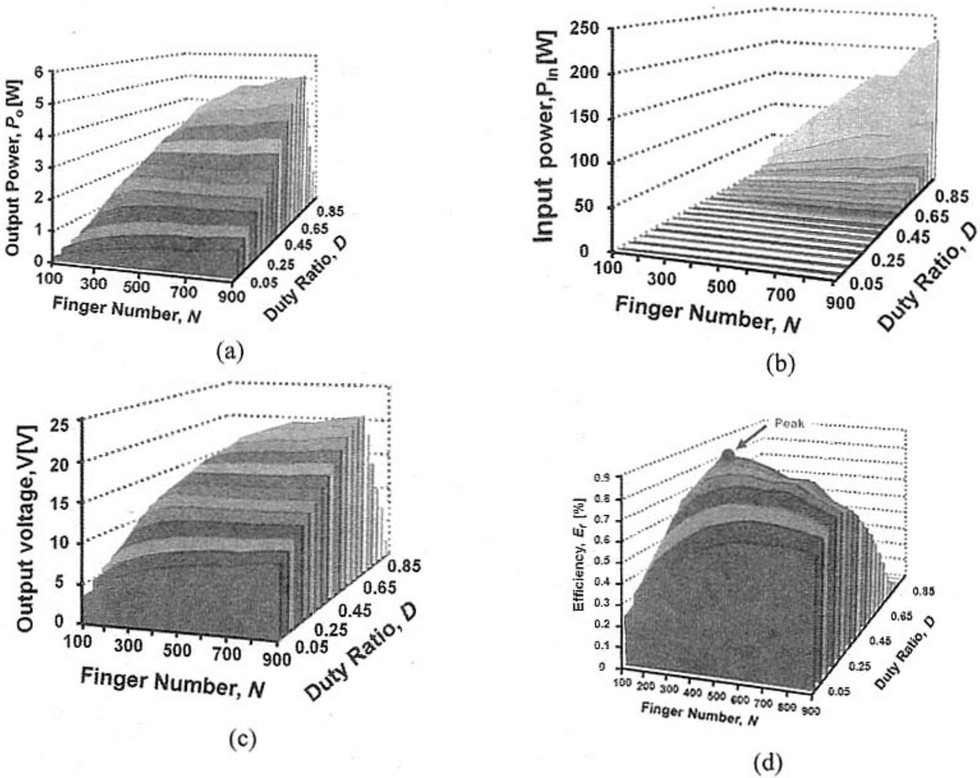
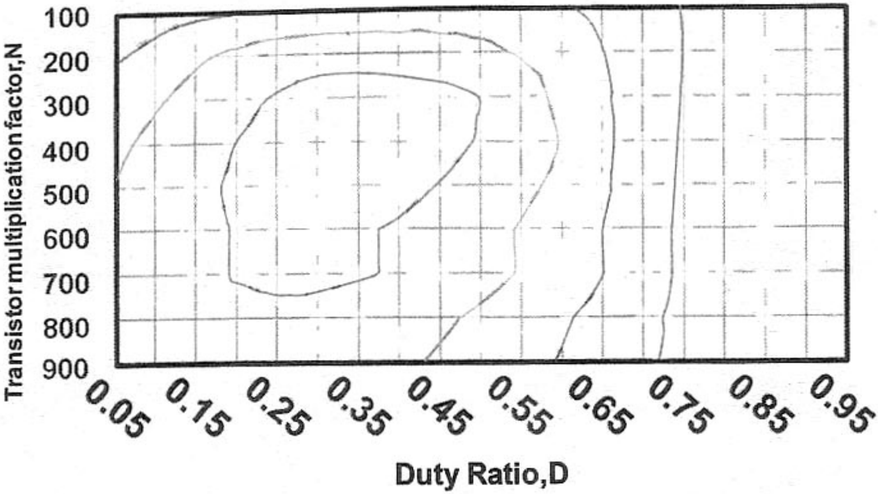
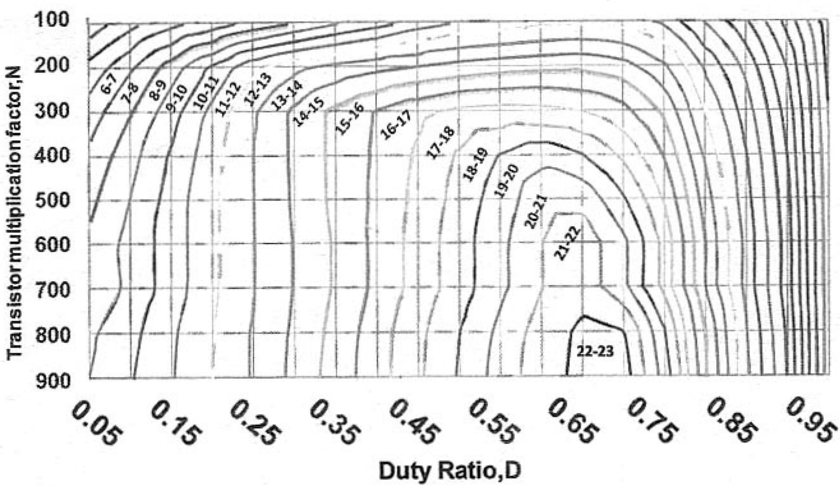


Fig.5: Relationship between number of on-state NMOS FETs, duty ratio, output voltage, input power, output power and efficiency.



(a) Constant efficiency



(b) Constant V_O contours

Fig.6: Simulation results for a class E amplifier.

Proposed Digitally-Controlled Amplifier

We aimed to design a digitally-controlled power amplifier with high efficiency. Digital control is suitable for fine CMOS implementation, but previous designs suffer from low efficiency. We have performed simulations—the results of which are shown in Fig. 5 and 6—relating NMOS FET width (the number of on-state NMOS FETs, N), duty ratio D, output voltage, input power, output power and efficiency. We see that for a given output power P_O, there can be multiple combinations of (N, D), and the efficiency is different for each. We propose the following implementation:

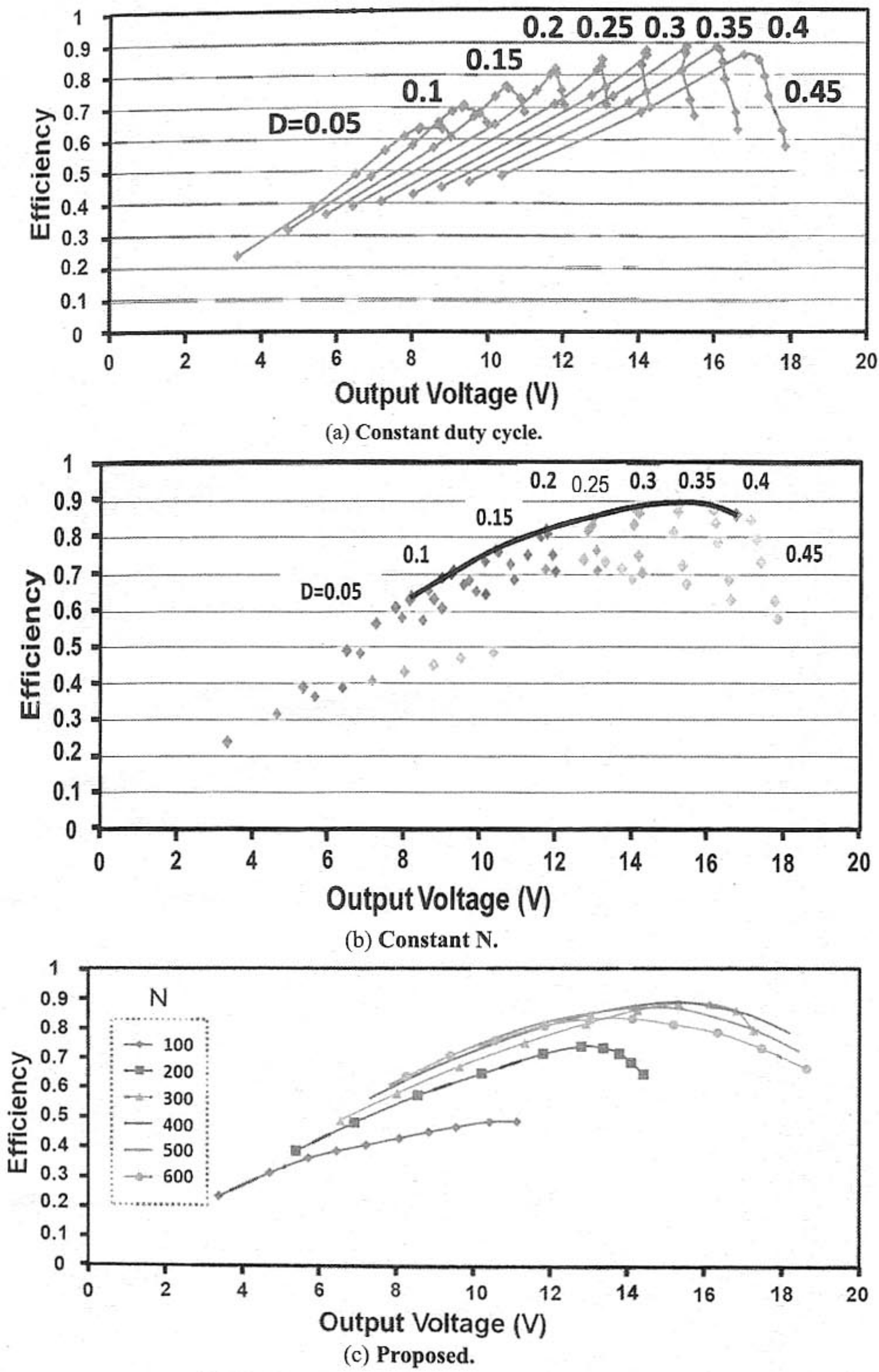
① Class E amplifier with NMOS switch array, where pulse width and position are digitally controlled.

② For each output power P_O (or output voltage amplitude V_O) store the (N, D) combination that realizes the highest efficiency in LUT memory.

③ During normal operation of the power amplifier, use stored (N, D) data with digital amplitude control for a targeted output voltage V_O, and also control the pulse position digitally for desired phase.

The above control system may be complicated, but it is relatively easy to implement with modern advanced digital technology.

Simulated efficiency with respect to output voltage is shown in Fig.7. For a targeted output voltage, the proposed method chooses N and D for peak efficiency, and we see that the efficiency of the proposed method can be higher than that for fixed N or for fixed D.



(a) Constant duty cycle.

(b) Constant N.

(c) Proposed.

Fig.7: Efficiency vs output voltage for duty ratio.

Analysis of Digitally-Controlled Amplifier

MOSFET Width, Efficiency and Output Power

There are a number of factors that affect the efficiency of the basic class E amplifier. Previous work has shown that changing either output voltage or duty cycle affects the efficiency [4, 5]. Models for the class E amplifier operating at high or low frequencies [6] have also been proposed. Our simulation results are validated by calculations (below) that explain how MOSFET width (which is equivalent to the number (N) of activated MOS switches) affects the basic class E amplifier.

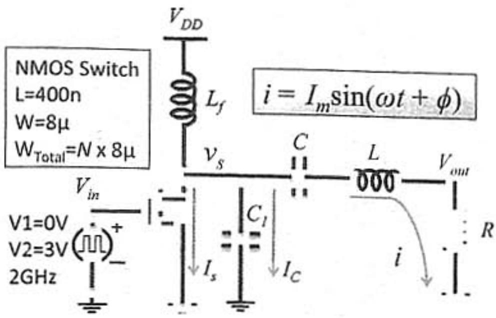


Fig.8: Simulated class E-like amplifier.

We assume that the transistor is an ideal switch in designing a class E amplifier. We are using a 0.18μm CMOS process with switching transistor parameters L=400nm, W=8μm, N=900 (total width of 7200μm) (Fig.8). Using an input voltage source V_{DD}=10V, the maximum output power is designed to be $P_{O(max)}$=5.00W with a driver signal of 2.00GHz and a 50% duty ratio using R=11.5Ω, L_f=40.4nH, C_1=1.27pF, C=1.18pF and L=6.43nH.

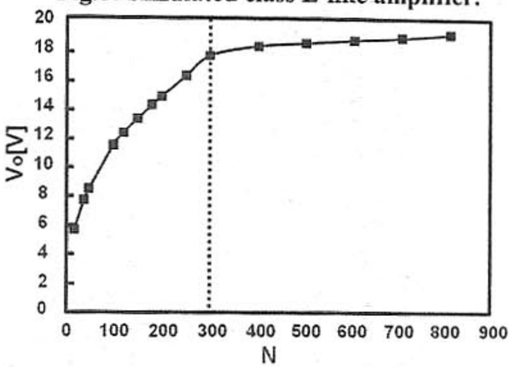


Fig.9: Effect of N on output voltage

We consider a digitally controlled amplifier in Fig.2. Fig.9 shows the effect of changing the number of on-state transistors, N.

(1) With $N > 300$, we notice that the output voltage remains approximately constant even as N increases (e.g., about 5% increase for N=800 compared with N=300). This range is used in a conventional class-E amplifier.

(2) For the range $0 < N < 300$, the output voltage increases with N, and this range is used for a digitally controlled amplifier (Fig.2)

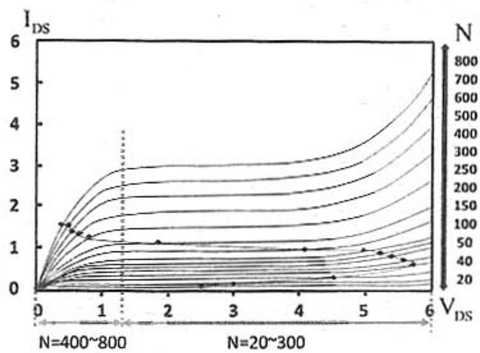


Fig.10: Switch transistor operating mode and N

For the range $0 < N < 300$, the MOSFET is seen to be operating in the saturation region, hence the drain current satisfies eq. (3):

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \quad (3)$$

When the transistor is in saturation, it can be thought of as a current source in series with a switch, which causes power loss.

Simulation results show the operating region of the switch transistor for different N values (Fig 10). The simulation shows that small transistors (N=20~300) operate in the saturation region, while large transistors (N=300~900) operate in the triode region when the transistor is on.

PWM, Efficiency and Output Voltage

It has been shown that using the switching nature of a class E amplifier can be used to improve the amplifier efficiency [1]. However, this previous analysis assumes the transistor to be an ideal switch.

It has also been shown that adjusting the duty cycle will affect efficiency [2], and an equation was provided to explain the relation between the instantaneous phase, ϕ and duty ratio. Given the duty ratio, the function $f(\phi)$ = VSM can be derived [3]. Changing the duty ratio affects the output power efficiency. Because the transistor is not an ideal switch, it has resistive power loss, since static power will be consumed when current passes through the switch. Because of this, a longer duty cycle means that the transistor is 'on' for a longer amount of time, and hence the static power consumption is larger. Changing the size of the transistor also changes the drain-to-source and gate-to-source capacitances, this affects both the output power and the signal linearity.

The work presented here focuses on how the transistor size affects the efficiency. In order to facilitate calculations, we assume $r \to \infty$. The switch turns on in the interval $0 < \omega t < \pi$, during which time the current through capacitor C_I is zero [1]. We have derived eq. (4) from the zero-voltage switching condition:

$$I_m = \frac{\frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2}{-\frac{2\cos\phi}{\pi} - \sin(\omega t + \phi)} \tag{4}$$

We notice in the above equation that increasing the width (W) of the switch transistor also increases the switch current. Since the output voltage is a function of the switch current, an increase in transistor width will also increase the output voltage as shown in eq. (5)

$$v_o = I_m \sin(\omega t + \phi) R \tag{5}$$

We have performed simulation with the parameter values in Table 1, and obtained the following:

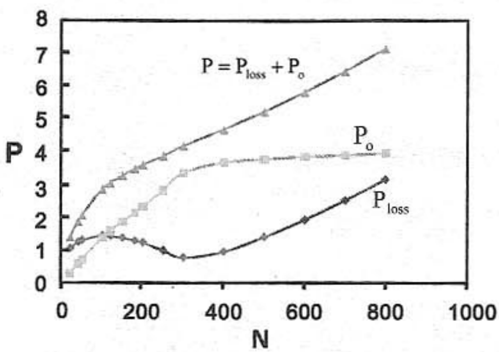
Calculation : I_S=1.40A, I_M=0.855A

Simulation : I_S=1.35A, I_M= 0.858A

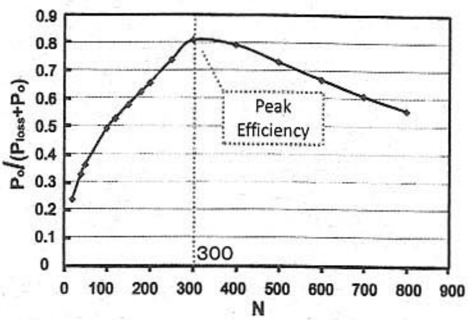
We see that theoretical and simulation results agree well.

Table 1: Parameter values used in simulation.

Simulation Parameters	
Parameter	*Value*
R	6 Ω
L	6.43 nH
C_1	1.267 pF
C	1.18 pF
L_f	40.376 nH
ϕ	π rad



(a) Output power, total power and power loss



(b) Efficiency.

Fig.11: Simulation results.

Simulation of Efficiency and Output Power

Simulation Program with Integrated Circuit Emphasis (SPICE) simulation results for output power, power loss and efficiency for a constant duty ratio are shown in Fig.11, and we observe the following:

(1) The output power changes little when the MOSFET width is larger than 300 x 8μm.

(2) As the size of the transistor is increased beyond $N = 300$, the power loss increases and hence the efficiency decreases.

(3) When the width is up to 300 x 8μm, the output power increases with MOSFET width (the digitally- controlled class E amplifier uses this region).

(4) When the size of the transistor is less than $N = 300$, the efficiency drops as N decreases. However the method we propose in Section 5 will improve the efficiency in this region.

Phase of Output Signal
We consider here the effects of duty and N on the output signal phase, and we found from simulation as follows:

For a given duty ratio D, we changed the transistor size N. For small N (N<300), the output voltage amplitude changes, but phase is little affected. On the other hand, for large N (N>300), the amplitude changes little, but the phase obviously changes.

When we use an ideal switch for the simulation, both amplitude and phase change continuously with D. Fig. 12 shows the effect of duty ratio on the output signal waveform for $(D, N) = (0.1, 400)$, $(D, N) = (0.3, 400)$. We see that both phase and the amplitude change as duty changes, which makes the pre-distortion LUT complicated [9] for separate control of amplitude and phase modulation.

Compared with PWM, using the relation between output amplitude and N for the small transistor situation is an easier way to implement amplitude modulation. As shown in Fig.13 for $(D, N) = (0.4, 75)$, $(0.4, 175)$, the amplitudes change but phase change is small.

Based on the above observation, we have to choose the best (D, N), and use pulse position control (Fig.14) to change the phase. We have to control D and N for both amplitude and phase modulation with high efficiency, which makes the LUT system complicated.

Note that there are some defined relations between duty and phase (eq. (6) and fig.15):

$$\phi = \tan^{-1}\left[\frac{\cos(2\pi D)-1}{2\pi(1-D)+\sin(2\pi D)}\right]+n\pi \tag{6}$$

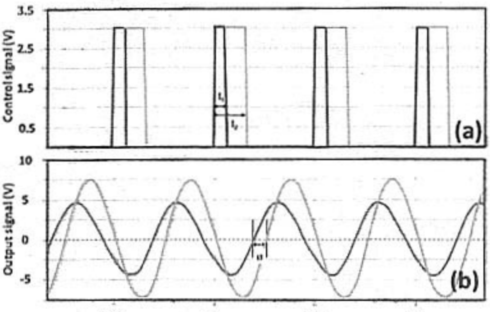


Fig.12: Simulation results for duty ratio change. (a) Gate input. (b) Output waveform.

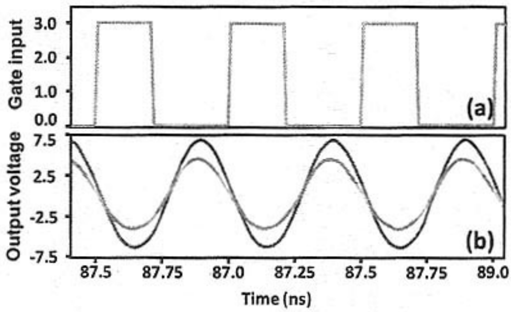


Fig.13: Simulation results for N change. (a) Gate input. (b) Output waveform.

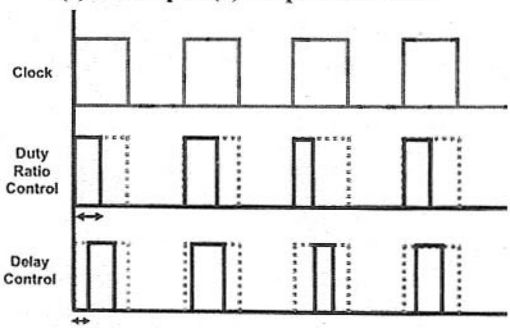


Fig.14: Pulse width modulation (PWM) and pulse position modulation (PPM)

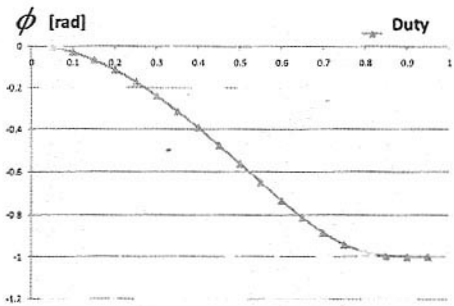


Fig.15: Duty versus phase shift

Model of Class E(-like) Amplifier

We have built a model of a class E amplifier for small as well as large MOSFETs in Fig.16 for simple and approximate calculation. Here the MOSFET is modeled by an ideal switch in series with a variable resistance and in parallel with a variable capacitor. Changing the number of on-state transistors N is equivalent to changing the resistance and capacitance values. For a small MOSFET, parasitic capacitance is small enough to ignore, and it is equivalent to an ideal switch in series with a resistor. For a large MOSFET, parasitic capacitance has a large effect, but resistance is small enough to be ignored. We have checked the accuracy of this model by SPICE simulation.

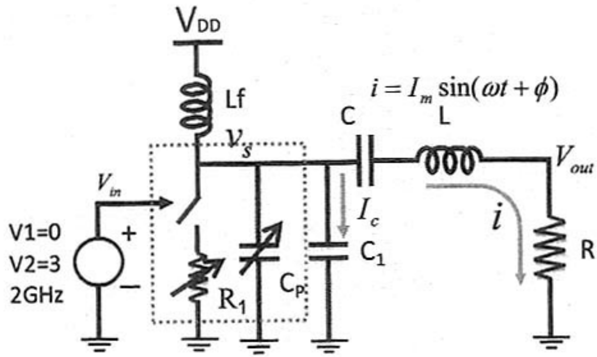


Fig.16: Model of a class E(-like) power amplifier for small as well as large MOSFETs.

Conclusions

This paper has described the analysis and design of digitally-controlled class-E(-like) power amplifiers, targeted for fine CMOS implementation. Conventional digitally-controlled class-E(-like) amplifiers use an NMOS switch array or digital PWM, but their efficiency is low; this paper proposes using a hybrid method, provided an analysis, and shows by simulation that it can maximize efficiency. Accordingly, when the amplifiers are operated at 35% duty cycle, the efficiency can reach a maximum of 89% with N=400, though the efficiency drops to 45% and 67% with N=100 and N=900 respectively. Using PWM control (together with PPM for phase control), a large enough N to achieve a high voltage output and NMOS switch array control for a low output voltage, we are able to achieve both a wide output voltage range and high efficiency.

Acknowledgement

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