BRIEF PAPER *Special Section on Analog Circuits and Related SoC Integration Technologies*

Design for Testability That Reduces Linearity Testing Time of SAR ADCs

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SUMMARY This brief paper describes design-for-testability (DFT) circuitry that reduces testing time and thus cost of testing DC linearity of SAR ADCs. We present here the basic concepts, an actual SAR ADC chip design employing the proposed DFT, as well as measurements that verify its effectiveness. Since the DFT circuit overhead is small, it is practicable.

key words: *SAR ADC, testing, DC linearity, design for testability, built-in self-test*

1. Introduction

Successive Approximation Register (SAR) ADCs are now widely used in applications — such as automotive electronics, factory automation, and pen digitizer applications — that require low cost, low power, medium speed, high accuracy and high reliability [1]–[6]. Such ADCs need to be production-tested using automatic test equipment (ATE); testing of DC linearity is very important, but testing of high-resolution low-sampling-rate SAR ADCs takes considerable time. This brief paper describes design-for-testability (DFT) circuitry that enables DC linearity testing time to be reduced. We have implemented the proposed DFT circuitry in an SAR ADC, and our chip measurement results validate the concept; the DFT circuit overhead is small, so it is practicable.

2. Proposed DFT for SAR ADC Linearity

An SAR ADC consists of a sample and hold circuit, a comparator, a DAC, a timing generator and SAR logic circuit, and operates based on the principle of a balance (Fig. 1). When testing high-resolution ADCs, DC linearity is one of the most important test items, and any method of reducing testing time while maintaining test accuracy can reduce testing cost [7], [8].

When testing the SAR ADC, we know (that is, we can control) the analog input value at each sampling time, so we can reduce the number of SAR conversion steps (and hence the SAR ADC DC linearity testing time) by preadjusting the reference voltages accordingly. We here describe circuitry that can be built into the SAR ADC to enable such adjustment of the reference voltage to be performed during testing.

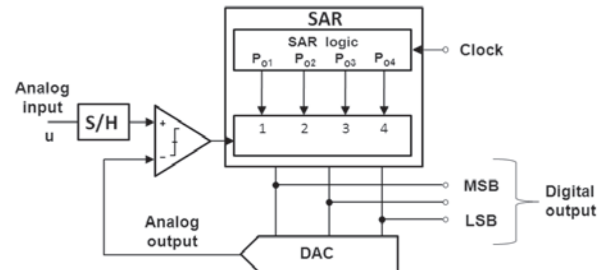

Fig. 1 Block diagram of an SAR ADC.

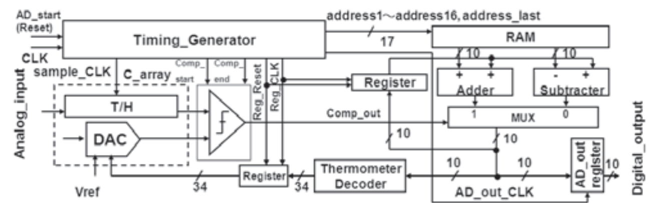

Fig. 2 Block diagram of our SAR ADC prototype with weighting coefficients RAM.

As shown in Fig. 2, the reference voltage levels that correspond to testing-time DAC inputs are stored in the RAM (or ROM) of our SAR ADC. For DC linearity testing, suppose that the SAR ADC is supplied with a staircase ramp input with very slow slope so that the value of the ramp input is controlled (known) at each sampling time, and suppose that the SAR ADC (5-bit, 5-step in this example) would normally use a 4-step binary search algorithm during testing to confirm that linearity is acceptable. Since we know the input value at each test point, if we preadjust the corresponding comparator reference voltages to values close to the input voltages, then we do not need a 4-step algorithm; fewer steps (say, 2 steps) will be sufficient, as illustrated in Fig. 3.

This reference voltage adjustment can be implemented with a small test-mode RAM (or ROM), a multiplexer, a programmable ring counter in the timing generator, plus a digital controller (Fig. 4); in test mode, an ATE can play the role of the digital controller, and the design may share the test mode RAM with the normal mode RAM. (The overhead chip area for the DFT was less than 3% in our SAR ADC design.) Fig. 5 shows its operation.

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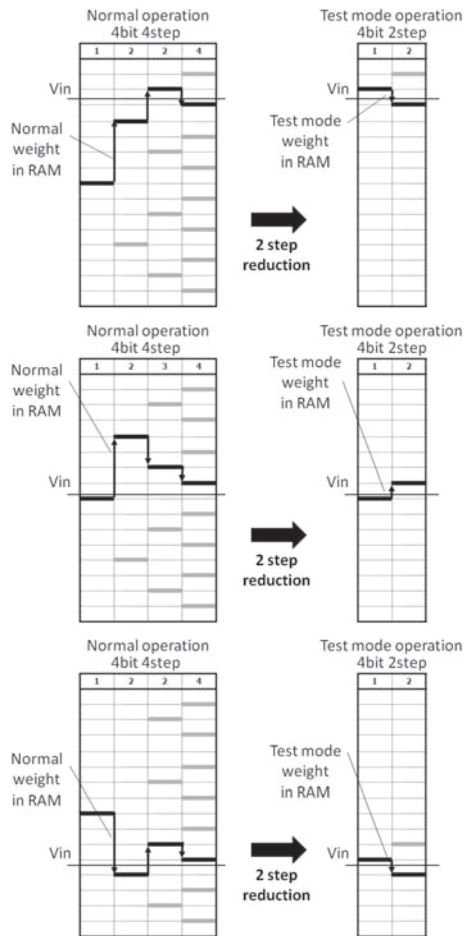


Fig. 3 Operation of SAR ADC with built-in test circuitry — the number of SAR ADC steps can be reduced from 4 to 2 in DC linearity test mode by preadjusting Vref corresponding to known value of analog input Vin.

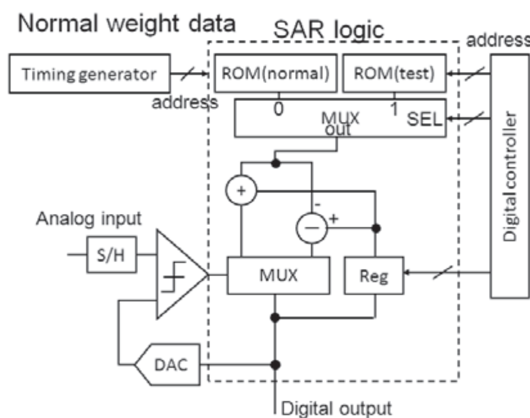


Fig. 4 SAR ADC with built-in circuitry to reduce DC-linearity testing time. The digital controller can be in an ATE.

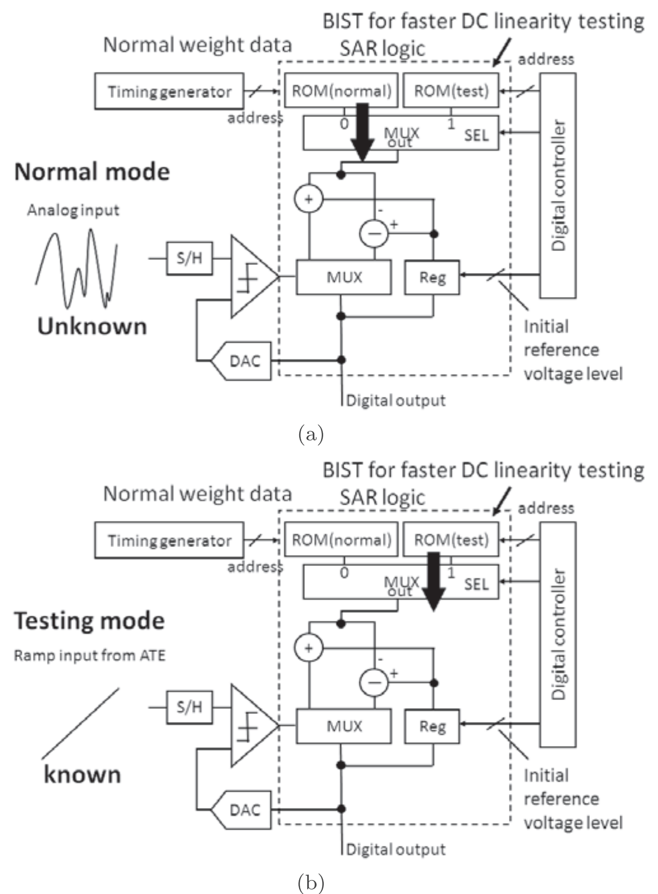


Fig. 5 Operation of the proposed built-in circuitry in Fig. 6. (a) Normal mode. (b) Test mode.

We note that testing and measurement are similar but different technologies. When measuring, the analog input value is uncontrollable and unknown. However, when testing, it is controllable and known.

For an actual 10-bit binary search SAR ADC whose INL may be expected to be within ± 8 LSBs, we found that the number of SAR ADC steps required at each test voltage could be reduced from 10 to 4. In our experience with an ATE, the ratios of the DC linearity testing time, SINAD testing time and ADC set up/data transfer time may be 88%: 9%: 3% in case of a 10 bit 100 kS/s SAR ADC (Table 1) [9]. Hence we can reduce testing time by approximately half using the above testing methodology.

Table 1 Typical ADC testing time with ATE.

	Content	Time
1)	Setup time for module	less than 1 msec
2)	Settling time for module and DUT	several msec
3)	DC linearity testing time	$2^{bit} \times (16 \sim 64) \times$ (ADC conversion time)
4)	SINAD testing time	$2^{bit} \times (1 \sim 4) \times$ (ADC conversion time)
5)	Time for data transfer and operation	several msec
6)	Other test time	several msec

Table 2 Our SAR ADC chip performance.

Resolution	10 bit
ENOB	9.5 bit
Sampling Speed	upto 3 MHz
Supply Voltage	1.5 V
Power Consumption	5.1 mW@3 MS/s
Technology	180 nm CMOS

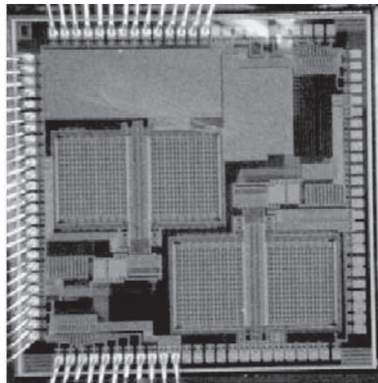


Fig. 6 Photo of chip (2.5 mm × 2.5 mm) with two SAR ADCs.

3. Chip Implementation and Measurement Results

So far we have done a brief validation of this methodology using a chip implementation of our SAR ADC that includes the additional testing-specific circuitry. Its performance summary is shown in Table 2, and its chip photo is shown in Fig. 6. Our measurement results in Fig. 7 show that the ADC output after 4 steps in testing mode is comparable to that after 10 steps of normal binary operation, which seems to validate the basic concepts of this testing methodology; the data in Figs. 7(a), (b) are almost the same if noise effects are removed.

4. Discussion

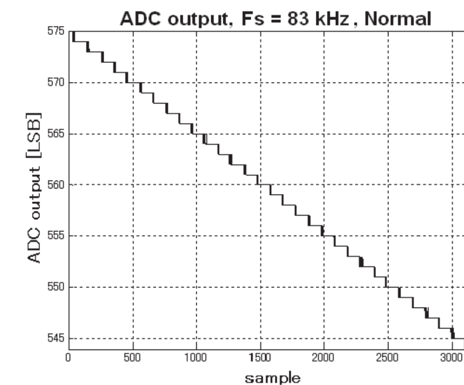
(i) The higher the resolution and the slower the sampling rate of an SAR ADC, the longer its linearity testing takes. The proposed testing method is effective in reducing testing time when overhead time for reference voltage presetting in test mode, e.g. when measuring SAR ADC offset and gain, is comparatively small [9].

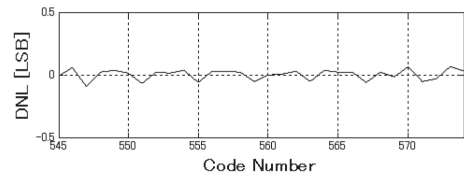
(ii) For high-speed sampling SAR ADCs, the proposed method cannot take care of the DAC output incomplete settling problem in earlier stages [3]–[6]; however in such cases, the SAR ADC can be tested in normal mode (not using the proposed method) because high-speed sampling ADC linearity testing time is relatively short.

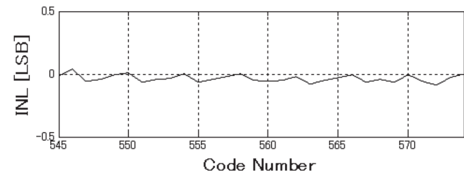
(iii) The DC linearity testing time of an n-bit ADC with sampling frequency of f_s is given as follows (Table 1):

$$(16 \sim 64) \times 2^n / f_s$$

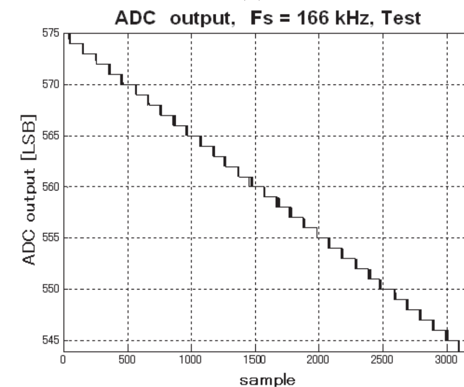
We assume here that a testing time of 1 sec. for a one-dollar chip is reasonable, and also that most of the ADC testing

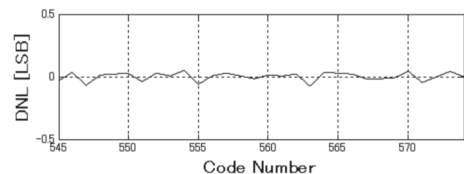


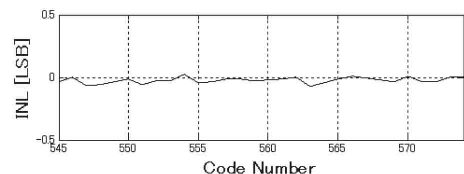




(a)







(b)

Fig. 7 Measurement results of 10 bit SAR ADC chip with built-in circuitry for reducing DC linearity testing time. (a) Normal mode (10 steps). (b) Proposed test mode (4 steps).

time is for DC linearity testing [9], [10]. If up to 200 msec is allowed for ADC testing time, then it would be preferable to use DFT for DC linearity testing for $f_s < 80$ kS/s ~ 320 kS/s in 10-bit ADC case, and $f_s < 320$ kS/s ~ 1.28 MS/s in 12-bit ADC case.

(iv) The proposed method uses fewer SAR ADC steps during testing, so it might be thought that noise contribution inside the SAR ADC circuit could conceivably cause errors. However, DNL is usually determined by the ramp histogram method, which has a noise-averaging function, so underestimation of noise effects on DNL is unlikely to be a problem. The noise floor of the SAR ADC can be found by applying a sinusoidal analog input and evaluating the output power spectrum using FFT - the time required for such testing would be quite short for high-resolution SAR ADCs.

(v) We would like to call to the reader's attention that while the proposed method uses embedded design-for-testability circuitry, the same functionality could be realized using an on-chip microcontroller [11]. When the SAR ADC chip contains an embedded microcontroller, such a microcontroller-assisted technique could be used. However, we note that our method does not require the microcontroller, and the circuit overhead for the proposed DFT is small; also, if there is an on-chip microcontroller, our proposed method allows the ADC and microcontroller to be tested in parallel.

(vi) An industry source [12] says that in his world of very large SoCs, analog circuits make up a small portion of the nodes, but represent 70% of the test costs and 45% of the test development time, thus analog design-for-testability (DFT) and built-in self-test (BIST) — such as proposed here — are likely to be increasingly adopted to reduce SoC testing costs.

5. Conclusions

We have described the DFT circuitry embedded in an SAR ADC for reducing DC linearity testing time. Since the circuit overhead for the DFT is small, it is practicable. Prototype chip measurements validate the basic concepts.

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