Architecture of High-Efficiency Digitally-Controlled Class-E Power Amplifier

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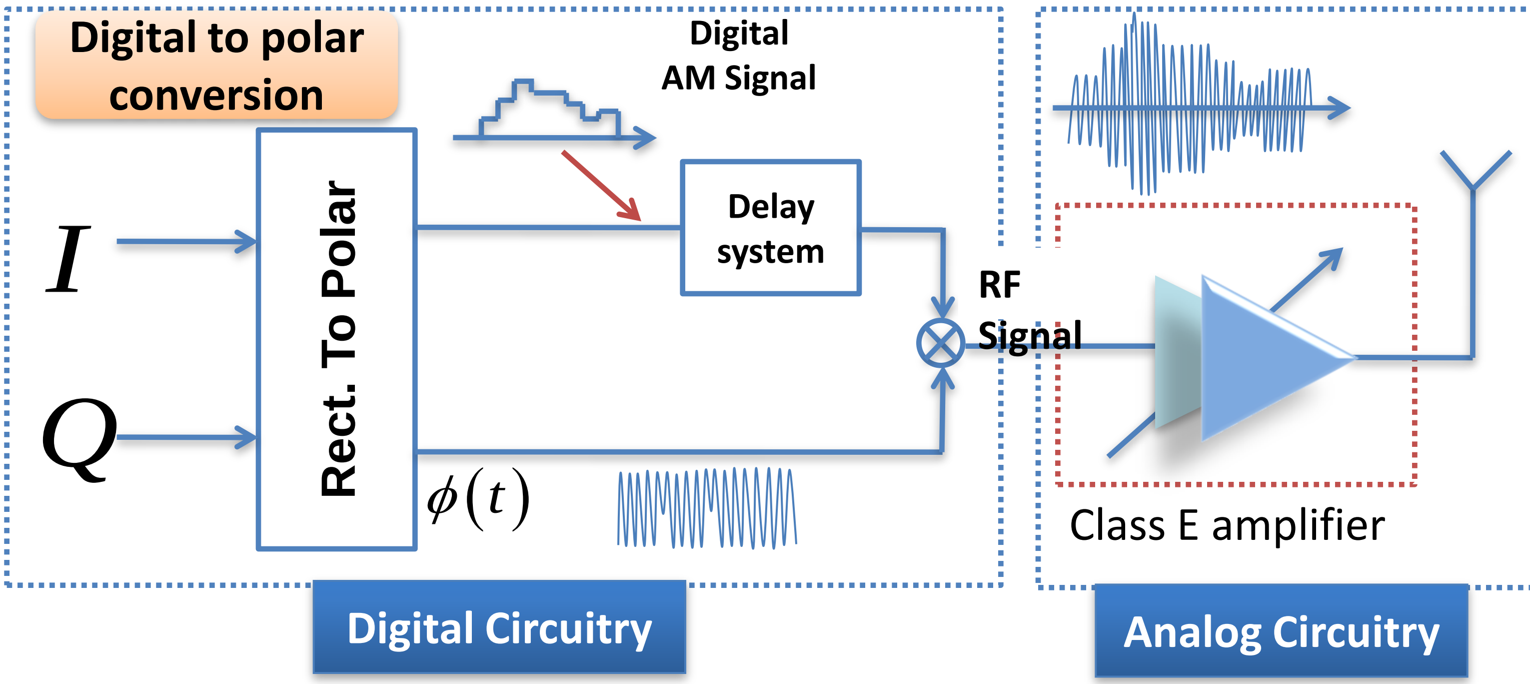
Research Background

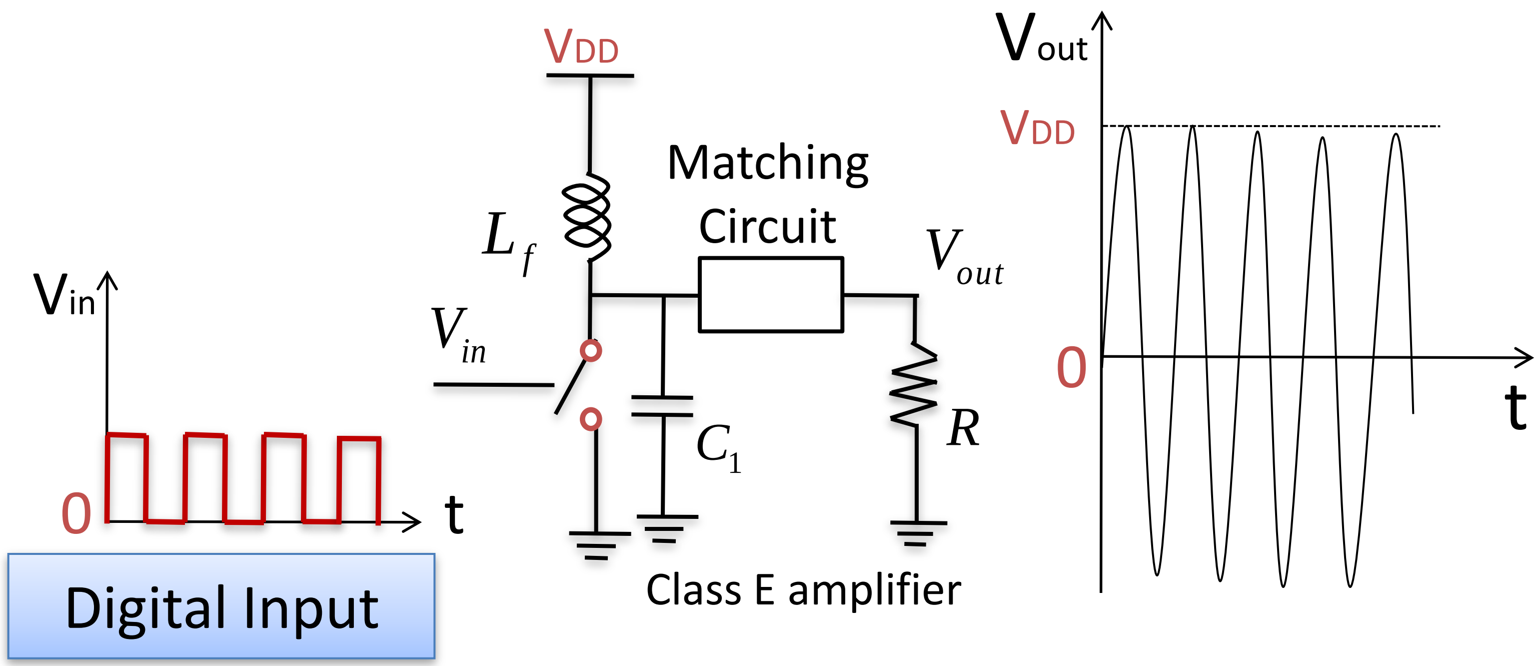
Realization of High Efficiency in Wireless Communication Systems



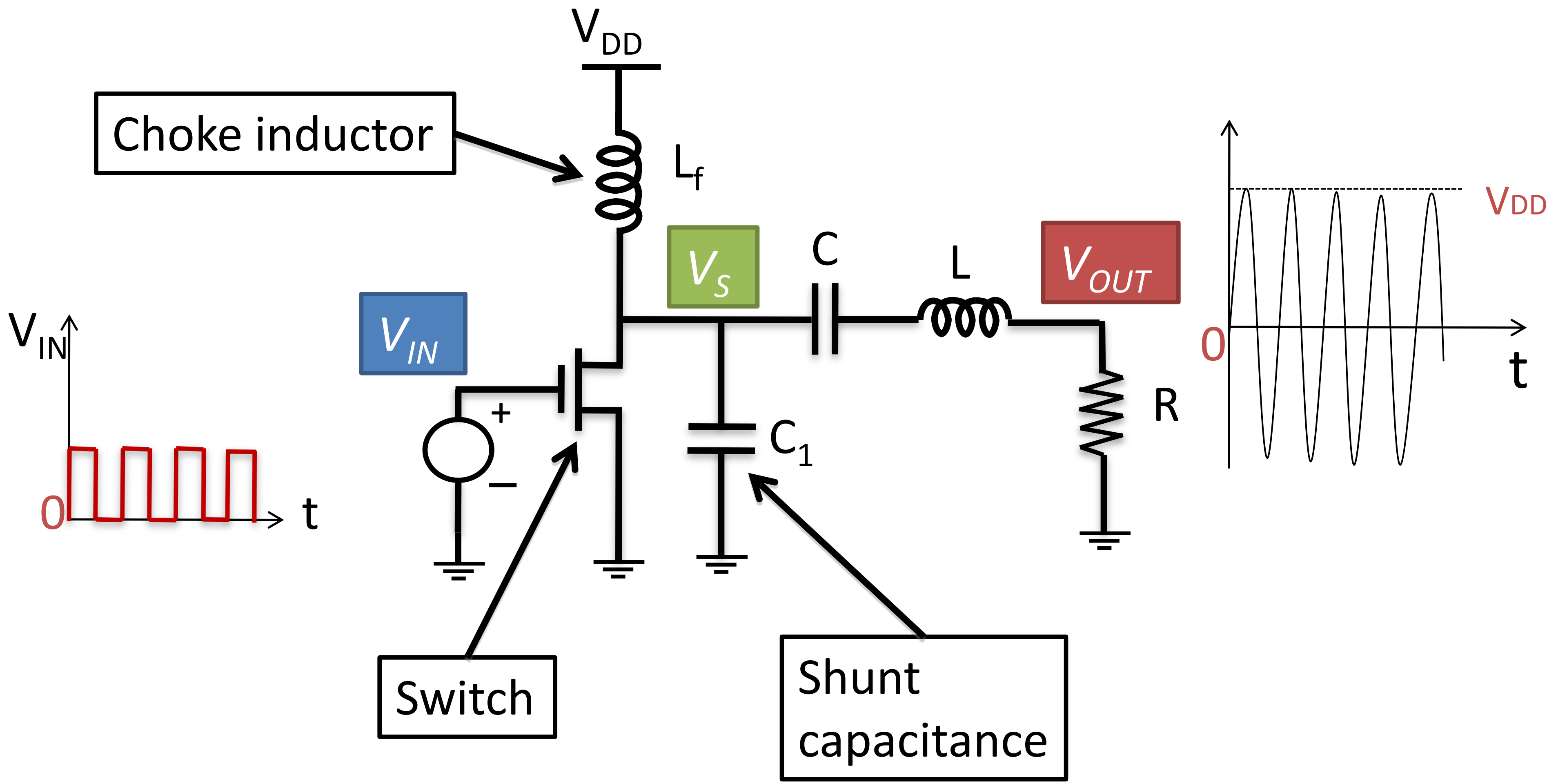
Amplitude modulation through digital control
Power amplifier can be implemented in fine CMOS

Class-E Amplifier Architecture

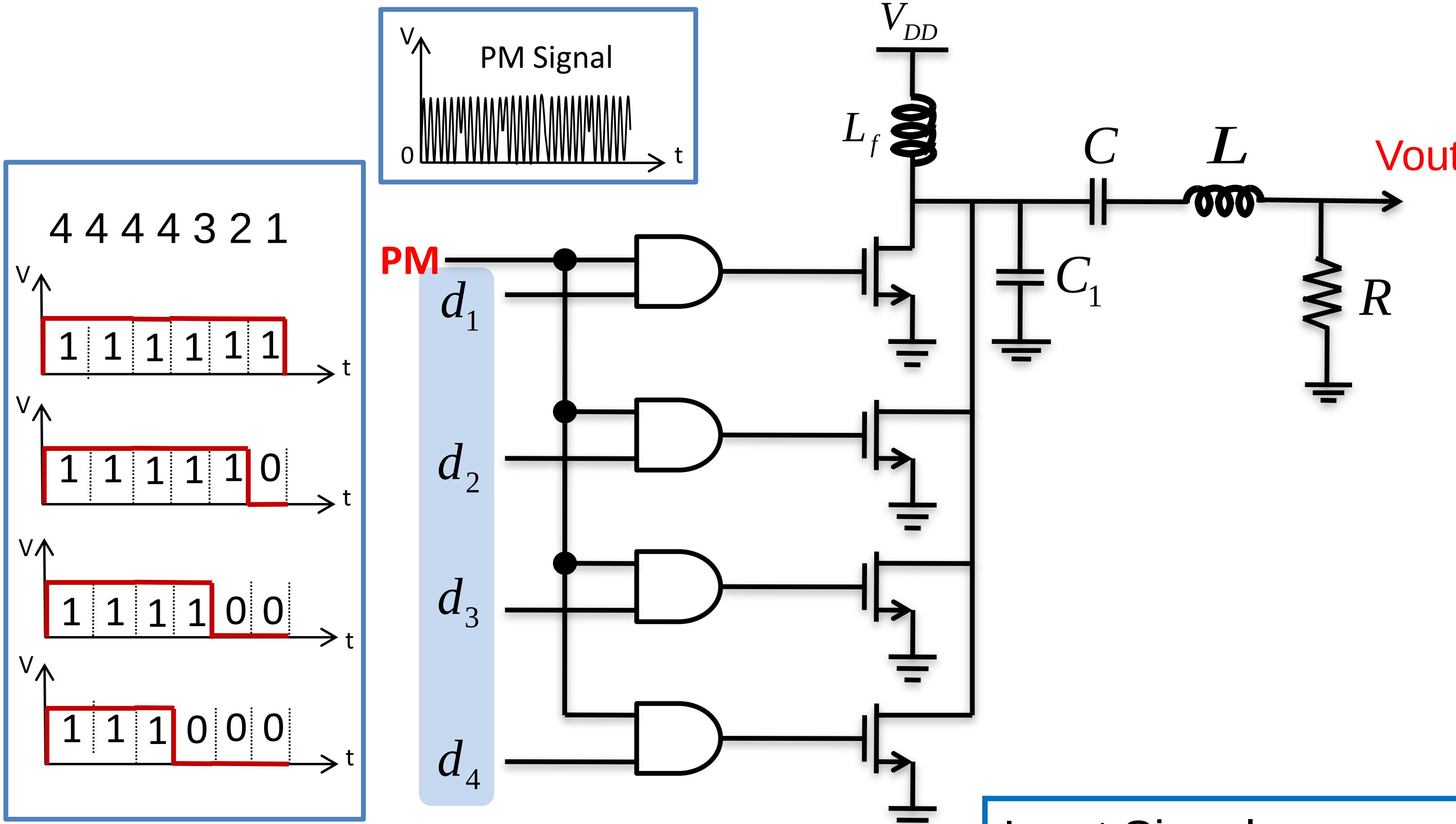
- High efficiency
  - Uses Zero Voltage Switching (ZVS)
- Can be controlled via digital input



Basic Class-E Amplifier Schematic



Digital Control of Output Voltage



Input Signal Plot

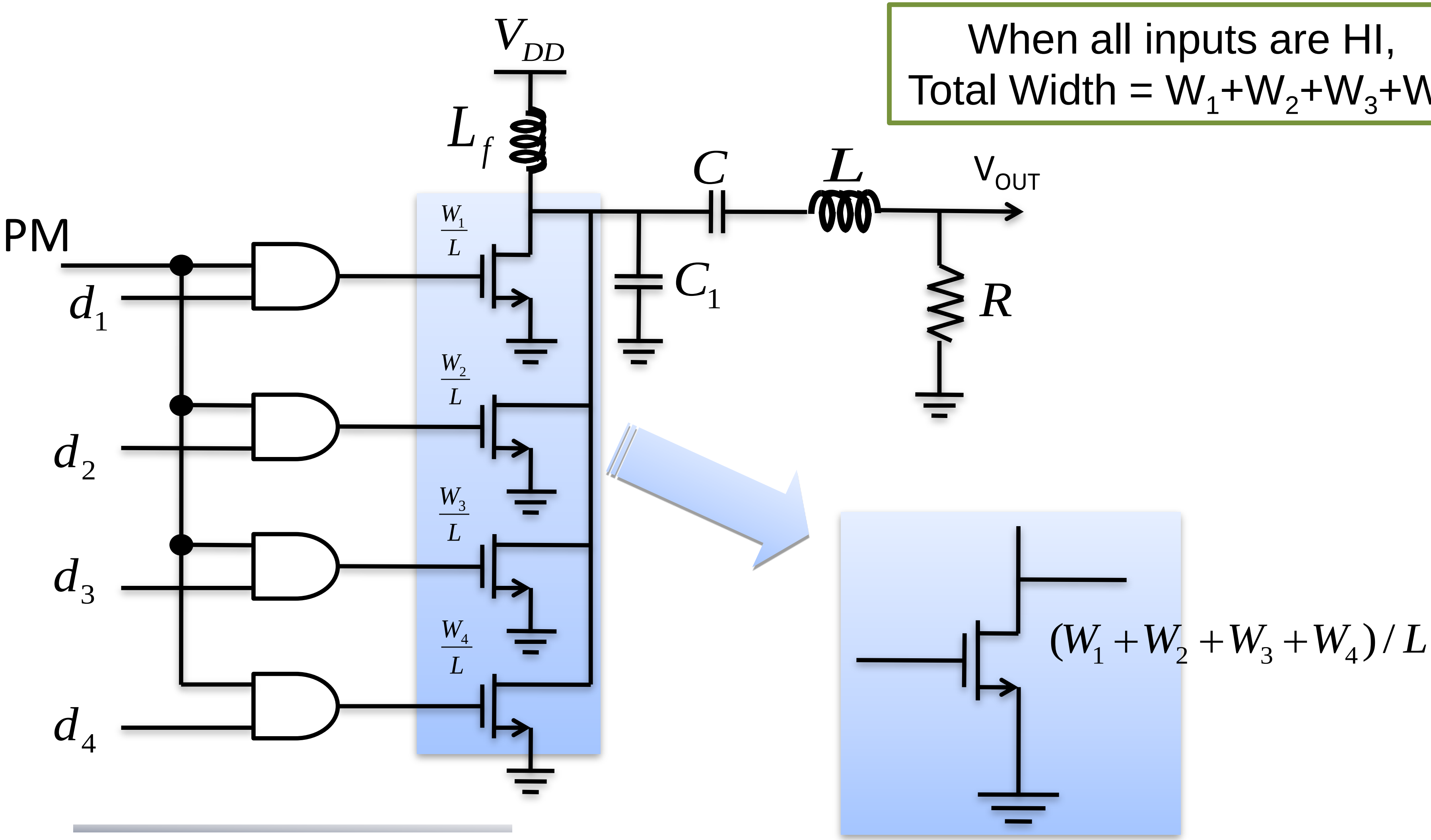
Input Signals

Phase: PM

Amplitude: d_1, d_2, d_3, d_4,…

Digital Control Structure

When all inputs are HI,
Total Width = $W_1+W_2+W_3+W_4$



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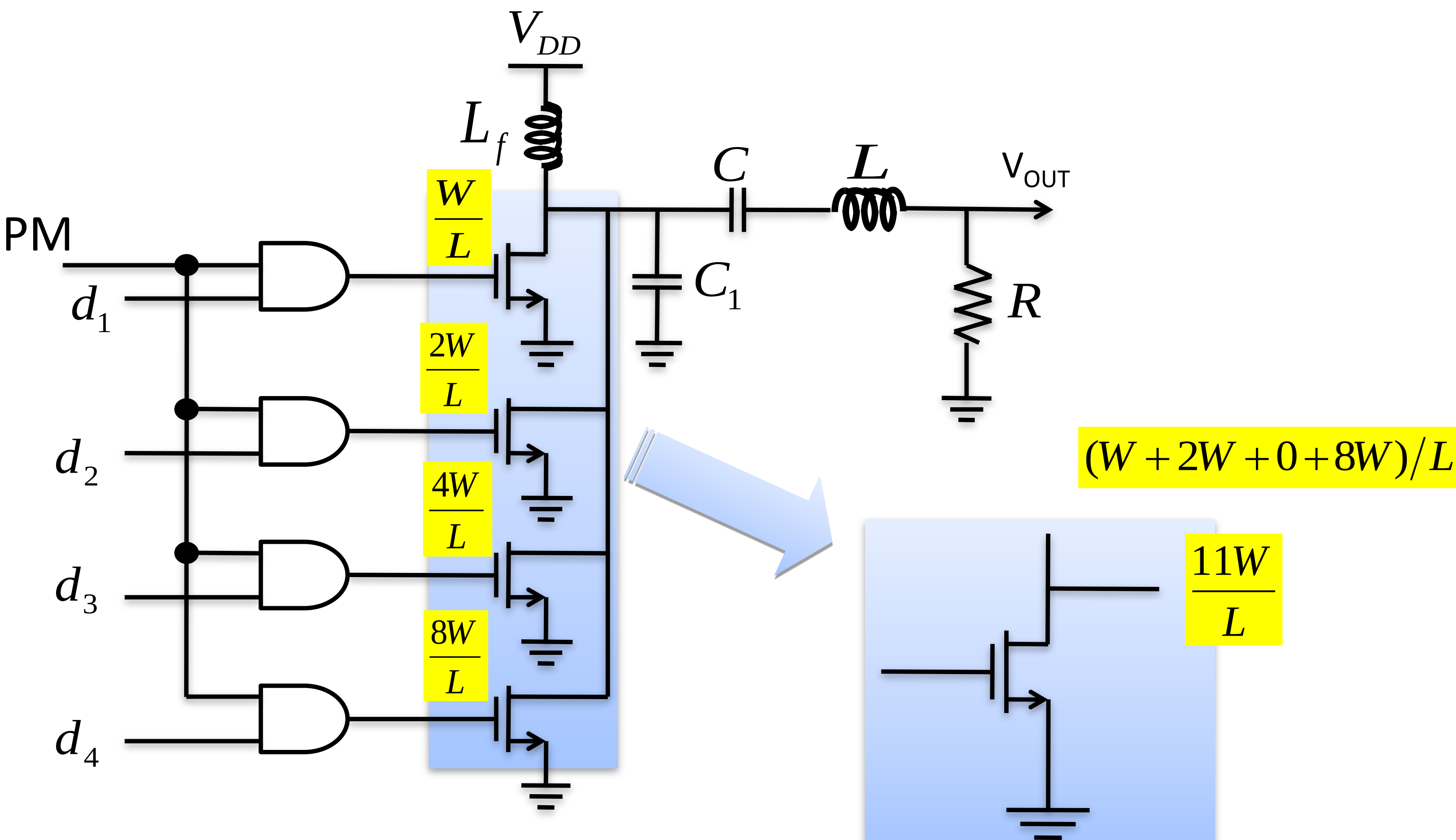
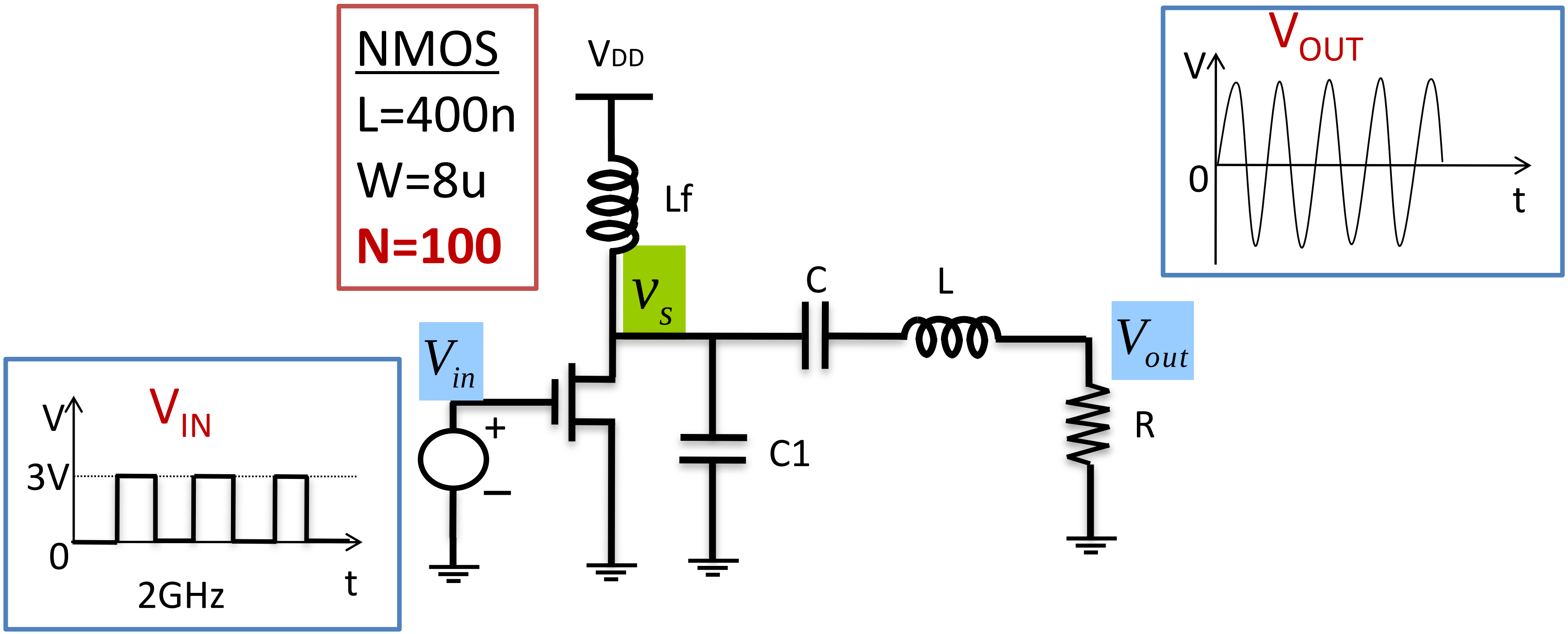
Binary-Weighted Transistor Size Example



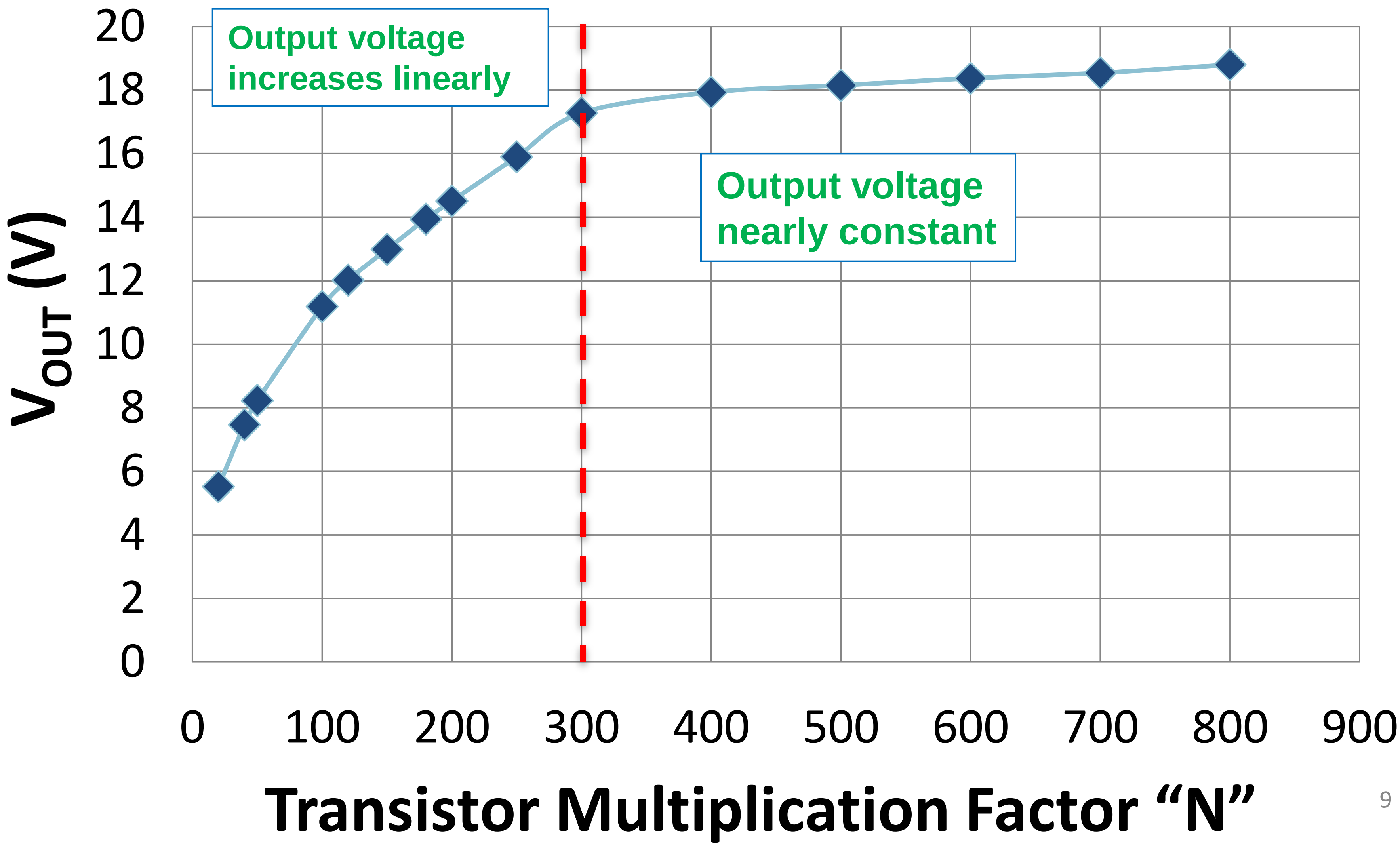
Effect of Total Width on Output Voltage



Note: N is the transistor multiplication factor

$$W_{total} = NW$$

Simulation: Effect of N on V_{OUT}



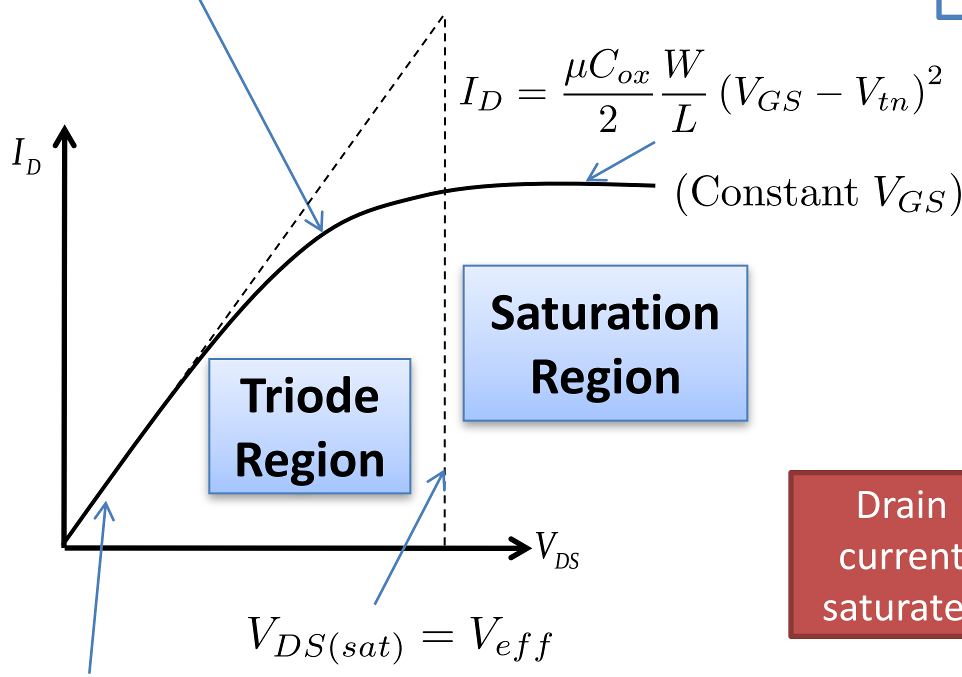
Output Voltage Modulation Investigation

- Large transistor (N>300)
  - Typical class-e amplifier
    - Output voltage constant
    - Transistor acts nearly like an ideal switch
- Small transistor (N<300)
  - Output voltage increases linearly with N
    - Can be exploited to implement digital control

Why does the transistor size affect the output voltage?

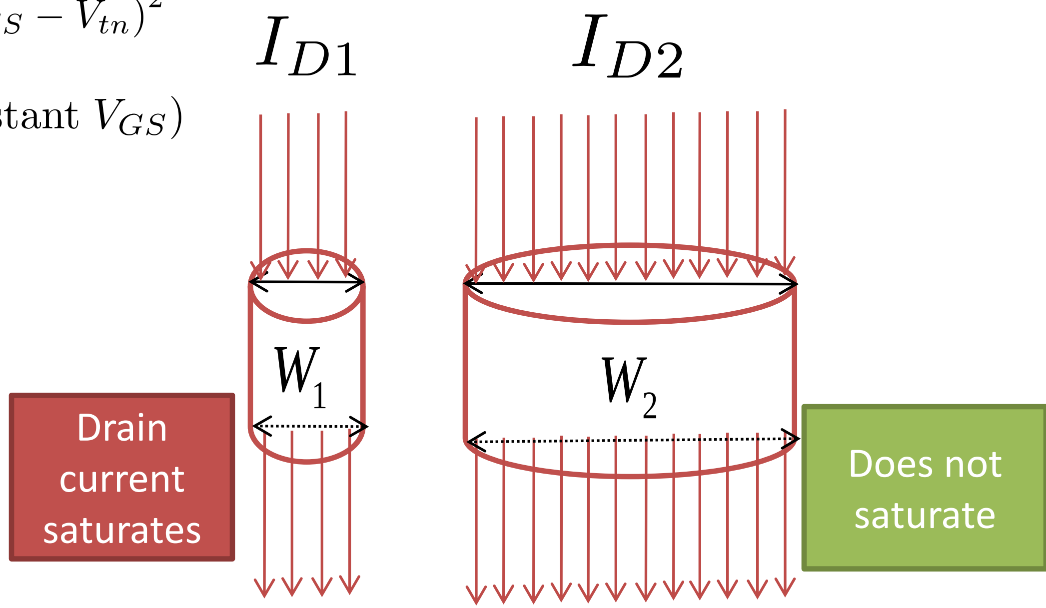
MOS Transistor Drain Current Characteristic

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$



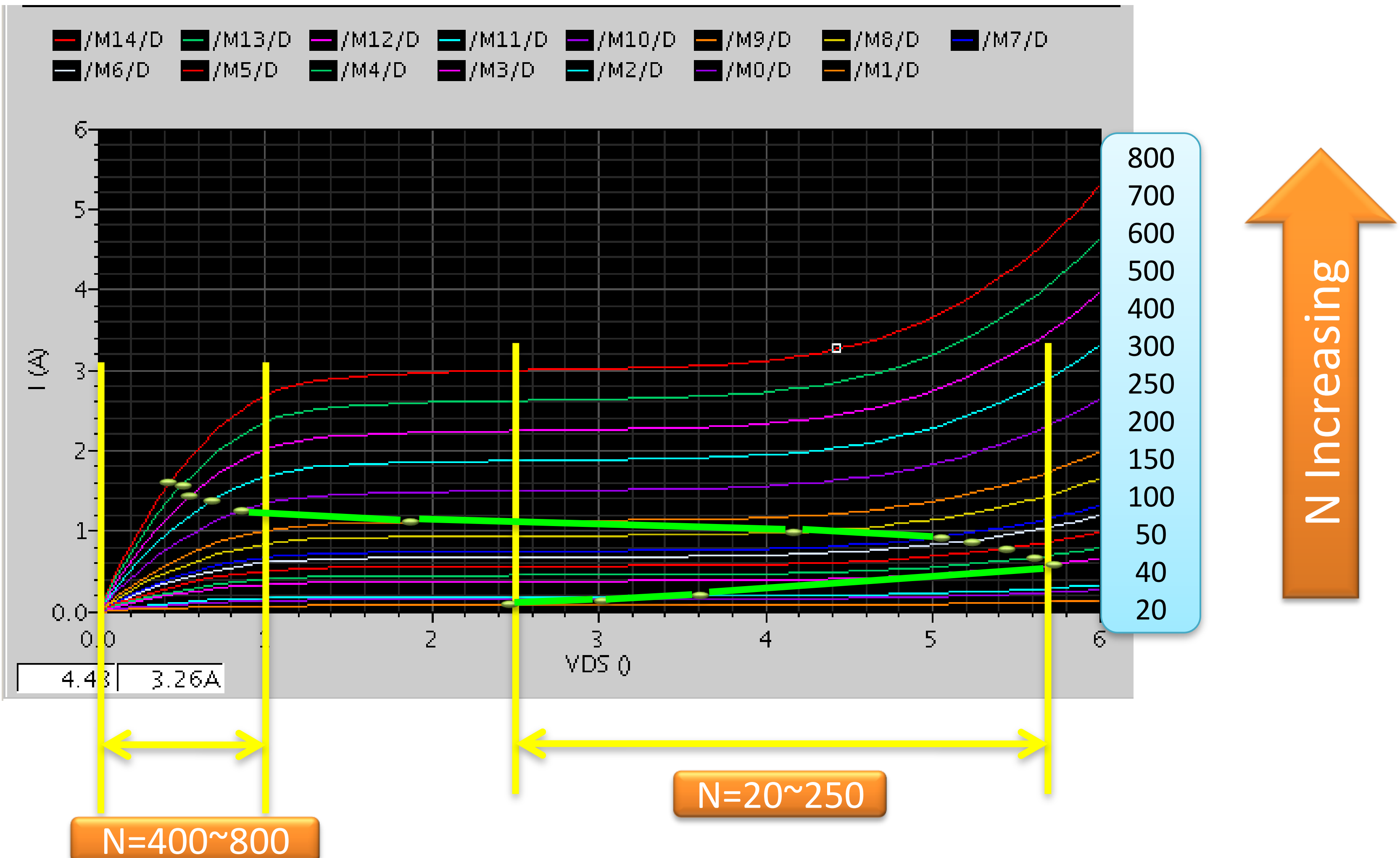
$$I_D \approx \mu C_{ox} \frac{W}{L} (V_{GS} - V_{tn}) V_{DS}$$

W increases ⇒ I_D increases



With a small W, the drain current tends to saturate

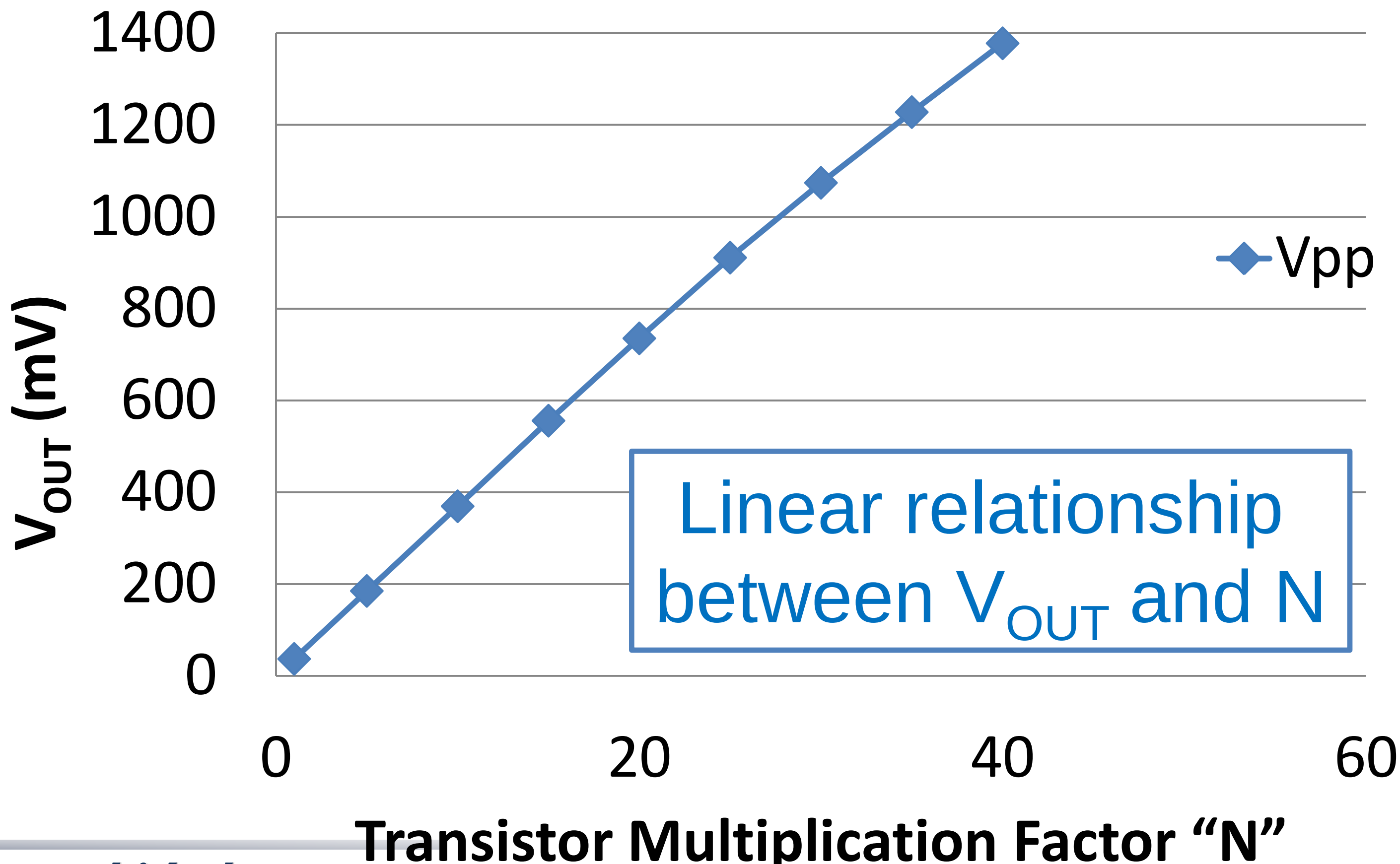
Relation Between MOS Current and Total W



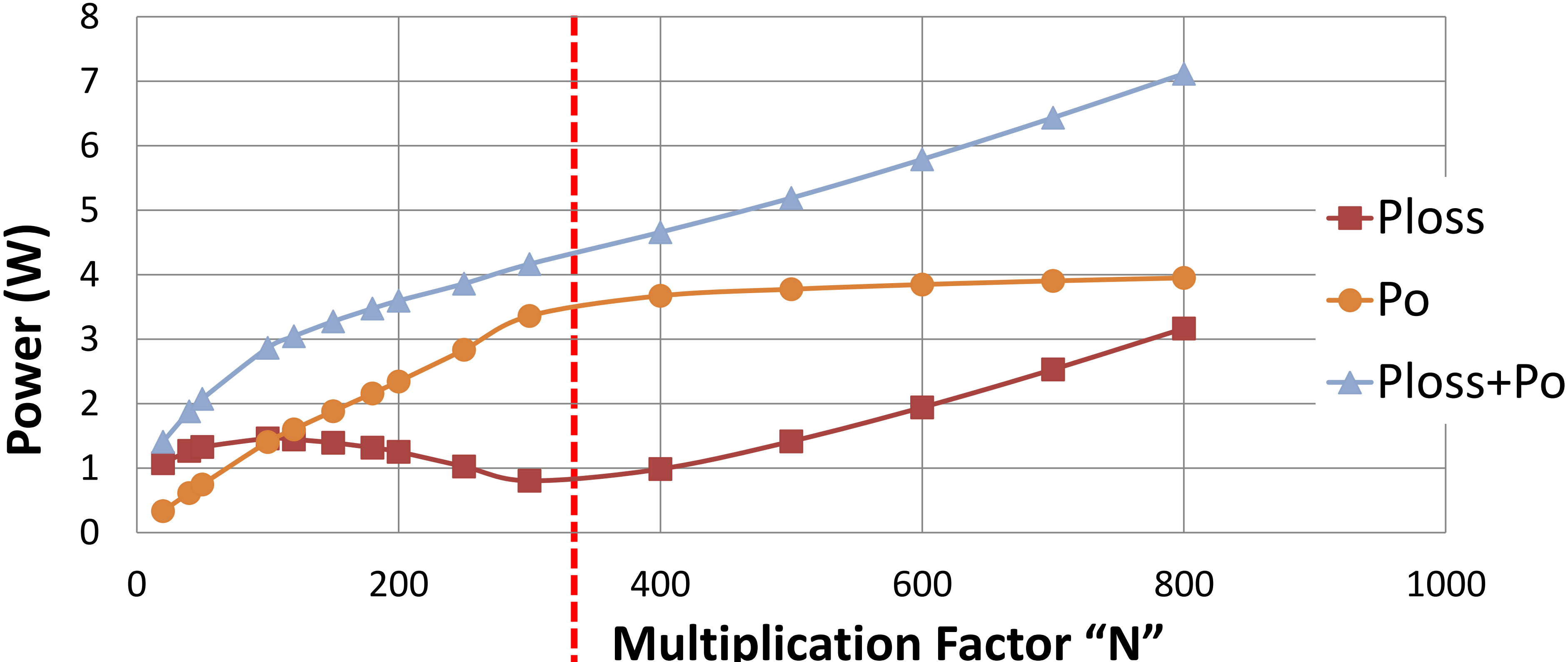
N increases ⇒ Drain current increases

Foundations for Digital Control

Note: not operating with ZVS
Not a true class-e amplifier



Output Power and Efficiency



-Output power increases linearly with N

-Losses increase linearly with N
-Output power nearly constant

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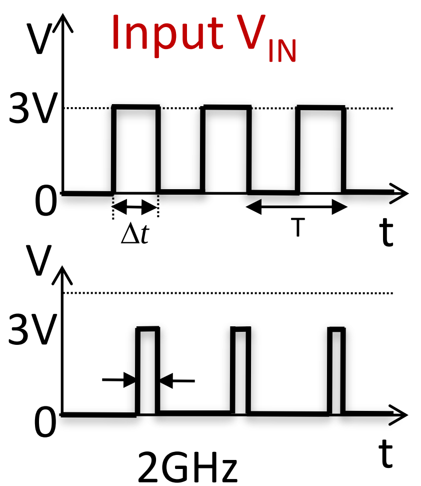
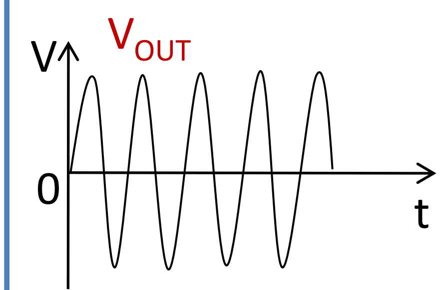
Controlling Input Duty Ratio

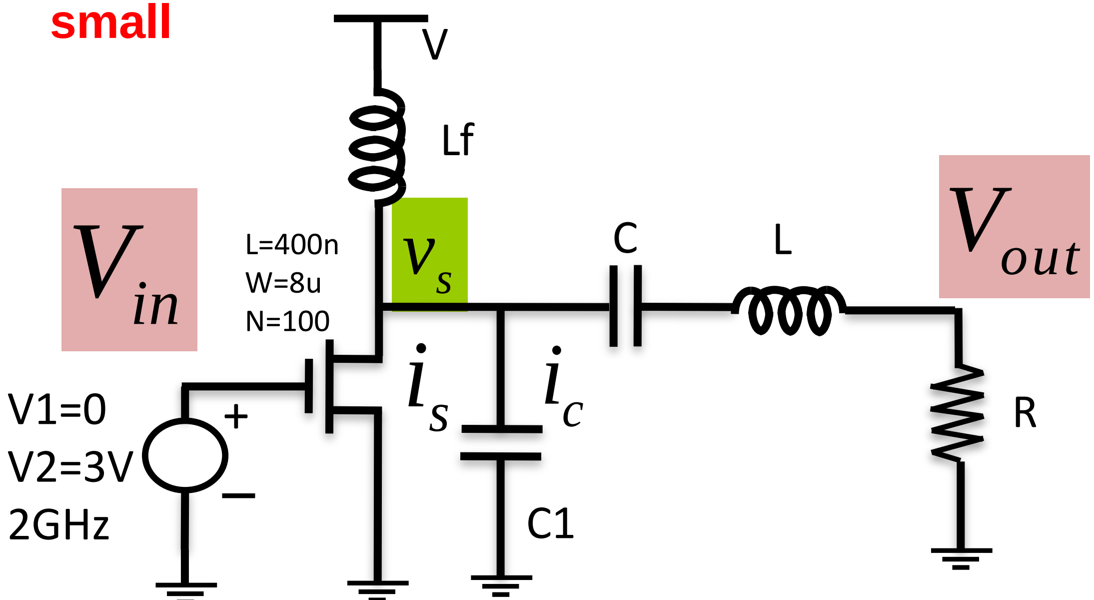
PWM Signal



Duty Ratio
BIG

Duty Ratio
small



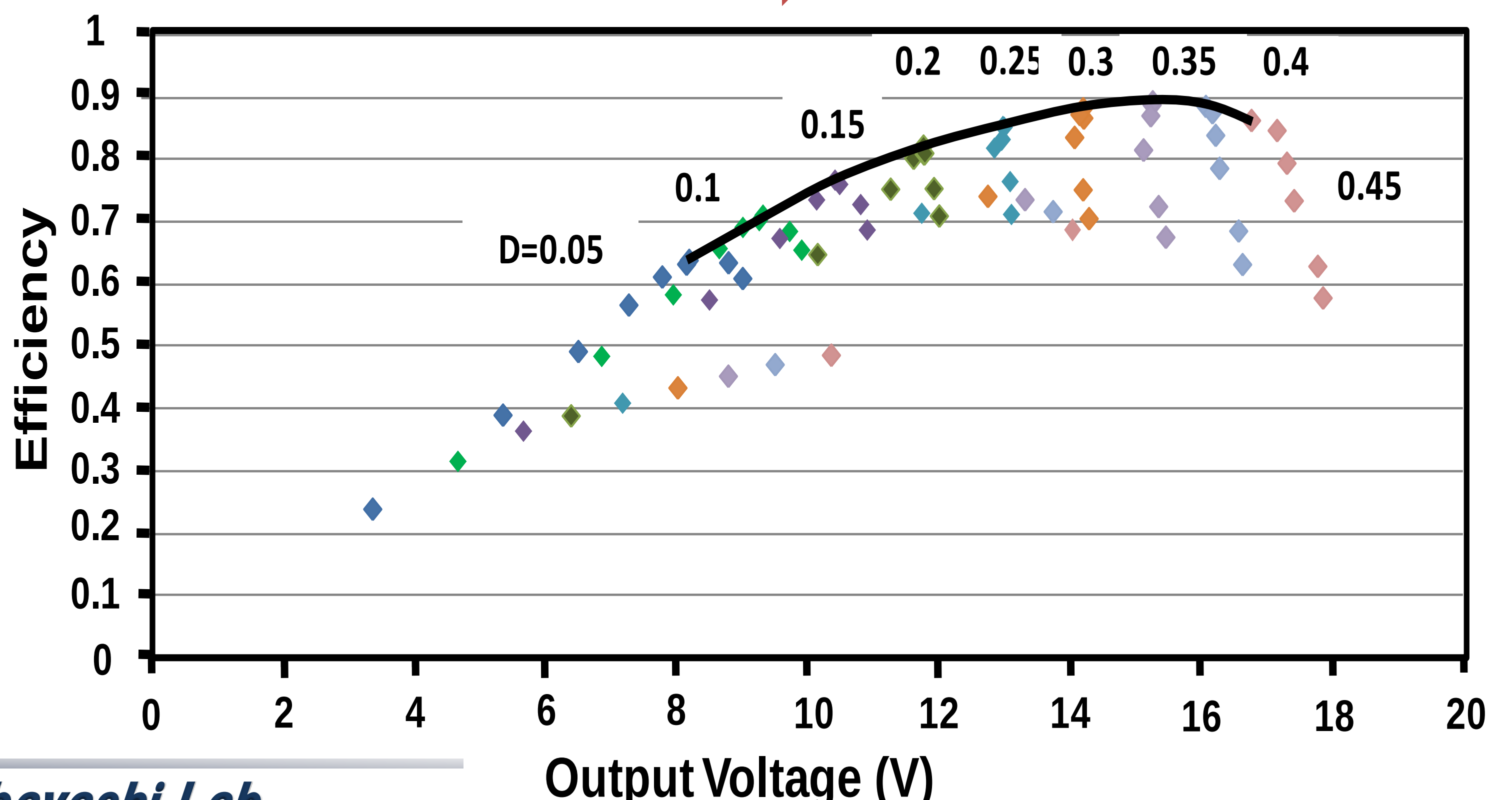


Duty Ratio= $\frac{\Delta t}{T}$

Proposed Amplitude Modulation Scheme

Adjusting number of "on" transistors and duty cycle

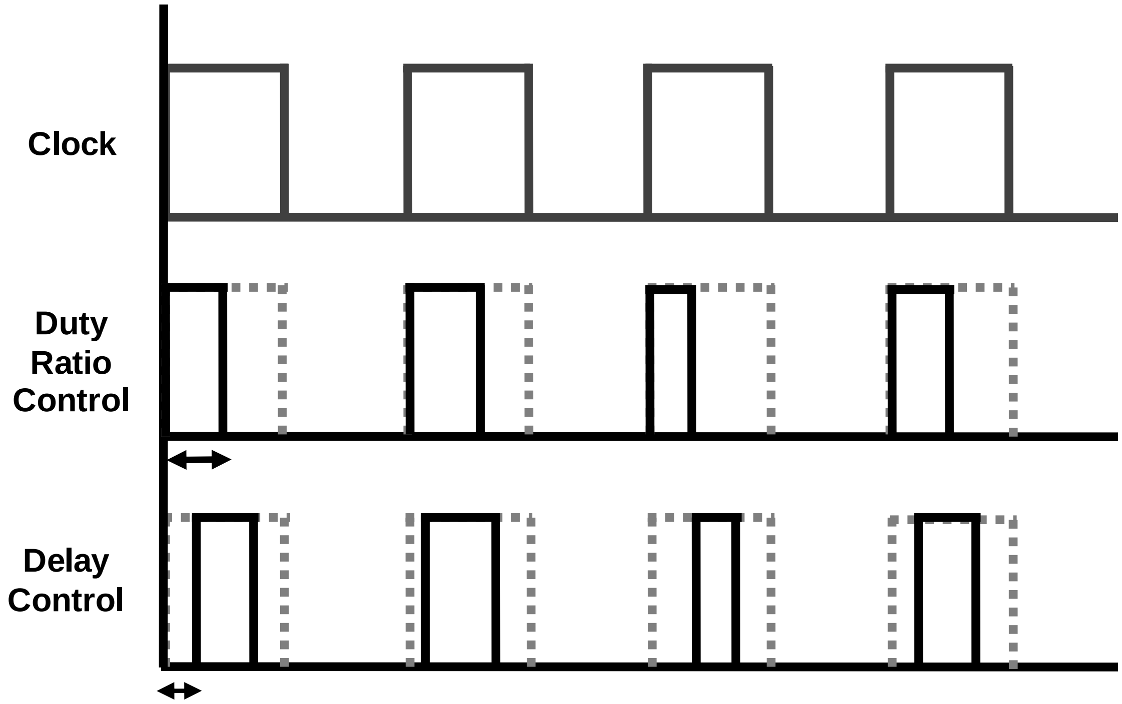
Control output voltage ⇨ Maximize efficiency



Phase Control

Pulse Position Modulation (PPM)

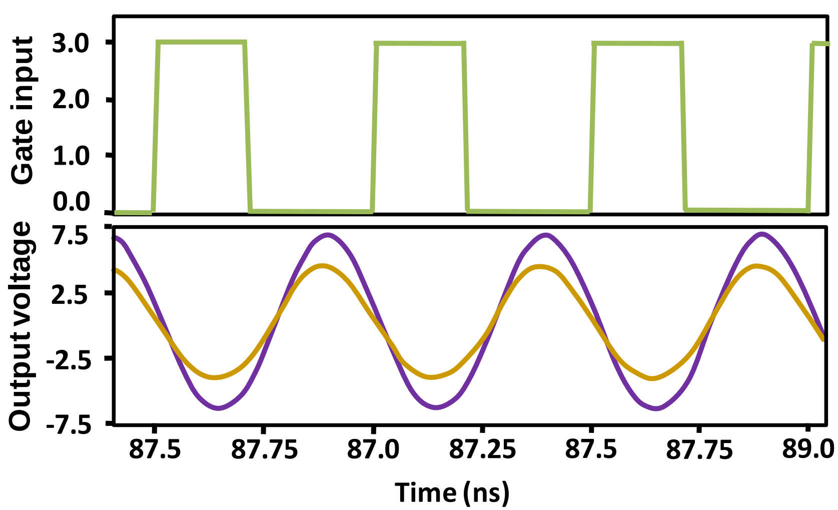
Can be realized



Amplitude and Phase Control

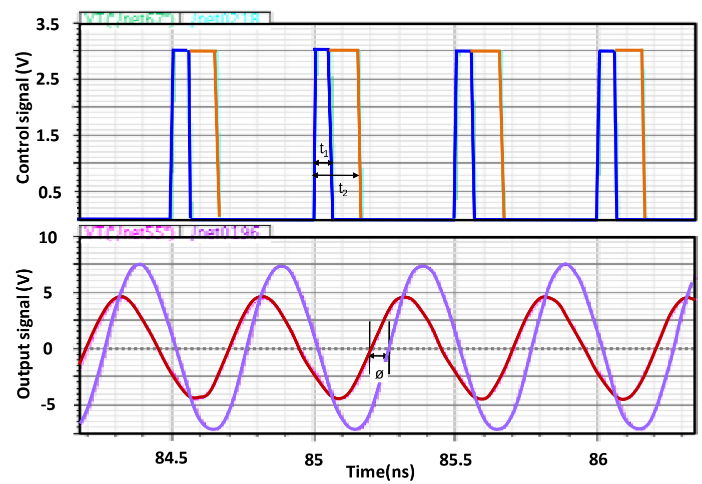
Change switch array "N"

Amplitude can be controlled
Phase does not change



Change Duty Cycle

Amplitude changes
Phase changes



$$\phi = \tan^{-1}\left[\frac{\cos(2\pi D) - 1}{2\pi(1-D) + \sin(2\pi D)}\right] + n\pi$$

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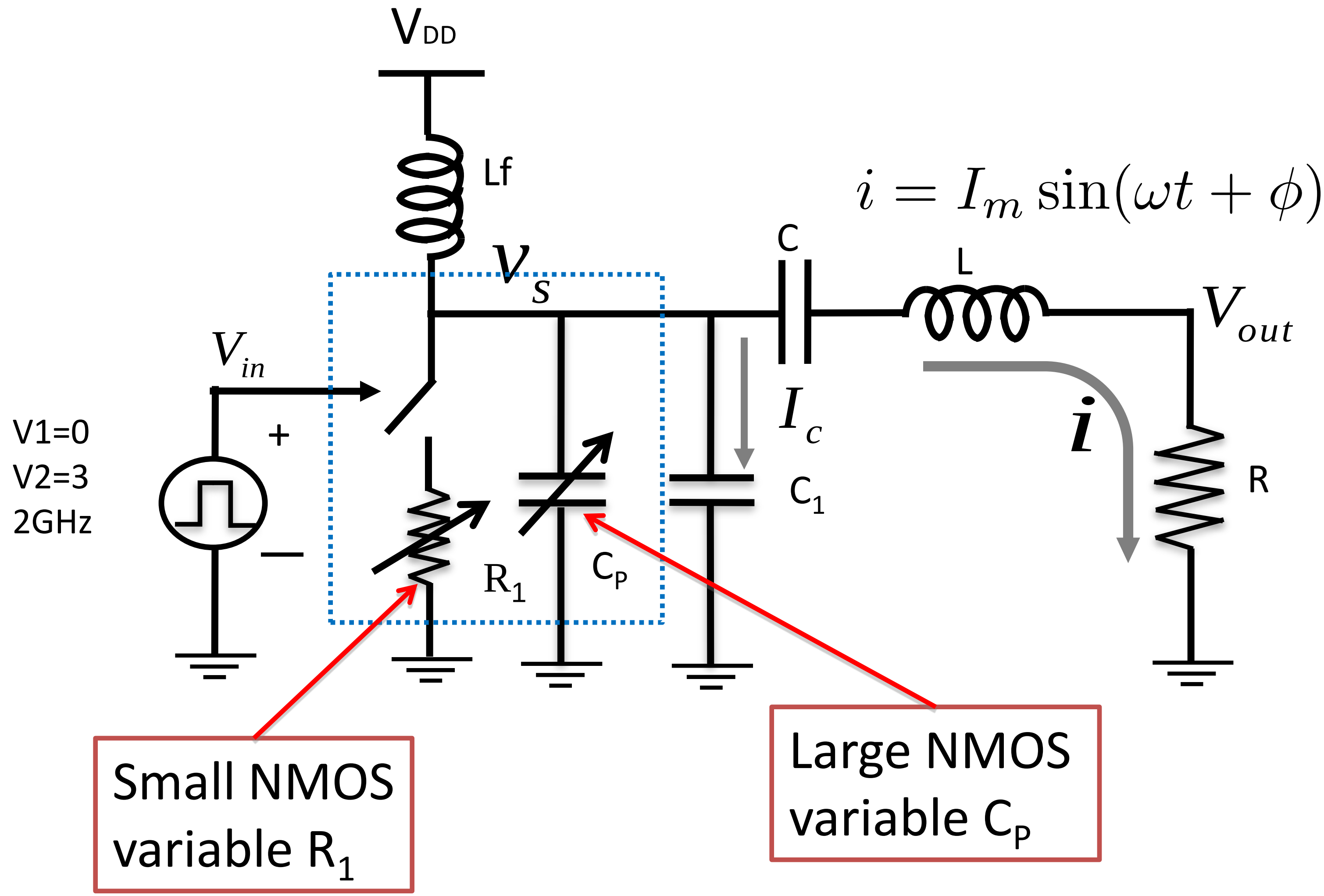
Class E Power Amplifier model



Proposed Digitally Controlled Amplifier

Choose desired amplitude, phase, efficiency

↓

Choose transistor array size, pulse width and delay

↓

Complicated system

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Feasible to implement with modern CMOS

Conclusion

- Described design and analysis of class-E amplifiers for digital control
- Using PWM with PPM for phase control
  – Large output voltage range, high efficiency
- Complicated digital control system
  – Easily implemented in modern CMOS processes

Fin

- Questions?

Questions from the Audience

- Doesn't the small transistor case have very low efficiency?
  - Yes, the efficiency is smaller than a typical class-e amplifier, but theoretically the highest achievable efficiency is 89%
- Can the small size case be modeled as a resistance?
  - Yes, our data shows that this can be modeled as a resistance.

Photos


Research Background
Realization of High Efficiency in Wireless Communication Systems
Digital to polar conversion
Digital AM Signal
Delay system
Rect. To Polar
RF Signal
Class E amplifier
Digital Circuitry
Analog Circuitry
2011 - Bali
Analog Very-Large-Scale-Integration
School of Electrical Engineering and Informatics
Bandung Institute of Technology, Indonesia


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